

HA17451P/FP

PWM Control Dual Switching Regulator IC

Description

The HA17451 is a PWM control IC containing the same two basic circuits for switching regulator. The two basic circuit is able to realize the perfect synchronous operation to common oscillator frequency.

So this IC has two output switches and is designed to be incorporated in Step-Up and Step-Down and Voltage Inverting applications.

The operation range versus input is wide, 3 ~ 40V. So the HA17451 is suitable for DC-to-DC converters, using the batteries.

Features

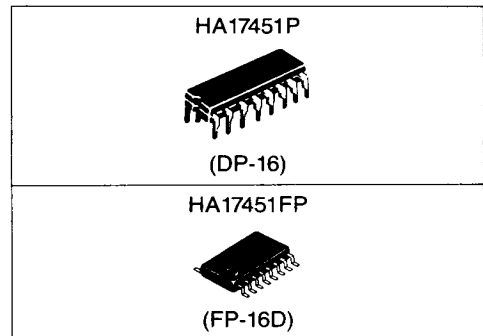
- Internal low drop out voltage regulator circuit ($V_{out} = 2.5V$, $V_{drop} = 0.2V$ typ.)
- Wide range of operating supply voltage 3V ~ 40V
- Large maximum output current,50mA (max.)
- Internal under voltage lockout protection circuit
High threshold voltage2.8V (typ.)
Low threshold voltage2.6V (typ.)
- Internal timer latch short protection circuit
- Low power dissipation1.5mA (typ.)
- Wide range of operating oscillation frequency
 $f_{osc} = 1KHz \sim 500KHz$
- Wide dead band range (D.B. duty 0 ~ 100%)
- Small surface mount package (SOP: small outline package) for high density PCB

Functions

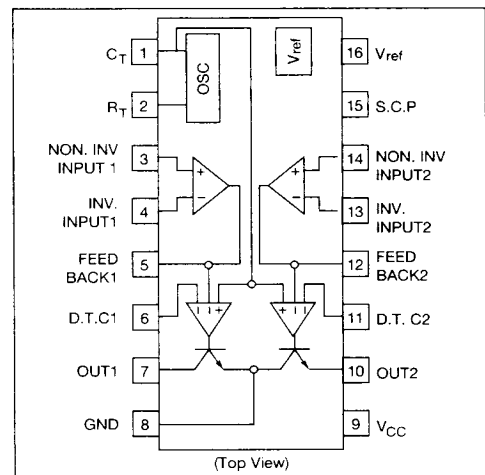
- Low drop out 2.5V reference voltage circuit
- Under voltage lockout protection circuit
- Timer latch short protection circuit
- Triangular waveform oscillation circuit
- Dead time control circuit
- Error amplifier circuit
- Output driver circuit
- PWM comparator circuit

Ordering Information

Type No.	Package
HA17451P	DP-16
HA17451FP	FP-16D



Pin Arrangement

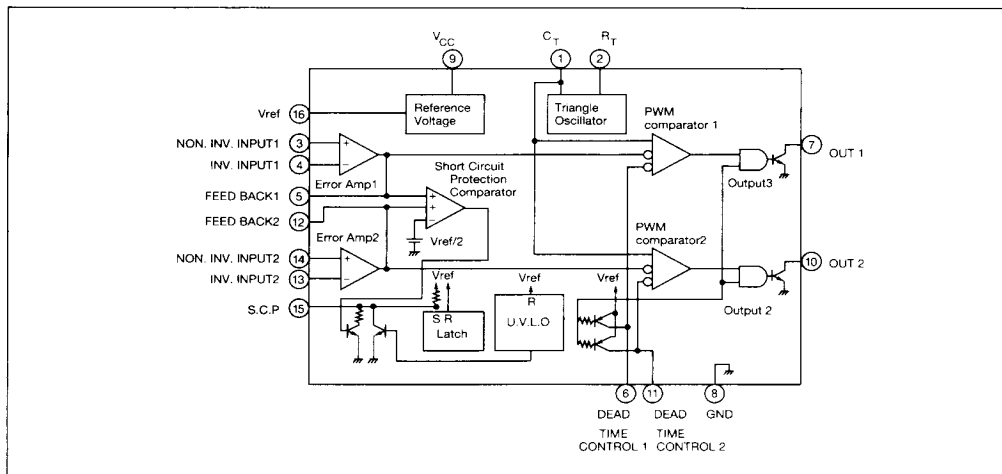


Pin Functions

Pin No.	Symbols	Functions
1	CT	Timing Capacitor
2	RT	Timing Resistor
3, 14	Non. Inv. Input	Non invert input of error amp.
4, 13	Inv. Input	Invert input of error amp.
5, 12	Feed Back	Output of error amp.
6, 11	D.T.C.	Dead time control
7, 10	OUT	Output
8	GND	Ground
9	VCC	Input voltage
15	S.C.P.	Short circuit protection
16	Vref	Reference voltage output



Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Power Supply Voltage	VCC	40	V	
Error Amp. Input Voltage	VI	20	V	
Collector Output Voltage	VO	40	V	
Collector Output Current	IO	50	mA	
Power Dissipation	PT	680	mW	1
Operation Temperature Range	Topr	-20 ~ +85	°C	
Storage Temperature Range	Tstg	-55 ~ +125	°C	

$$T_j(\text{max.}) = \theta_j - a \cdot PC(\text{max.}) + T_a$$

($\theta_j - a$ is thermal resistance value during mounting, and PC (max.) maximum value of IC power dissipation.)

Therefore, to keep $T_j(\text{max.}) \leq 125^\circ\text{C}$, wiring density and board material must be selected according to the board thermal conductivity ratio shown below.

Be careful that the value of PC (max.) does not exceed that of PT.

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

- Note: 1. In HA17451P a value of $T_a < 45^\circ\text{C}$ is permissible.
If more than 8.3mW/°C derating must be performed.
In HA17451FP allowable junction temperature of IC, $T_j(\text{max.})$, is shown below.

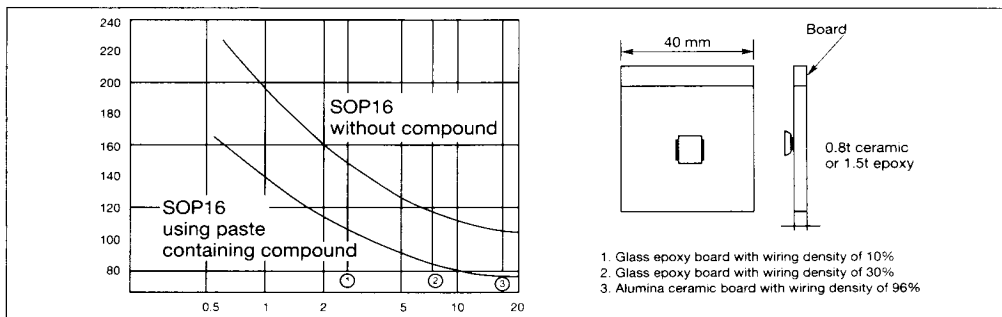


Figure 1. Thermal resistance of SOP



Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 6\text{V}$, $f_{osc} = 200\text{KHz}$)

Item	Symbol	Test Condition	min.	Spec typ.	max.	Unit
(1) Reference Section						
Output Voltage	V_{ref}	$I_O = 1\text{mA}$	2.40	2.50	2.60	V
Voltage Drop	V_{drop}	$I_O = 1\text{mA}$	—	0.2	0.5	V
Line Regulation	Line	$V_{CC} = 3.0 \sim 40\text{V}$	—	2	12.5	mV
Load Regulation	Load	$I_O = 0.1 \sim 1\text{mA}$	—	1	7.5	mV
Temperature Stability	RTC1	$T_a = -20 \sim 25^\circ\text{C}$	—	-0.1	—	%
	RTC2	$T_a = 25 \sim 85^\circ\text{C}$	—	-0.1	—	%
Short Circuit Current	I_{OS}	$V_{ref} = 0\text{V}$	3	10	30	mA
(2) Under Voltage Lockout Protection Section						
High Level Threshold	V_{th}	$I_O = 0.1\text{mA}$	—	2.8	—	V
Low Level Threshold	V_{tl}	$I_O = 0.1\text{mA}$	—	2.6	—	V
Hysteresis Width	V_{HYS}	$I_O = 0.1\text{mA}$	140	200	—	mV
Reset Voltage	V_R	$I_O = 0.1\text{mA}$	1.5	1.9	—	V
(3) Protection Section						
Input Threshold	V_{TPC}		0.65	0.7	0.75	V
Input Standby Voltage	V_{STBY}	No Pull Up	140	185	230	mV
Input Latch Voltage	V_l	No Pull Up	—	60	120	mV
Input Source Current	I_{bpc}		10	15	20	μA
Comparator Threshold Voltage	V_{tc}	5 pin, 12 pin	—	1.18	—	V
(4) Oscillator Section						
Frequency	f_{osc}	$C_T = 330\text{pF}$, $R_T = 10\text{K}\Omega$	—	200	—	KHz
Initial Accuracy	f_{dev}		—	10	—	%
Voltage Stability	f_{dv}		—	1	—	%
Temperature Stability	f_{dT1}	$T_a = -20 \sim 25^\circ\text{C}$	—	-0.4	—	%
	f_{dT2}	$T_a = 25 \sim 85^\circ\text{C}$	—	-0.2	—	%
(5) Dead Time Control Section						
Input Bias Current	I_{bdt}		—	—	1	μA
Latch Mode Source Current	I_{dt}		80	145	—	μA
Latch Input Voltage	V_{dt}		2.3	—	—	V
Input Threshold Voltage	V_{t0}	$f_{osc} = 10\text{KHz}$ Duty Cycle = 0%	—	2.05	2.25	V
Input Threshold Voltage	V_{t100}	$f_{osc} = 10\text{KHz}$ Duty Cycle = 100%	1.20	1.45	—	V
(6) Error Amp Section						
Input Offset Voltage	V_{IO}	$V_O (5, 12 \text{ P}_{in}) = 1.25\text{V}$	-6	—	6	mV
Input Offset Current	I_{IO}	$V_O (5, 12 \text{ P}_{in}) = 1.25\text{V}$	-100	—	100	nA
Input Bias Current	I_B	$V_O (5, 12 \text{ P}_{in}) = 1.25\text{V}$	—	160	500	nA
Common Mode Input Voltage Range	V_{ICR}	$V_{CC} = 3 \sim 40\text{V}$	1.0	—	1.45	V
Open Loop Gain	A_V	$R_{NF} 200\text{K}\Omega$	70	80	—	dB
Band Width	GB		—	1.5	—	MHz
Common Mode Rejection Ratio	$CMRR$		60	80	—	dB
Maximum Output Voltage	V_{OM+}		$V_{ref} - 0.1$	—	—	V
	V_{OM-}		—	—	1.0	V
Output Sink Current	I_{OM+}	$V_O = 1.25\text{V}$	0.5	1.6	—	mA
Output Source Current	I_{OM-}	$V_O = 1.25\text{V}$	-45	-70	—	μA

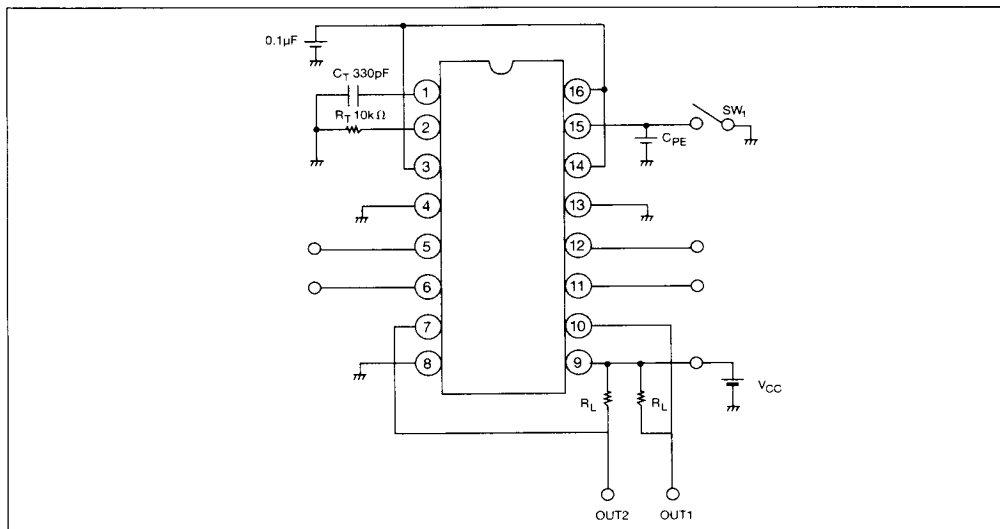


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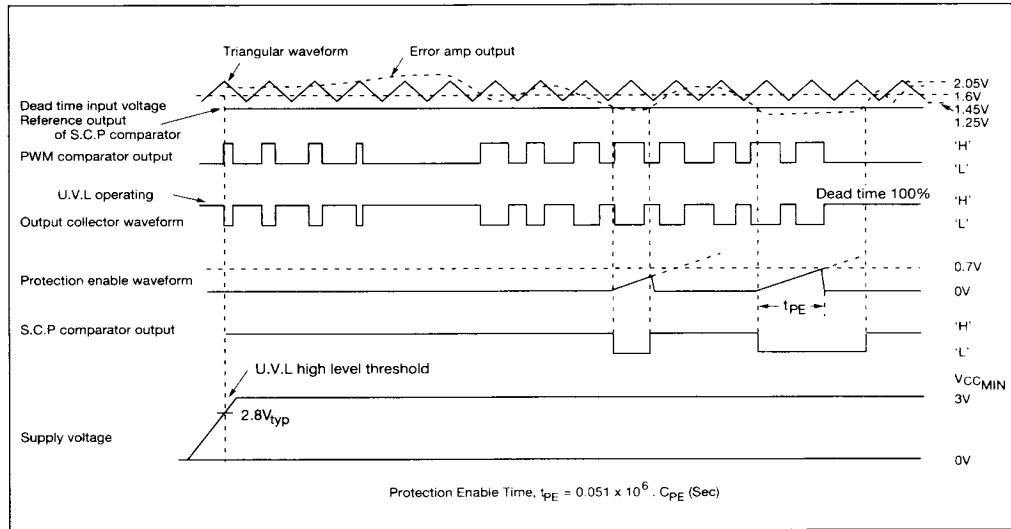
Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 6\text{V}$, $f_{osc} = 200\text{KHz}$) (Cont'd.)

Item	Symbol	Test Condition	min.	Spec typ.	max.	Unit
(7) Output Section						
Collector Off-State Current (1)	$I_{Leak(1)}$	$V_O = 40\text{V}$	—	—	10	μA
Collector Off-State Current (2)	$I_{Leak(2)}$	$V_O = 40\text{V}$ $V_{CC} = \text{Open}$	—	—	10	μA
Saturation Voltage	V_{sat}	$I_O = 10\text{mA}$	—	1.2	2	V
Short Current	I_{oss}	$V_O = 6\text{V}$	—	120	—	mA
(8) PWM Comparator Section						
Input Threshold Voltage	V_{t0}	$f_{osc} = 10\text{KHz}$ Duty Cycle = 0%	—	2.05	2.25	V
Input Threshold Voltage	V_{t100}	$f_{osc} = 10\text{KHz}$ Duty Cycle = 100%	1.20	1.45	—	V
Input Sink Current	I_{sink}	$V_O(5, 12 \text{ Pin}) = 1.25\text{V}$	0.5	1.6	—	mA
Input Source Current	I_{source}	$V_O(5, 12 \text{ Pin}) = 1.25\text{V}$	-45	-70	—	μA
(9) Total Current Section						
Standby Current	I_{ccs}	Output Off-State	—	1.5	2.0	mA
Average Supply Current	I_{cca}	$R_T = 10\text{K}\Omega$	—	1.9	2.6	mA

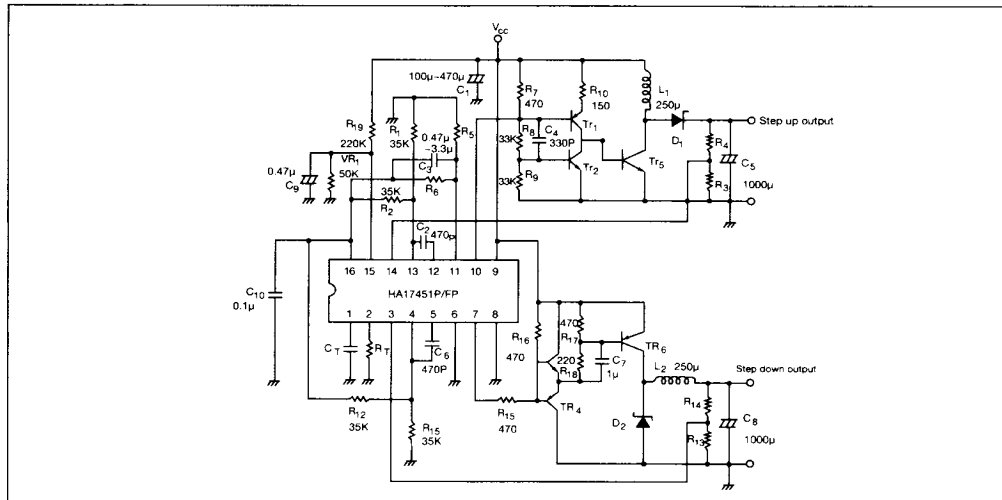
Measurement Circuit



Waveform Timing



System Configuration

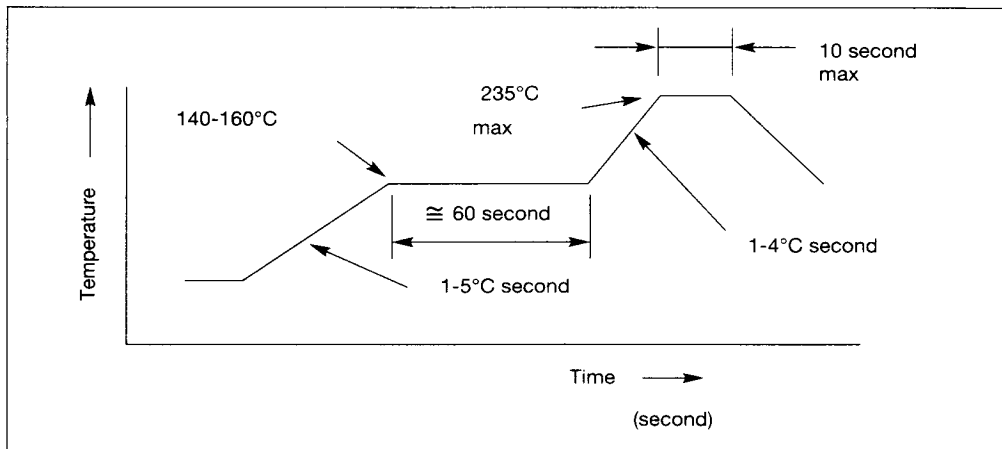


High Frequency Dual Switching Regulator System

Solder Mounting Method

1) Small and light surface-mount packages require special attentions on solder mounting. On solder mounting, pre-heating before soldering is needed. The following figure shows an example of infrared rays reflow.

2) The difference of thermal expansion coefficient between mounted substrates and IC lead may cause a failure like solder peeling or solder wet, and electrical characteristics may change by thermal stress. Therefore, mounting should be done after sufficient confirmation for especially in case of ceramic substrates.



An Example of Infrared Rays Reflow Conditions

