

# HAT1048R

## Silicon P Channel Power MOS FET Power Switching

# RENESAS

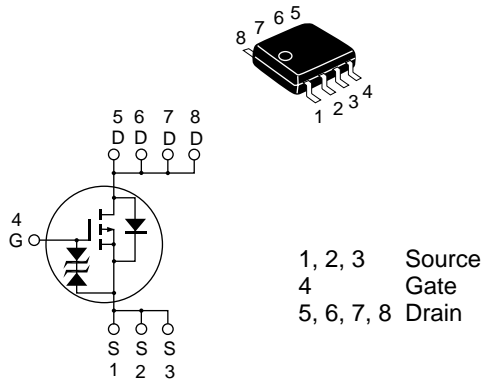
ADE-208-1223A (Z)  
2nd. Edition  
Jan. 2001

### Features

- Capable of -4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 6.0 \text{ m}\Omega$  typ (at  $V_{GS} = -10\text{V}$ )

### Outline

SOP-8



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	-16	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-128	A
Body-drain diode reverse drain current	$I_{DR}$	-16	A
Channel dissipation	$Pch$ <sup>Note2</sup>	2.5	W
Channel to Ambient Thermal Impedance	$\theta_{ch-a}$ <sup>Note2</sup>	50	°C/W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	- 55 to + 150	°C

Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

## Electrical Characteristics (Ta = 25°C)

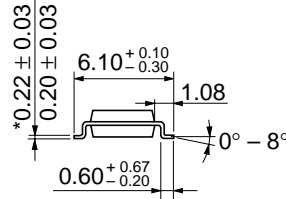
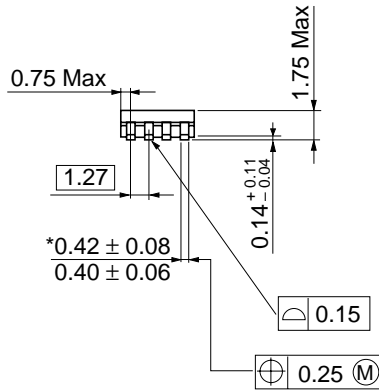
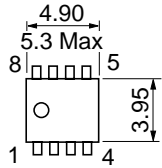
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	(6.0)	(7.0)	$\text{m}\Omega$	$I_D = -8 \text{ A}$ , $V_{GS} = -10 \text{ V}$ <sup>Note3</sup>
	$R_{DS(on)}$	—	(9.5)	(13.5)	$\text{m}\Omega$	$I_D = -8 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	(18)	(30)	—	S	$I_D = -8 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	(5700)	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	$C_{oss}$	—	(1250)	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	(710)	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	(105)	—	nc	$V_{DD} = -10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	(14)	—	nc	$V_{GS} = -10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	(20)	—	nc	$I_D = -16 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	(25)	—	ns	$V_{GS} = -10 \text{ V}$ , $I_D = -8 \text{ A}$
Rise time	$t_r$	—	(45)	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	(140)	—	ns	$R_L = 1.25 \text{ }\Omega$
Fall time	$t_f$	—	(55)	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	(-0.85)	(-1.10)	V	$I_F = -16 \text{ A}$ , $V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	(50)	—	ns	$I_F = -16 \text{ A}$ , $V_{GS} = 0 \text{ diF/dt} = 50 \text{ A/}\mu\text{s}$

Note: 3. Pulse test

## Package Dimensions

As of January, 2001

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL           NorthAmerica       : <http://semiconductor.hitachi.com/>  
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### For further information write to:

Hitachi Semiconductor  
 (America) Inc.  
 179 East Tasman Drive,  
 San Jose, CA 95134  
 Tel: <1> (408) 433-1990  
 Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
 Electronic Components Group  
 Dornacher Straße 3  
 D-85622 Feldkirchen, Munich  
 Germany  
 Tel: <49> (89) 9 9180-0  
 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
 Electronic Components Group.  
 Whitebrook Park  
 Lower Cookham Road  
 Maidenhead  
 Berkshire SL6 8YA, United Kingdom  
 Tel: <44> (1628) 585000  
 Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
 Hitachi Tower  
 16 Collyer Quay #20-00,  
 Singapore 049318  
 Tel: <65>-538-6533/538-8577  
 Fax : <65>-538-6933/538-3877  
 URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
 (Taipei Branch Office)  
 4/F, No. 167, Tun Hwa North Road,  
 Hung-Kuo Building,  
 Taipei (105), Taiwan  
 Tel : <886>-(2)-2718-3666  
 Fax : <886>-(2)-2718-8180  
 Telex : 23222 HAS-TP  
 URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
 Group III (Electronic Components)  
 7/F., North Tower,  
 World Finance Centre,  
 Harbour City, Canton Road  
 Tsim Sha Tsui, Kowloon,  
 Hong Kong  
 Tel : <852>-(2)-735-9218  
 Fax : <852>-(2)-730-0281  
 URL : <http://www.hitachi.com.hk>

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