

HAT2043R

Silicon N Channel Power MOS FET
High Speed Power Switching

HITACHI

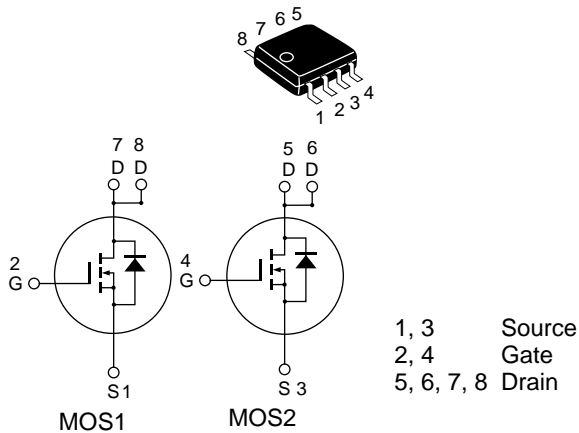
ADE-208-668D (Z)
5th. Edition
February 1999

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	64	A
Body-drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	Pch ^{Note2}	2.0	W
Channel dissipation	Pch ^{Note3}	3.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	- 55 to + 150	°C

Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

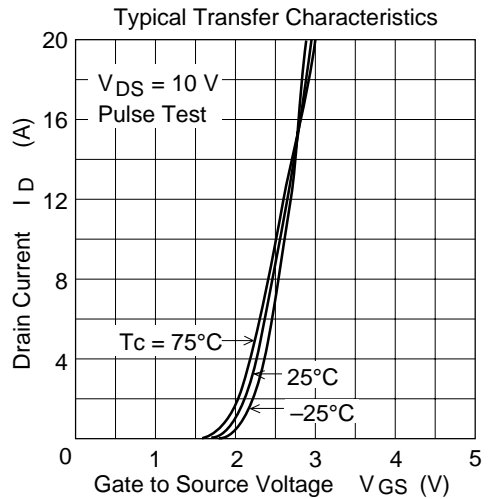
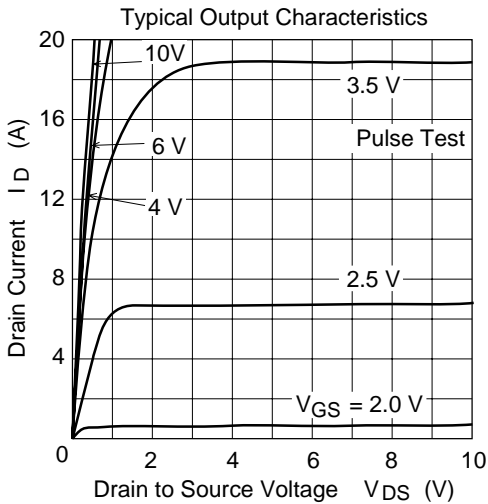
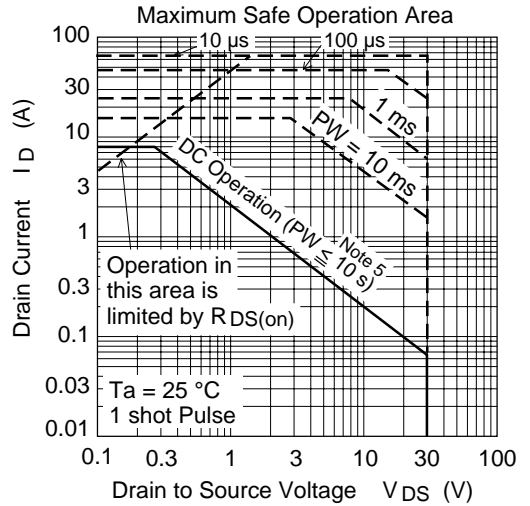
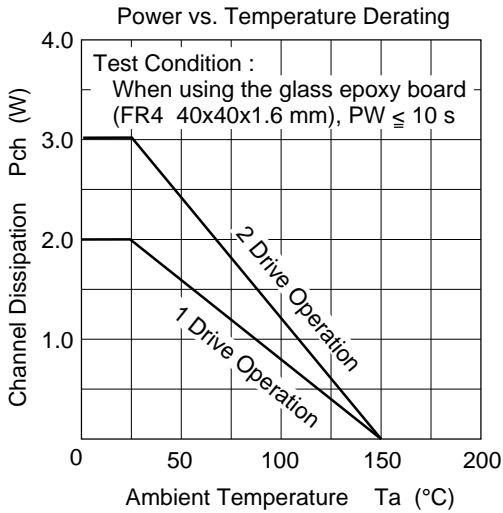
3. 2 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

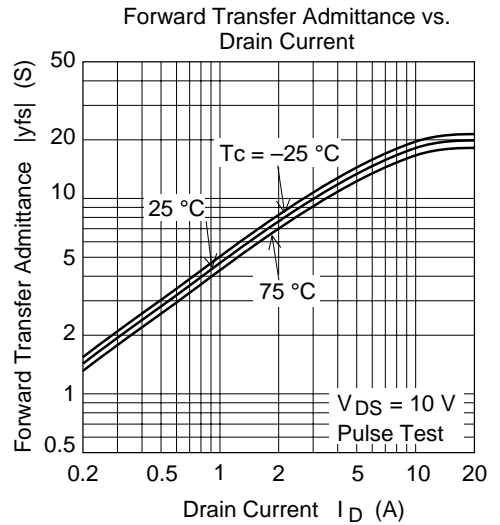
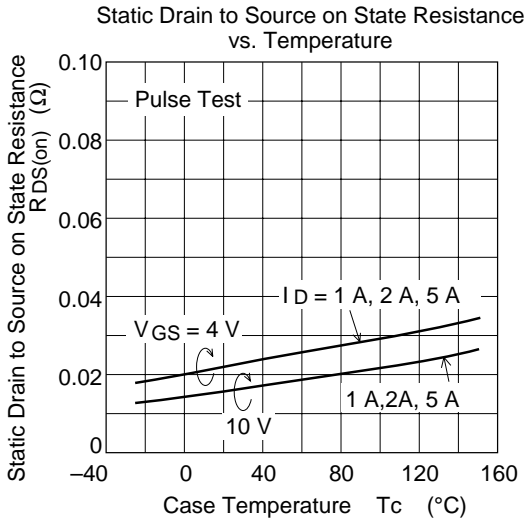
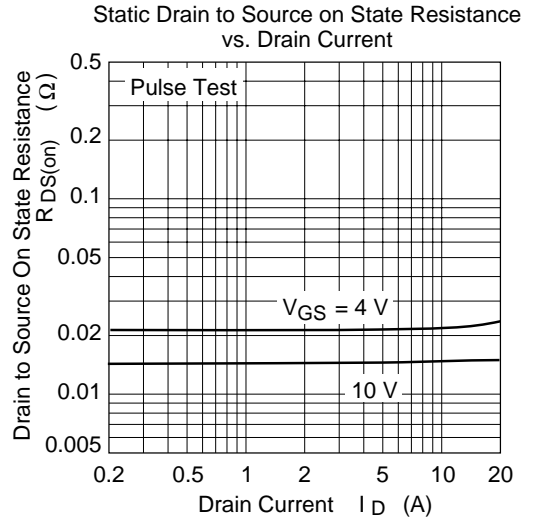
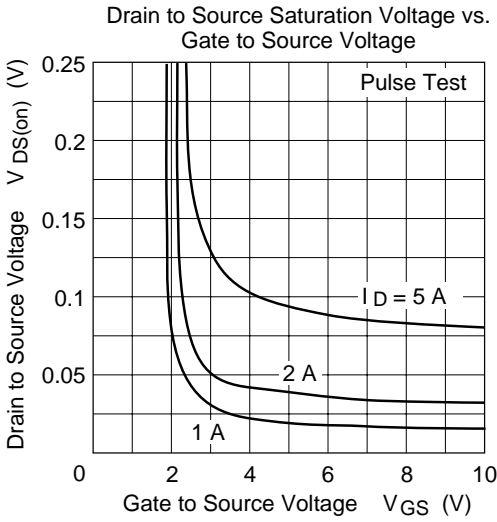
Electrical Characteristics (Ta = 25°C)

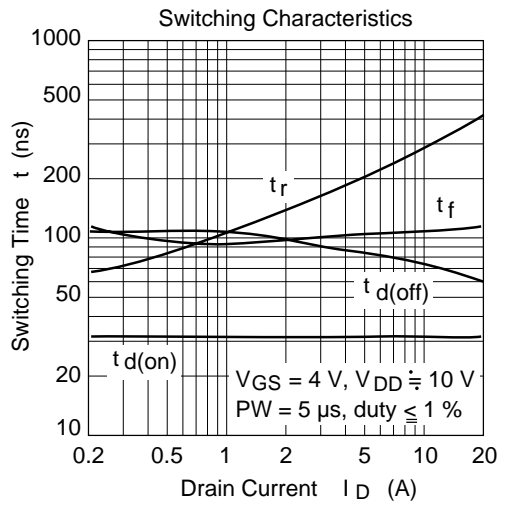
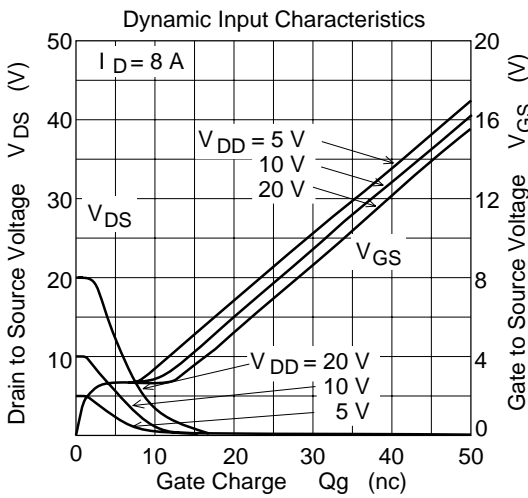
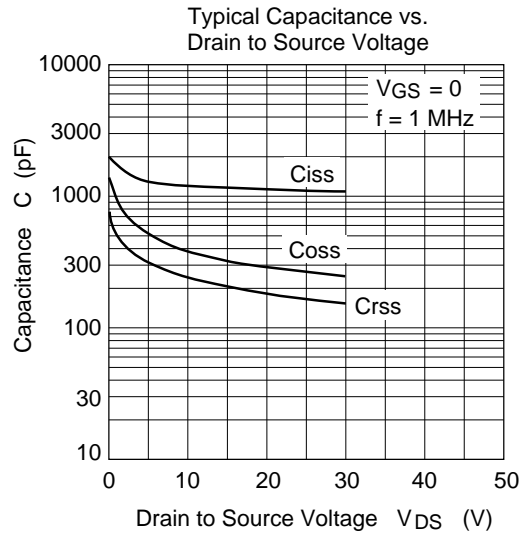
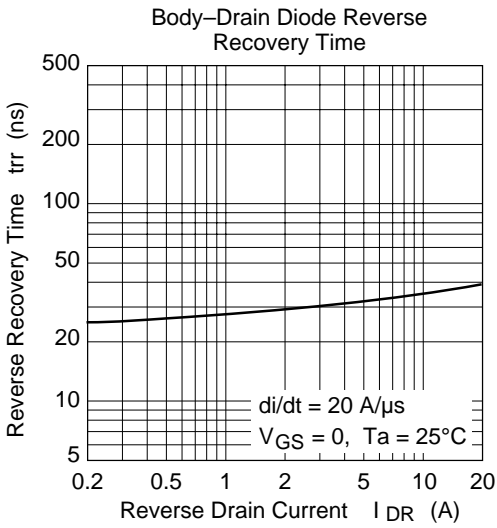
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.016	0.022	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	0.022	0.029	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	9	14	—	S	$I_D = 4 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	Ciss	—	1170	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	390	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	240	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	32	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	22	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	10	—	nc	$I_D = 8 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	32	—	ns	$V_{GS} = 4 \text{ V}$, $I_D = 4 \text{ A}$
Rise time	t_r	—	190	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	110	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.84	1.09	V	$IF = 8 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$IF = 8 \text{ A}$, $V_{GS} = 0$ $diF/dt = 20 \text{ A}/\mu s$

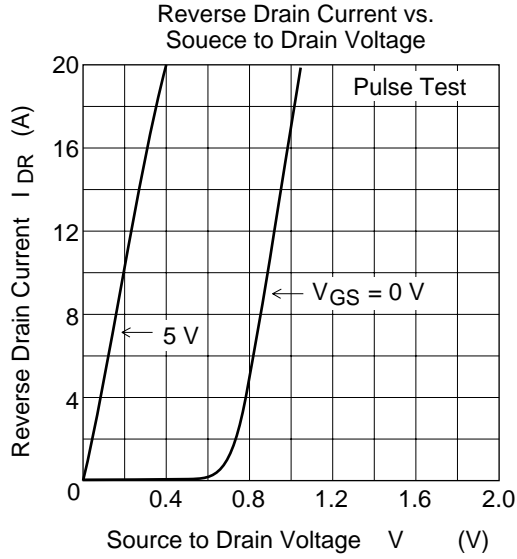
Note: 4. Pulse test

Main Characteristics

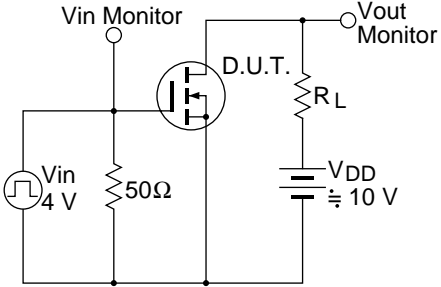




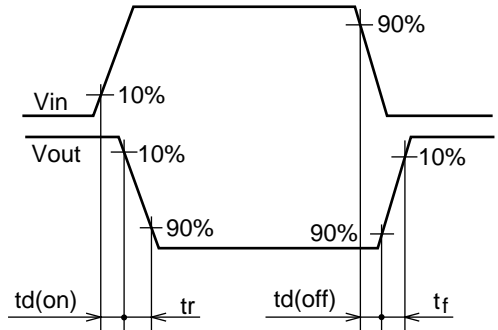




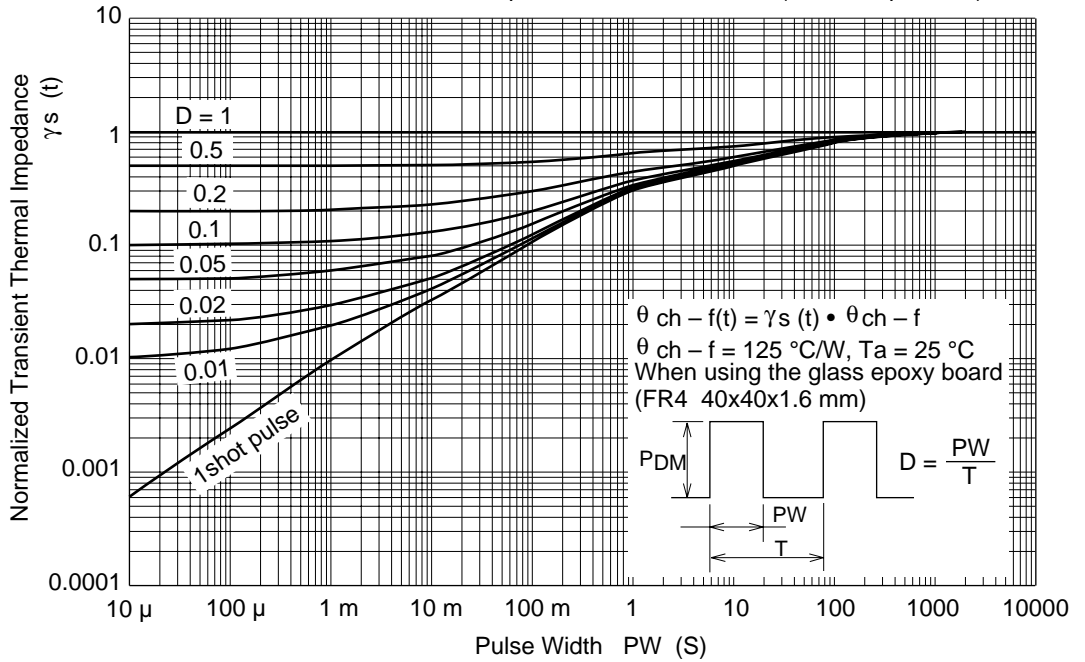
Switching Time Test Circuit



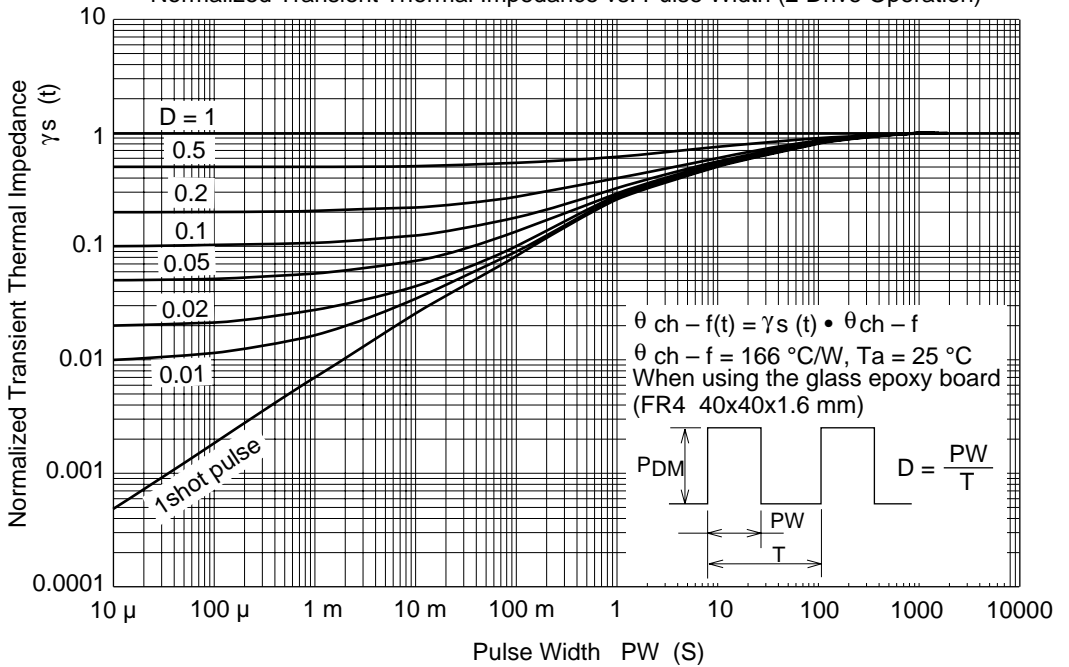
Switching Time Waveform



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

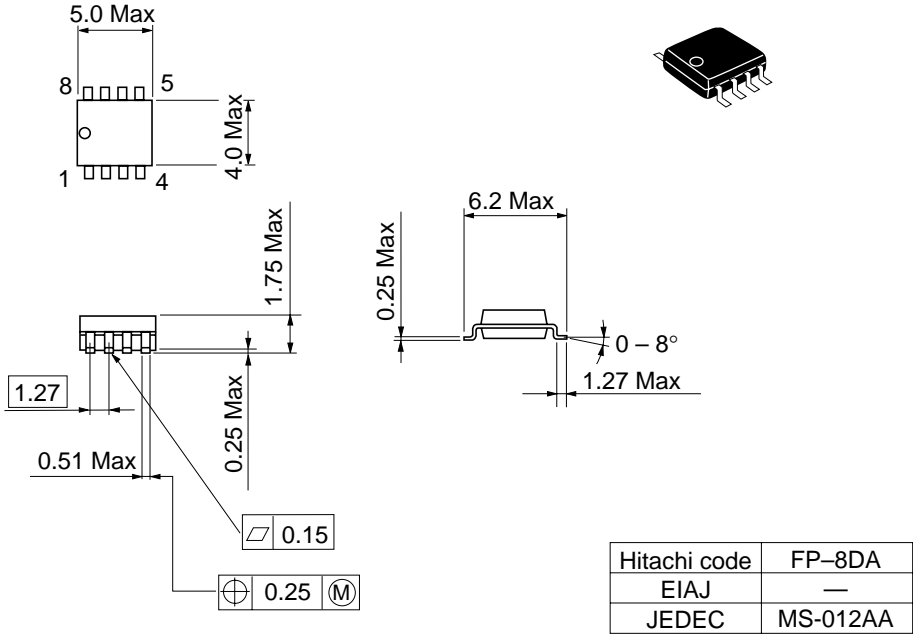


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

Unit: mm



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