# HAT2058R

## Silicon N Channel Power MOS FET
## High Speed Power Switching

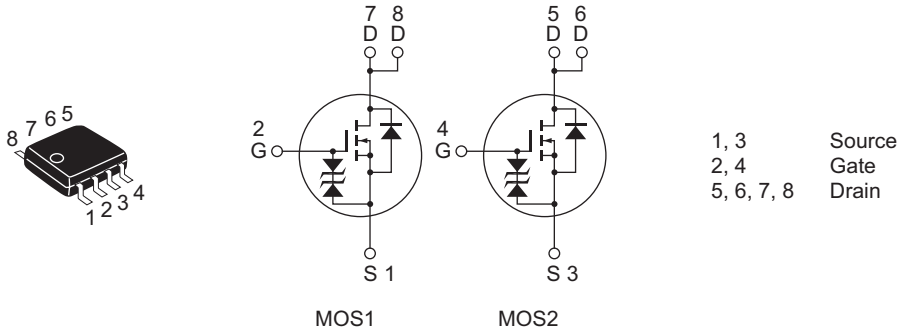
REJ03G1174-0300
Rev.3.00
Aug 25, 2009

### Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting
- "J" is for Automotive application
  High temperature D-S leakage guarantee
  Avalanche rating

### Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV> )




### Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 100 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ Note 2 | 4 | A |
| Drain peak current | $I_{D\ (pulse)}$ Note 1 | 32 | A |
| Body-drain diode reverse drain current | $I_{DR}$ | 4 | A |
| Avalanche current | $I_{AP}$ Note 4 | — | A |
| Avalanche energy | $E_{AR}$ Note 4 | — | mJ |
| Channel dissipation | Pch Note 2 | 2 | W |
| | Pch Note 3 | 3 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

## Electrical Characteristics

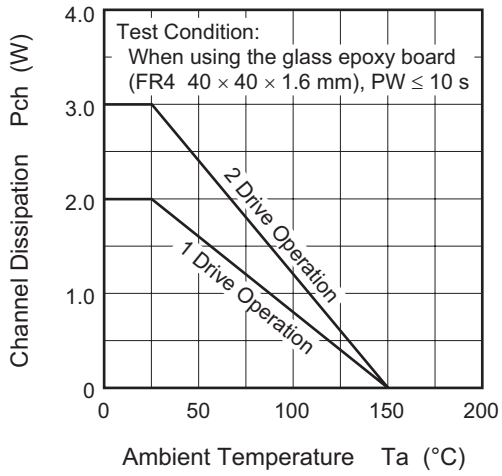
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)\ DSS}$ | 100 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)\ GSS}$ | ±20 | — | — | V | $I_G$ = ±100 μA, $V_{DS}$ = 0 |
| Zero gate voltage drain current | $I_{DSS}$ | — | — | 1 | μA | $V_{DS}$ = 100 V, $V_{GS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | μA | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS\ (off)}$ | 1.0 | — | 2.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Forward transfer admittance | $\|y_{fs}\|$ | 3 | 5 | — | S | $I_D$ = 2 A, $V_{DS}$ = 10 V Note 5 |
| Static drain to source on state resistance | $R_{DS\ (on)}$ | — | 120 | 145 | mΩ | $I_D$ = 2 A, $V_{GS}$ = 10 V Note 5 |
| | $R_{DS\ (on)}$ | — | 150 | 180 | mΩ | $I_D$ = 2 A, $V_{GS}$ = 4 V Note 5 |
| Input capacitance | Ciss | — | 420 | — | pF | $V_{DS}$ = 10 V, $V_{GS}$ = 0 |
| Output capacitance | Coss | — | 180 | — | pF | f = 1 MHz |
| Reverse transfer capacitance | Crss | — | 100 | — | pF | |
| Turn-on delay time | $t_{d\ (on)}$ | — | 10 | — | ns | $V_{GS}$ = 10 V, $I_D$ = 2 A, |
| Rise time | $t_r$ | — | 30 | — | ns | $V_{DD}$ ≅ 30 V |
| Turn-off delay time | $t_{d\ (off)}$ | — | 110 | — | ns | |
| Fall time | $t_f$ | — | 60 | — | ns | |
| Body-drain diode forward voltage | $V_{DF}$ | — | 0.85 | 1.1 | V | $I_F$ = 4 A, $V_{GS}$ = 0 Note 5 |
| Body-drain diode reverse recovery time | $t_{rr}$ | — | 75 | — | ns | $I_F$ = 4 A, $V_{GS}$ = 0<br>$di_F/dt$ = 50 A/μs |

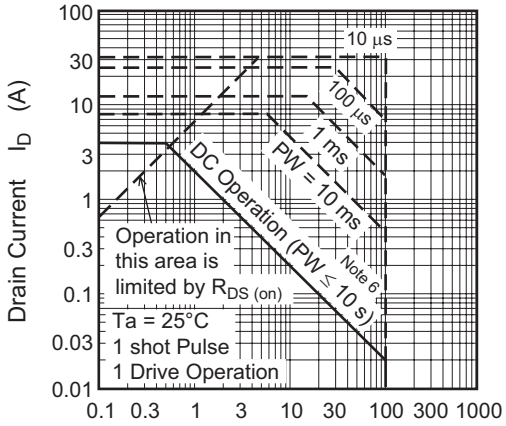
Note: 5. Pulse test

## Main Characteristics

Power vs. Temperature Derating

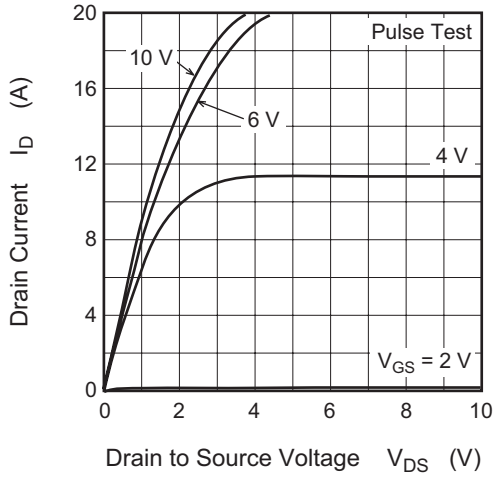



Maximum Safe Operation Area

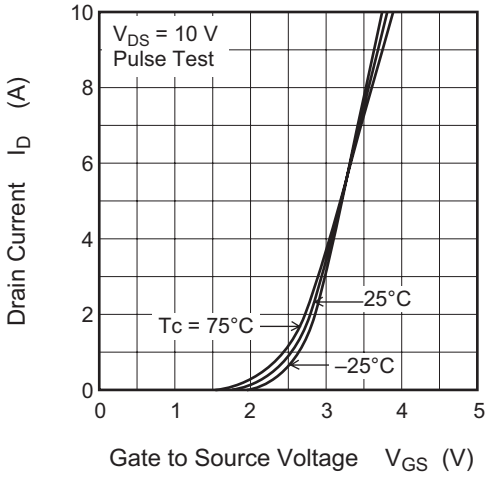



Note 6:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm)

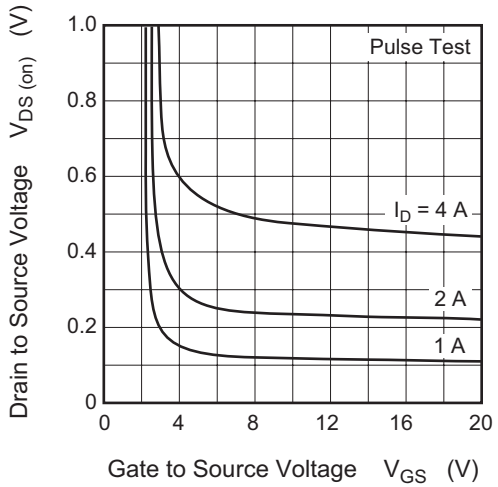
Typical Output Characteristics



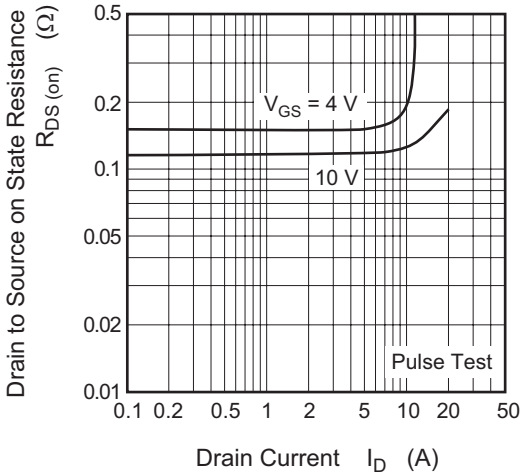

Typical Transfer Characteristics



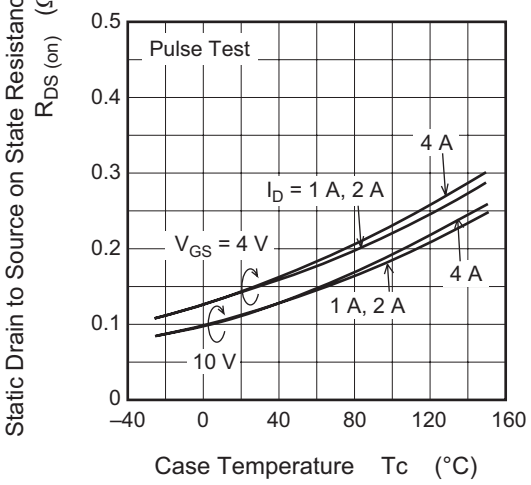

Drain to Source Saturation Voltage vs.
Gate to Source Voltage



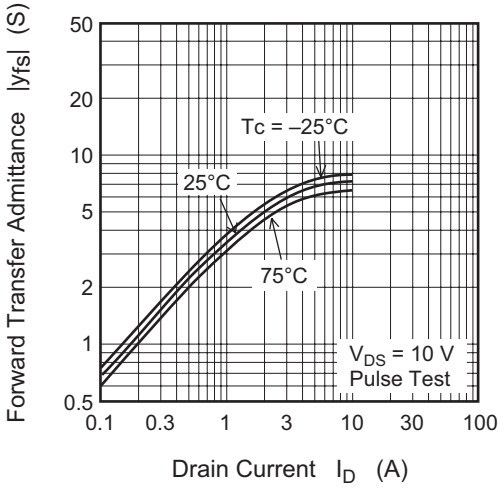

Static Drain to Source on State Resistance
vs. Drain Current



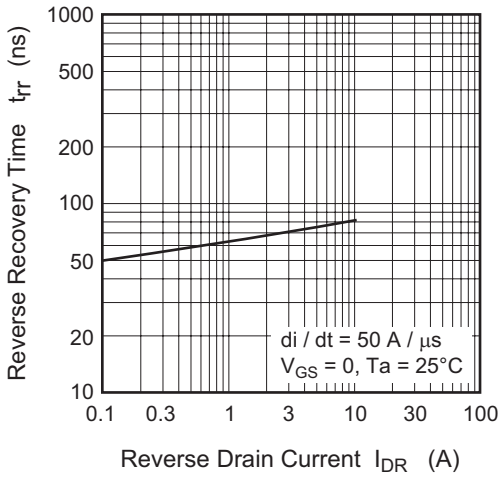
Static Drain to Source on State Resistance vs. Temperature



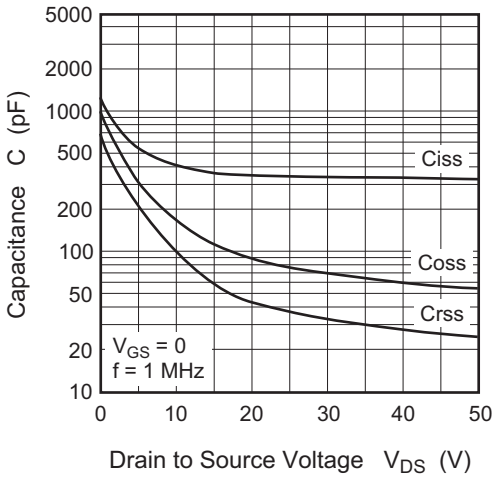

Forward Transfer Admittance vs. Drain Current



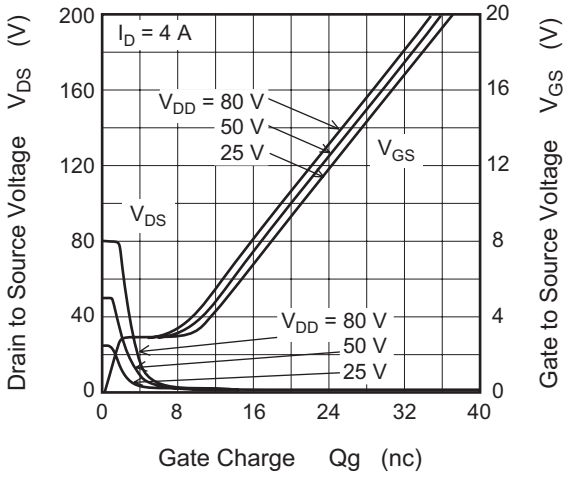

Body-Drain Diode Reverse Recovery Time



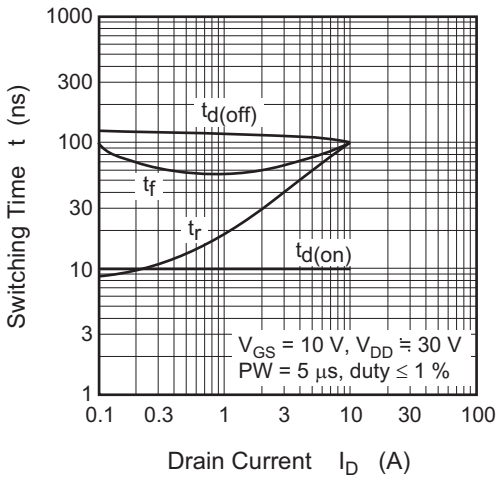

Typical Capacitance vs. Drain to Source Voltage



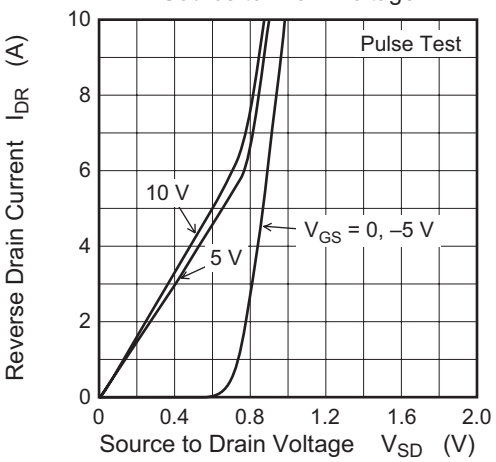

Dynamic Input Characteristics



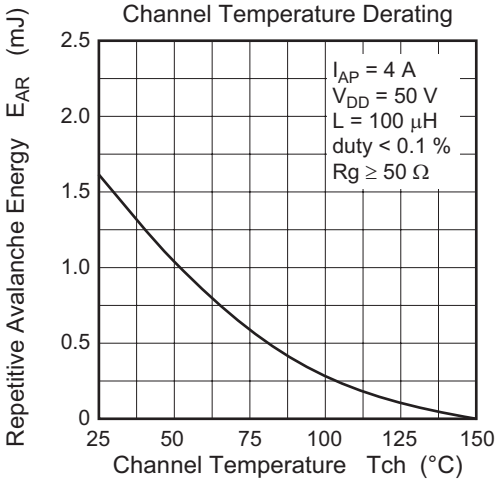

Switching Characteristics



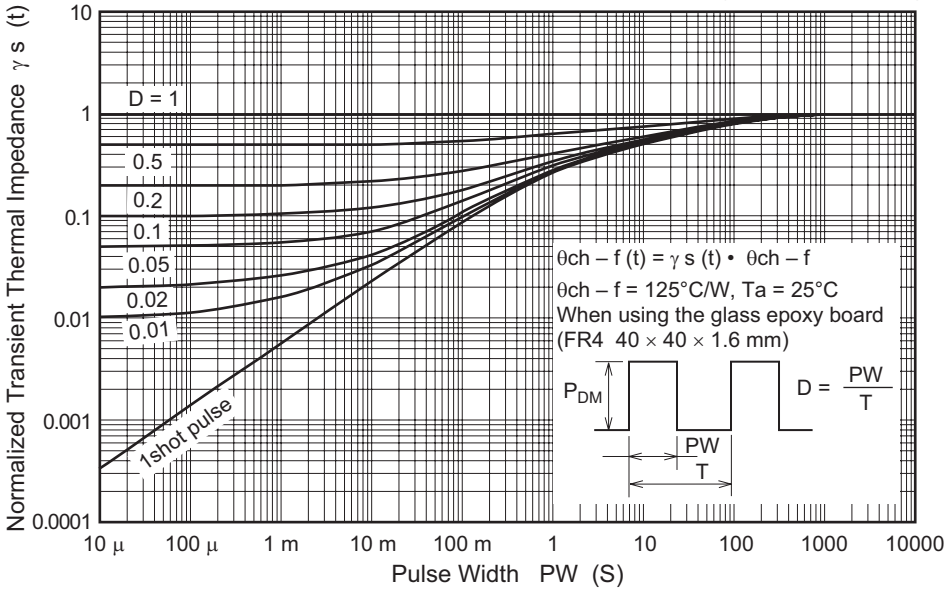
Reverse Drain Current vs.
Source to Drain Voltage



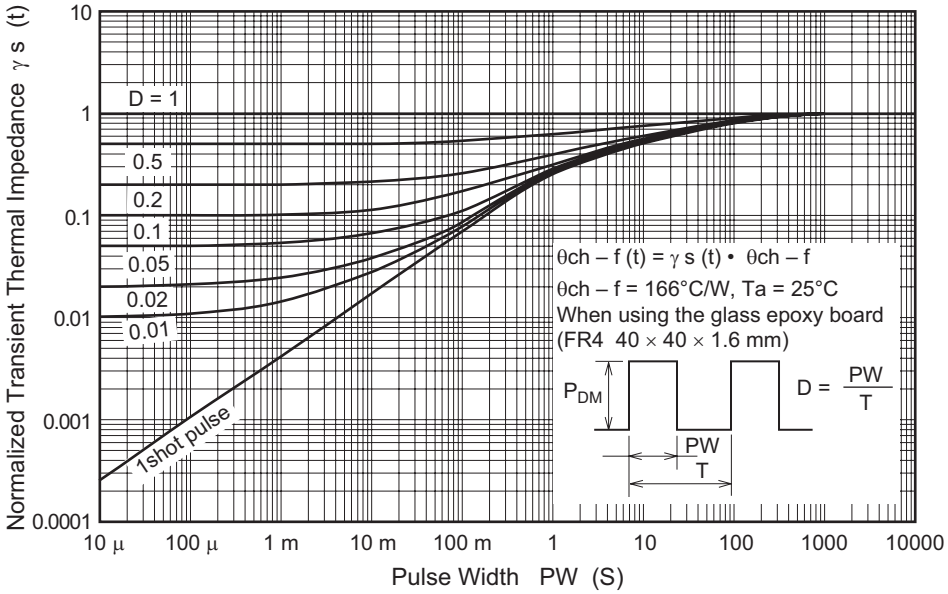

Maximum Avalanche Energy vs.
Channel Temperature Derating



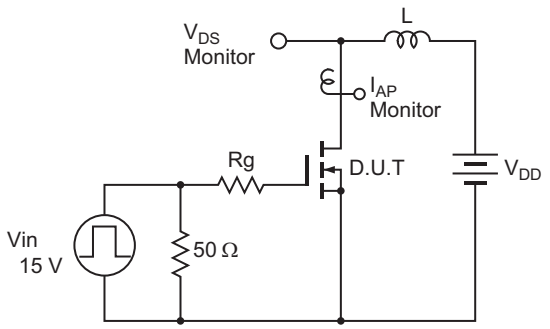

Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)




Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)

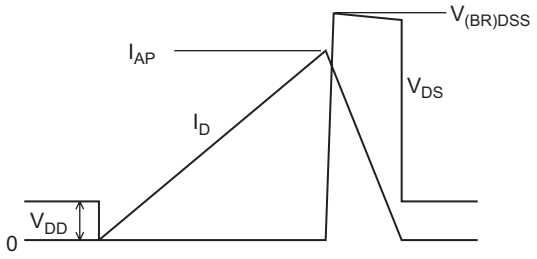


Avalanche Test Circuit

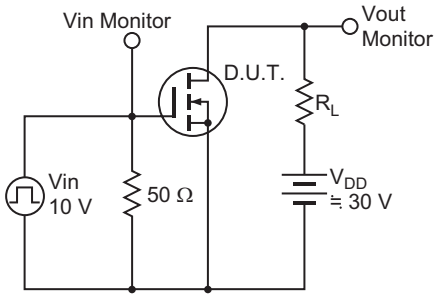



Avalanche Waveform

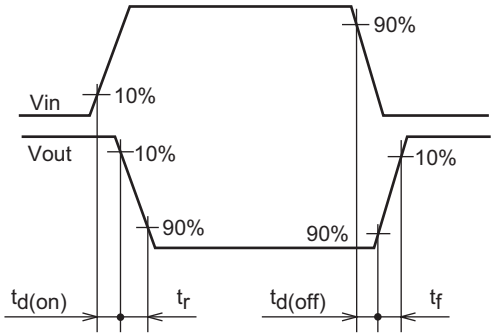
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$




Switching Time Test Circuit

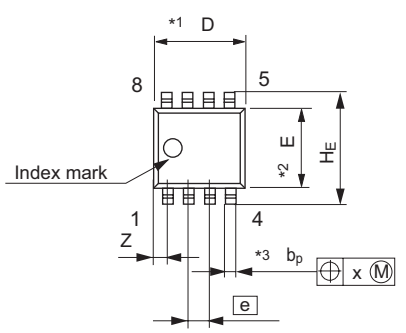


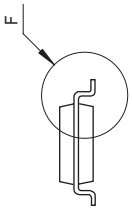

Switching Time Waveform

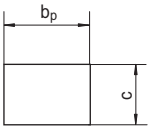


## Package Dimensions

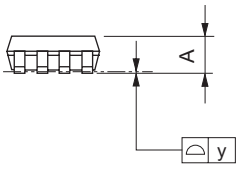
| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|---|
| SOP-8 | P-SOP8-3.95 × 4.9-1.27 | PRSP0008DD-D | FP-8DAV | 0.085g |

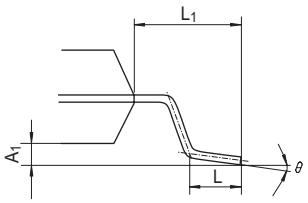



Terminal cross section
(Ni/Pd/Au plating)




Detail F

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 4.90 | 5.3 |
| E | — | 3.95 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.10 | 0.14 | 0.25 |
| A | — | — | 1.75 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | — | — | — |
| θ | 0° | — | 8° |
| $H_E$ | 5.80 | 6.10 | 6.20 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.1 |
| Z | — | — | 0.75 |
| L | 0.40 | 0.60 | 1.27 |
| $L_1$ | — | 1.08 | — |

## Ordering Information

| Part Name | Quantity | Shipping Container |
|---|---|---|
| HAT2058R-EL-E | 2500 pcs | Taping |

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Colophon .7.2