

HAT2169N

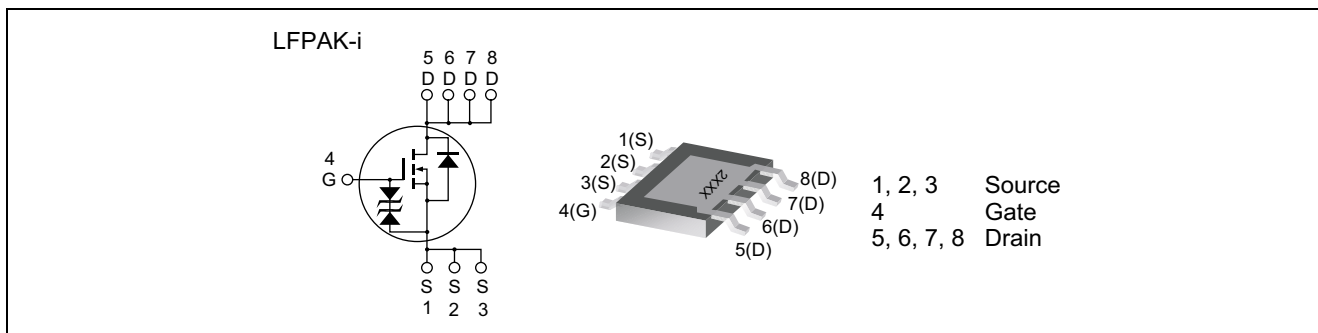
Silicon N Channel Power MOS FET Power Switching

Preliminary
Rev.0.01
May.29.2005

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 3.1 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	50	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Avalanche current	I_{AP} ^{Note 2}	30	A
Avalanche energy	E_{AR} ^{Note 2}	72	mJ
Channel dissipation	P_{ch} ^{Note 3}	30	W
Channel to Case Thermal Resistance	θ_{ch-C}	4.17	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	- 55 to + 150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

Electrical Characteristics

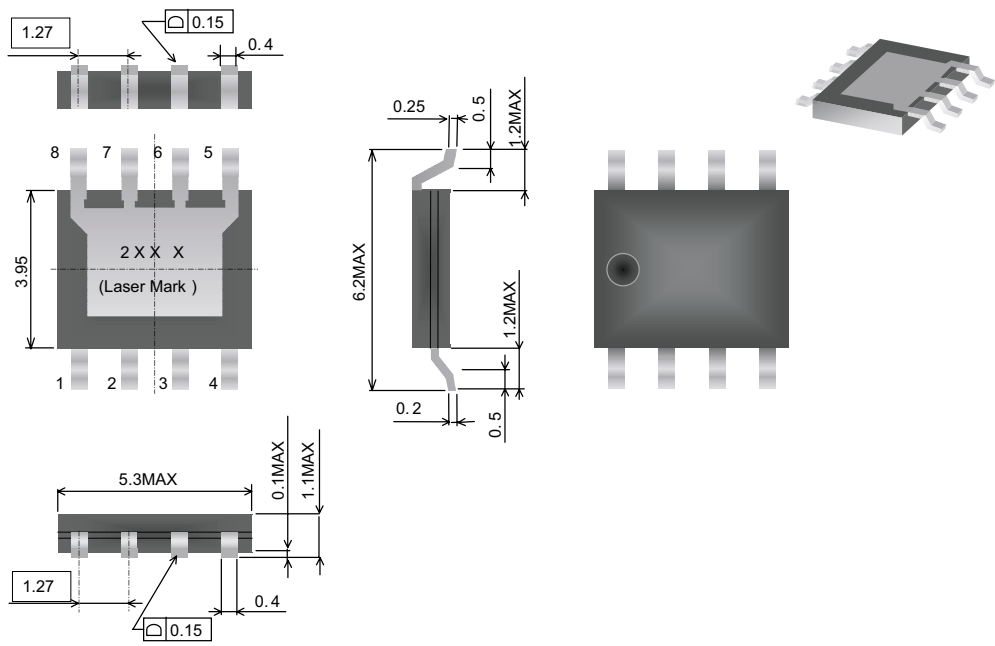
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.1	3.8	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	4.3	6.3	$\text{m}\Omega$	$I_D = 25 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	39	65	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	6650	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	890	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	360	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	0.5	—	Ω	
Total gate charge	Q_g	—	45	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	21	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	10	—	nC	$I_D = 50 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$
Rise time	t_r	—	64	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_L = 0.4 \text{ }\Omega$
Fall time	t_f	—	9.5	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 50 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions

Unit: mm



Package Code	LFPAK-i
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g