HAT2210R

Silicon N Channel Power MOSFET with Schottky Barrier Diode High Speed Power Switching

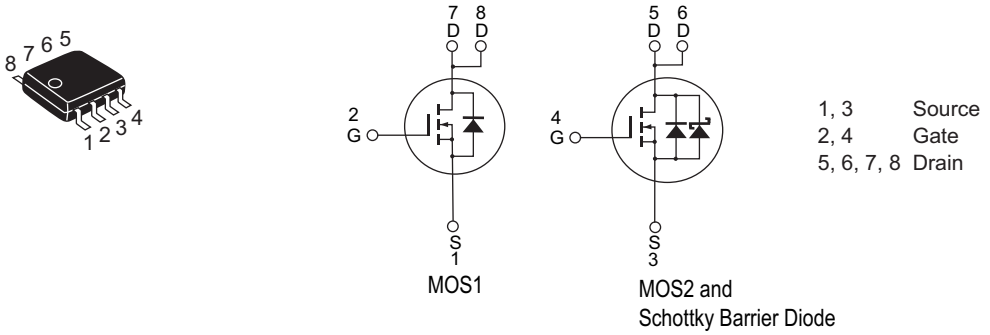
R07DS1368EJ0301
Rev.3.01
Jan 20, 2017

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Built-in Schottky Barrier Diode

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2 & SBD	
Drain to source voltage	V_{DSS}	30	30	V
Gate to source voltage	V_{GSS}	±20	±12	V
Drain current	I_D	7.5	8.0	A
Drain peak current	$I_{D(pulse)}$ Note1	60	64	A
Reverse drain current	I_{DR}	7.5	8.0	A
Channel dissipation	Pch Note2	1.5	1.5	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	19	24	mΩ	I_D = 3.75 A, V_{GS} = 10 V Note3
	$R_{DS(on)}$	—	27	40	mΩ	I_D = 3.75 A, V_{GS} = 4.5 V Note3
Forward transfer admittance	$\|y_{fs}\|$	9	15	—	S	I_D = 3.75 A, V_{DS} = 10 V Note3
Input capacitance	Ciss	—	630	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	155	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	57	—	pF	f = 1MHz
Total gate charge	Qg	—	4.6	—	nC	V_{DD} = 10 V
Gate to source charge	Qgs	—	2.2	—	nC	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	1.2	—	nC	I_D = 7.5 A
Turn-on delay time	$t_{d(on)}$	—	7	—	ns	V_{GS} =10 V, I_D = 3.75 A
Rise time	t_r	—	14	—	ns	V_{DD} ≈ 10 V
Turn-off delay time	$t_{d(off)}$	—	36	—	ns	R_L = 2.66 Ω
Fall time	t_f	—	3.4	—	ns	R_g = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.85	1.11	V	IF = 7.5 A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	17	—	ns	IF =7.5 A, V_{GS} = 0 diF/ dt = 100 A/μs

Notes: 3. Pulse test

• MOS 2 & Schottky Barrier Diode

(Ta = 25°C)

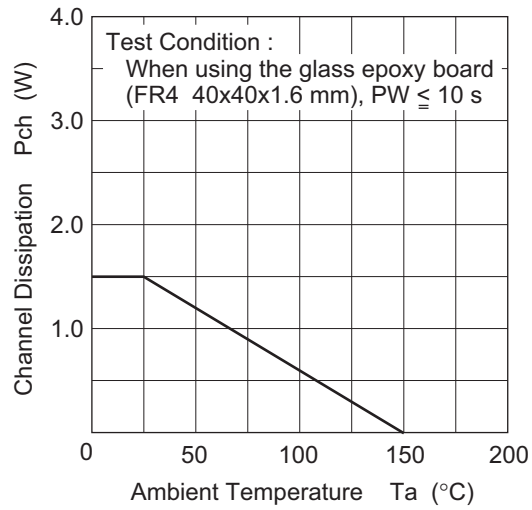
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±12 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	m A	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.4	—	2.5	V	V_{DS} = 10 V, I_D =1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	17	22	mΩ	I_D =4 A, V_{GS} = 10 V Note3
	$R_{DS(on)}$	—	21	29	mΩ	I_D = 4 A, V_{GS} = 4.5 V Note3
Forward transfer admittance	$\|y_{fs}\|$	15	25	—	S	I_D = 4 A, V_{DS} = 10 V Note3
Input capacitance	Ciss	—	1330	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	230	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	92	—	pF	f = 1MHz
Total gate charge	Qg	—	11	—	nC	V_{DD} = 10 V
Gate to source charge	Qgs	—	3.8	—	nC	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	3.2	—	nC	I_D = 8 A
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10 V, I_D = 4 A
Rise time	t_r	—	16	—	ns	V_{DD} ≈ 10 V
Turn-off delay time	$t_{d(off)}$	—	43	—	ns	R_L = 2.5 Ω
Fall time	t_f	—	3.9	—	ns	R_g = 4.7 Ω
Schottky Barrier diode forward voltage	V_F	—	0.5	—	V	IF = 3.5 A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	15	—	ns	IF = 8 A, V_{GS} = 0 diF/ dt = 100 A/μs

Notes: 3. Pulse test

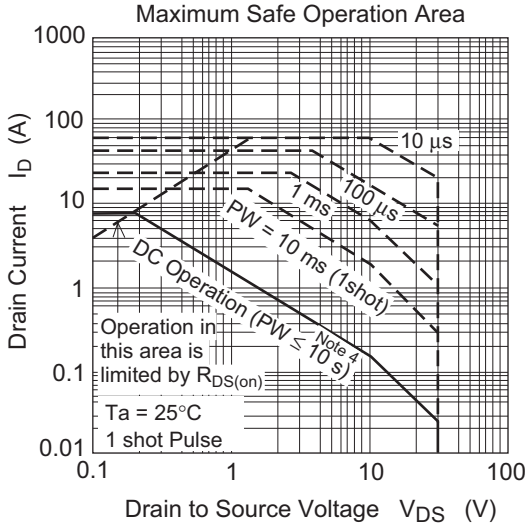
Main Characteristics

• MOS 1

Power vs. Temperature Derating

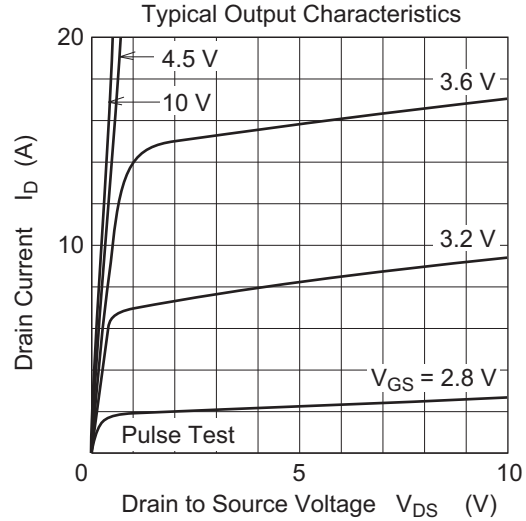


Maximum Safe Operation Area

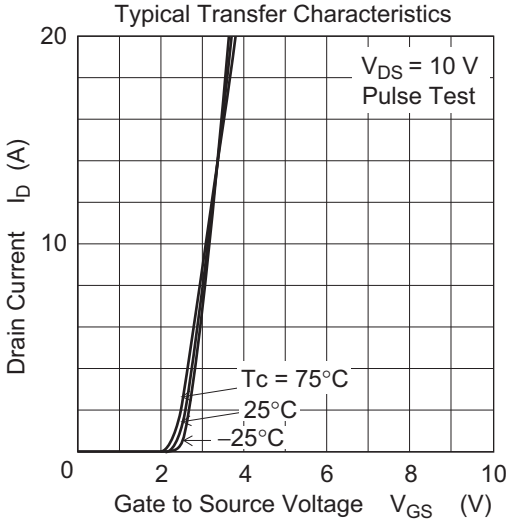


Note 4 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

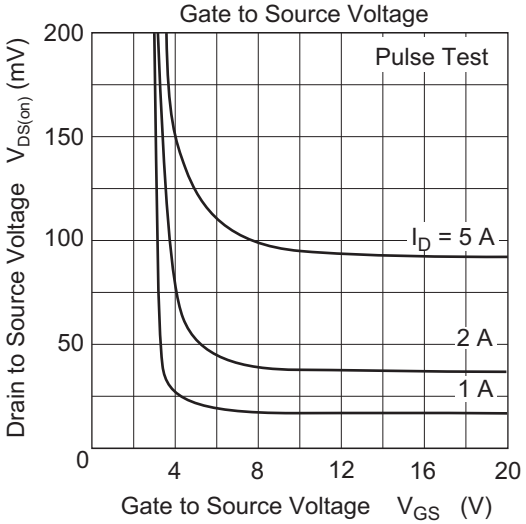
Typical Output Characteristics



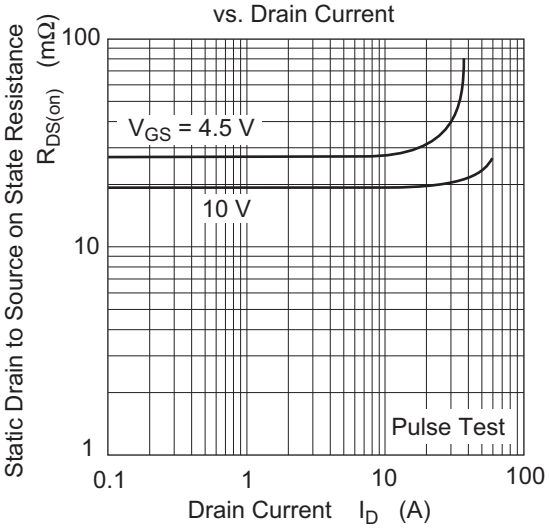
Typical Transfer Characteristics



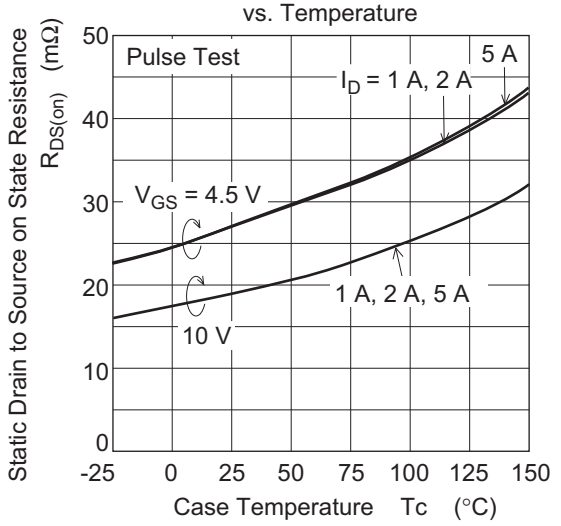
Drain to Source Saturation Voltage vs
Gate to Source Voltage



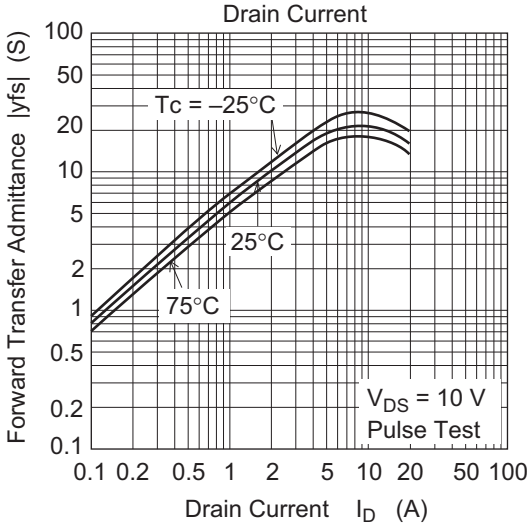
Static Drain to Source on State Resistance
vs. Drain Current



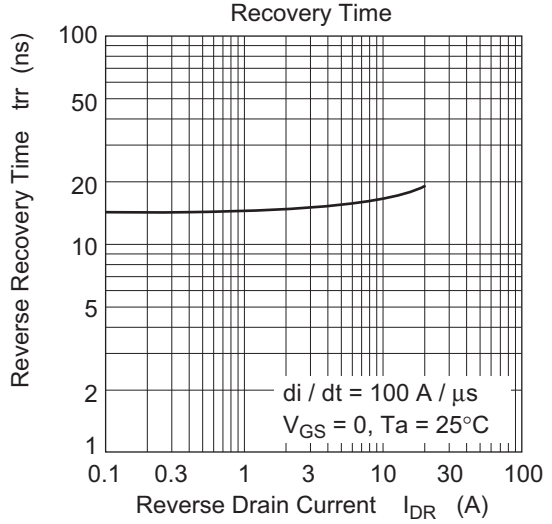
Static Drain to Source on State Resistance vs. Temperature



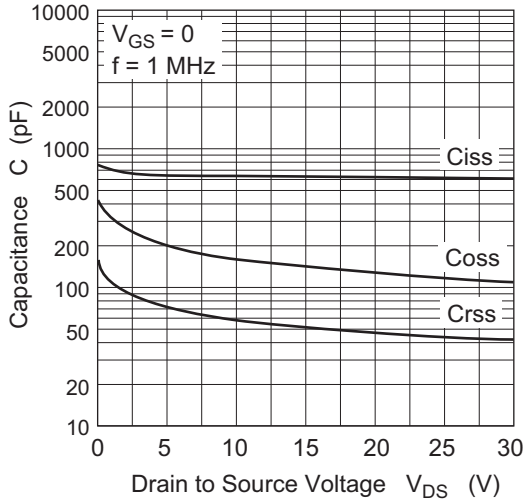
Forward Transfer Admittance vs. Drain Current



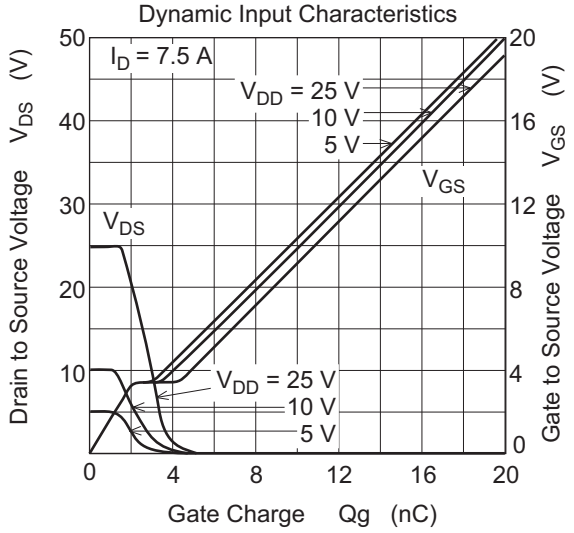
Body-Drain Diode Reverse Recovery Time



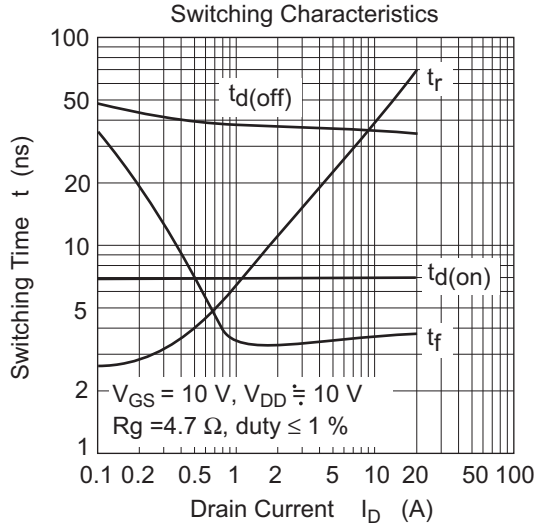
Typical Capacitance vs. Drain to Source Voltage

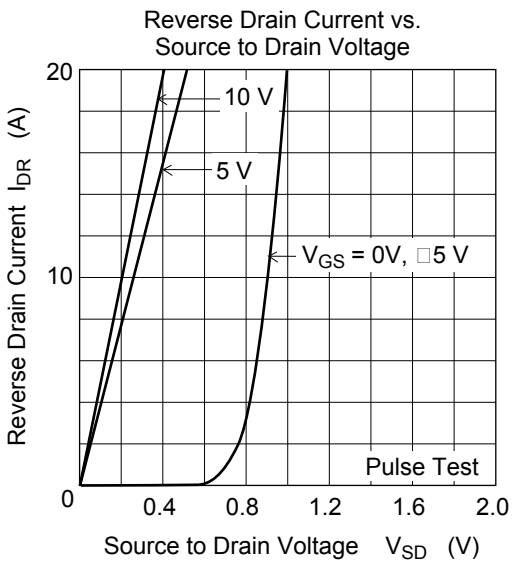


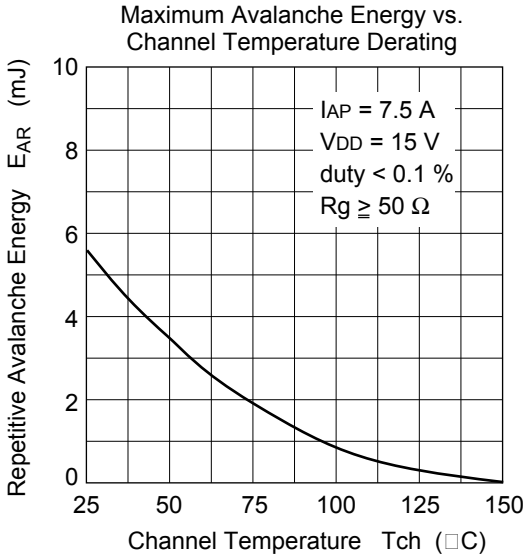
Dynamic Input Characteristics

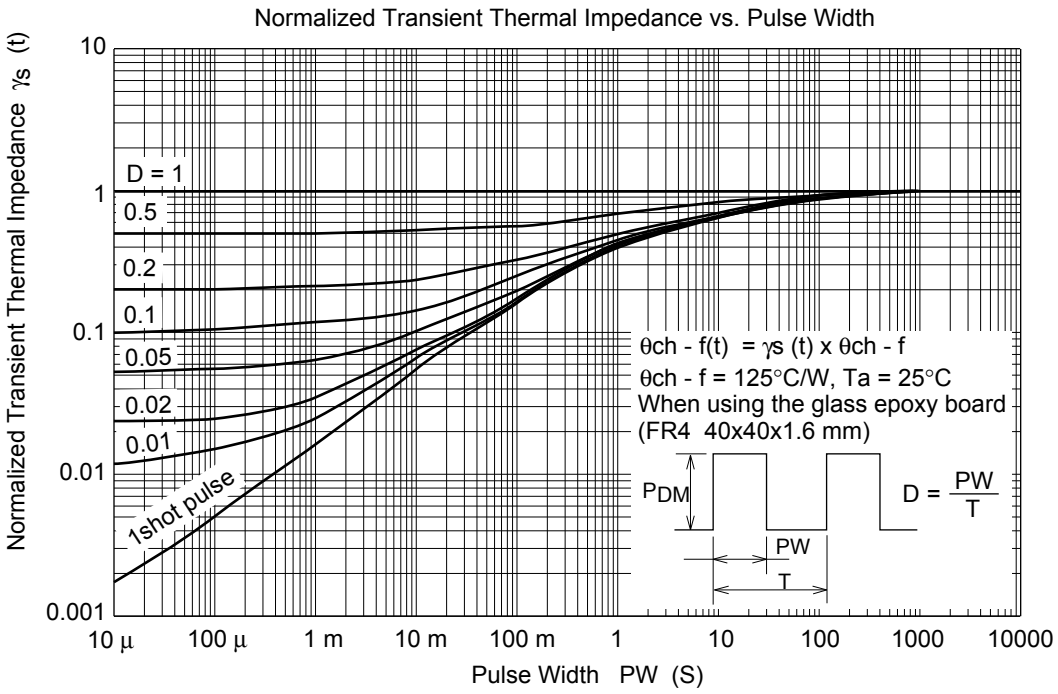


Switching Characteristics



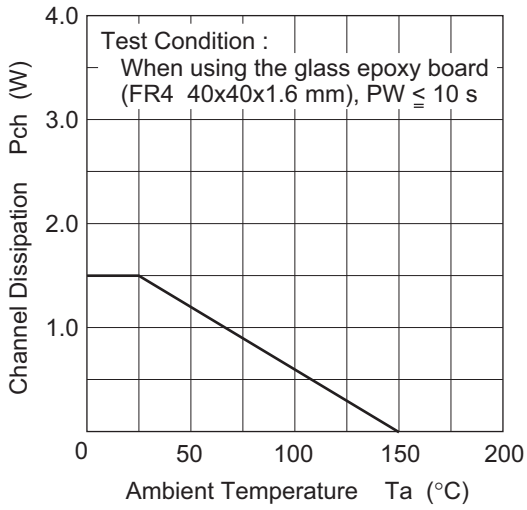

Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current IDR (A)
20
10
0
10 V
5 V
VGS = 0V, 5 V
Pulse Test
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage VSD (V)


Maximum Avalanche Energy vs.
Channel Temperature Derating
Repetitive Avalanche Energy EAR (mJ)
10
8
6
4
2
0
IAP = 7.5 A
VDD = 15 V
duty < 0.1 %
Rg ≧ 50 Ω
25
50
75
100
125
150
Channel Temperature Tch (C)

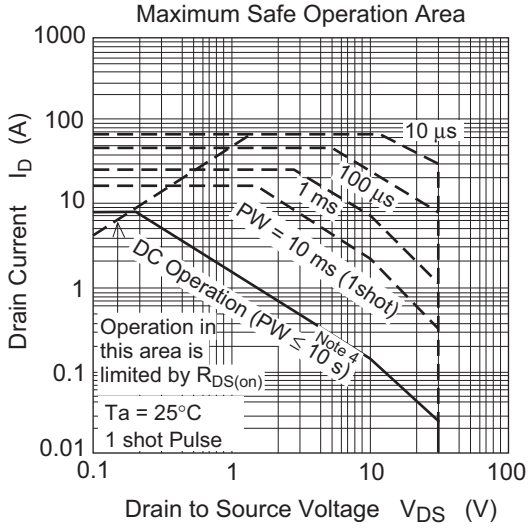

Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 125°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

• MOS 2 & Schottky Barrier Diode

Power vs. Temperature Derating



Maximum Safe Operation Area



Note 4 :
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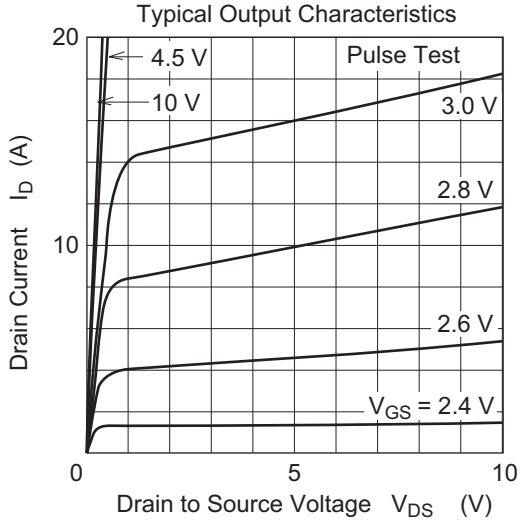
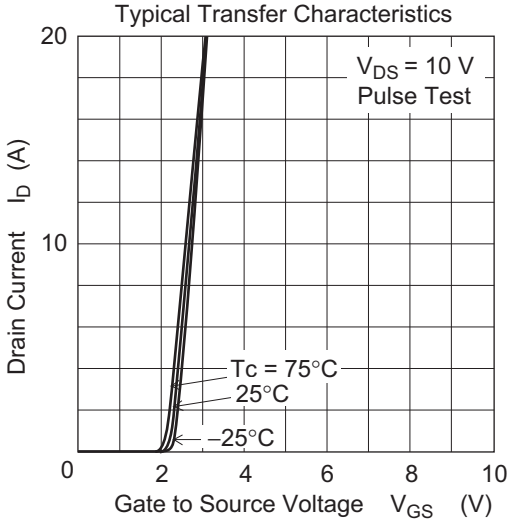
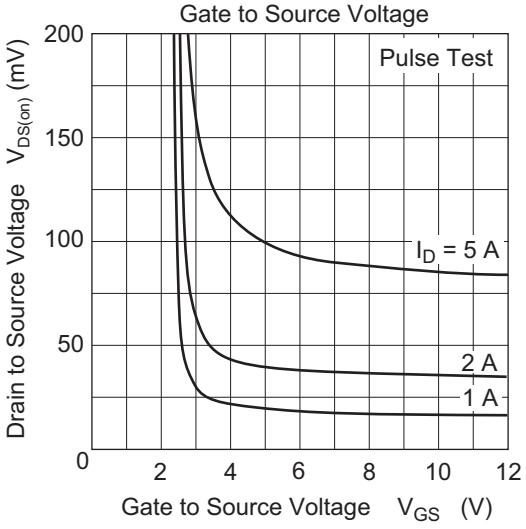
Typical Output Characteristics



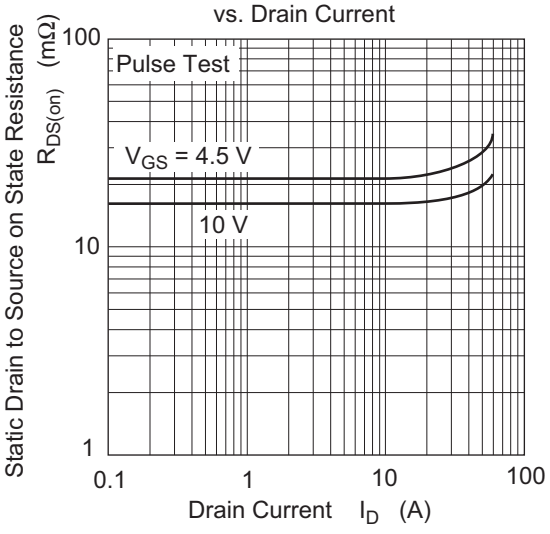
Typical Transfer Characteristics



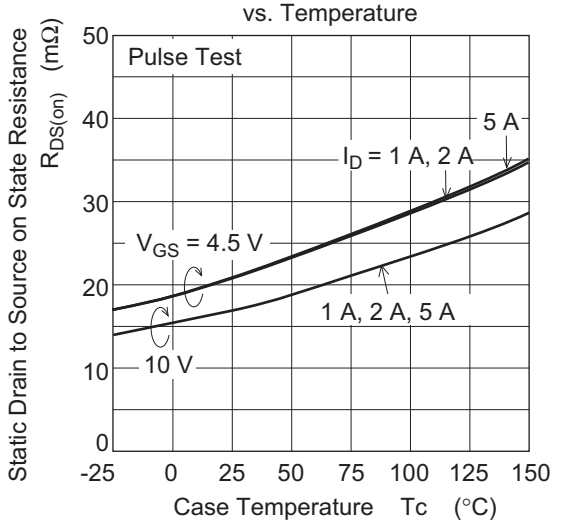
Drain to Source Saturation Voltage vs
Gate to Source Voltage



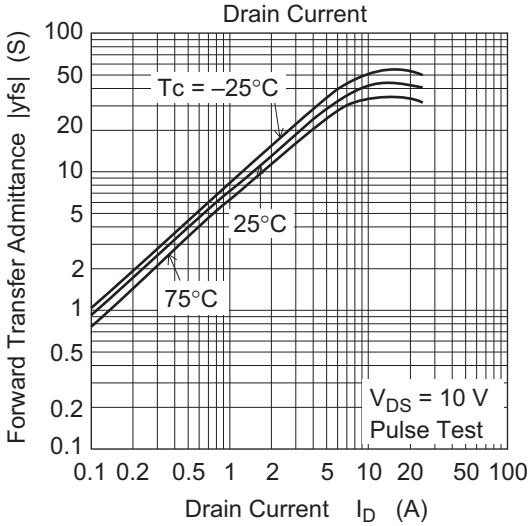
Static Drain to Source on State Resistance
vs. Drain Current



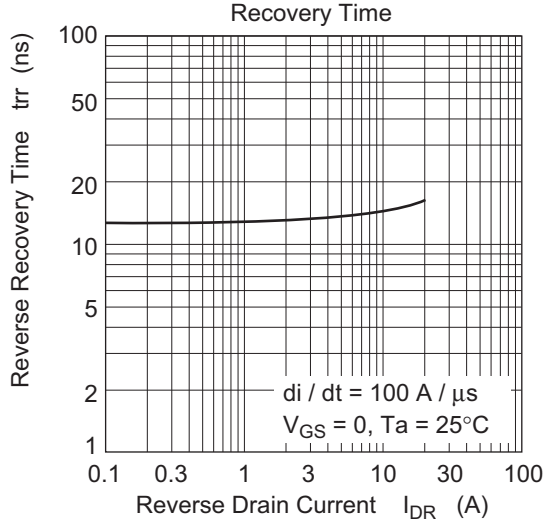
Static Drain to Source on State Resistance vs. Temperature



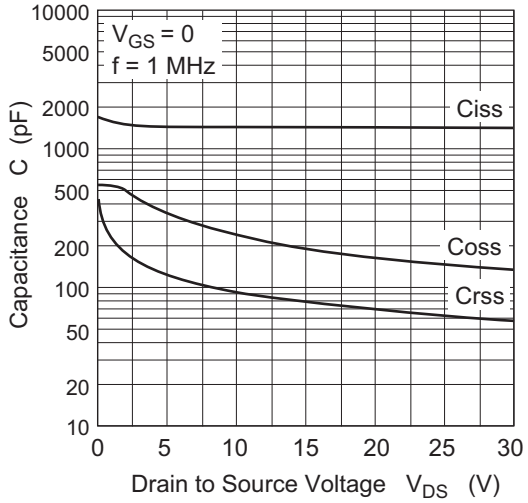
Forward Transfer Admittance vs. Drain Current



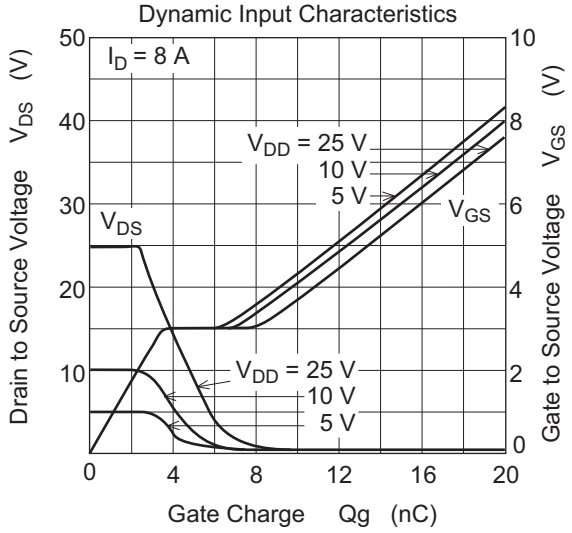
Body-Drain Diode Reverse Recovery Time



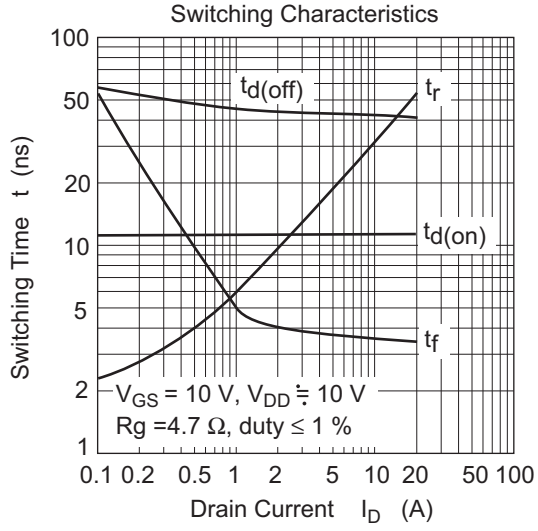
Typical Capacitance vs. Drain to Source Voltage



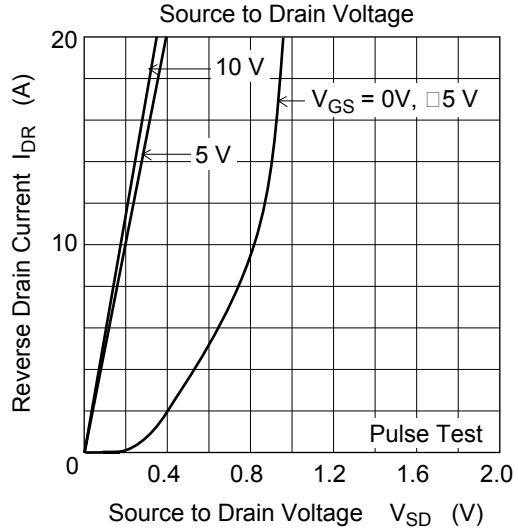
Dynamic Input Characteristics



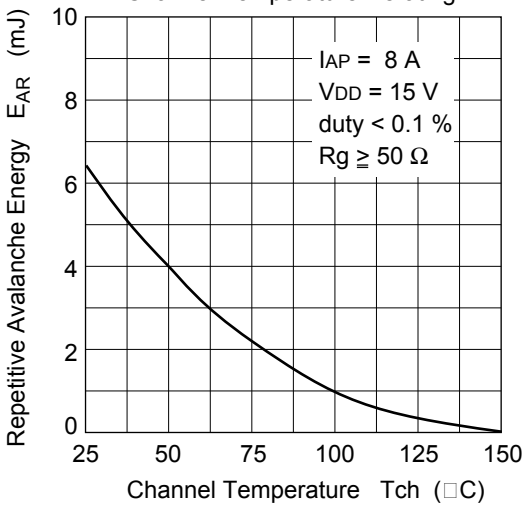
Switching Characteristics



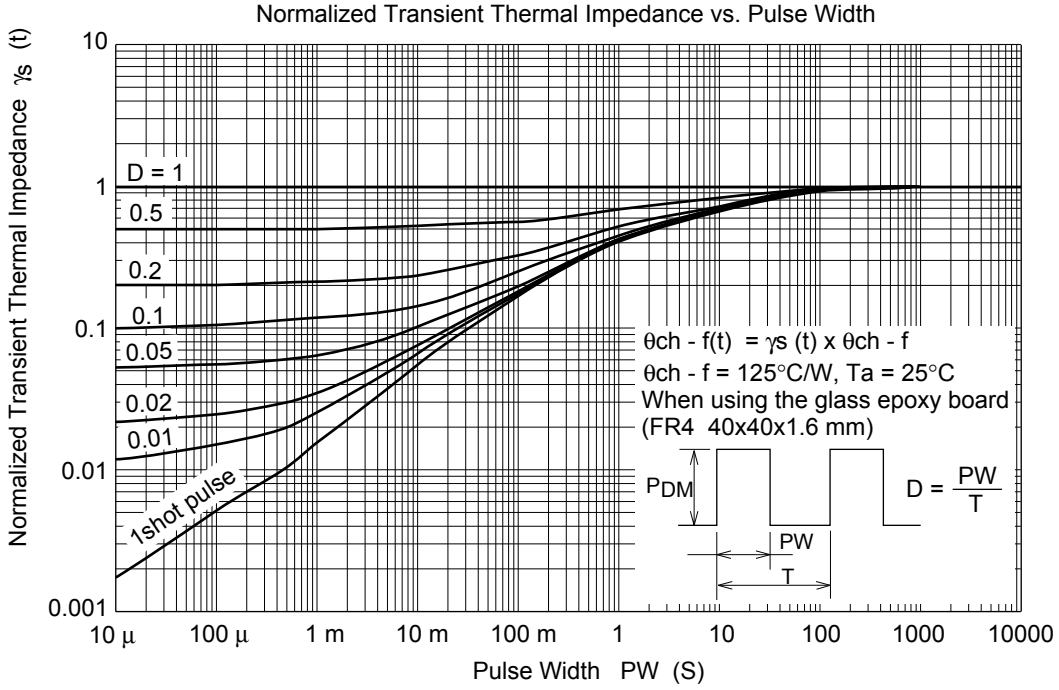
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

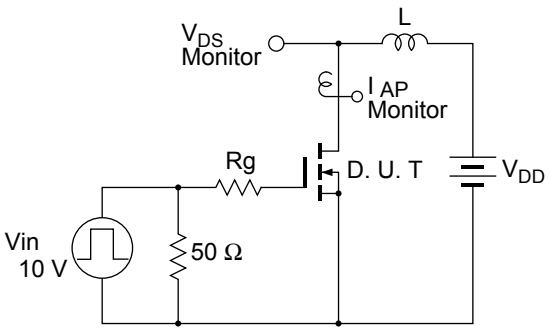


Normalized Transient Thermal Impedance vs. Pulse Width



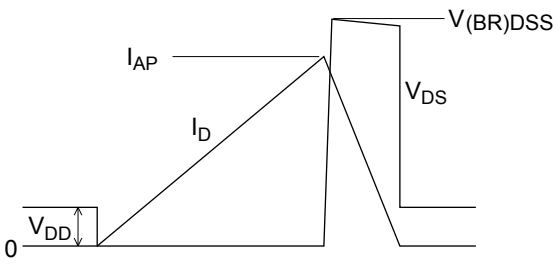
• Common

Avalanche Test Circuit

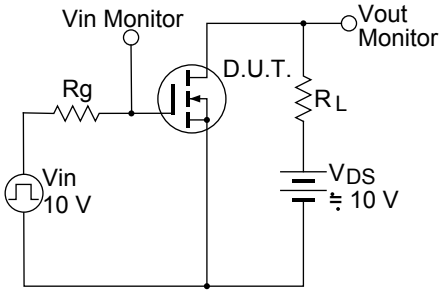


Avalanche Waveform

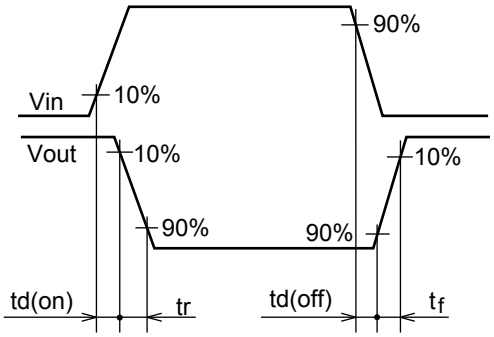
$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

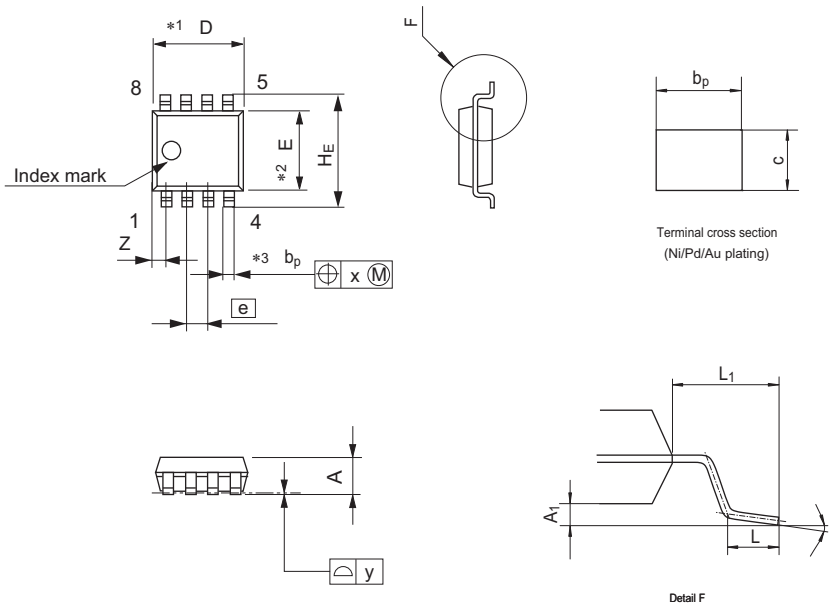


Switching Time Waveform



Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
HAT2210R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales Office to check the state of production before ordering the product.

General Precautions in the Handling of Power MOSFET and IGBT Products

The following usage notes are applicable to general purpose Power MOSFET and IGBT products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Derating

Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it are within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

2. Quality grade
   - The quality grade of this product is “Standard”.
   - If you plan to use this product to “High quality” application, please inform to Renesas.
   - Fail safe system is necessary to prevent malfunction even if this product is broken.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
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