HB56D136 Series

1,048,576-word × 36-bit High Density Dynamic RAM Module

HITACHI

ADE-203-209A (Z)
Rev 1.0
Sept. 20, 1994

Description

The HB56D136 is a 1-M × 36-bit dynamic RAM module, mounted 8 pieces of 4 Mbit DRAM (HM514400CS/CLS) sealed in SOJ package and 2 pieces of 2 Mbit DRAM (HM512200BS/BLS) sealed in SOJ package. An outline of the HB56D136 is 72-pin single in-line package.

Therefore, the HB56D136 makes high density mounting possible without surface mount technology. The HB56D136 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

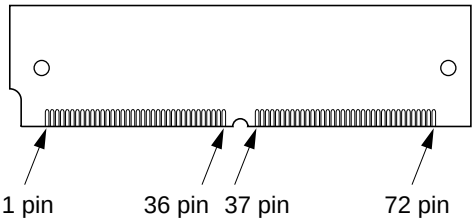
Features

- 72-pin
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode: 5.46 W/4.94 W/4.41 W (max)
  - — Standby mode: 105 mW (max)
    5.25 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms
  128 ms (L-version)
- 3 variations of refresh
  - — $\overline{\text{RAS}}$ only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56D136BW-6C	60 ns	72-pin SIP socket type	Gold
HB56D136BW-7C	70 ns		
HB56D136BW-8C	80 ns		
HB56D136BW-6CL	60 ns		
HB56D136BW-7CL	70 ns		
HB56D136BW-8CL	80 ns		
HB56D136SBW-6C	60 ns	72-pin SIP socket type	Solder
HB56D136SBW-7C	70 ns		
HB56D136SBW-8C	80 ns		
HB56D136SBW-6CL	60 ns		
HB56D136SBW-7CL	70 ns		
HB56D136SBW-8CL	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

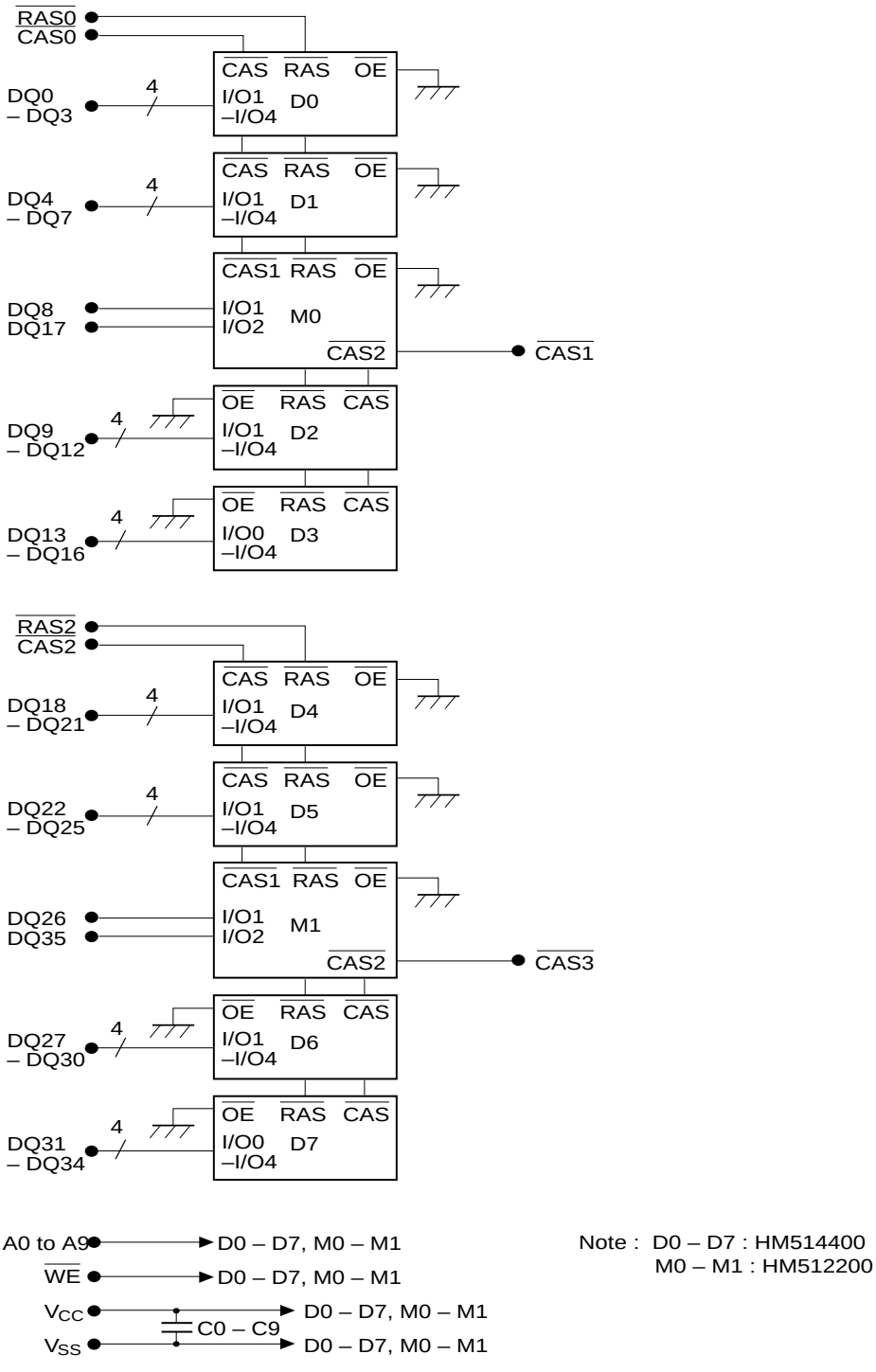
Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
DQ0 – DQ35	Data-in/data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pinout

		HB56D136		
Pin No.	**Pin Name**	**60 ns**	**70 ns**	**80 ns**
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	–1.0 to +7.0	V
	(Output)	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	10	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0V)

		HB56D136								
		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**Notes**
Operating current	I_{CC1}	—	1040	—	940	—	840	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	1, 2
Standby current	I_{CC2}	—	20	—	20	—	20	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	10	—	10	—	10	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.0	—	1.0	—	1.0	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, Add., Din = V_{IH} or V_{IL} Dout = High-Z	4
$\overline{RAS}$-only refresh current	I_{CC3}	—	1040	—	940	—	840	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	50	—	50	—	50	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC6}	—	1040	—	940	—	840	mA	t_{RC} = min	
First page mode current	I_{CC7}	—	1000	—	900	—	800	mA	t_{PC} = min	1, 3
Battery backup operating current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.0	—	2.0	—	2.0	mA	t_{RC} = 125 µs t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Add., Din = V_{IH} or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V and 0 ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	80	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	95	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	50	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

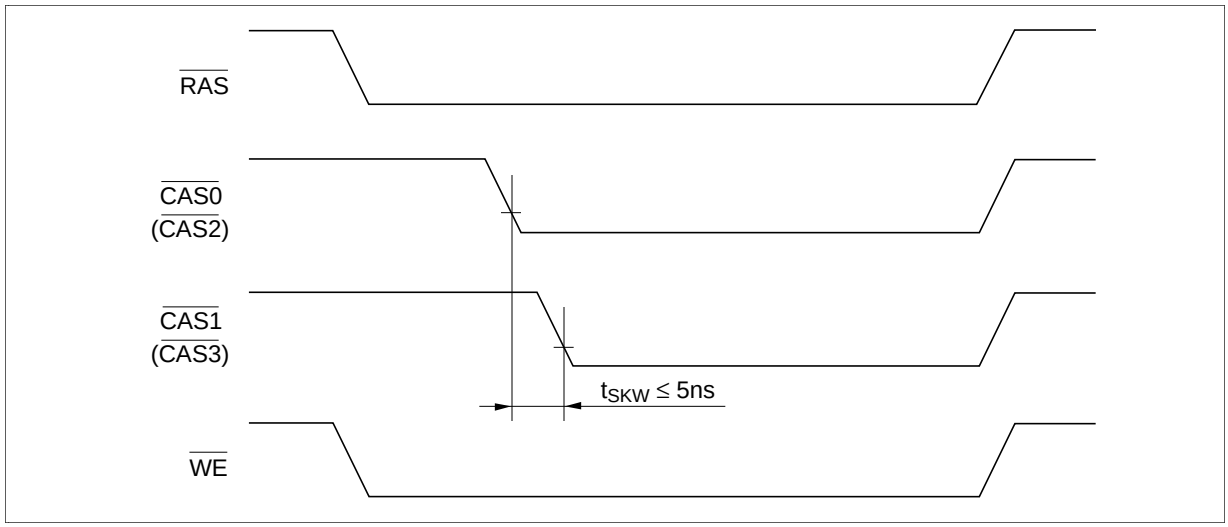
AC Characteristics

- Refer to the HB56D236 Series data sheet.
- The HB56D136 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available ($\overline{OE}$ pin is fixed to V_{SS}).

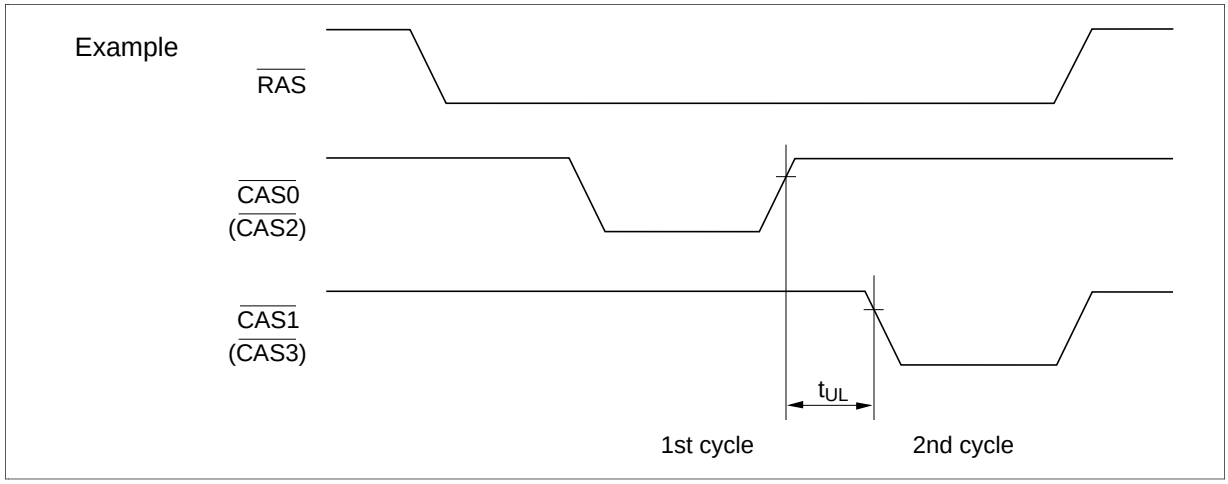
Notes on 2$\overline{CAS}$ control

(1) In one memory cycle, activate both of 2$\overline{CAS}$s ($\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) 5 ns or less.

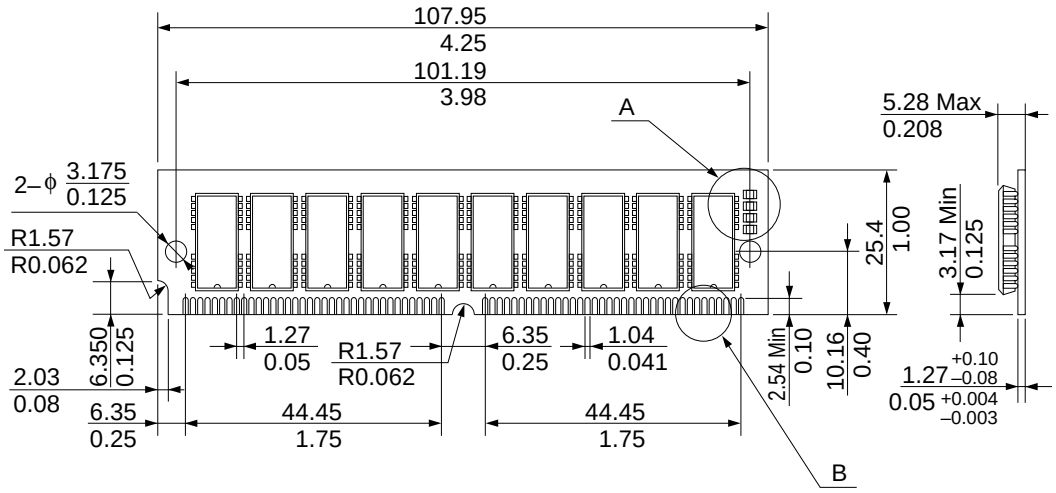


(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL} the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).

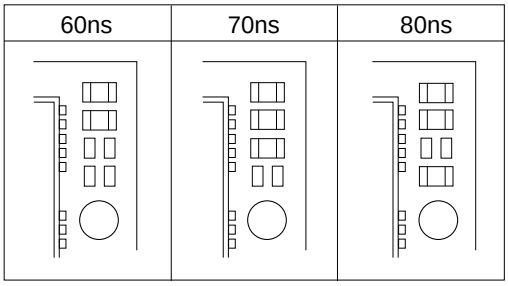


Physical Outline

Unit: mm/inch



Detal A



Detal B