PNP and NPN Dual Digital Transistors

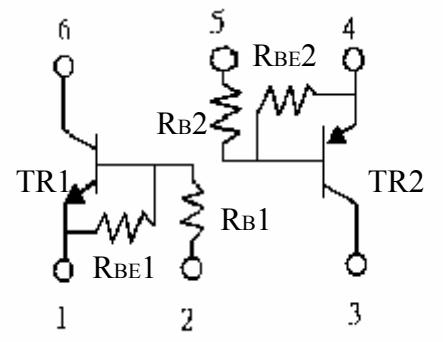
HBCA123JS6R

Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input for PNP transistor, and negative biasing of the input for NPN transistor. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- One DTA123J chip and one DTC123J chip in a SOT-363 package.
- Mounting by SOT-323 automatic mounting machines is possible.
- Mounting cost and area can be cut in half.
- Transistor elements are independent, eliminating interference.
- Pb-free lead plating and halogen-free package.

Equivalent Circuit

HBCA123JS6R

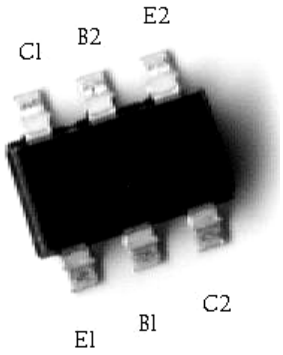


R_{B1}=2.2kΩ , R_{B2}=2.2kΩ

R_{BE1}=47kΩ , R_{BE2}=47kΩ

Outline

SOT-363R



Ordering Information

Device	Package	Shipping	Marking
HBCA123JS6R	SOT-363 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel	35

Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limits		Unit
		Tr1(NPN)	Tr2(PNP)	
Supply Voltage	V_{CC}	50	-50	V
Input Voltage	V_{IN}	-5~+12	-12~+5	V
Output Current	I_O	100	-100	mA
	$I_{O(max.)}$	100	-100	mA
Total Power Dissipation	Pd	150 (Note)		mW
Junction Temperature	Tj	150		°C
Storage Temperature	Tstg	-55~+150		°C

Note : 120mW per element must not be exceeded.

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	833	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	357	°C/W

Characteristics (Ta=25℃)

•Tr1(NPN)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	$V_{I(off)}$	-	-	0.5	V	V_{CC}=5V, I_O=100μA
	$V_{I(on)}$	1.1	-	-	V	V_O=0.3V, I_O=5mA
Output Voltage	$V_{O(on)}$	-	-	0.3	V	I_O/I_I=5mA/0.25mA
Input Current	I_I	-	-	3.6	mA	V_I=5V
Output Current	$I_{O(off)}$	-	-	0.5	μA	V_{CC}=50V, V_I=0V
DC Current Gain	G_I	80	-	-	-	V_O=5V, I_O=10mA
Input Resistance	R_1	1.54	2.2	2.86	kΩ	-
Resistance Ratio	R_2/R_1	17	21	26	-	-
Transition Frequency	f_T	-	250	-	MHz	V_{CE}=10V, I_C=5mA, f=100MHz *

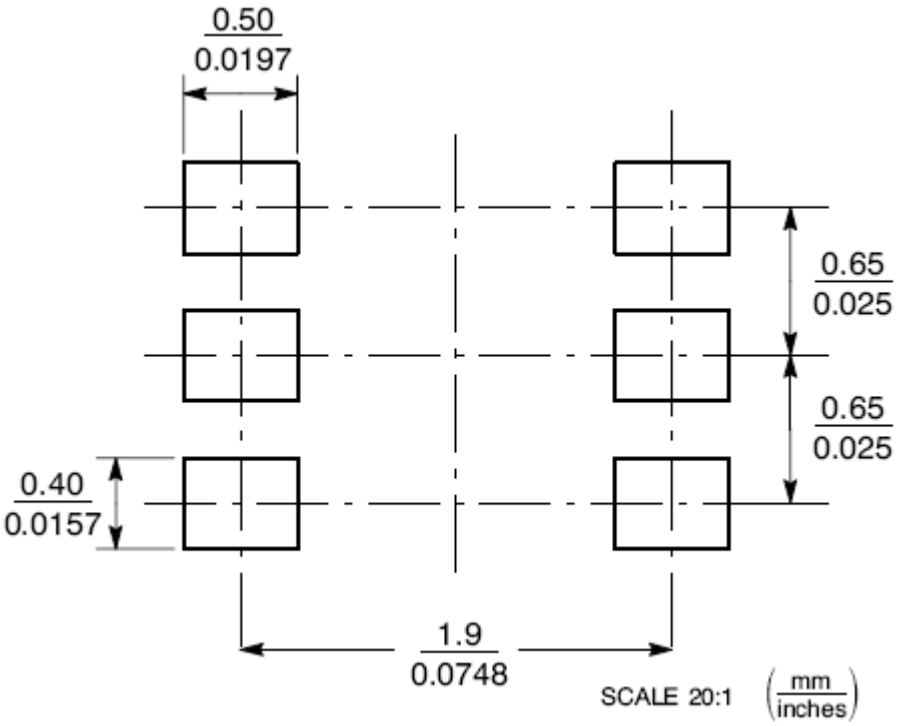
* Transition frequency of the device

•Tr2(PNP)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	$V_{I(off)}$	-	-	-0.5	V	V_{CC}=-5V, I_O=-100μA
	$V_{I(on)}$	-1.1	-	-	V	V_O=-0.3V, I_O=-5mA
Output Voltage	$V_{O(on)}$	-	-	-0.3	V	I_O/I_I=-5mA/-0.25mA
Input Current	I_I	-	-	-3.6	mA	V_I=-5V
Output Current	$I_{O(off)}$	-	-	-0.5	μA	V_{CC}=-50V, V_I=0V
DC Current Gain	G_I	80	-	-	-	V_O=-5V, I_O=-10mA
Input Resistance	R_1	1.54	2.2	2.86	kΩ	-
Resistance Ratio	R_2/R_1	17	21	26	-	-
Transition Frequency	f_T	-	250	-	MHz	V_{CE}=-10V, I_C=-5mA, f=100MHz *

* Transition frequency of the device

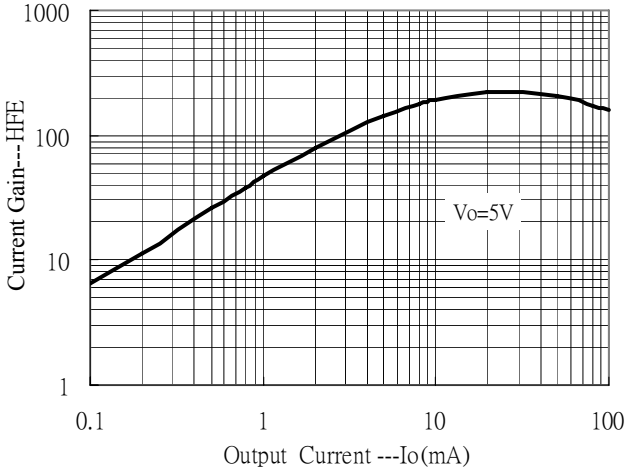
Recommended Soldering Footprint



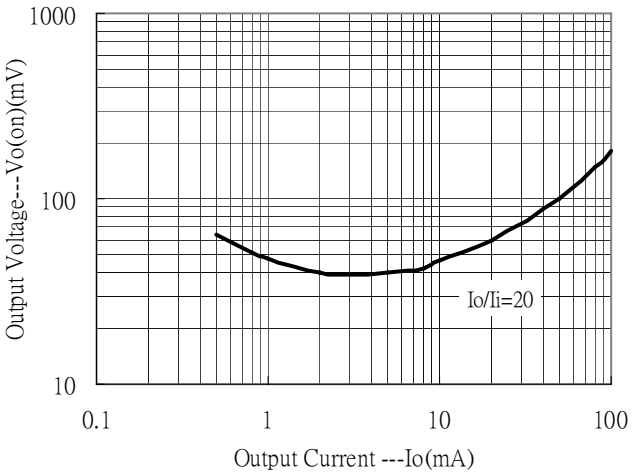
Typical Characteristics

•Tr1(NPN)

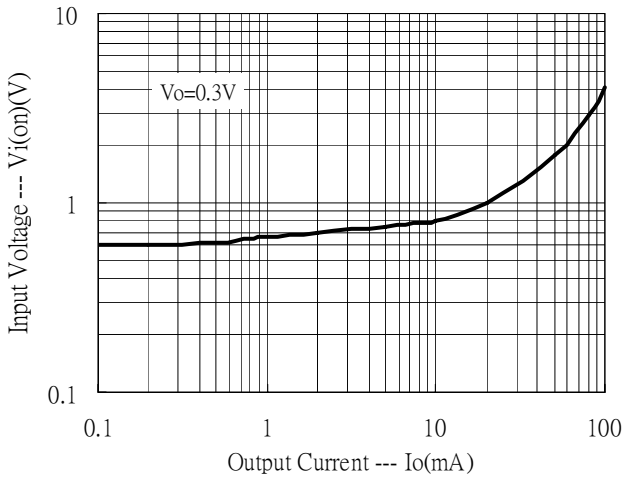
DC Current Gain vs Output Current



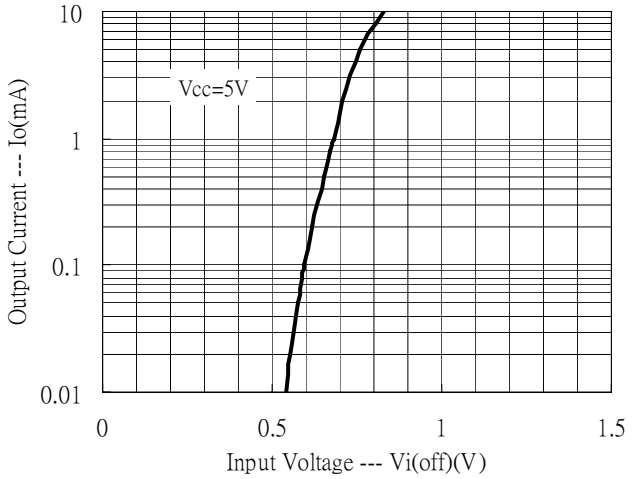
Output Voltage vs Output Current



Input Voltage vs Output Current (ON Characteristics)

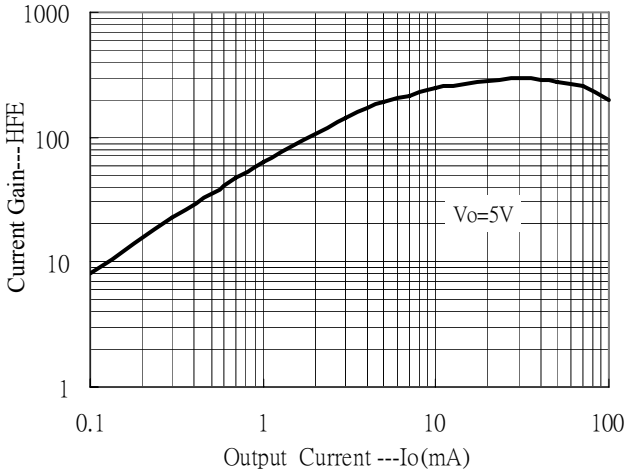


Output Current vs Input Voltage (OFF Characteristics)

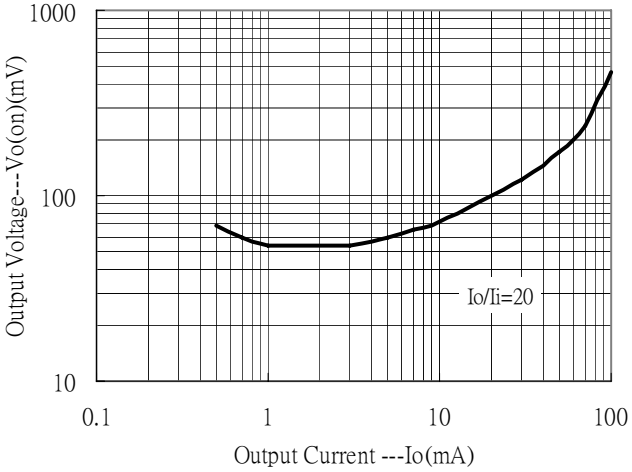


•Tr2(PNP)

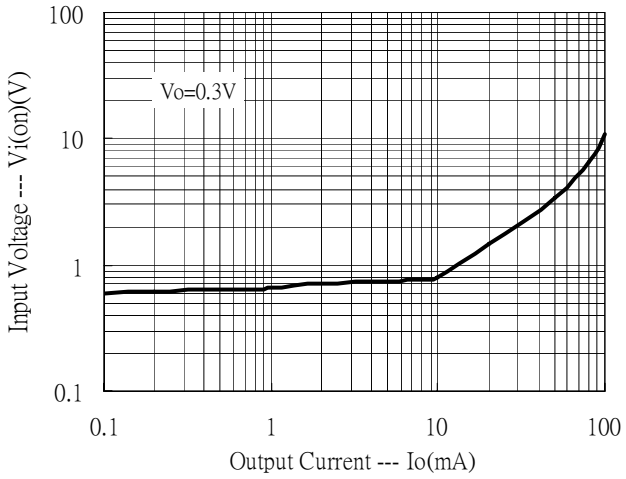
DC Current Gain vs Output Current



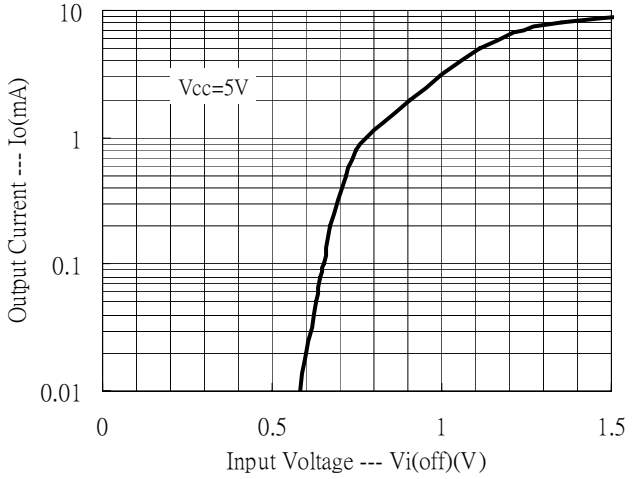
Output Voltage vs Output Current



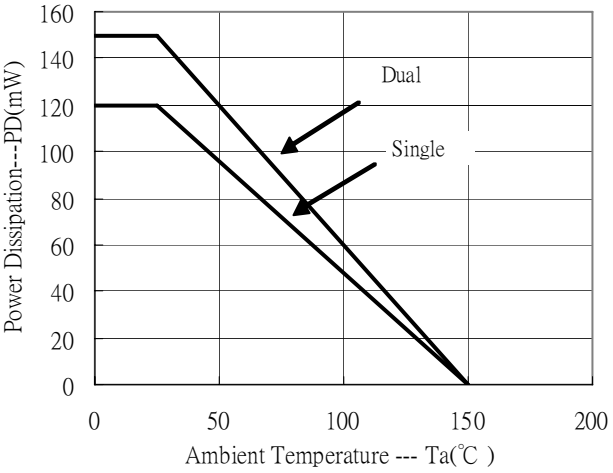
Input Voltage vs Output Current (ON Characteristics)



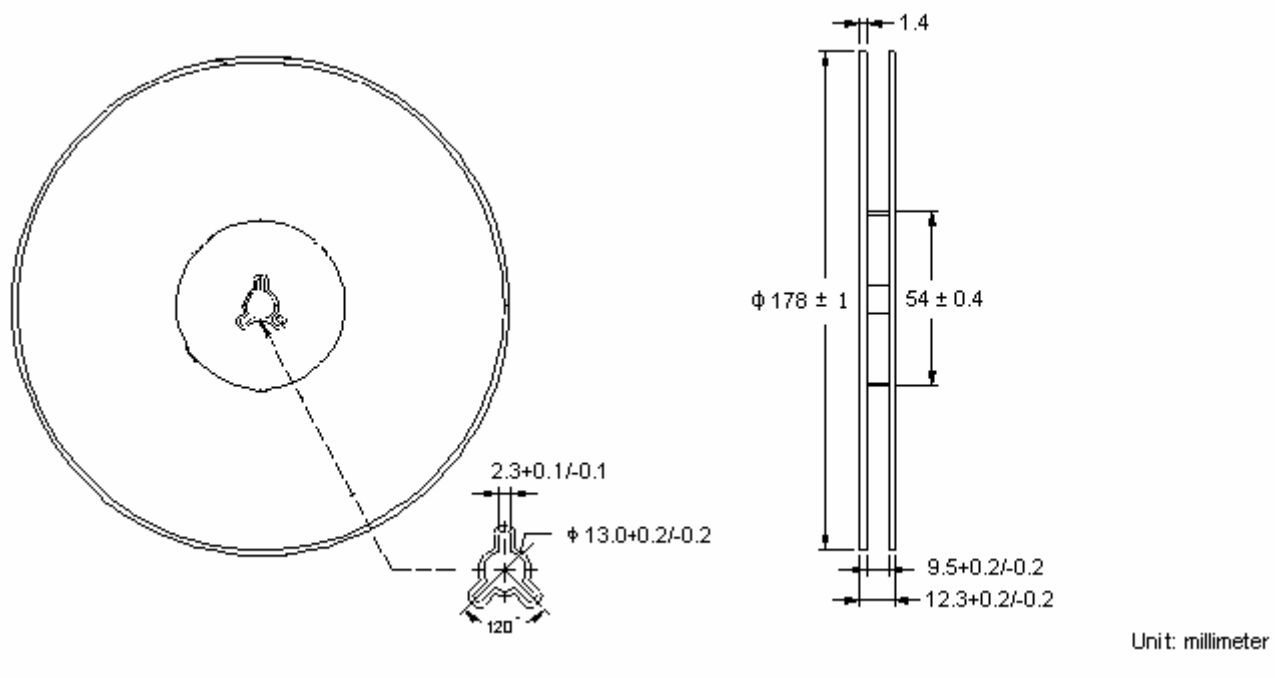
Output Current vs Input Voltage (OFF Characteristics)



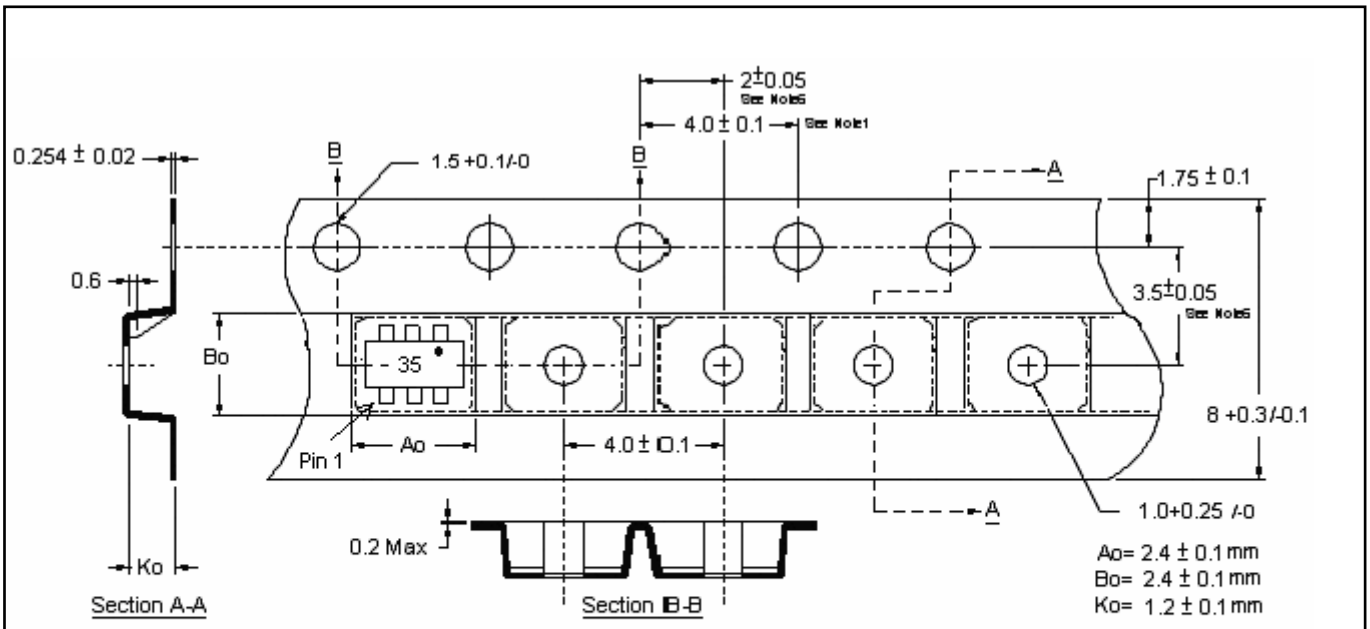
Power Derating Curves



Reel Dimension



Carrier Tape Dimension



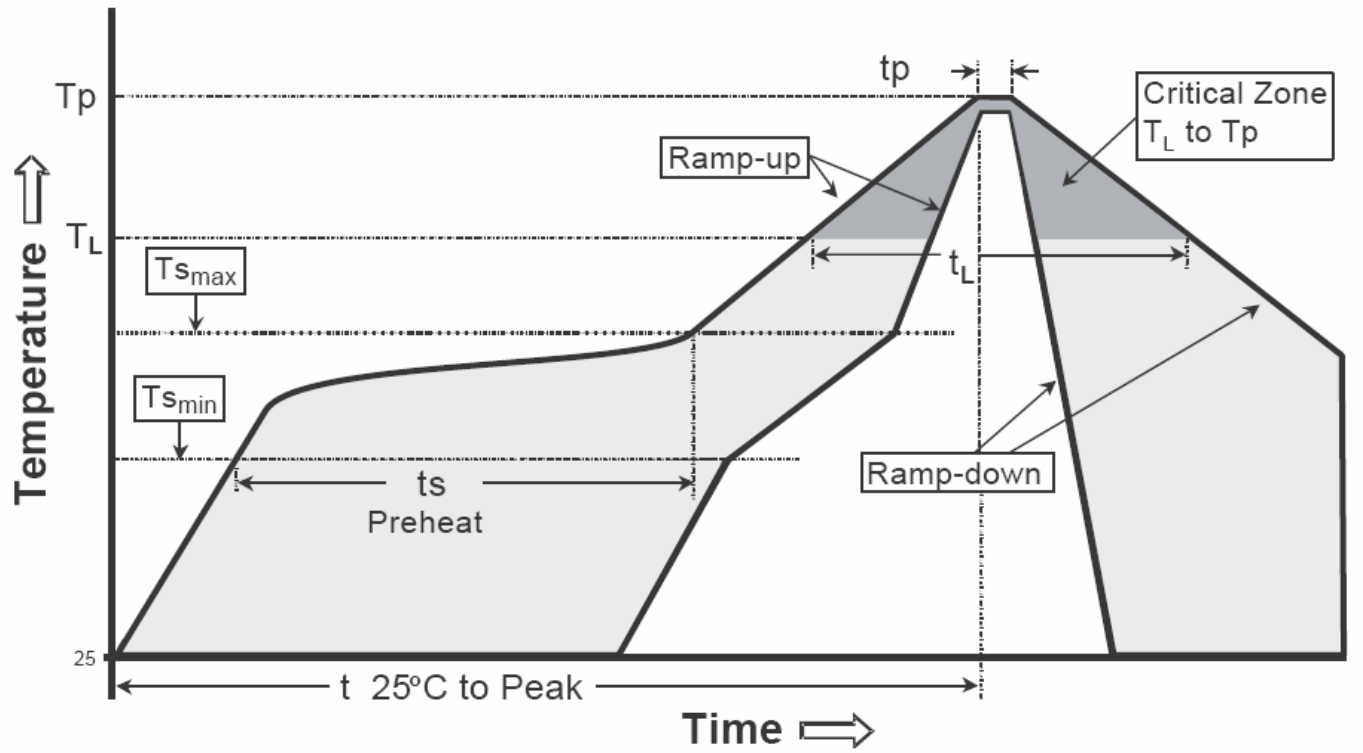
Notes:
1. 10 sprocket hole pitch cumulative tolerace ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

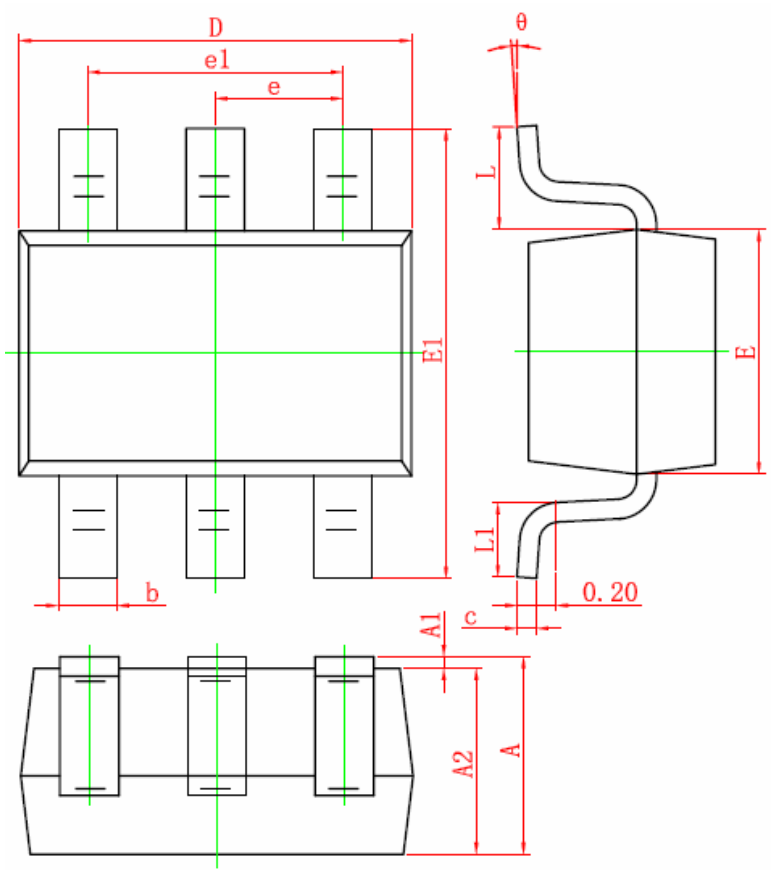
Recommended temperature profile for IR reflow



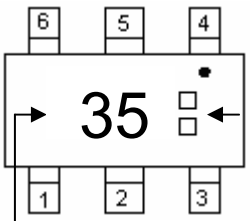
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



Marking:



Date Code:
Year + Month
Year : 6→2006, 7→2007,…, etc
Month : 1→Jan 2→Feb, …, 9→Sep, A→Oct, B→Nov, C→Dec

Device Code

6-Lead SOT-363R Plastic Surface Mounted Package
CYStek Package Code: S6R

Style:
Pin 1. Emitter1 (E1)
Pin 2. Base1 (B1)
Pin 3. Collector2 (C2)
Pin 4. Emitter2 (E2)
Pin 5. Base2 (B2)
Pin 6. Collector1 (C1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650 TYP		0.026 TYP	
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525 REF		0.021 REF	
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.