

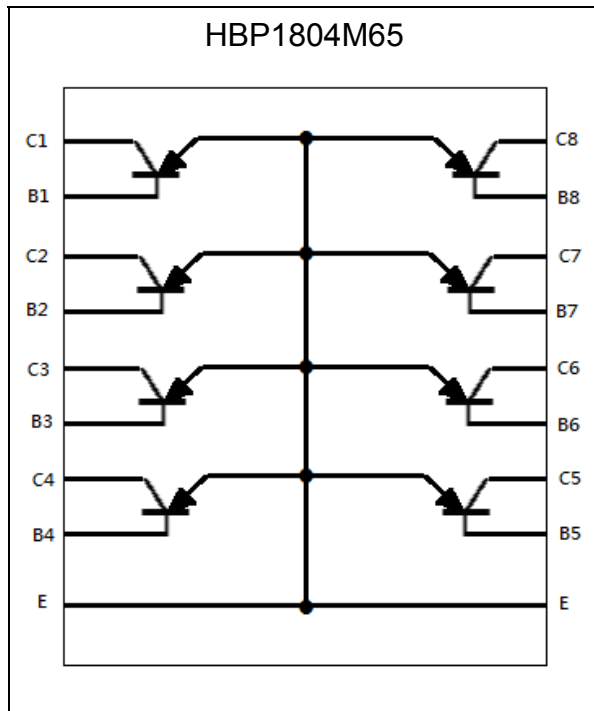
Octuple High Voltage PNP Epitaxial Planar Transistor

HBP1804M65

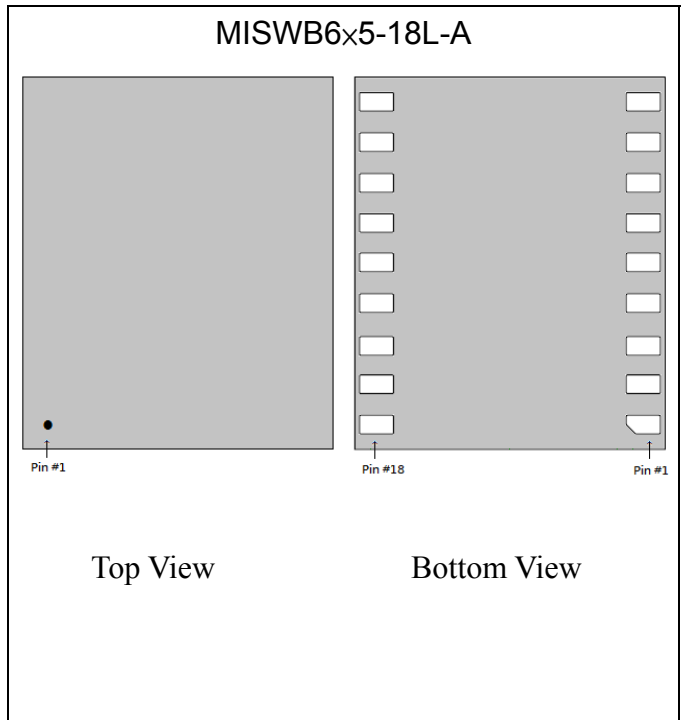
Description

- High breakdown voltage. ($BV_{CEO} = -400V$)
- Low saturation voltage, typical $V_{CE(sat)} = -0.17V$ at $I_c/I_B = -20mA/-1mA$.
- Complementary to HBN1803M65
- Pb-free lead plating and halogen-free package

Equivalent Circuit



Outline





The following ratings and characteristics apply to each transistor in this device.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	-400	V
Collector-Emitter Voltage	V _{CEO}	-400	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current	I _C	-300	mA
Total Power Dissipation	P _d	1.5	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

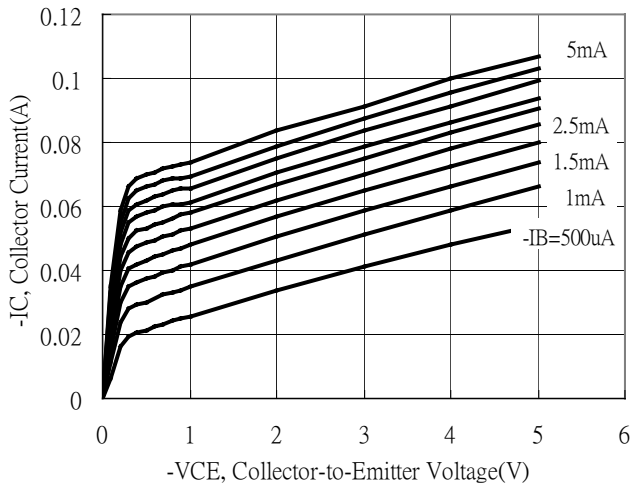
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	-400	-	-	V	I _C =-50μA
BV _{CEO}	-400	-	-	V	I _C =-1mA
BV _{EBO}	-5	-	-	V	I _E =-50μA
I _{CB0}	-	-	-100	nA	V _{CB} =-400V
I _{CES}	-	-	-100	nA	V _{CE} =-300V, R _{EB} =0Ω
I _{EBO}	-	-	-100	nA	V _{EB} =-5V
*V _{CE(sat)}	-	-0.17	-0.3	V	I _C =-20mA, I _B =-1mA
*V _{CE(sat)}	-	-0.18	-0.3	V	I _C =-50mA, I _B =-5mA
*V _{CE(sat)}	-	-0.18	-0.3	V	I _C =-100mA, I _B =-20mA
*V _{BE(sat)}	-	-0.73	-1	V	I _C =-20mA, I _B =-2mA
*h _{FE}	50	-	300	-	V _{CE} =-10V, I _C =-10mA
*h _{FE}	40	-	-	-	V _{CE} =-10V, I _C =-100mA
f _T	-	100	-	MHz	V _{CE} =-10V, I _C =-10mA, f=5MHz
C _{ob}	-	4.6	-	pF	V _{CB} =-10V, I _E =0A, f=1MHz

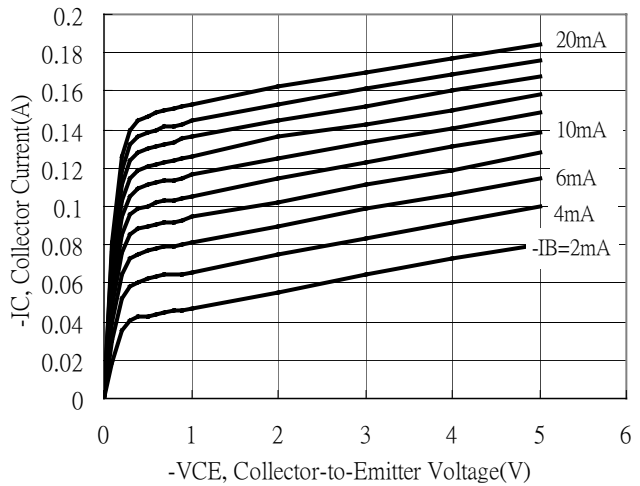
*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Typical Characteristics

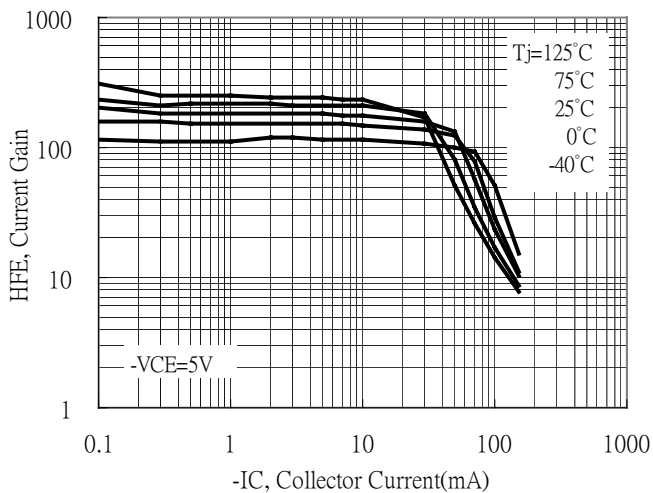
Emitter Grounded Output Characteristics



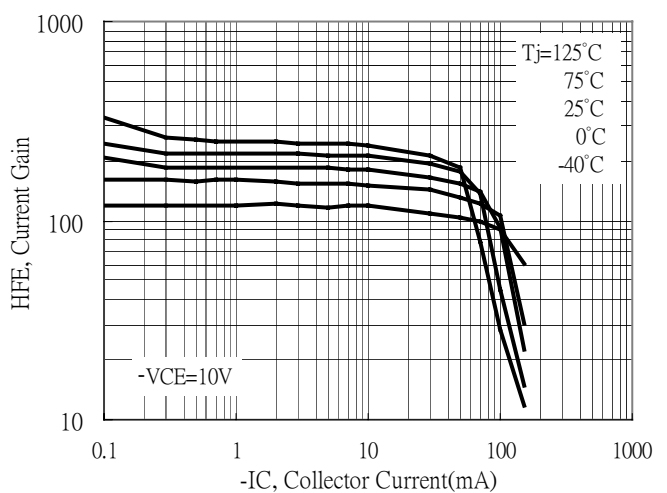
Emitter Grounded Output Characteristics



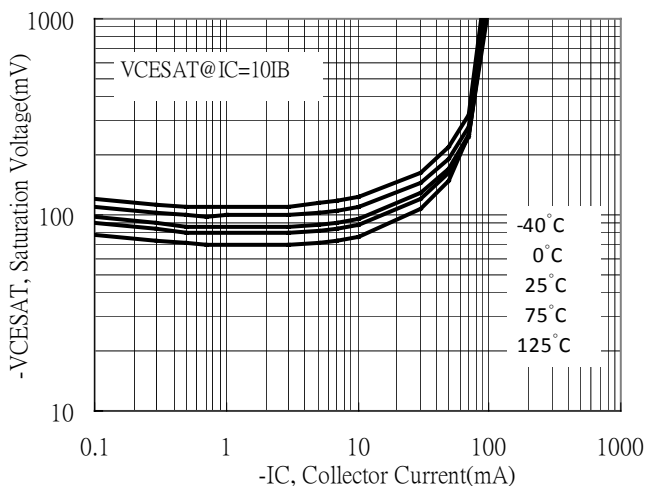
Current Gain vs Collector Current



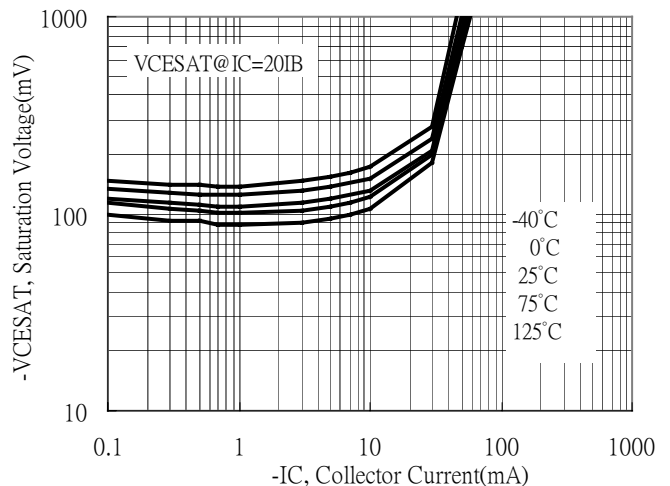
Current Gain vs Collector Current



Saturation Voltage vs Collector Current



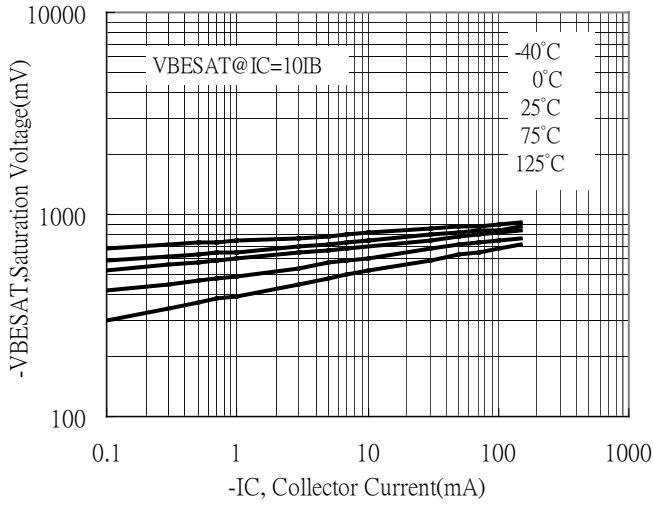
Saturation Voltage vs Collector Current



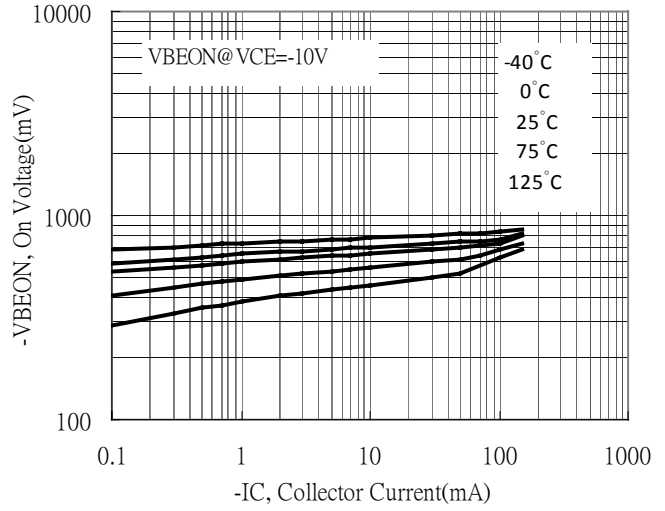


Typical Characteristics(Cont.)

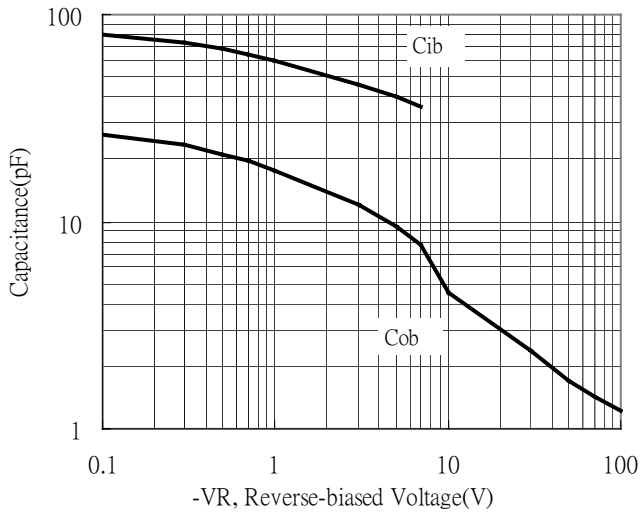
Saturation Voltage vs Collector Current



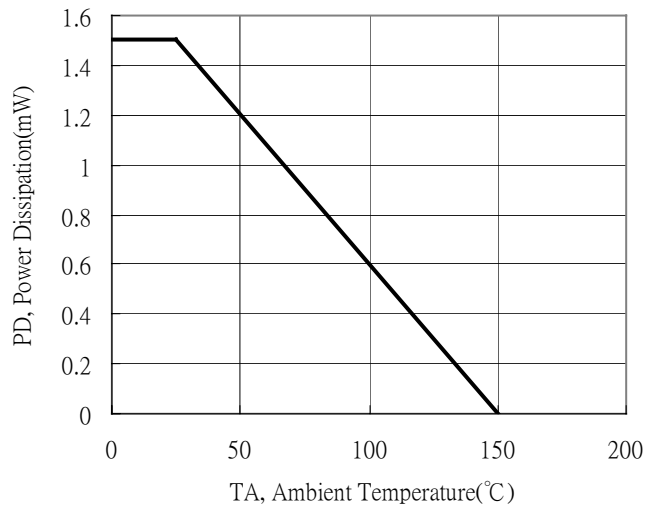
On Voltage vs Collector Current



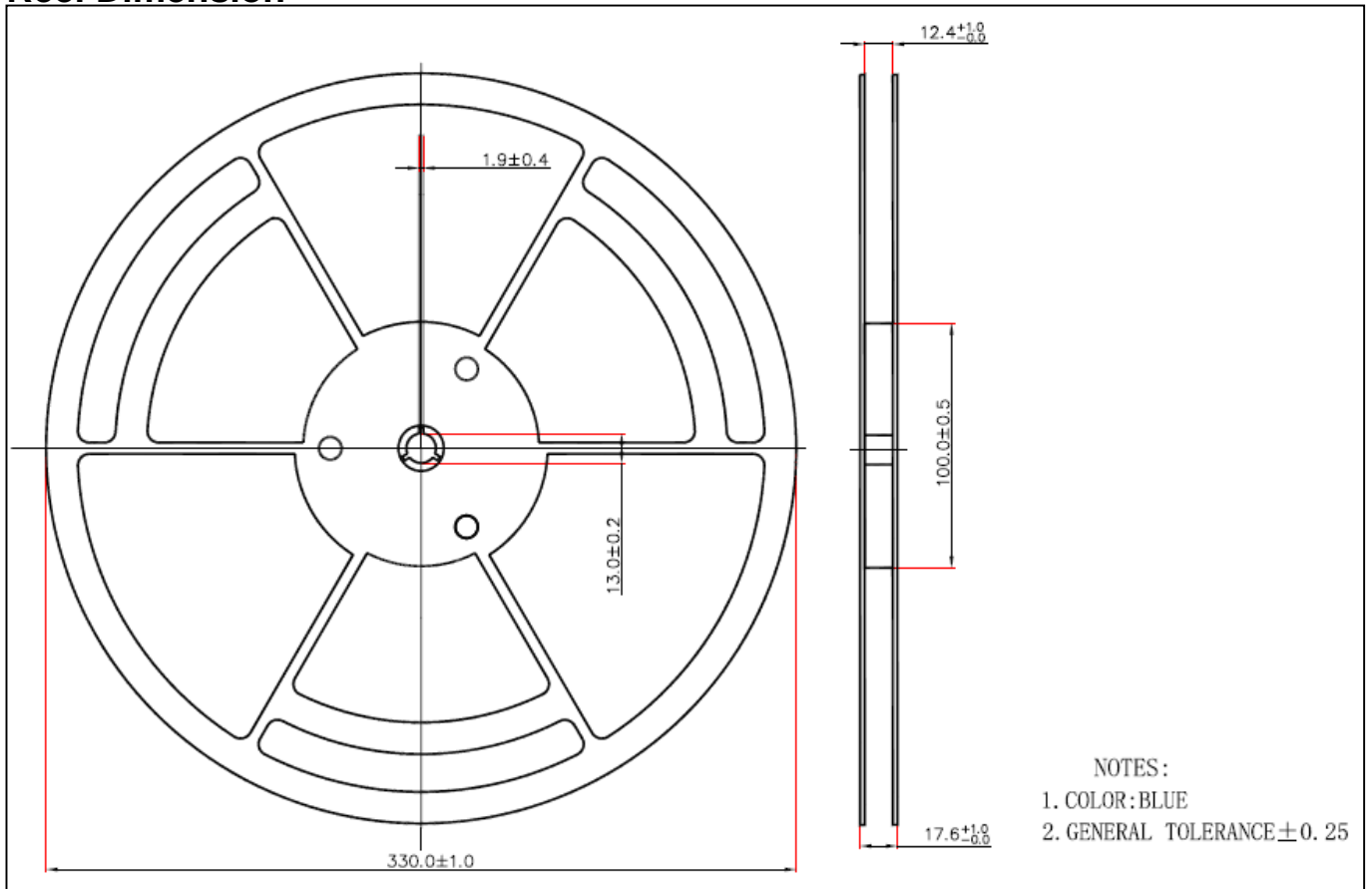
Capacitance vs Reverse-biased Voltage



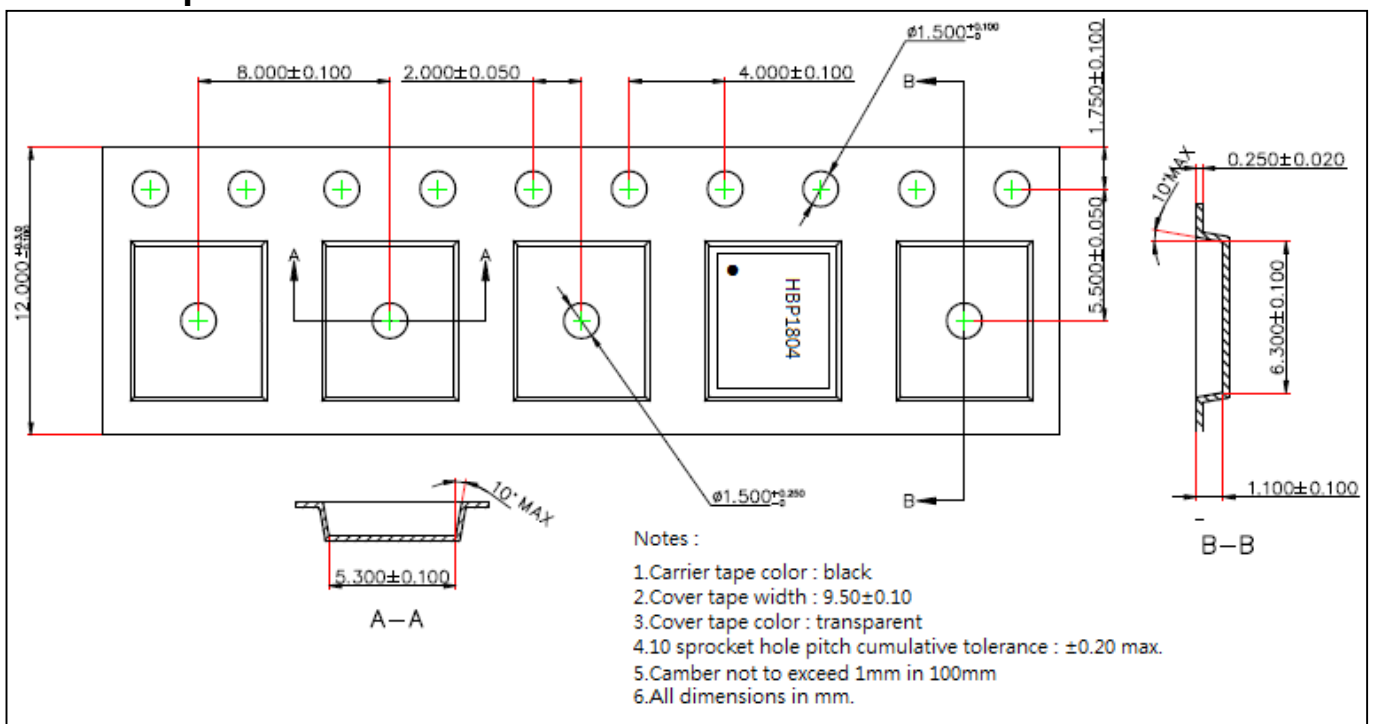
Power Derating Curve



Reel Dimension



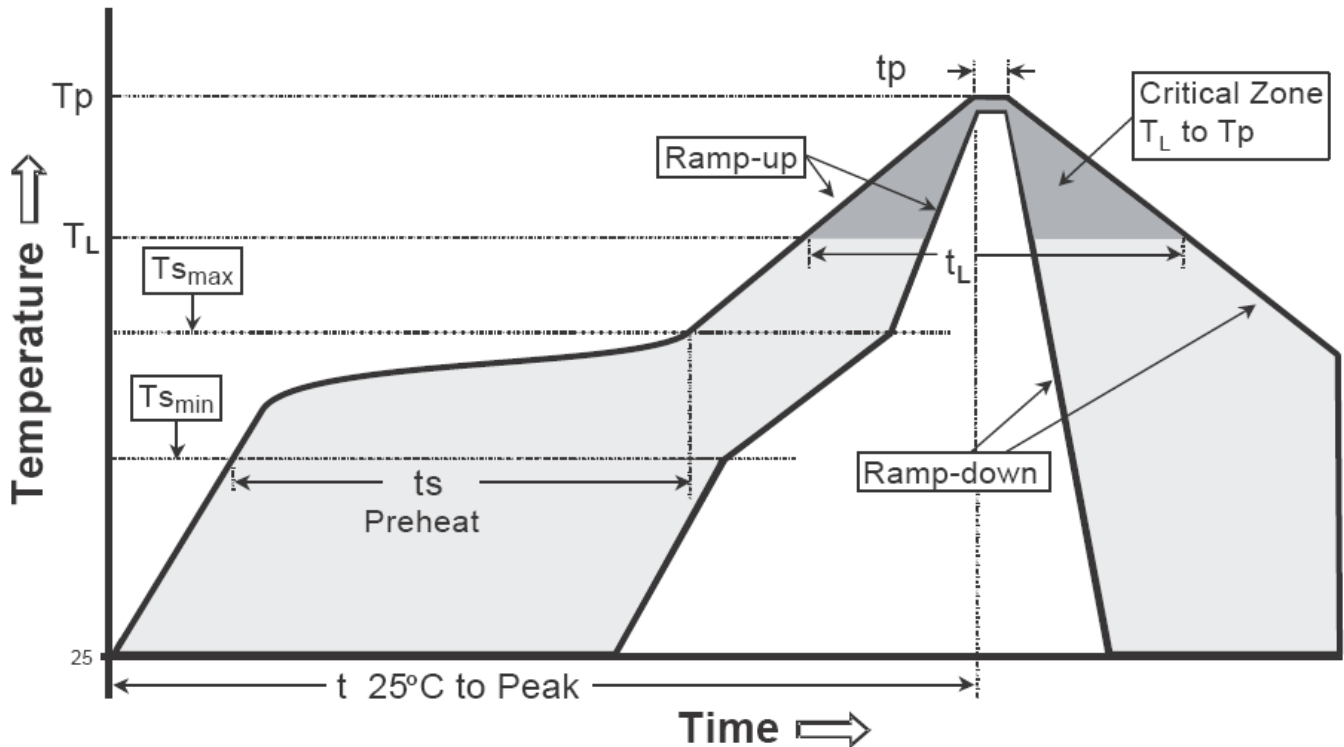
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

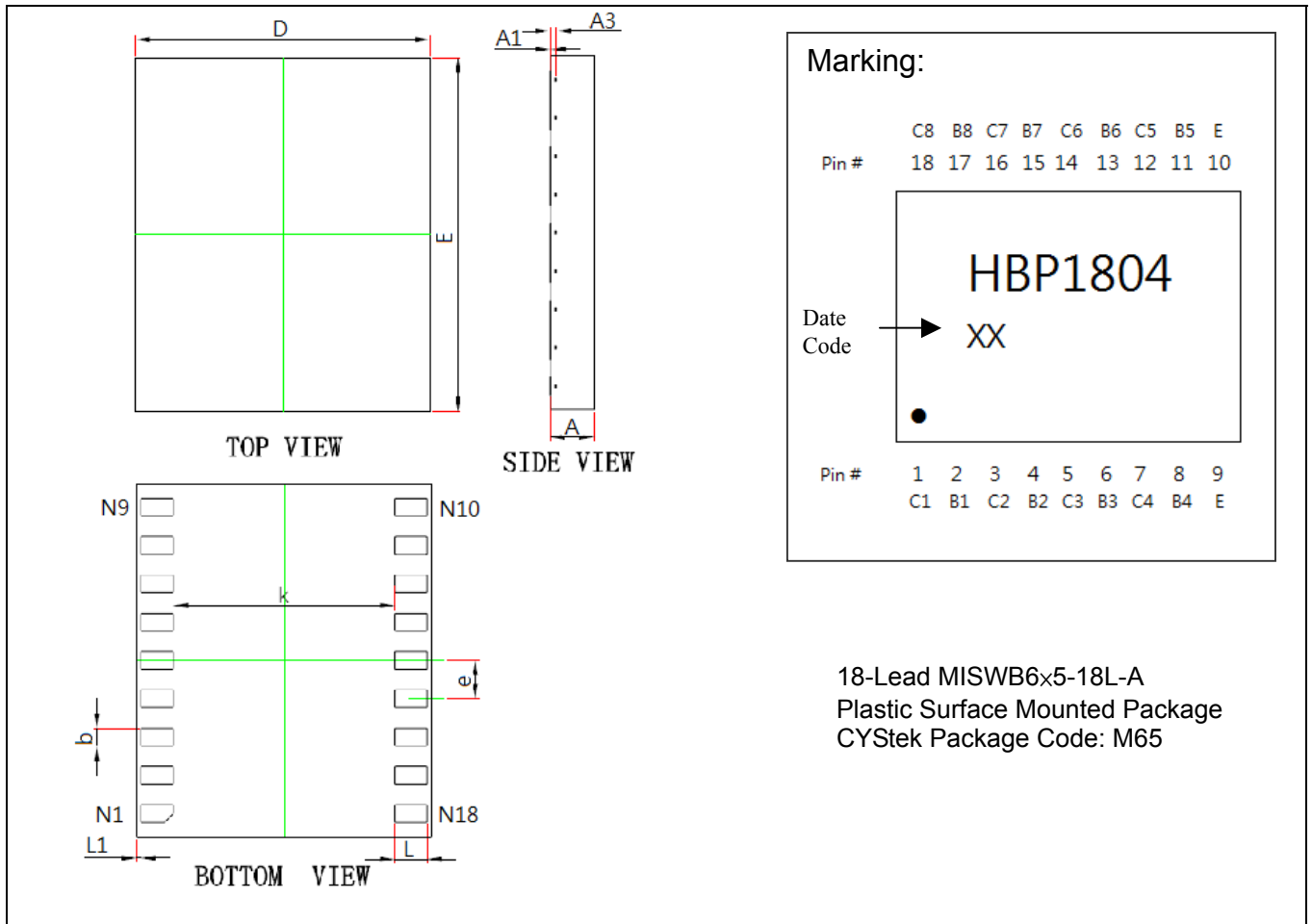
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

MISWB6x5-18L-A Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031	k	3.750	REF	0.148	REF
A1	0.000	0.046	0.000	0.002	b	0.250	0.350	0.010	0.014
A3	0.110	REF	0.004	REF	e	0.0531	0.0689	1.35	1.75
D	4.900	5.100	0.193	0.201	L	0.650	BSC	0.026	BSC
E	5.900	6.100	0.232	0.240	L1	0.075	REF	0.003	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.