Data Sheet | January 1997 | File Number 2887.2

PCM Transcoder

The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution) and AMI (Alternate Mark Inversion).

The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible.

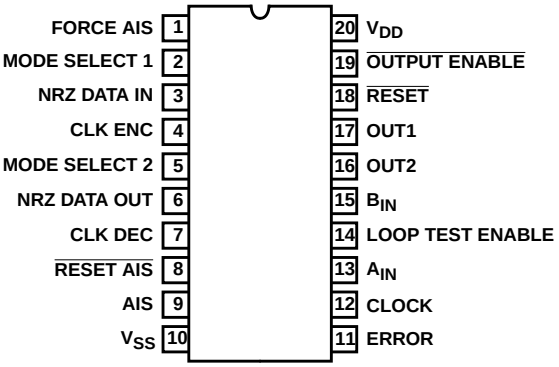
Application Note #573, "The HC-5560 Digital Line Transcoder," by D.J. Donovan is available.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HC3-5560-5	0 to 70	20 Ld PDIP	E20.3

Pinout

HC-5560
(PDIP)
TOP VIEW



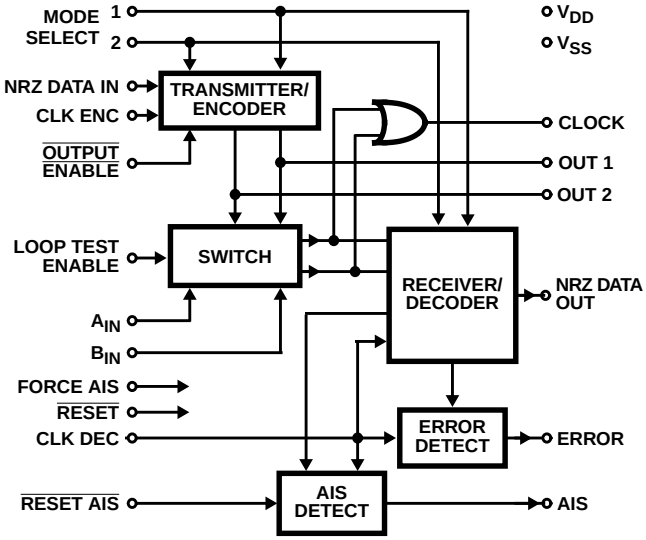
Features

- Single 5V Supply . . . . . .10mA (Typ)
- Mode Selectable Coding Including:
  - AMI (T1, T1C)
  - B8ZS (T1)
  - HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces MJ1440, MJ1471 and TCM2201 Transcoders

Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellors, Digital Cross-Connects (DSXs), T1 Compressors, etc.
- Related Literature
  - AN573, The HC-5560 Digital Line Transcoder

Functional Diagram



Absolute Maximum Ratings

Voltage at Any Pin . . . . . GND -0.3V to V_{DD} 0.3V
Maximum V_{DD} Voltage 7.0V

Operating Conditions

Operating Temperature Range . . . . . 0^oC to 70^oC
Operating V_{DD} . . . . . 5V ±5%

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
PDIP Package 67
Maximum Junction Temperature . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^o

Die Characteristics

Transistor Count 4322
Die Dimensions . . . . . .119 mils x 133 mils
Substrate Potential . . . . . +V
Process . . . . . SAJI CMOS

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, Typical parameters at 25^oC, Min-Max parameters are over operating temperature range. V_{DD} = 5V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS					
Quiescent Device Current	I_{DD}			100	µA
Operating Device Current			10		mA
OUT1, OUT2 Low (Sink) Current (V_{OL} = 0.4V)	I_{OL1}	3.2			mA
All Other Outputs Low (Sink) Current (V_{OL} = 0.8V)	I_{OL2}	2			mA
All Outputs High (Source) Current (V_{OH} = 4V)	I_{OH}	2			mA
Input Low Current	I_{IL}			10	µA
Input High Current	I_{IH}			10	µA
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.4			V
Input Capacitance	C_{IN}			8	pF

Electrical Specifications

Unless Otherwise Specified, Typical parameters at 25^oC, Min-Max parameters are over operating temperature range. V_{DD} = 5V

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
DYNAMIC SPECIFICATIONS						
CLK ENC, CLK DEC Input Frequency	f_{CL}				8.5	MHz
CLK ENC,CLK DEC Rise Time (1.544MHz)	t_{RCL}	1, 2		10	60	ns
Fall Time	t_{FCL}	1, 2		10	60	ns
Rise Time (2.048MHz)	t_{RCL}	1, 2		10	40	ns
Fall Time	t_{FCL}	1, 2		10	40	ns
Rise Time (6.3212MHz)	t_{RCL}	1, 2		10	30	ns
Fall Time	t_{FCL}	1, 2		10	30	ns
Rise Time (8.448MHz)	t_{RCL}	1, 2		5	10	ns
Fall Time	t_{FCL}	1, 2		5	10	ns

Electrical Specifications Unless Otherwise Specified, Typical parameters at 25°C, Min-Max parameters are over operating temperature range. V_{DD} = 5V **(Continued)**

PARAMETER	SYMBOL	FIGURE	MIN	TYP	MAX	UNITS
NRZ-Data In to CLK ENC Data Setup Time	t_S	1	20	-	-	ns
Data Hold Time	t_H	1	20	-	-	ns
A_{IN}, B_{IN} to CLK DEC Data Setup Time	t_S	2	15	-	-	ns
Data Hold Time	t_H	2	5	-	-	ns
CLK ENC to OUT1, OUT2	t_{DD}	1	-	23	80	ns
OUT1, OUT2 Pulse Width (CLK ENC Duty Cycle = 50%)						
f_{CL} = 1.544MHz	t_W	1	-	324	-	ns
f_{CL} = 2.048MHz	t_W	1	-	224	-	ns
f_{CL} = 6.3212MHz	t_W	1	-	79	-	ns
f_{CL} = 8.448MHz	t_W	1	-	58	-	ns
CLK DEC to NRZ-Data Out	t_{DD}	2	-	25	54	ns
Setup Time CLK DEC to $\overline{\text{Reset AIS}}$	t_{S2}	3	35	-	-	ns
Hold Time of $\overline{\text{Reset AIS}}$ = '0'	t_{H2}	3	20	-	-	ns
Setup Time $\overline{\text{Reset AIS}}$ = '1' to CLK DEC	t_{S2}	3	0	-	-	ns
$\overline{\text{Reset AIS}}$ to AIS output	t_{PD5}	3	-	-	42	ns
CLK DEC to Error output	t_{PD4}	3	-	-	62	ns

Pin Descriptions

PIN NUMBER	FUNCTION	DESCRIPTION
1	Force AIS	Pin 19 must be at logic '0' to enable this pin. A logic '1' on this pin forces OUT1 and OUT2 to all '1's. A logic '0' on this pin allows normal operation.
2, 5	Mode Select 1, Mode Select 2	MS1 / MS2 / Functions As 0 / 0 / AMI 0 / 1 / B8ZS 1 / 0 / B6ZS 1 / 1 / HDB3
3	NRZ Data In	Input data to be encoded into ternary form. The data is clocked by the negative going edge of CLK ENC.
4	CLK ENC	Clock encoder, clock for encoding data at NRZ Data In.
6	NRZ Data Out	Decoded data from ternary inputs A_{IN} and B_{IN}.
7	CLK DEC	Clock decoder, clock for decoding ternary data on inputs A_{IN} and B_{IN}.
8, 9	$\overline{\text{Reset AIS}}$, AIS	Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to zero provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ period or sets AIS to '1' if less than 3 zeros have been decoded in the preceding two $\overline{\text{Reset AIS}}$ periods. A period of $\overline{\text{Reset AIS}}$ is defined from the bit following the bit during which $\overline{\text{Reset AIS}}$ makes a high to low transition to the bit during which $\overline{\text{Reset AIS}}$ makes the next high to low transition.
10	V_{SS}	Ground reference.
11	Error	A logic '1' indicates that a violation of the line coding scheme has been decoded.
12	Clock	"OR" function of A_{IN} and B_{IN} for clock regeneration when pin 14 is at logic '0', "OR" function of OUT1 and OUT2 when pin 14 is at logic '1'.
13, 15	A_{IN}, B_{IN}	Inputs representing the received PCM signal. A_{IN} = '1' represents a positive going '1' and B_{IN} = '1' represents a negative going '1'. A_{IN} and B_{IN} are sampled by the positive going edge of CLK DEC. A_{IN} and B_{IN} may be interchanged.

Pin Descriptions (Continued)

PIN NUMBER	FUNCTION	DESCRIPTION
14	LTE	Loop Test Enable, this pin selects between normal and loop back operation. A logic '0' selects normal operation where encode and decode are independent and asynchronous. A logic '1' selects a loop back condition where OUT1 is internally connected to A_{IN} and OUT2 is internally connected to B_{IN}. A decode clock must be supplied.
16, 17	OUT1, OUT2	Outputs representing the ternary encoded NRZ Data In signal for line transmission. OUT1 and OUT2 are in return to zero form and are clocked out on the positive going edge of CLK ENC. The length of OUT1 and OUT2 is set by the length of the positive clock pulse.
18	$\overline{\text{Reset}}$	A logic '0' on this pin resets all internal registers to zero. A logic '1' allows normal operation of all internal registers.
19	$\overline{\text{Output Enable}}$	A logic '1' on this pin forces outputs OUT1 and OUT2 to zero. A logic '0' allows normal operation.
20	V_{DD}	Power to chip.

Functional Description

The HC-5560 TRANSCODER can be divided into six sections: transmission (coding), reception (decoding), error detection, all ones detection, testing functions, and output controls.

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ Data In) into two binary unipolar return to zero (RZ) output signals (OUT1, OUT2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRz Data Out).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ Data Out signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 15 for AMI, 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ Data Out stream with the Error output active.

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signaled by a high level at the Alarm Indication Signal (AIS) output. This is also known as Blue Code. The AIS output is set to a high level when less than three zeros are received during one period of $\overline{\text{Reset AIS}}$ immediately followed by another period of $\overline{\text{Reset AIS}}$ containing less than three zeros. The AIS output is reset to a low level upon the first period of $\overline{\text{Reset AIS}}$ containing 3 or more zeros.

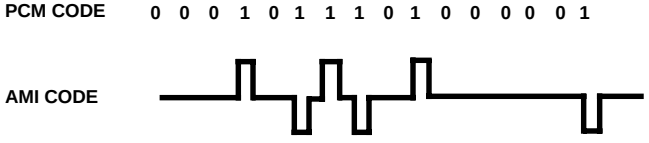
A logic high level on LTE enables a loopback condition where OUT1 is internally connected to A_{IN} and OUT2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, NRZ Data In appears at NRZ Data Out (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation.

The output controls are $\overline{\text{Output Enable}}$ and Force AIS. These pins allow normal operation, force OUT1 and OUT2 to zero, or force OUT1 and OUT2 to output all ones (AIS condition).

Line Code Descriptions

AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. Zeros are coded as the absence of a pulse and ones are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

e.g.,



To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1s is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

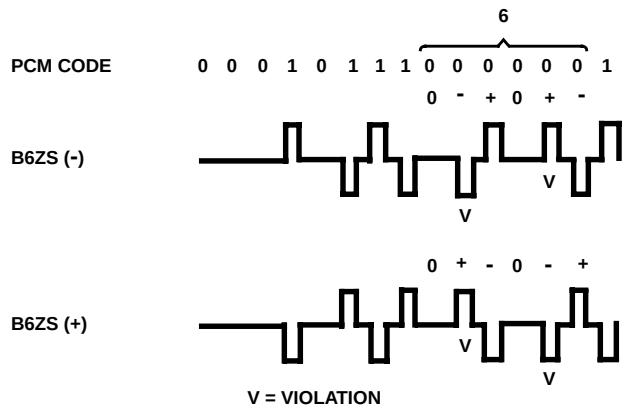
A method for insuring minimum logic 1 density by substituting bipolar code in place of strings of 0s is called BNZS or Bipolar

with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0+- 0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+- 0-+.

One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.

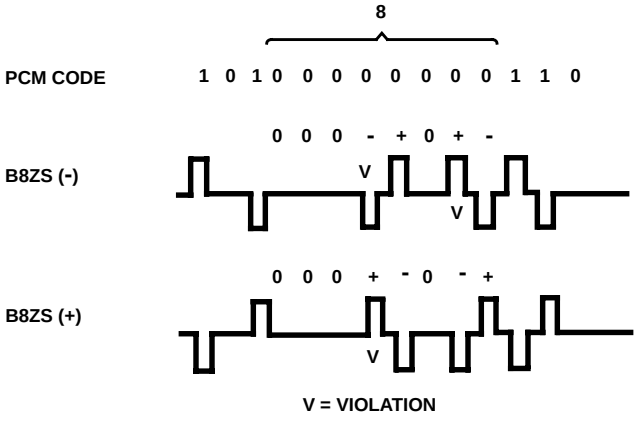
e.g.,



B8ZS is used commonly in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

1. If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+ 0+-.
2. If the immediate preceding pulse is of (+) polarity then code each group of 8 zeros as 000+-0-+.

e.g.,

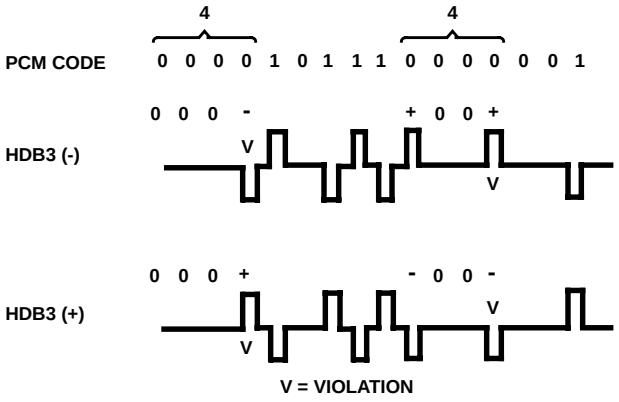


The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048MHz and 8.448MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rule:

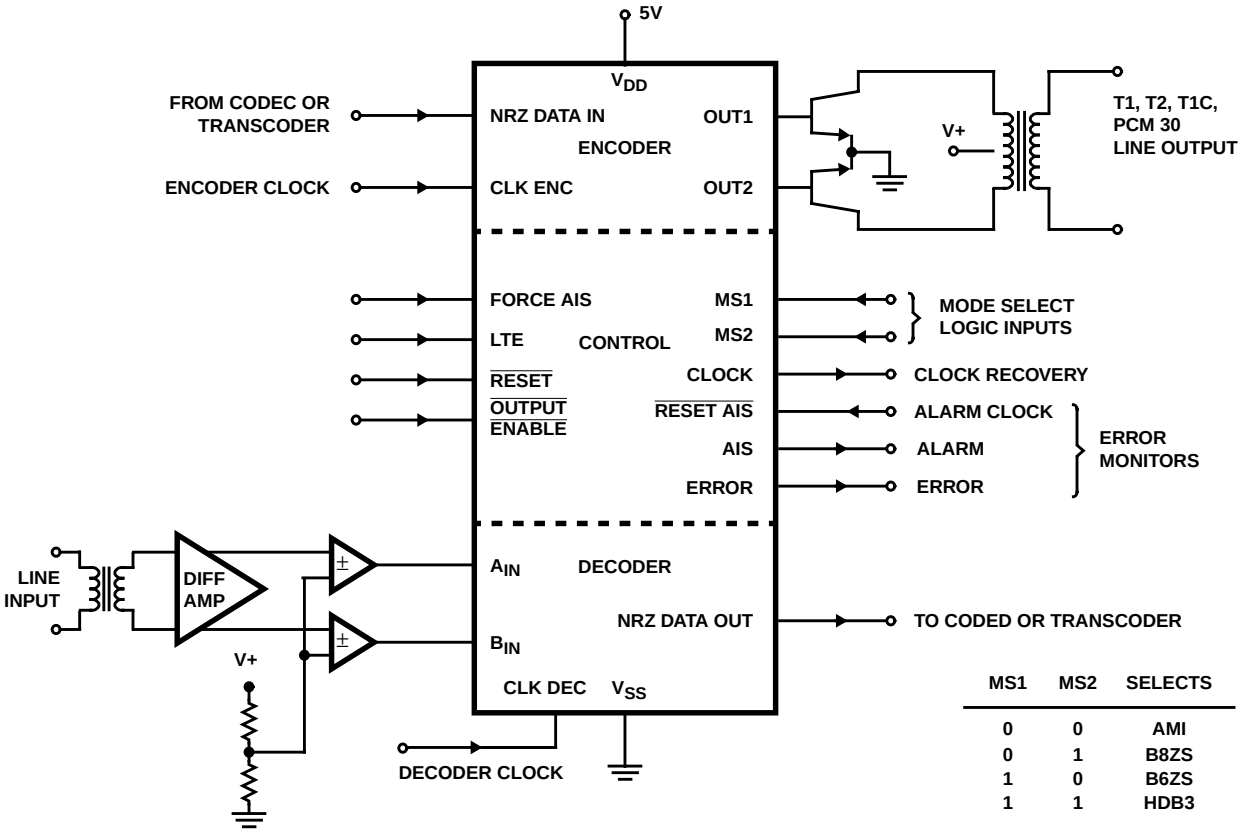
1. If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).
2. If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.

e.g.,



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

Application Diagram



MS1	MS2	SELECTS
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

Timing Waveforms

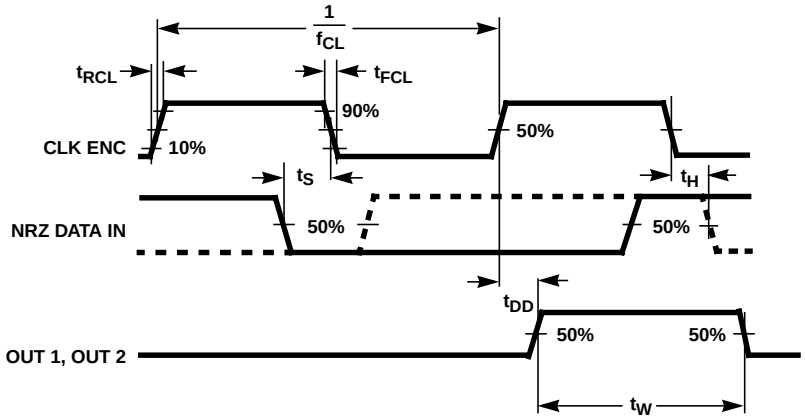


FIGURE 1. TRANSMITTER (CODER) TIMING WAVEFORMS

Timing Waveforms (Continued)

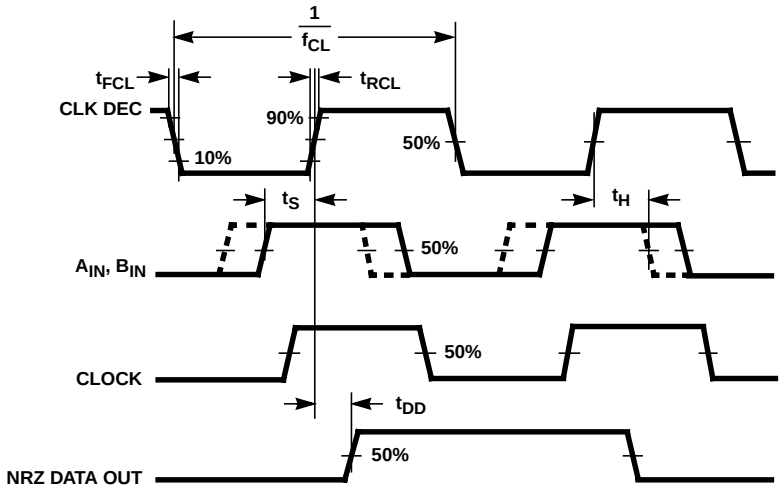


FIGURE 2. RECEIVER (DECODER) TIMING WAVEFORMS

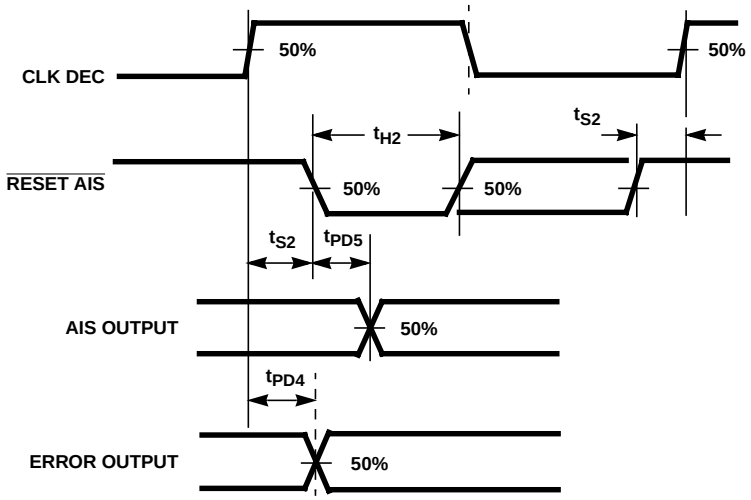


FIGURE 3. $\overline{\text{RESET AIS}}$ INPUT, AIS OUTPUT, ERROR OUTPUT

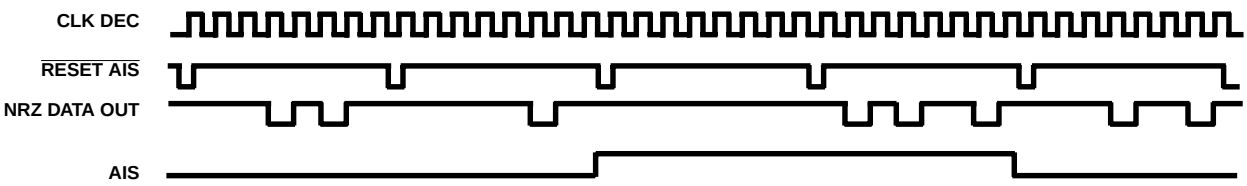


FIGURE 4.

Two consecutive periods of $\overline{\text{Reset AIS}}$, each containing less than three zeros, sets AIS to a logic ‘1’ and remains in a logic ‘1’ state until a period of $\overline{\text{Reset AIS}}$ contains three or more zeros.

Timing Waveforms (Continued)

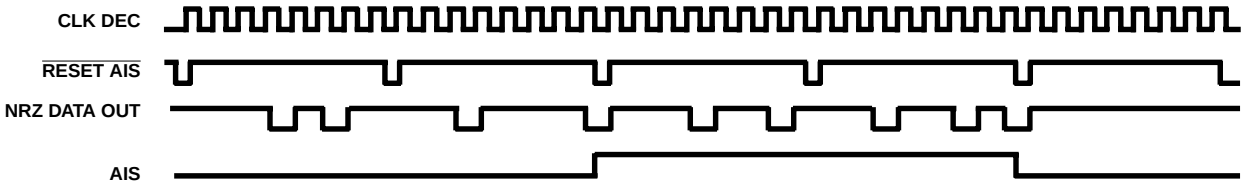


FIGURE 5.

Zeros which occur during a high to low transition of Reset AIS are counted with the zeros that occurred before the high to low transition.

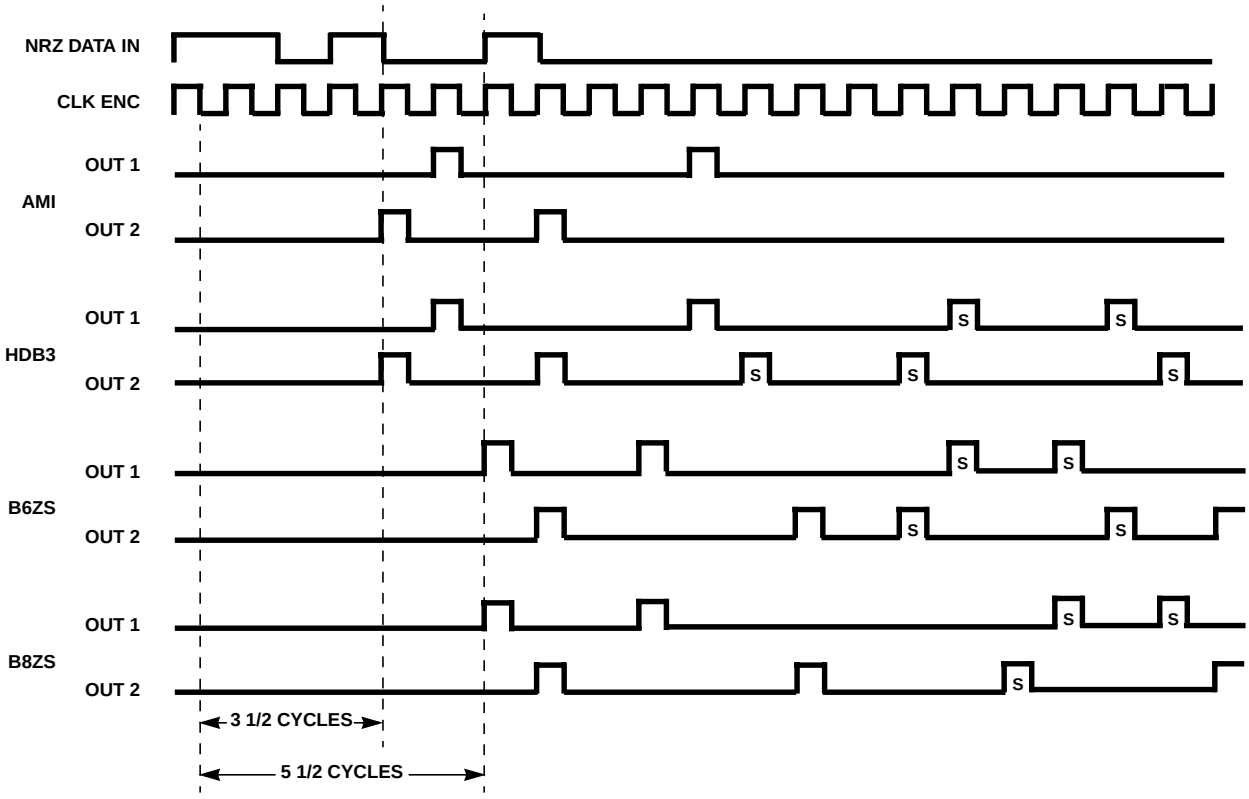


FIGURE 6. ENCODE TIMING AND DELAY

Data is clocked on the negative edge of CLK ENC and appears on OUT1 and OUT2. OUT1 and OUT2 are interchangeable. Bipolar violations and all other pulses inserted by the line coding scheme to encode strings of zeros are labeled with an “S”.

Timing Waveforms (Continued)

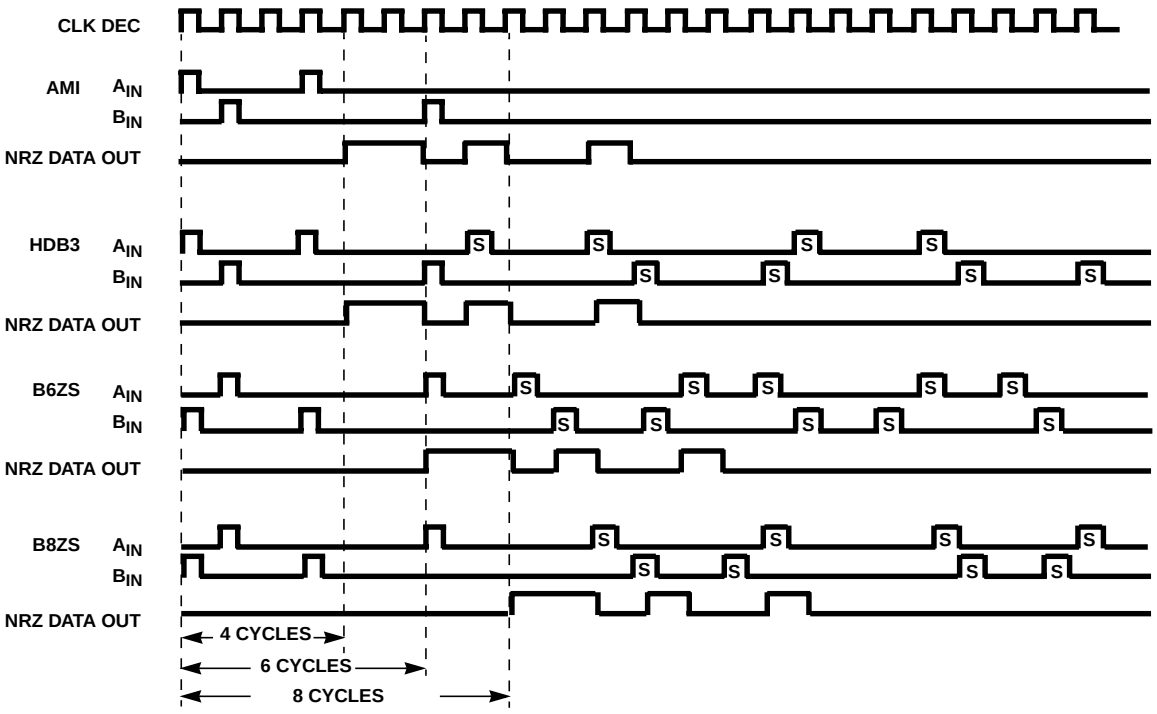


FIGURE 7. DECODE TIMING AND DELAY

Data that appears on A_{IN} and B_{IN} is clocked by the positive edge of CLK DEC, decoded, and zeros are inserted for all valid line code substitutions. The data then appears in non-return to zero to zero form at output NRZ Data Out. A_{IN} and B_{IN} are interchangeable.

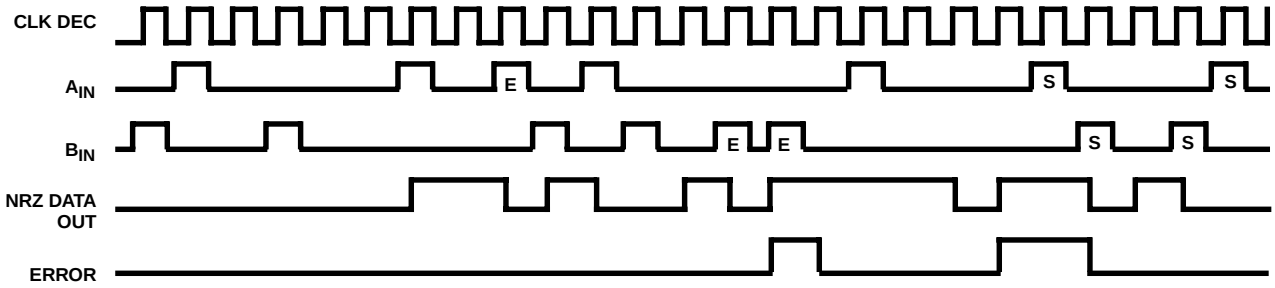


FIGURE 8.

The ERROR signal indicates bipolar violations that are not part of a valid substitution.