Honeywell

4551872 HONEYWELL/SS ELEK, MIL 03E 00236 D

HC20000

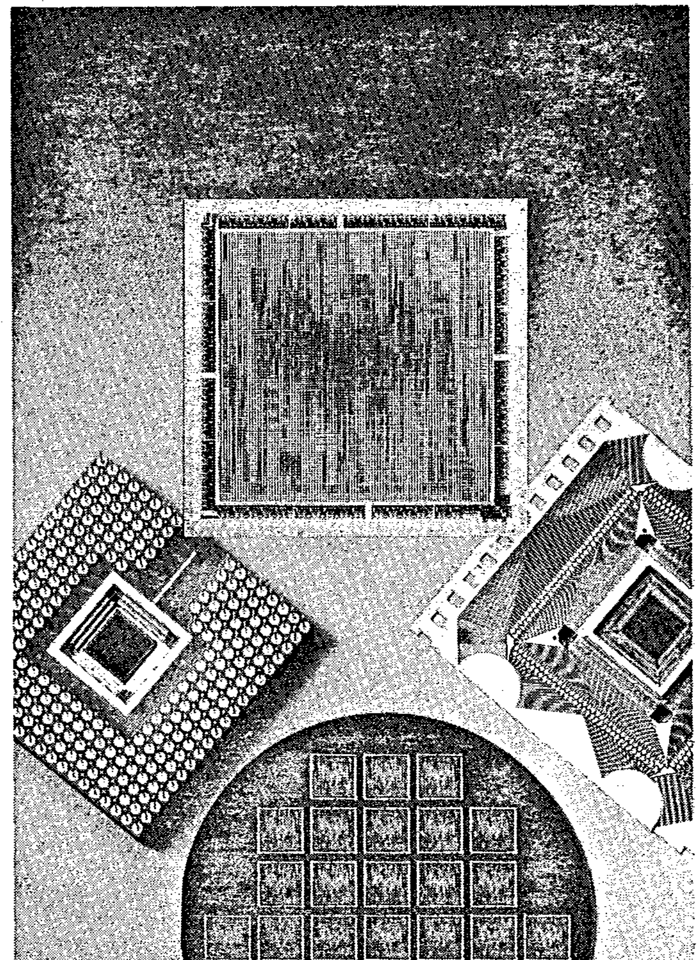
Preliminary

HIGH-PERFORMANCE CMOS GATE ARRAY

FEATURES

- Performance Optimized Series of 1.2-Micron CMOS Gate Arrays
- TTL and CMOS I/O Interfaces
- Over 110 Library Macrocells Designed for Optimized System Performance
- Standard Megacell Capability
- High Density Advanced Packages
- Available in Military and Commercial Versions
- Proven VLSI Design System (VDS) Toolkit™
- Boundary and Internal Scan
- VHSIC Built-In Self Test (BIST) Testability Protocols
- MIL-M-38510 Qualification Pending
- MIL-STD 883C Class B and Modified Class S Screening

Honeywell's CMOS gate arrays offer the designer complete ASIC design capability coupled with state-of-the-art CMOS 1.2-micron manufacturing capability. Depending on the system design, three compatible array families are available: HC, HCT and HCS.



ARRAY TYPES

	HC	HCT	HCS
Application	Commercial/ Military	Tactical Military	Strategic Military
Radiation Environment	None	Tactical	Full Strategic
Process	CMOS-III	CMOS-III/ RICMOS™	RICMOS™
Array Sizes	20K	5K 15K	5K* 10K* 15K

*Consult Honeywell for availability.

This data sheet addresses the design and manufacturing capability of Honeywell's HC high-performance CMOS gate array.

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DESCRIPTION

The high-performance HC20000 gate array offers improved system performance, testability and space reduction benefits to advanced military avionics and commercial CPU designers. The HC20000 is manufactured using a production level 1.2-micron, two-level metal CMOS process. The Array is based upon a unique ten-transistor physical cell that allows architecture specific memory elements to be built on-array for improved system performance.

HC ARRAY PHYSICAL ATTRIBUTES

Device	HC20000
Total Gates (6T)	20,097
Equivalent 2-Input NAND Gates *	17,382
Total Pins	284
Total I/O	238
Input Only	98
Power & Ground	40
Test/Clock	6

* Usable gates at 85% utilization, includes ~2K test gates

HC FEATURES/BENEFITS

Features	Benefits
• 17K Equivalent Usable Gates • 238 I/O Pins • TTL and CMOS Interfaces • High Level of Logic Integration • Performance Programmable Macrocells	• Flexible System Partitioning • Fewer I/O Boundary Crossings • Optimized System Performance • Reduced Board Space Required • Increased System Reliability
• Soft Macrocell Function Capability	• Low-risk, Low-cost Implementation of DoD Standard Communications and Testability Protocols
• Macrocell Library Compatibility with HCT and HCS CMOS Gate Arrays	• Upward Migration Path for Systems Requiring Strategic Radiation Hardness
• Proven VLSI Design System (VDS) Toolkit™	• Minimized Design Risk • Faster Deployment of Military Systems • Support for Present and Emerging DoD Standards
• User Selectable Built-In Test Options	• Simplified Design Debug and System Test • Reduced Manufacturing Test Time and Cost
• Advanced Packaging with Logic Densities of 20,000 Gates/Inch^2 of Board Space	• Reduced Board Space Required
• MIL-M-38510 Qualification Pending	• Reduced Program-Specific Qualification Costs
• Dedicated Quick-Turn Prototype Facility	• Quicker Deployment of Military Systems

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DESIGN AND MANUFACTURING CAPABILITIES

Honeywell offers a complete design and manufacturing capability, illustrated in Figure 1. The following table lists the corresponding software for each highlighted block.

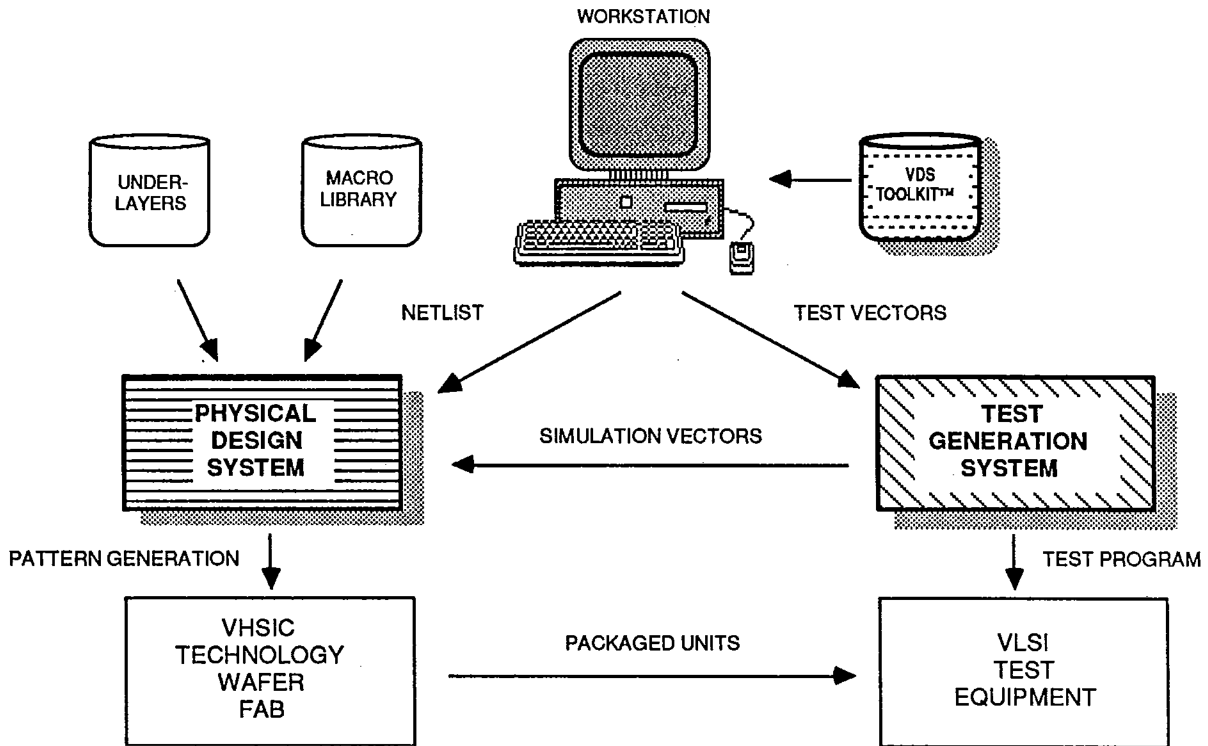

FIGURE 1. HONEYWELL'S DESIGN AND MANUFACTURING CAPABILITIES

VDS SOFTWARE™ AND MACROCELL LIBRARY

Customer Service	Macrocell Library	VDS Software™
VDS ToolKit™ (Front-End Design)	- Symbols - Simulation Models - Tech Table - Design Manual	- HDB™ - VERIFY™ - DELAY™ - DFA™ - NETLISTERS - SIM INTERFACE - DAMSEL™
Physical Design System (Back-End Design)	- Transistor Schematics - Topology	- XPL - MERLYN-G - ERC/DRC/LOGICV/PG - CALMA - PERFBIAS™
Test Generation System	- RIGEL™ Models	- RIGEL™ - MIGHT™

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VLSI DESIGN SYSTEM (VDS)™

VDS™ is a design methodology and CAD system that helps assure first pass design success resulting in faster deployment of a military system. Honeywell's design methodology consists of the VDS Toolkit™, a physical design service, and a test generation service. The VDS Toolkit™ is a comprehensive, technology-independent ASIC design package that equips the ASIC designer with VDS Software™ and a macrocell library. The toolkit is accessed via a user-friendly, graphical human interface, providing maximum flexibility and efficiency in the front-end design process.

All phases of the design cycle are supported by Honeywell from schematic capture through test vector generation. The VDS Toolkit™ is currently available on Mentor workstations and can be ported to other design platforms.

DESCRIPTION	MENTOR™ APPLICATION	HONEYWELL VDS TOOLKIT™	HONEYWELL VDS™ DESIGN SERVICES
Schematic Entry	NETED/SYMED		
Schematic Capture	EXPAND		
Error Checking - fanout exceeds drive capability - unconnected macro inputs/outputs - external signal not connected through I/O buffer		VERIFY™	
Design Statistics - cell inventory and utilization - I/O inventory and utilization - total number of nets and pins		VERIFY™	
Propagation Delay Calculation - intrinsic delay of each path within each macrocell - additional delay of fanout and interconnect capacitance - at user-defined power supply voltage and junction temperature - pre/post route options		DELAY™	
Functional Simulation	QUICKSIM	SIM I/F MODELS	LASAR-6
Fault Analysis			LASAR-6
Static Timing Analysis		DAMSEL™	
Test Program Generation - produces ANDO compatible functional and/or scan test vectors - accepts output files from Mentor, DAISY, and LASAR-6 simulators			MIGHT™
Automatic Test Vector Generation			RIGEL™
Automatic Placement - Netlists received by magnetic media or dial-up field transfer			XPL
Automatic Routing			MERLYN-G
Automatic Performance Biasing			PERFBIAS™

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SILICON UNDERLAYERS

A gate array is a semicustom device assembled on a matrix of X columns by Y rows of physical cells. The physical cell in the HC Array Family consists of ten uncommitted transistors. This array of uncommitted transistors, along with the **I/O ring,** are called **underlayers** and are common to all **personalizations** of the gate array. The I/O ring consists of I/O buffers, a clock distribution network, and power busses. The macrocell library contains the data needed to connect the transistors of one or more physical cells to form a **logic function**.

The HC array's I/O buffers have the following characteristics:

- Built-in configurable test logic
- Dedicated I/O and input only functions
- 8mA TTL output drive
- CMOS or TTL input and output configurable interface
- ESD input protection greater than 2000 volts

Each I/O buffer can be independently used as an input only, output only, or I/O function. The output buffer has a high impedance state. The input and output portions of the I/O buffer act independently.

CMOS/TTL INPUT INTERFACE CHARACTERISTICS

Interface	Logic HI	Logic LO	Switchpoint
CMOS	3.5 V min	1.5 V max	Vdd/2 typ.
TTL	2.0 V min	0.8 V max	1.3 V typ.

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PERFORMANCE PROGRAMMABLE MACROCELL LIBRARY

Honeywell provides an accurately modeled and highly flexible macrocell library that has been optimized for maximum synchronous system performance. The library contains approximately 110 hard-wired data path elements ranging from inverters to flip-flops, adders and shifters.

The CMOS 1.2-micron macrocell library has been characterized at the device level through extensive SPICE modeling. The resulting SPICE K-factors are stored in a technology table and used in circuit simulation and the simulation results compared to actual test arrays. Each macrocell has been evaluated over the entire military temperature range, voltage and process spectra to ensure accuracy and guaranteed worst case delays.

The CMOS 1.2-micron macrocell library provides these benefits in new system designs:

- a common library of over 110 cells including bit-width programmable register, counter and multiplexer macrocells to maximize array efficiency, and minimize dynamic power.

- performance programmable NAND, NOR and inverter macrocells to optimize critical path performance.

- static and dynamic register bits are constructed using CMOS transmission gates and optional serial-scan testability to allow the tradeoff of minimum register area (dynamic) with minimum register power (static) during the design process.

- architecture specific soft RAM macrocells can be constructed to provide improved system performance by eliminating I/O delays required during accessing off-array memory.

The table below provides performance data for selected LSI functions designed with the CMOS macrocell library. The Macrocell Performance Guide shows the area, intrinsic delay, and additional metal loading delays for macrocells in the HC library.

LSI FUNCTION PERFORMANCE

Function		Typical Case (1) (ns)	Worst Case (2) (ns)	Cell Count
16-bit Adder/Subtractor		7	13	302
32-bit Fast Adder with Full Carry Look Ahead		11	23	445
32-bit x 32-bit Word Register File (1 Read /1 Write)	Read Write	8 16	15 30	1,300
16-word x 1-bit RAM (1 Read / 1 Write)		7	12	108

(1) V_{dd} = 5.0V, T_j = +25°C, Process = Nominal
(2) V_{dd} = 4.5V, T_j = +150°C, Process = Worst case

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MACROCELL PERFORMANCE GUIDE

($T_j = 25°C$; $V_{dd} = 5.0V$; $T_{in} = 1ns$; Process = Nominal) (Typical)

Cell Description	Cell Name	Cell Size (wxh)	Cell Count	Base Rising (ns)	Load Factor Rising (ns/pF)	Base Falling (ns)	Load Factor Falling (ns/pF)	Input Cap. (pF)
Inverters/Buffers								
Inverter	INV0	1x1	1	.183	.527	.188	.566	.192
Power Inverter	INV1	1x1	1	.208	.360	.081	.235	.365
Double Power Inverter	INV2	1x2	2	.206	.176	.078	.142	.668
Balanced Drive Inverter	INV3	1x1	1	.207	.371	.116	.369	.334
Non-Inverting Buffer	BUF1	1x1	1	.469	.518	.571	.406	.127
Delay Macro	BUF4	2x1	2	1.886	1.024	1.858	.713	.127
AND, OR, NAND, & NOR								
2-NAND	ND2	1x1	1	.276	.983	.186	.850	.128
3-NAND	ND3	1x1	1	.342	.97	.301	1.070	.113
4-NAND	ND4	1x2	2	.477	.911	.494	1.32	.123
6-NAND	ND6	2x2	4	1.195	.520	1.118	.431	.126
2-AND	AND2	1x1	1	.533	1.105	.539	.640	.123
5-AND	AND5	2x1	2	1.245	1.173	.681	.734	.123
Power 2-NAND	ND2H	1x2	2	.289	.388	.214	.356	.364
Power 3-NAND	ND3H	1x2	2	.419	.493	.386	.548	.283
2-NOR	NOR2	1x1	1	.512	1.337	.194	.446	.191
3-NOR	NOR3	3x1	3	1.041	.542	.839	.409	.151
6-NOR	NOR6	2x2	4	1.362	.599	1.010	.650	.126
Power 2-NOR	NORH	1x2	2	.440	.673	.158	.252	.379
2-OR	OR2	1x1	1	.420	.104	.732	.743	.128
AND/OR, OR/AND Gates								
1-2 AND/OR/Invert	AOI1	1x1	1	.463	1.638	.218	.745	.112
2-2 AND/OR/Invert	AOI2	3x1	3	1.139	.527	.983	.391	.128
3-3 AND/OR/Invert	AOI3	3x1	3	1.042	1.010	1.028	.645	.127
Power 1-2 AND/OR/Invert	AOIH	1x2	2	.485	.946	.211	.407	.267
1-2 OR/AND/Invert	OAI1	1x1	1	.450	1.509	.306	.939	.129
2-2-1 OR/AND/Invert	OAI3	2x1	2	.840	1.714	.603	1.106	.131
Power 1-2 OR/AND/Invert	OIAH	1x2	2	.471	.754	.273	.432	.268
3-3-3 AND/OR	AO3	2x2	4	.850	.977	.779	1.089	.114
1-2-3-4 AND/OR	AO4	2x3	6	.930	.997	.986	1.190	.115
1-3 OR/AND	OA1	2x2	4	.639	.903	.766	1.037	.203
Exclusive OR/NOR Gates								
Exclusive-OR	EXOR	3x1	3	.913	.535	.704	.438	.225
Exclusive-NOR	EXNR	3x1	3	.575	.541	.667	.461	.247
4-Bit Exclusive-OR	EXO4	2x3	6	1.730	.532	1.748	1.938	.202
8-Bit Exclusive-OR	EXO8	6x3	18	2.238	.541	2.114	.445	.263
10-Bit Exclusive-NOR	EXN9	4x5	20	2.612	.537	2.323	.439	.185
2-2 AND/Exclusive-OR	AXO2	2x2	4	1.217	.571	1.138	.495	.143
Priority/Decode								
2 to 4 Decode w/ Enable	DEC2	2x5	10	1.469	.588	1.173	.441	.188
3 to 8 Decode w/ Enable	DEC3	6x3	18	1.852	.525	1.690	.401	.324
8-Bit Priority Selector	SEL8	3x5	15	1.070	1.398	.861	.630	.233
4-Bit Priority Encoder	ENC4	2x2	4	.500	1.438	.514	.755	.248

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MACROCELL PERFORMANCE GUIDE (continued)

(T_j = 25° C; V_{dd} = 5.0V; T_{in} = 1ns; Process = Nominal) (Typical)

Cell Description	Cell Name	Cell Size (wxh)	Cell Count	Base Rising (ns)	Load Factor Rising (ns/pF)	Base Falling (ns)	Load Factor Falling (ns/pF)	Input Cap. (pF)
Multiplexers								
2 to 1 Multiplexer	MXC2/ MXE2	2x1 2x1	4	1.072	.547	1.091	.496	.119
2 to 1 Multiplexer with Complement Enable	MXC3/ MXE3	3x2 3x1	9	1.362	1.042	1.335	1.053	.138
4 to 1 Multiplexer with Enable	MXC4/ MCE4	2x2 2x2	8	1.300	.969	1.474	.869	.196
8 to 1 Multiplexer with Enable	MXC8/ MXE8	2x3 2x5	16	1.622	1.092	1.886	1.160	.122
Flip-Flops (F/F)								
Dynamic F/F	DFC1/ DFE1	2x2 2x1	6	1.456	.985	1.497	.799	.126
Dynamic F/F w/Clk. En. & Sync. Set/Clr.	DFC2/ DFE2	3x4 3x1	15	1.364	.889	1.293	.764	.124
Dynamic F/F w/Clk. En.	DFC3/ DFE3	2x4 2x1	10	1.734	1.055	1.663	.892	.176
Dynamic F/F w/ 2-1 MUX Data Input	DFC4/ DFE4	2X4 2X1	10	1.850	1.061	1.791	.844	.167
Dynamic F/F w/Clk. En. and 2-1 MUX Data In.	DFC5/ DFE5	3X4 3X1	15	2.130	1.019	2.042	.759	.207
Static F/F w/ Clk En. & Sync. Clr.	DFC6/ DFE6	2x3 2x2	10	2.680	.541	2.273	.466	.257
Single F/F	SFF2	2x4	8	1.37	.488	1.26	.550	.130
Quad D Latch	QDL	2x4	8	.796	.477	.959	.563	.302
SCAN Flip-Flop (F/F)								
SCAN Reg Cont'l w/reset	DSC6/	5x3	15	.633	.0835	.511	.0656	.420
SCAN F/F Ele. w/reset	DSE6	5X1	5	1.264	.944	1.241	.651	.150
SCAN Reg. Cont'l w/set	DSC8/	5x3	15	.590	.078	.605	.072	.312
SCAN F/F Ele. w/set	DSE8	5X1	5	1.265	.944	1.242	.652	.150
Miscellaneous								
4-Bit Up/Dn Counter w/ Parallel Load	CNT4	5x7	35	2.03	.509	2.46	.889	.190
4-Bit Shifter	SFC1/ SFE1	3x4 3x4	24	1.240	.528	1.187	.455	.258
4-Bit Adder	ADD4	6x8	48	1.889	.794	1.621	.805	.263
4-Bit Partial Adder	ADD5	3x3	9	1.808	1.07	1.845	.878	.257
Single-Bit Adder	ADD1	2x3	6	1.713	.766	1.586	.688	.215
4-Bit Comparator	CMP1	3x5	15	1.819	.540	1.774	.429	.241
4-Bit Magnitude Comp.	CMP4	4x7	28	2.081	1.163	2.050	.794	.198
4-Bit Incrementer	INC4	4x6	24	1.530	.566	1.686	.519	.255
4-Bit Decrementer	DCR4	4x5	20	1.828	.565	1.559	.458	.236
16-Word x N-Bit Simul. Rd/Wr RAM	MMC1/ MME1	18x4xN 18x2	108	2.898	1.197	3.105	1.258	.407

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MACROCELL PERFORMANCE GUIDE (continued)

(T_j = 25° C; V_{dd} = 5.0V; T_{in} = 1ns; Process = Nominal) (Typical)

Cell Description	Cell Name	Cell Size (wxh)	Cell Count	Base Rising (ns)	Load Factor Rising (ns/pF)	Base Falling (ns)	Load Factor Falling (ns/pF)	Input Cap. (pF)
HC I/O Cells*								
Clock Driver (Low Drive)	CLKA	—	—	2.760	.0096	2.77	.011	4.0
Clock Driver (High Drive)	CLKB	—	—	1.770	.0078	1.920	.0081	5.50
2-Stage CMOS Input (CTL)	CIN2	—	—	.990	.499	.942	.581	3.0
2-Stage TTL Input (CTL)	CIN3	—	—	.571	.425	1.480	.660	3.0
Unused Input w/SCAN	I000	—	—	—	—	—	—	—
Unused Input only w/SCAN	I003**	—	—	3.515	.985	3.01	1.068	3.0
CMOS Inv. Input w/SCAN w/Input SCAN Reg.	I103**	—	—	.813	.400	.881	.475	3.0
2-Stage CMOS Input Only w/ SCAN	I203	—	—	4.050	.967	3.743	1.005	3.0
2-Stage TTL Input Only w/ SCAN	I303	—	—	3.857	.930	3.937	1.060	3.0
Unused I/O Buffer	B000	—	—	—	—	—	—	—
Unused I/O w/ SCAN	B004**	—	—	4.25	.914	3.845	.986	.069
CMOS Low Drive Output w / SCAN	B014**	—	—	.961	.0953	1.181	.1120	4.0
CMOS Output w/ SCAN	B021	—	—	3.44	.042	3.14	.057	4.0
CMOS High Drive Output w/ SCAN	B024**	—	—	3.44	.0423	3.140	.0567	4.0
5V TTL Output Buffer w/ SCAN	B041	—	—	3.61	.085	3.24	.038	4.0
8mA TTL Output w/ SCAN	B044**	—	—	3.410	.0790	3.060	.0353	4.0
CMOS Invert Input w/ SCAN	B104**	—	—	.813	.400	.881	.475	4.0
2-Stage CMOS Input w/ SCAN	B203	—	—	1.55	.75	1.43	.775	3.0
2-Stage CMOS Input w/ SCAN	B204**	—	—	1.44	.700	1.350	.720	3.20
2-Stage CMOS I/O w/SCAN	B224**	—	—	2.44	.371	2.245	.388	4.0
2-Stage TTL Input w/SCAN	B303	—	—	.982	.69	2.00	.89	3.0
2-Stage TTL Input w/SCAN	B304	—	—	.926	.647	1.880	.823	3.20
2-Stage TTL Input/ CMOS High Drive Out w/SCAN	B324**	—	—	2.183	.344	2.51	4.39	4.0
2-Stage TTL I/O w/ SCAN	B344**	—	—	2.296 2.030	.383 .118	2.62 2.020	.464 .118	4.0 .667
SCAN Control Circuitry	CC02	—	—					
BIST Control Circuitry	CC03	—	—	2.61	.117	2.73	.118	.667
CMOS High Drive Output For Test-Data-Out	COT2	—	—	2.887	.043	5.470	.039	4.0
TTL Output For Test-Data-Out	COT4	—	—	2.843	.071	5.023	.033	4.0

* All TTL outputs have 8mA drive capability.
**For use with BIST (Built-In Self-Test)

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CALCULATING PERFORMANCE

Each macrocell has its own intrinsic base delay and load factor. Macrocell performance is influenced by temperature, voltage, and process variations. Intrinsic base delay is also a factor of the input edge rate.

When calculating the propagation delay of a macrocell or logic path, temperature, voltage, process, input capacitance of the next macrocell, and capacitive loading due to metal interconnect must be considered.

Macrocells using a control hat and elements (e.g., DFC1, DFE1) require an additional load per element.

In the following equation for calculating the propagation delay, T_{pd}, the input edge rate for the intrinsic base delay is 1 ns.

Best case/worst case delay values can be obtained from Honeywell's CMOS Design Manual.

$$T_{pd} = [\,T_b + (LF \times C_i) + (EF \times (N_e - 1))]$$

where,

T_b = Intrinsic base delay at 25° C, 5V, nominal process, ns
LF = Load factor for macrocell, ns/pF
C_i = Total capacitive load = $C_{in} + C_{metal}$, pF
EF = Element factor for control that macrocell, ns/element
N_e = Number of elements attached to the control hat

Example 1.

Assume a 2-input NAND gate, ND2, 25°C, 5V, nominal process, fanout = 2 identical 2-input NAND gates.

From Macrocell Performance Guide, C_{in} = 0.128 pF.
From Metal Load vs. Fanout, interconnect capacitance = 0.375 pF

$$T_{pd}(\text{Rising}) = [\,T_b + (LF \times C_i)]$$
$$= [0.276 + (0.983 \times ((2 \times 0.128) + 0.375))] = 0.896 \text{ ns}$$

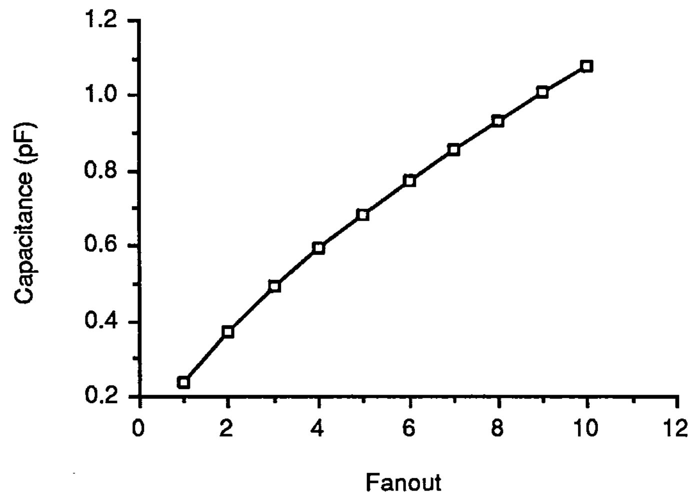
Example 2.

Assume a 2:1 multiplexer with 4 elements (MXC2/MXE2), 25°C, 5V, nominal process, fanout = 4 2-input NAND gates.
EF = 0.05

From Macrocell Performance Guide, C_{in}= 0.119 pF.
From Metal Load vs. Fanout, interconnect capacitance = 0.592 pF (worst case)

$$T_{pd}(\text{Falling}) = [\,T_b + (LF \times C_i) + (EF \times (N_e - 1))]$$
$$= [1.091 + (0.496 \times ((4 \times 0.119) + 0.592)) + (0.05\,(4-1))]$$
$$= 2.033 \text{ ns}$$

METAL LOAD vs. FANOUT



$C(\text{metal}) = (0.238) \times (\text{Fanout})^{0.657}$

(Nominal)

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POWER DISSIPATION

Power dissipation of a CMOS circuit is difficult to calculate because it is extremely dependent upon such conditions as switching frequency, load capacitance, supply voltage, input rise or fall time and temperature.

Typically, power consumption of a CMOS gate array is comprised of array power and I/O power. The array is dominated by AC power ($CV^2 f$), which is controlled by the logic function (how heavily loaded each gate is and how fast they switch). Within the array, power is dissipated by two components: the clock and the rest of the array. The I/O buffers are dominated by DC power (I*V), although AC power is an important consideration. A first-order approximation of power dissipation can be made by summing array power (PI), output buffer power (PE) and clock power (PC) as follows:

$$PT = (PI + \sum_{n=1}^{x} PE_n + PC)$$

where x is the number of output buffers.

Maximum power dissipation should not exceed a level at which the junction temperature (Tj) will exceed 150°C. Tj = PT x TRja + Ta where TRja is thermal resistivity of the package from junction to ambient and Ta is ambient temperature for the condition of device cooled by free air.

Array Power

$PI = G \times P \times f^{0.88} \times Vdd^{2.25} \times 0.23 \times 10^{-3}$ in milliWatt, where

G = equivalent gates (number of physical cells used x 1.5).
P = fraction of gates which switch, on the average, each clock cycle (0<P<1).
f = clock frequency in MHz.
Vdd = array supply voltage.

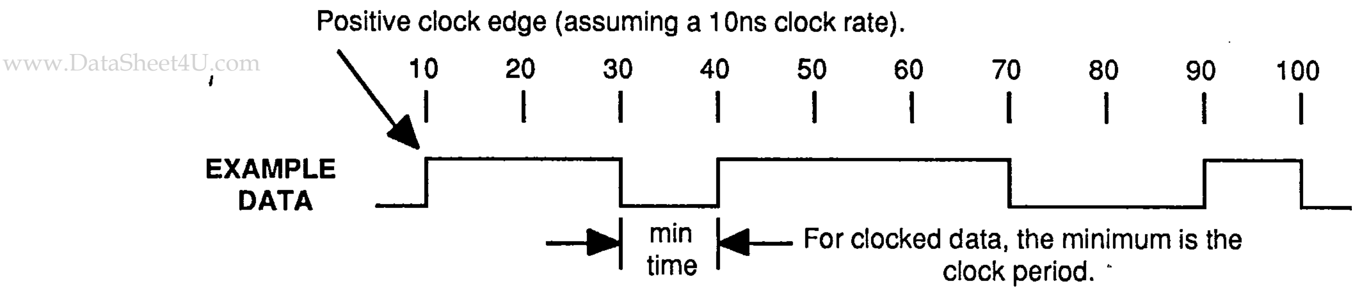
It is expected that .1 < P < .4 is normal system operation for a majority of the array designs.

Output Buffer Power (Single Buffer)

Case 1:
Output buffer drives a transmission line with only one pulse present at a time.

CRITERIA: $2T_d$ < (minimum time between data changes)
T_d = one-way delay on transmission line, in ns.
$T_d = L \times V_p$
L = length of line, in inches
V_p = .100 ns/in 50 ohm coax
= .185 ns/in PC board, 50 ohm, glass-epoxy

These numbers are approximations. Use actual values if available.



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POWER DISSIPATION (cont'd)

$PE = T \times Vddx^2 \times (C_l + C_{tl})$ in milliWatt, where:

T = number of positive logic transitions per nanosecond, on the average. For the example above, this is 3/100 = 0.03.

C_l = lumped load capacitance, in pF, made up of array input pin capacitance and PC board via capacitance.

C_{tl} = transmission line capacitance, in pF, made up of PC board foil capacitance and coax capacitance, 50 ohm.

Vddx = output buffer power supply.

Case 2:
Output buffer drives a transmission with two or more pulses present at a time.
CRITERIA: $2T_d >$ (minimum time between data changes)

$$PE(max) = Vddx^2 \left(T \times C_l + \frac{1}{2Z_0} \frac{\min\{T_0, T_1\}}{T_0 + T_1} \times 10^3 \right) \text{ in milliWatt,}$$

where:

Z_0 = path characteristic impedance, in ohms
{ } = minimum of values in brackets
T_0 = average time signal is at logic LO
T_1 = average time signal is at logic HI

For the example above, $\frac{\min\{T_0, T_1\}}{T_0 + T_1} = \frac{4}{10} = 0.4$

Note that the expression for this case is indicated as a maximum. Although it is theoretically possible to dissipate the maximum power, it is realistically not probable. Power dissipation for long lines that may contain more than one pulse on the line at one time is a complex function of duty cycle, line length and frequency.

Clock Power

$$PC = (30 + C_c + 0.26 \times L + 5.24 \times B) \times f^{0.88} \times Vdd^{2.25} \times 10^{-3} \text{ in milliWatt,}$$

where:

f = Clock frequency, in MHz.
Vdd = Array supply voltage.
C_c = Total clock bus capacitance composed of metal and macro clock pin capacitances, in pF.
B = Total number of clocked macros, e.g., DFC1.
L = Total number of elements in stacked flip-flop macros, e.g., DFE1.

Constants used in PC formula are derived from actual test results.

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DESIGN-FOR-TEST AND MAINTAINABILITY

Design-for-Test and Maintainability

Today's designs often carry demanding component and system-level test and maintenance requirements. Honeywell provides support for a full range of Design-For-Test (DFT) techniques, intended to reduce design debug time, board and module costs, and field system down time. **Built-In Self-Test** reduces test costs and improves system maintainability. **Boundary Scan** simplifies testing of board interconnects and provides excellent fault isolation. **Serial Scan** generates high-fault-coverage test patterns which simplify system and software checkout. Honeywell also offers automatic test program generation in the form of MIGHT™, and an automatic, deterministic test pattern generation system with RIGEL™.

MIGHT™

The MIGHT™ system provides automatic test program generation for Honeywell gate arrays. Test programs are automatically generated and formatted, simplifying a process that requires weeks of manual development and expensive debug time on the tester. The shell and menu approach allows rapid integration of new technologies, expands to any language driven ATE, and achieves a new standard in test quality control.

RIGEL™

RIGEL™ is an automatic, deterministic single stuck-at fault test pattern generation system. It is based on an enhanced D-algorithm. Fundamental to its use is the circuit implementation of Honeywell Scan Design (HSD), a scan structured approach to design for test. The RIGEL™ test generation tools provide a greater than 98 percent fault coverage of permanent single stuck-at faults.

BUILT-IN SCAN CIRCUITRY

The HC gate array supports synchronous scan design and boundary scan design testability methods.

Serial Scan Design

Designs which provide easy application of stimulus and easy measurement of responses are necessary to make circuits thoroughly testable. Honeywell's primary technique that supports this is called Synchronous Scan Design (SSD). SSD specifies that registers in the circuit have an ability to also be reconfigured into a serial shift register (Figure 2). The serial chain is able to be loaded with test input and unloaded with test responses from the component edge. Honeywell's RIGEL™ automatic test generation tool can be used to build a test that is capable of detecting greater than 98% of all permanent single stuck-at type faults. These tests are applied and gathered using SSD.

Boundary Scan Design

The boundary scan method is also fully supported utilizing scan-compatible input, output, and I/O buffer macrocells. Figures 3 and 4 illustrate the scan circuitry associated with each input and each output buffer,

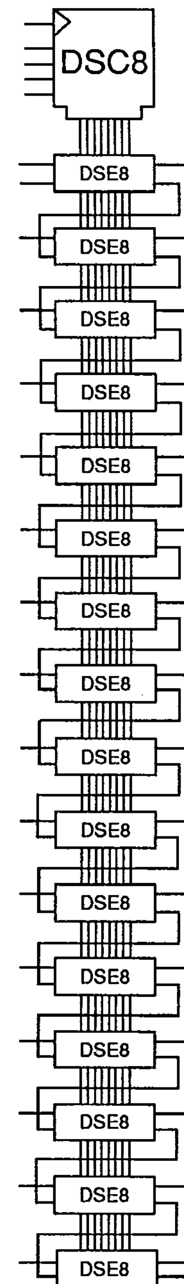

FIGURE 2. 16-BIT D-REGISTER IN SERIAL SCAN PATH

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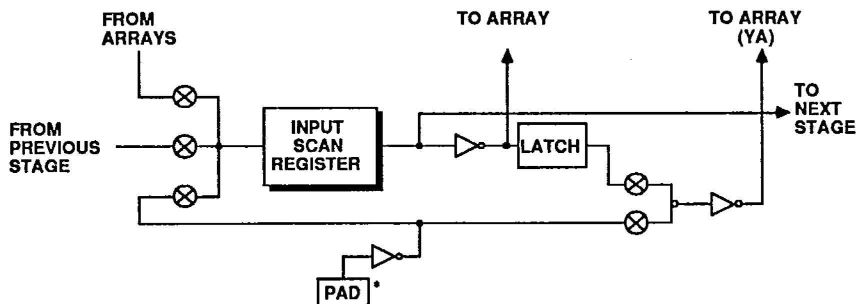

FIGURE 3. INPUT SCAN REGISTER

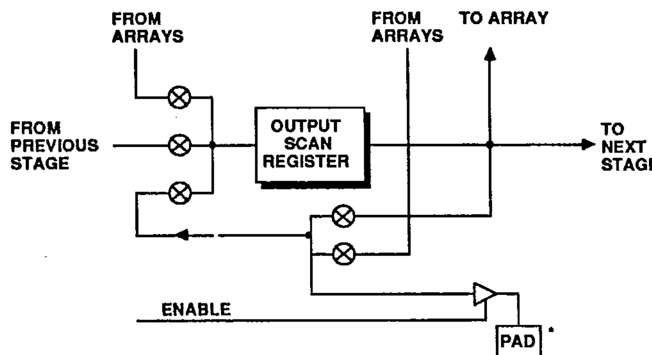

FIGURE 4. OUTPUT SCAN REGISTER

respectively. If an I/O buffer is selected, the circuitry contained in Figures 3 and 4 is tied together. Note that each scan register is connected to the next register in such a way as to configure an input scan ring and an output scan ring around the periphery of the array. Also note that logic can be done between registers by entering and leaving the array. With these options, the user can design logic for generating serial pseudo-random test patterns, and, by adding logic to the output scan path, can generate a signature analysis result. The macrocell library also includes the CC02 cell, which contains the logic necessary to control the scan registers associated with the I/O cells.

Built-In Self-Test

The Built-In Self-Test (BIST) testability protocols of the Department of Defense VHSIC Phase 2 program are fully supported via the use of Honeywell's Test Interface Unit (TIU), Test and Maintenance Controller (TMC), and the Element Test and Maintenance Bus (ETM-bus).

Honeywell's Test-bus Interface Unit (TIU) chip interfaces between the busses in the hierarchical test-bus structure shown below. This device is rapidly gaining acceptance as a DoD and industry standard. The TIU broadcasts and receives test control and data signals and acts as either a bus master or slave for the back-plane based VHSIC Test and Maintenance bus (TM-bus). It supports dual TM-

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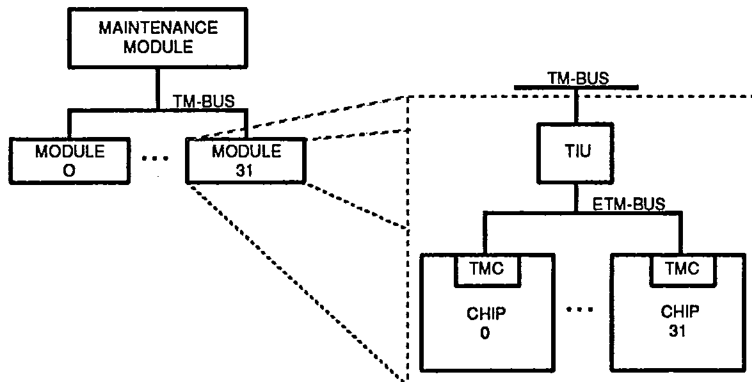

FIGURE 5. VHSIC TESTABILITY ARCHITECTURE

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busses for increased fault tolerance. A microprocessor and memory interface increases the capabilities of the TIU as a TM-bus master or as the test interface on an application module. The Joint Test Action Group (JTAG-) bus and the Element Test and Maintenance (ETM-) bus ports provide standard test and maintenance control at the chip level. Honeywell's TIU supports multiple JTAG/ETM ports to handle large boards with up to 128 JTAG- or ETM-bus compatible components.

The ETM-bus is a multidrop, synchronous bus that transfers bit-serial test and maintenance instructions and data between a master device and up to 32 slave elements on other chips in a module. The slave element is the on-chip TMC, a function block that controls the test and maintenance features such as chip initialization, serial scan, debug, and built-in self-test. Figure 5 illustrates how the TIU and TMC are used in a testable VHSIC system to assure low cost field maintenance and quick design debug.

User configurable built-in self-test methodologies can also be implemented using the scan macrocells in the HC macrocell library.

ADVANCED PACKAGING

The HC array is available in advanced single and multi-array packages to reduce board and module space, quickly debug brassboard and prototype systems, and improve system reliability through reduction of array junction temperatures.

Leaded chip carriers (LDCC) and pin grid array (PGA) packages, available in open or proprietary tooling, are supported over the military temperature range for a variety of military and commercial applications.

Honeywell's advanced MICROPAK-II™ multi-array module provides packaging techniques for assembly of multiple HC series CMOS arrays and cache memory die into a single hermetically sealed ceramic module. MICROPAK-II™ multi-array modules dramatically improve systems' reliability, and reduce system volume and cost. Consult Honeywell for more details.

The HC20000 is available in a 256 LDCC and a 284 PGA package. If more specific packaging information is needed, please contact your Honeywell representative.

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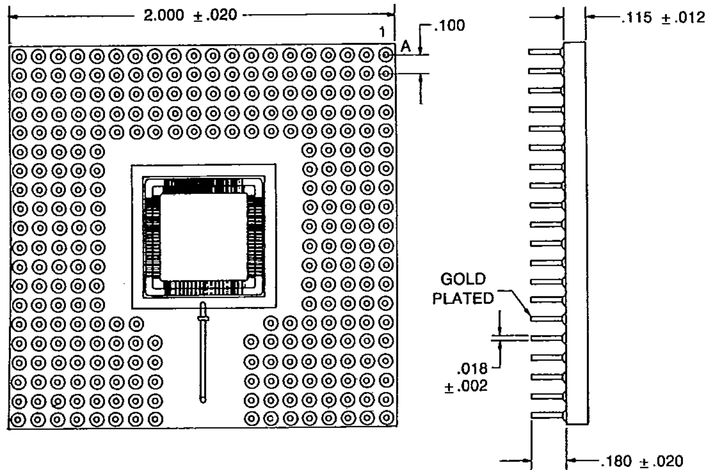
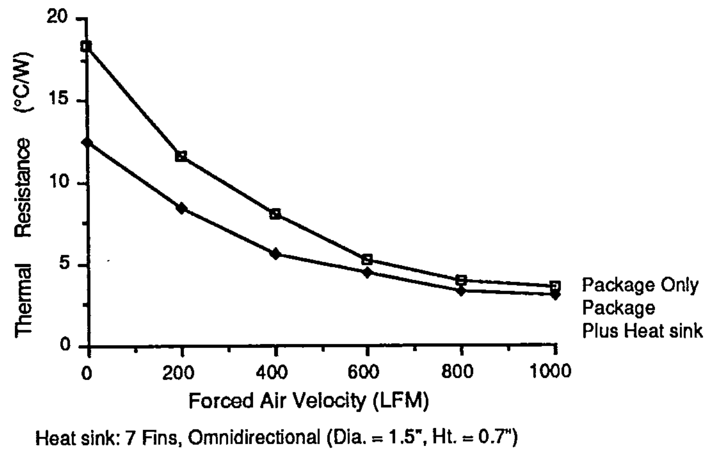
284 PIN GRID ARRAY

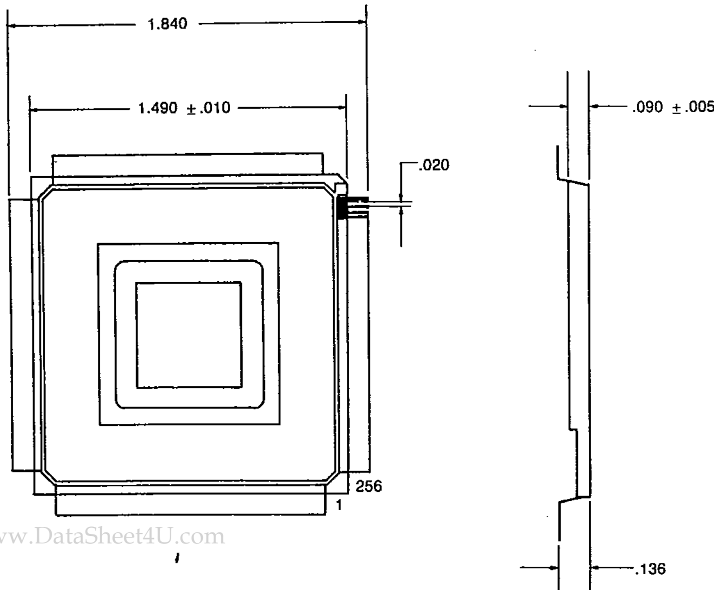


THERMAL CHARACTERISTICS



Heat sink: 7 Fins, Omnidirectional (Dia. = 1.5", Ht. = 0.7")

256 LEADED CHIP CARRIER



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QUALIFICATION AND SCREENING

The HC20K array is qualified and screened to the most advanced military or commercial standards.

For military applications, the array will be generically qualified to MIL-M-38510/605 requirements. Program specific qualification data is available, at an additional charge, upon request from Honeywell.

Figures 6 and 7 illustrate MIL-STD-883C Class B or modified Class S flows available.

For advanced commercial CPU applications, the HC20K can be qualified to Honeywell's commercial specification or to customer-specific qualification flows.

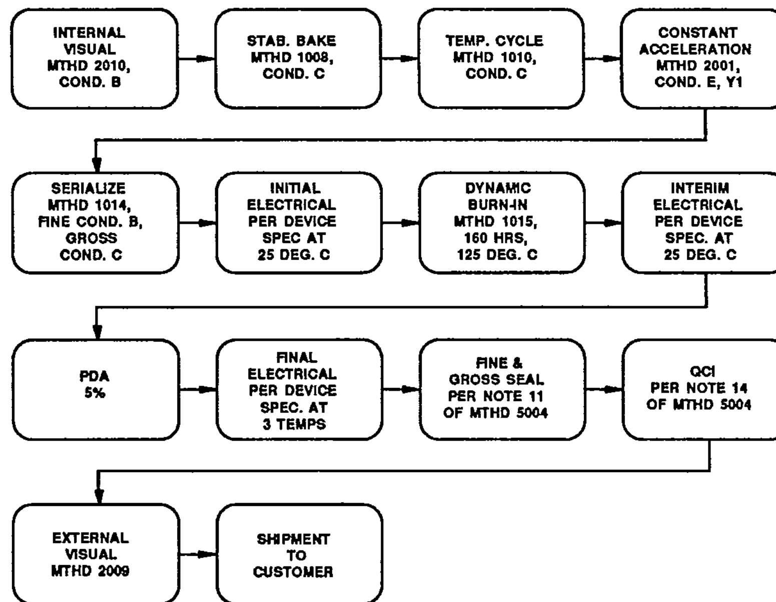

FIGURE 6. MIL-STD-883C CLASS B PRODUCT FLOW

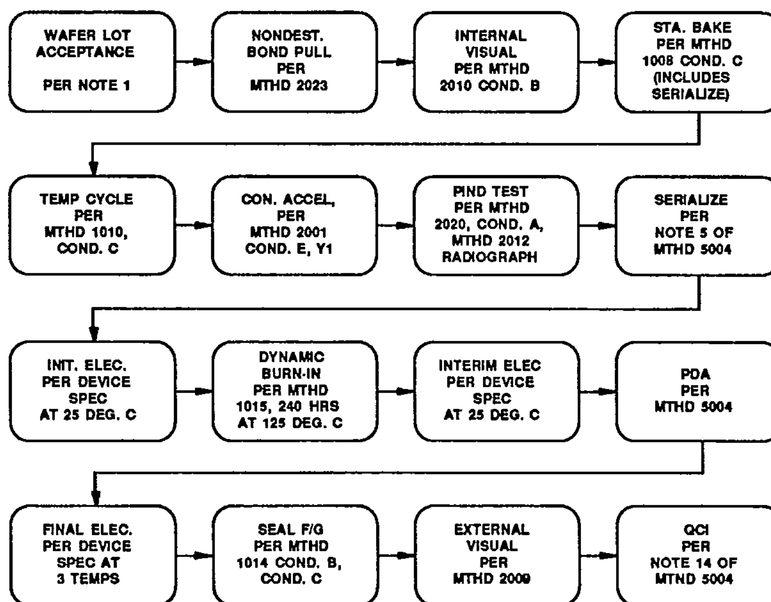

FIGURE 7. MODIFIED MIL-STD-883C CLASS S PRODUCT FLOW

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ABSOLUTE MAXIMUM RATINGS

Parameter	Description	Ratings		Units
		Min.	Max.	
V_{dd}	DC Supply Voltage	-0.3	7.0	V
V_i	Input Voltage	-0.3	V_{dd} +0.3	V
I_i	DC Input Current	-100	100	µA
I_o	DC Output Current	-10	10	mA
T_a	Operating Ambient Temperature	-55	+125	°C
T_s	Storage Temperature	-65	+150	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Parameter	Description	TTL		CMOS		Units	Test Conditions (1) (2)
		Min.	Max.	Min.	Max.		
V_{il}	Low Level Input Voltage		0.8		1.5	V	Recognized as Low Signal Over Recommended V_{dd} & T_a
V_{ih}	High Level Input Voltage	2.0		3.5		V	Recognized as High Signal Over Recommended V_{dd} & T_a
V_{ol}	Low Level Output Voltage		0.4			V	V_{dd}= 4.5V, I_{ol} = 8mA
					.05	V	V_{dd}= 4.5V, I_{ol} < 1µA
V_{oh}	High Level Output Voltage	2.4				V	V_{dd}= 4.5V, I_{oh}= - 4mA
				V_{dd} -0.05		V	V_{dd}= 4.5V, I_{oh} > -1µA
I_{il} (3)	Low Level Input Current	-50		-50		µA	V_{in} = 0.5V*
I_{ih} (3)	High Level Input Current	-20		-20		µA	V_{in} = V_{dd}*
I_{ozl} (3)	3-State Output Off Leakage Current Low	-50		-50		µA	V_{out} = V_{ss}
I_{ozh} (3)	3-State Output Off Leakage High	-20		-20		µA	V_{out} = V_{dd}
I_{os} (3)	Output Short Circuit Current	-96	-15	-96	-15	mA	V_{out} = V_{ss} (5)
C_{in} (4)	Input Capacitance		3.0		3.0	pF	INPUT ONLY
			4.0		4.0	pF	BIDIRECTIONAL
C_{out} (4)	Output Capacitance		4.0		4.0	pF	BIDIRECTIONAL

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(1) Power supply voltage V_{dd} = 5.0V ±10%.
(2) Ambient temperature range T_a is -55°C to +125°C.
(3) Current entering a pin is defined as positive. Current leaving a pin is defined as negative. For specifying current on input or output pins, the most negative value is the minimum and the most positive value is the maximum.
(4) Values for C_{in} and C_{out} do not include package capacitance.
(5) For I_{os} testing, not more than one output should be shorted at a time, nor for more than one second.

*Includes pull-down device

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