RCA Solid State Division

Power Hybrid Circuits

HC2500

H-1697

(Approx. 1/2 Actual Size)

Multi-Purpose, Low-Distortion 7-Ampere Operational Amplifier

Linear Amplifier for Applications in Industrial and Commercial Equipment

Features:

- Bandwidth: 30 kHz at 60 W
- High power output: up to 100 W(rms)
- High output current: 7 A (peak)
- Low IMD and THD
- Adjustable idling current
- Stability with resistive or reactive loads
- Single or split power supply (30 to 75 V, single, ±15 to ±37.5, split)
- Class AB output stage
- Direct coupling to load
- Socket available
- Rugged package with heavy leads
- Light weight: 100 grams

RCA type HC2500● is a complete solid-state hybrid amplifier in a compact hermetic package. It employs a quasi-complementary-symmetry output circuit with hometaxial-base output transistors.

The HC2500 is a low-distortion, 100-watt linear amplifier. The output section can be externally biased class AB for low intermodulation and total harmonic distortion. Terminals are available for external frequency compensation, external short-circuit protection, and inverting and non-inverting inputs.

The HC2500 is recommended for the following applications; servo amplifiers (ac, dc, PWM), deflection amplifiers, power operational amplifiers, voltage regulators, driven inverters, hi-fi amplifiers, PA systems, and solenoid drivers.

● Derived from RCA Dev. No. TA8651A.

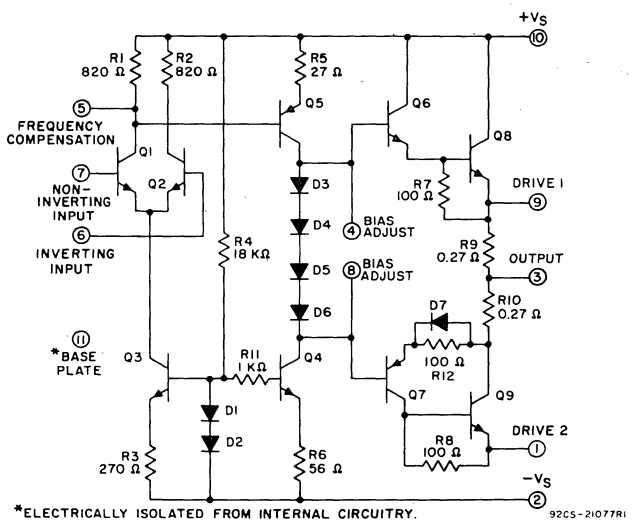


Fig. 1—Schematic diagram of type HC2500 operational amplifier.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE:
Between leads 1 and 10 ..... 75 V
OUTPUT CURRENT (Peak) ..... 7 A
TOTAL DISSIPATION:
Per output device ..... See Figs. 4 & 5
TEMPERATURE RANGE:
Storage ..... −55 to +125°C
Output junction ..... −55 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance ≥ 1/8 in. (3.17 mm) from
case for 10 s max. ..... 235°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C and Supply Voltage (V_S) = ±37.5 V*

CHARACTERISTIC	SYMBOL	REFERENCE FIG. NO.	TEST CONDITIONS				LIMITS			UNITS
			SPECIAL NOTES	FREQ. (f)–kHz	OUTPUT POWER (P_O)–W	LOAD RESIST. (R_L)–Ω	MIN.	TYP.	MAX.	
Offset Voltage	V_{offset}	3	Measured Pin 3 to Gnd	–	–	4	–	–	±250	mV
Quiescent Current	I_o	3	Idling Current < 1 mA	–	–	Open	–	–	±30	mA
Output Voltage Swing	V_{OUT}		Peak dc voltage	0	200	4	28	–	–	V
Closed-Loop Bandwidth	f_H	3		–	1	4	43	–	–	kHz
Total Harmonic Distortion	THD	15		1	60	4	–	0.3	0.5	%
Closed-Loop Voltage Gain	A_{CL}	3		1	1	4	31	32	–	
Thermal Resistance	$R_{\theta JC}$	5		–	–	–	–	–	2	°C/W

ELECTRICAL CHARACTERISTICS

Typical Values (for Design Guidance), *At Case Temperature (T_C) = 25°C and Supply Voltage (V_S) = ±37.5*

Open-Loop Voltage Gain	A_{OL}	8, 19	Idling current = 50 mA	1	25	4	–	70	–	dB
Input Offset Voltage	V_{IO}	20		–	0	Open	–	±10	–	mV
Input Offset Current	I_{IO}	20		–	0	Open	–	7	–	μA
Input Bias Current	I_{IB}	20		–	0	Open	–	20	–	μA
Common-Mode Input Impedance	R_{CM}	22		0.005	0	Open	–	1	–	MΩ
Common-Mode Input-Voltage Range	V_{ICR}			0.5	100	4	–	32	–	V
Common-Mode-Rejection Ratio	CMRR			0.005	0	Open	–	50	–	dB
Supply-Voltage Ripple-Rejection Ratio	V_{RR}			0.06	0	4	–	30	–	dB
Intermodulation Distortion	IMD	14	Idling current = 50 mA	–	0.05	4	–	0.06	–	%
Slew Rate	SR	18	A_{CL} = 2 C_c = 100 pF	0.5 Square Wave	–	4	–	4.3	–	V/μs
Idling-Current Drift	ΔI_i	17	25°C to 100°C	–	–	4	–	1	–	mA/°C

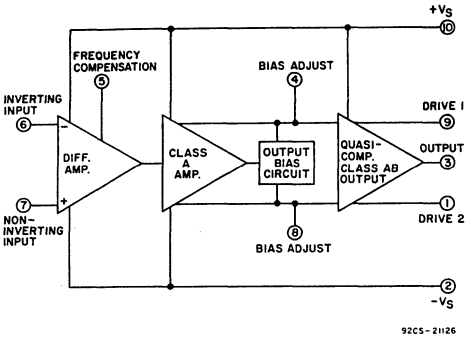


Fig. 2 – Block diagram of HC2500 100-watt class AB amplifier.

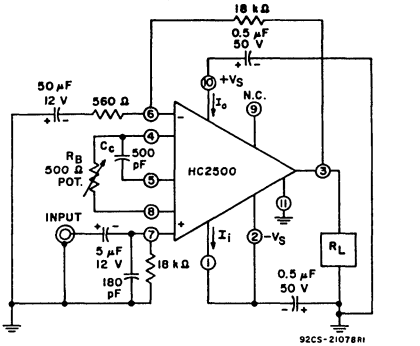


Fig. 3 – Typical test circuit with split supply for measuring A_{CL}, I_i, I_o, V_{offset}, f_H, THD, and IMD.

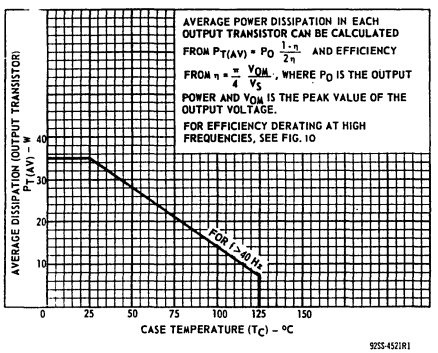


Fig. 4 – Dissipation (average) derating curve for each output transistor (for symmetrical waveforms with f >40 Hz).

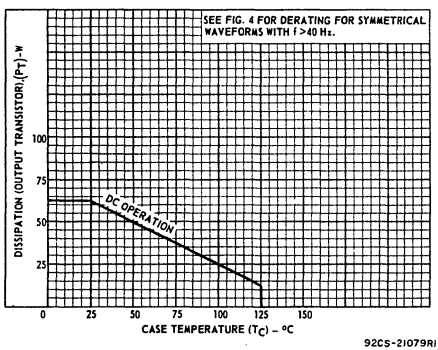


Fig. 5 – Dissipation derating curve for each output transistor.

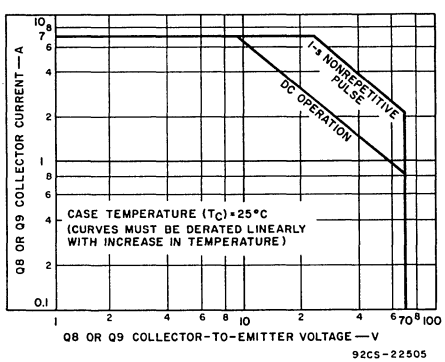


Fig. 6 – Maximum operating area for HC2500.

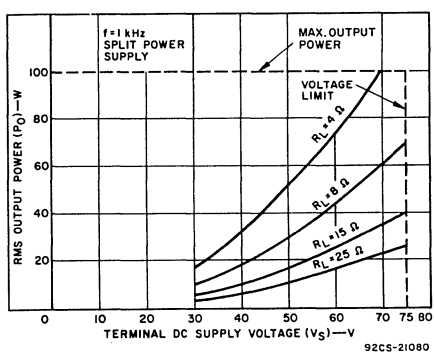


Fig. 7 – Output power as a function of supply voltage, with various values of load resistance, for symmetrical sine-wave operation.

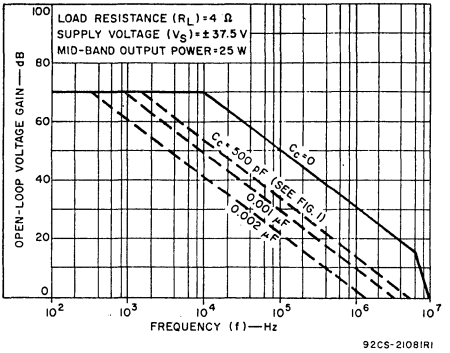


Fig. 8 — Typical open-loop voltage gain vs. frequency.

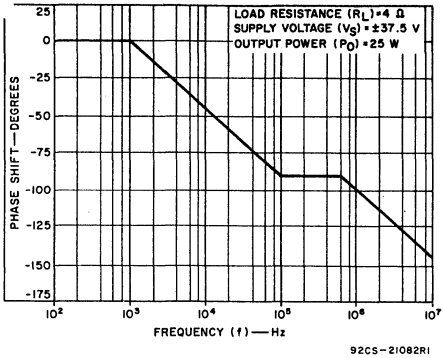


Fig. 9 — Typical open-loop phase shift vs. frequency.

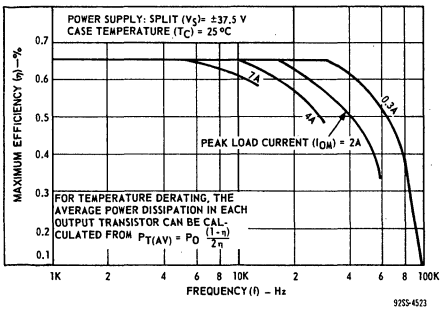


Fig. 10 — Maximum efficiency vs. frequency for several values of peak load current.

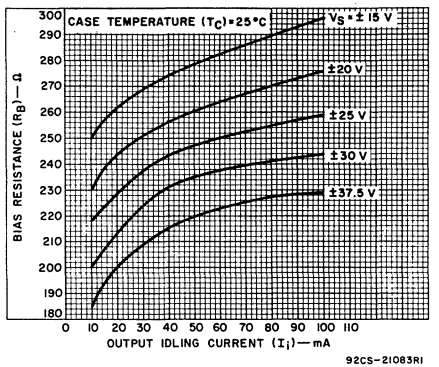


Fig. 11 — Bias resistor (R_B in Fig. 3) value vs. output idling current (I_I).

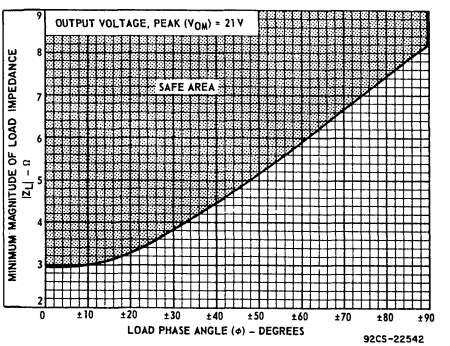


Fig. 12 — Minimum load impedance vs. load phase angle and safe area of operation.

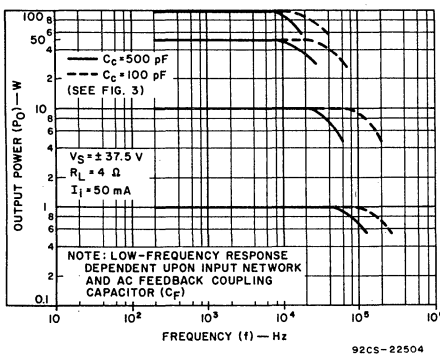


Fig. 13 — Output power vs. frequency.

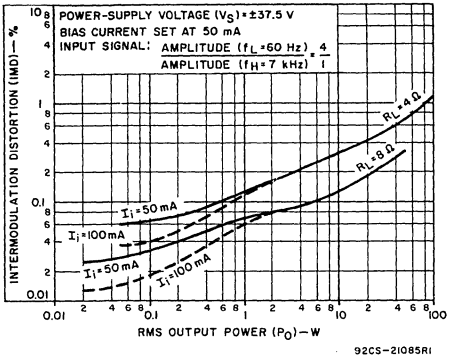


Fig. 14 — Typical intermodulation distortion vs. rms output power.

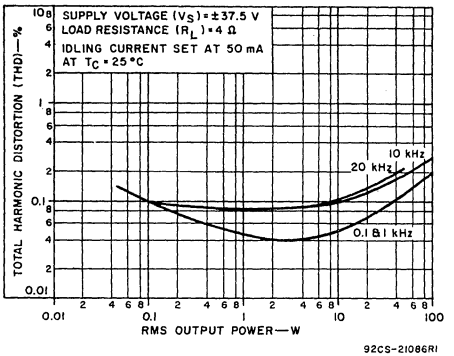


Fig. 15 — Typical total harmonic distortion vs. rms output power.

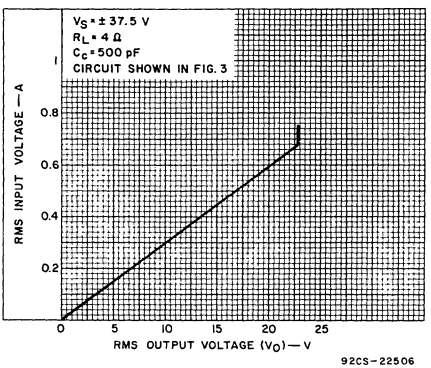


Fig. 16 — Input sensitivity.

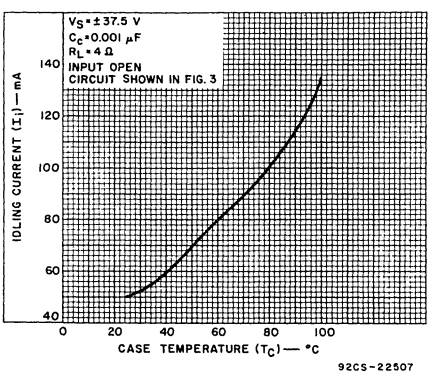


Fig. 17 — Typical idling-current dirft.

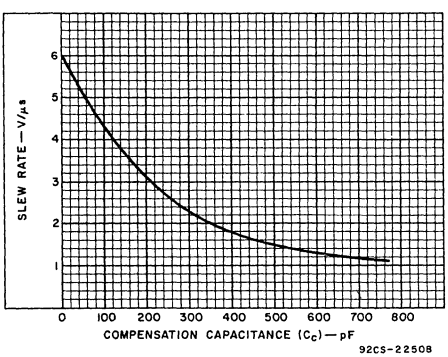


Fig. 18 — Typical slew rate vs. value of compensation capacitor, C_C (test circuit shown in Fig. 21).

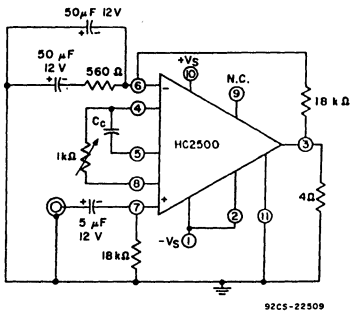
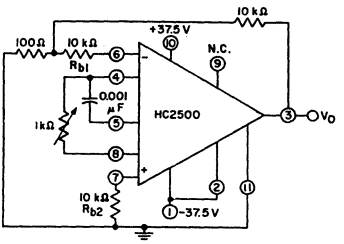


Fig. 19 — Test circuit for open-loop gain and phase response.



$$V_{IO} = -\frac{V_O}{100} \text{ with } R_{b1} \text{ and } R_{b2} \text{ shorted}$$

$$I_{IO} = -\frac{V_O}{100\,R_{b2}}$$

$$I_{Ib} = \frac{\pm V_O}{100\,R_{b2}} \text{ with } R_{b1} \text{ shorted}$$

92CS-22510

Fig. 20 — Test circuit for input offset voltage and current test.

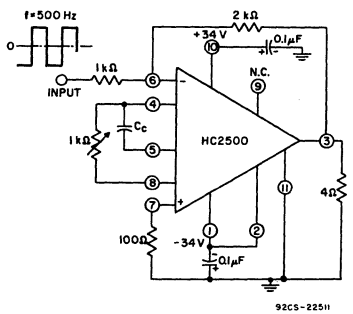
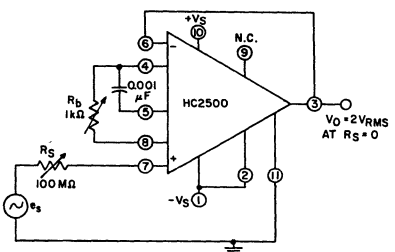


Fig. 21 — Circuit used to test slew rate.



$R_{CM} = 9\,R_S$ with series resistance (R_S) increased from zero until output voltage (V_O) is reduced by 10%.

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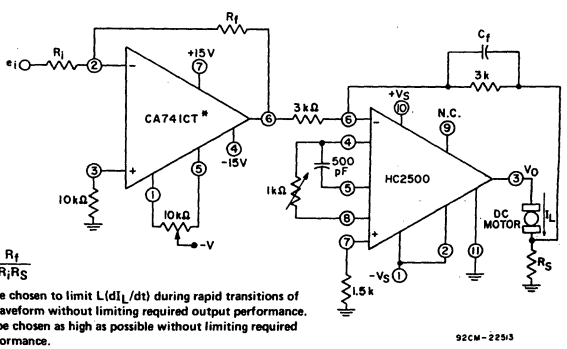
Fig. 22 — Test circuit for measuring common-mode input resistance.

TYPICAL APPLICATION CIRCUITS

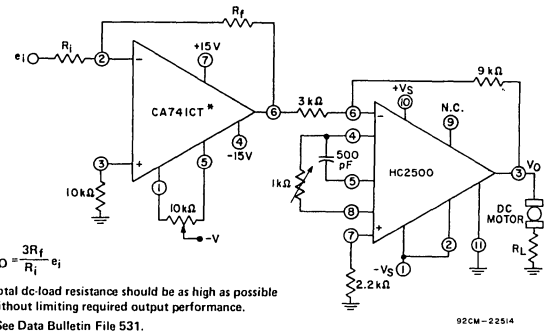


$$|I_L| = |e_i|\frac{R_f}{R_i R_S}$$

C_f should be chosen to limit $L(dI_L/dt)$ during rapid transitions of the input waveform without limiting required output performance. R_S should be chosen as high as possible without limiting required output performance.

*See Data Bulletin File 531.

Fig. 23 — Current-feedback motor-control circuit.



$V_O = \frac{3R_f}{R_i} e_i$

Total dc-load resistance should be as high as possible without limiting required output performance.

*See Data Bulletin File 531.

Fig. 24 — Voltage-feedback motor-control circuit.

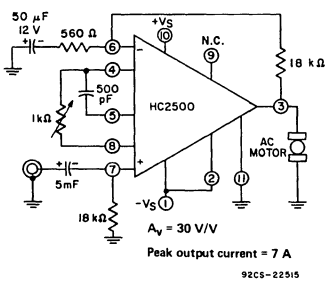
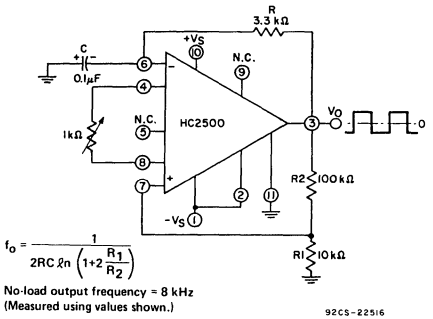


Fig. 25 — AC motor control.



$f_o = \frac{1}{2RC \ln\left(1+2\frac{R_1}{R_2}\right)}$

Fig. 26 — High-power astable multivibrator.

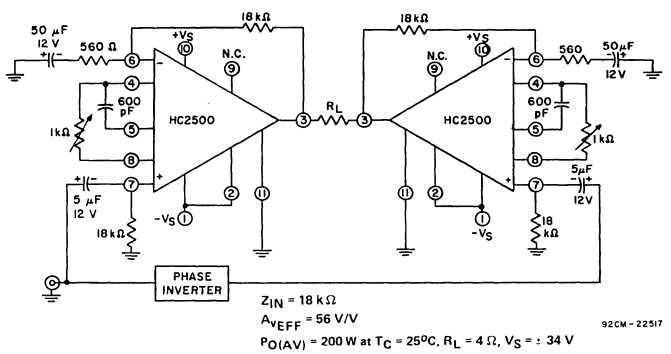
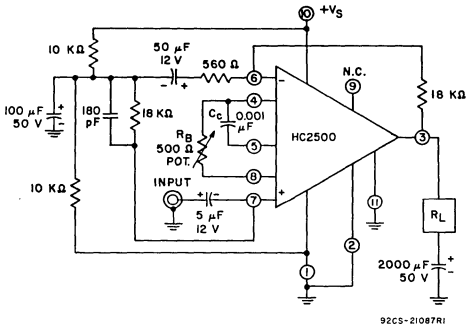


Fig. 27 — Bridge circuit for loads greater than 100 watts.



V_S	54 V
P_{out}	60 W
Idling Current (R_B = 168 Ω	50 mA
THD	0.15%
IMD @ 50 mW	0.06%
V_{offset} Pin 3 To Gnd.	+ 100 mV
Efficiency	64%
R_L	4 ohms

Fig. 28 — Typical circuit connections for operation of HC2500 with single-ended supply, and performance data.

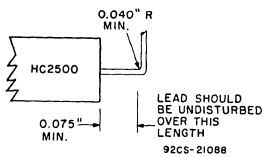


Fig. 29 — Recommended lead-bending specification.

COMPARISON CHART

TYPE	IM DIST. @ 50 mW	OUTPUT PROTECTION NETWORK	OPERATING MODE	FREQUENCY COMPENSATION	COMMUTATING DIODES
HC2500	0.06%	NO	CLASS AB	CAPACITOR ON SIGNAL TERMINALS	NO
HC2000H	5.8%	YES	CLASS B	LC FILTER ON OUTPUT	YES