TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4051AP, TC74HC4051AF, TC74HC4051AFT
TC74HC4052AP, TC74HC4052AF, TC74HC4052AFT
TC74HC4053AP, TC74HC4053AF, TC74HC4053AFN, TC74HC4053AFT

TC74HC4051AP/AF/AFT 8 – CHANNEL ANALOG MULTIPLEXER / DEMULITIPLEXER
TC74HC4052AP/AF/AFT DUAL 4 – CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER
TC74HC4053AP/AF/AFN/AFT TRIPLE 2 – CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel×2 configuration and the TC74HC4053A has a 2 channel×3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal (V_{CC}-V_{EE}) can then be switched by the small logical amplitude (V_{CC}-GND) control signal.

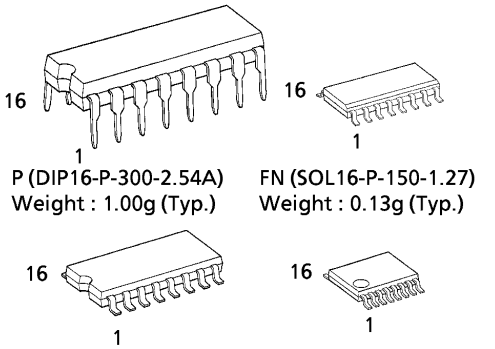
For example, in the case of V_{CC}=5V, GND=0V, V_{EE}=-5V, signals between-5V and+5V can be switched from the logical circuit with a single power supply of 5V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} = 15ns(typ.) at V_{CC} = 5V, V_{EE} = 0V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Low ON Resistance ····· R_{ON} = 50Ω (typ.) at V_{CC}-V_{EE} = 9V
- High Noise Immunity ····· THD = 0.02% (typ.) at V_{CC}-V_{EE} = 9V
- Pin and Function Compatible with 4051/4052/4053B

(Note) The JEDEC SOP (FN) is not available in Japan.



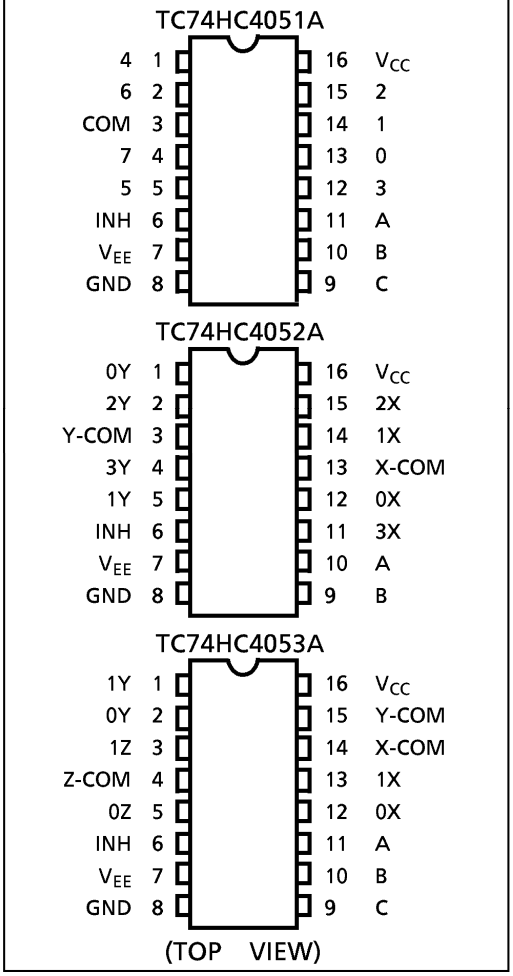
P (DIP16-P-300-2.54A) Weight : 1.00g (Typ.)

FN (SOL16-P-150-1.27) Weight : 0.13g (Typ.)

F (SOP16-P-300-1.27) Weight : 0.18g (Typ.)

FT (TSSOP16-P-0044-0.65) Weight : 0.06g (Typ.)

PIN ASSIGNMENT



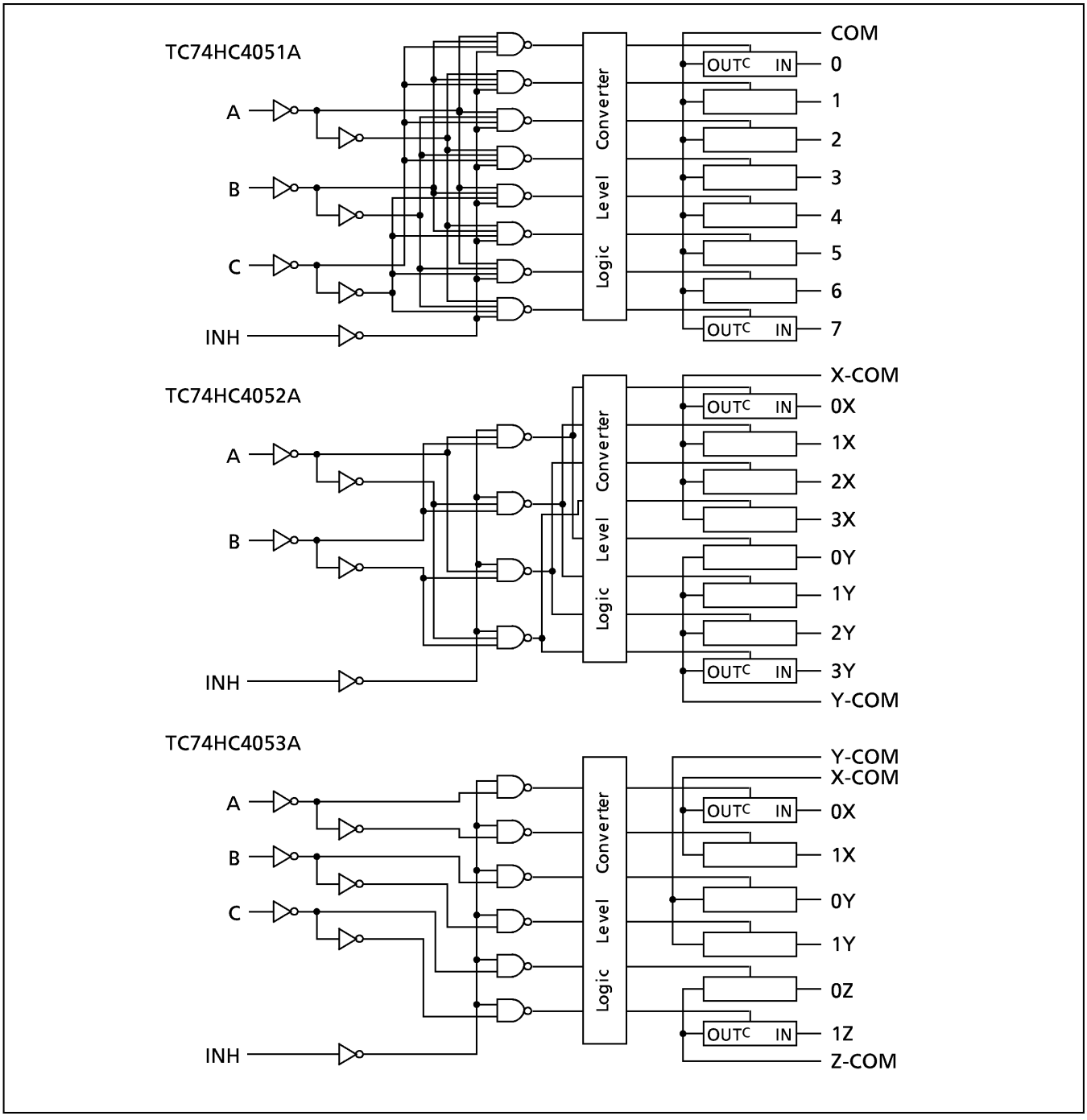
TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X,0Y,0Z
L	L	L	H	1	1X, 1Y	1X,0Y,0Z
L	L	H	L	2	2X, 2Y	0X,1Y,0Z
L	L	H	H	3	3X, 3Y	1X,1Y,0Z
L	H	L	L	4	– –	0X,0Y,1Z
L	H	L	H	5	– –	1X,0Y,1Z
L	H	H	L	6	– –	0X,1Y,1Z
L	H	H	H	7	– –	1X,1Y,1Z
H	X	X	X	NONE	NONE	NONE

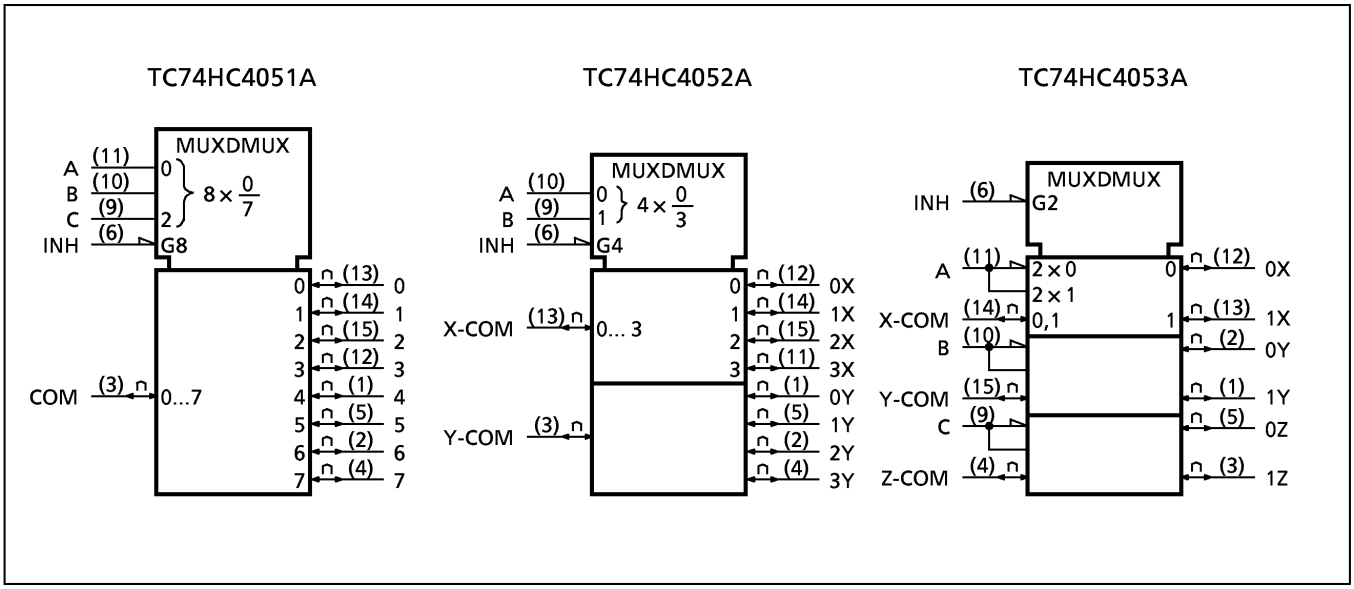
X : Don't Care, * : Except HC4052A

961001EBA2

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
Supply Voltage Range	V_{CC}-V_{EE}	−0.5~13	V
Control Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
Switch I/O Voltage	$V_{I/O}$	V_{EE} − 0.5~V_{CC} + 0.5	V
Control Input Diode Current	I_{ICK}	± 20	mA
I/O Diode Current	I_{IOK}	± 20	mA
Switch through Current	I_T	± 25	mA
DC V_{CC} or Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP, TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	2~6	V
Supply Voltage Range	V_{EE}	−6~0	V
Supply Voltage Range	V_{CC}-V_{EE}	2~12	V
Control Input Voltage	V_{IN}	0~V_{CC}	V
Switch I/O Voltage	$V_{I/O}$	V_{EE}~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Control Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{EE} (V)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Control Input Voltage	V_{IHC}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Control Input Voltage	V_{ILC}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
ON Resistance	R_{ON}	$V_{IN} = V_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND −4.5 −6.0	4.5 4.5 6.0	— — —	85 55 50	180 120 100	— — —	225 150 125	Ω
		$V_{IN} = N_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} \leq 2mA$	GND GND −4.5 −6.0	2.0 4.5 4.5 6.0	— — — —	150 70 50 45	— 150 100 80	— — — —	— 190 125 100	Ω
Difference of ON Resistance Between Switches	$\triangle R_{ON}$	$V_{IN} = V_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND −4.5 −6.0	4.5 4.5 6.0	— — —	10 5 5	30 12 10	— — —	35 15 12	Ω
Input / Output Leakage Current (SWITCH OFF)	I_{OFF}	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_{IN} = V_{ILC}$ or V_{IHC}	GND −6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	nA
Switch Input Leakage Current (SWITCH ON)	I_{IZ}	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{ILC}$ or V_{IHC}	GND −6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	nA
Control Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	GND −6.0	6.0 6.0	— —	— —	4.0 8.0	— —	40.0 80.0	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns, GND = 0V)

PARAMETER	SYMBOL	TEST CONDITION	V_{EE} (V)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Phase difference between Input and Output	ϕ I/O	ALL TYPES	GND	2.0	—	25	60	—	75	ns
			GND	4.5	—	6	12	—	15	
			GND	6.0	—	5	10	—	13	
			−4.5	4.5		4	—	—	—	
Output Enable Time	t_{pZL} t_{pZH}	*1 4051	GND	2.0	—	64	225	—	280	
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
			−4.5	4.5		18	—	—	—	
		*1 4052	GND	2.0	—	64	225	—	280	
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
			−4.5	4.5		18	—	—	—	
		*1 4053	GND	2.0	—	50	225	—	280	
			GND	4.5	—	14	45	—	56	
			GND	6.0	—	12	38	—	48	
			−4.5	4.5		14	—	—	—	
Output Disable Time	t_{pLZ} t_{pHZ}	*1 4051	GND	2.0	—	100	250	—	315	
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
			−4.5	4.5		29	—	—	—	
		*1 4052	GND	2.0	—	100	250	—	315	
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
			−4.5	4.5		29	—	—	—	
		*1 4053	GND	2.0	—	95	225	—	280	
			GND	4.5	—	30	45	—	56	
			GND	6.0	—	26	38	—	48	
			−4.5	4.5		26	—	—	—	
Control Input Capacitance	C_{in}	ALL TYPES	—	—	—	5	10	—	10	pF
COMMON Terminal Capacitance	C_{IS}	4051	−5.0	5.0	—	36	70	—	70	
		4052			—	19	40	—	40	
		4053			—	11	20	—	20	
SWITCH Terminal Capacitance	C_{OS}	4051	−5.0	5.0	—	7	15	—	15	
		4052			—	7	15	—	15	
		4053			—	7	15	—	15	
Feedthrough Capacitance	C_{IOS}	4051	−5.0	5.0	—	0.95	2	—	2	
		4052			—	0.85	2	—	2	
		4053			—	0.75	2	—	2	
Power Dissipation Capacitance	C_{PD}	*2 4051	GND	5.0	—	70	—	—	—	
		4052			—	71	—	—	—	
		4053			—	67	—	—	—	

* 1: $R_L = 1k\Omega$

* 2: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

ANALOG SWITCH CHARACTERRISTICS (GND = 0V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION			V_{EE} (V)	V_{CC} (V)	TYP.	UNIT
Sine Wave Distortion (T.H.D)		RL = 10kΩ, C_L = 50pF, f_{IN} = 1kHz	V_{IN} = 4.0V_{P-P}		−2.25	2.25	0.025	%
			V_{IN} = 8.0V_{P-P}		−4.5	4.5	0.020	
			V_{IN} = 11.0V_{P-P}		−6.0	6.0	0.018	
Frequency Responce (Switch ON)	f_{MAX}	Adjust f_{IN} Voltage to obtain 0dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter reads −3dB. R_L = 50Ω, C_L = 10pF, f_{IN} = 1MHz, Sine Wave	*1	ALL	−2.25	2.25	120	MHz
			*2	4051			45	
				4052			70	
				4053			95	
			*1	ALL	-4.5	4.5	190	
			*2	4051			70	
				4052			110	
				4053			150	
			*1	ALL	−6.0	6.0	200	
			*2	4051			85	
				4052			140	
				4053			190	
Feed through Attenuation (Switch OFF)		Vin is centered at (V_{CC} - V_{EE}) / 2, Adjust input for 0dBm. R_L = 600Ω, C_L = 50pF, f_{IN} = 1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	
Crosstalk (Control Input to Signal Output)		R_L = 600Ω, C_L = 50pF, f_{IN} = 1MHz, Square Wave ($t_r = t_f$ = 6ns)			−2.25	2.25	60	mV
					−4.5	4.5	140	
					−6.0	6.0	200	
Crosstalk (Between any switches)		Adjust V_{IN} to obtain 0dBm at Input. R_L = 600Ω, C_L = 50pF, f_{IN} = 1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	

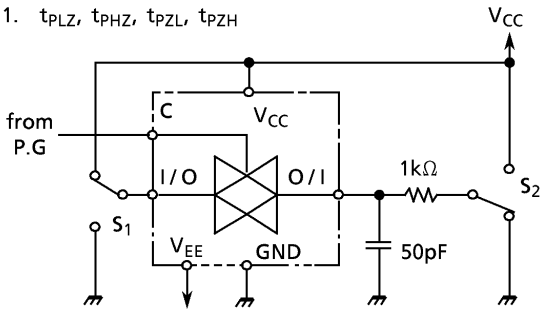
*1 : Input COMMON Terminal, and measured at SWITCH Terminal.

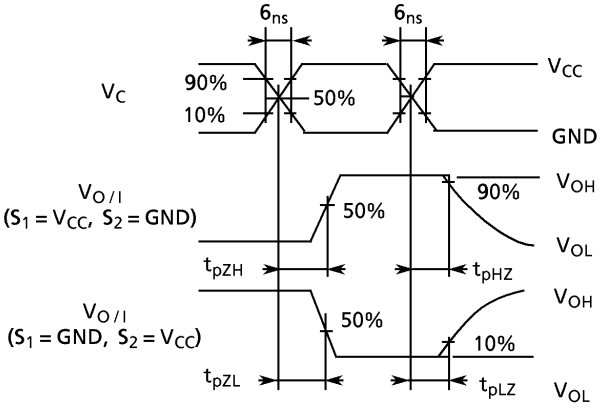
*2 : Input SWITCH Terminal, and measured at COMMON Terminal.

NOTE : These characteristics are determined by design of devices.

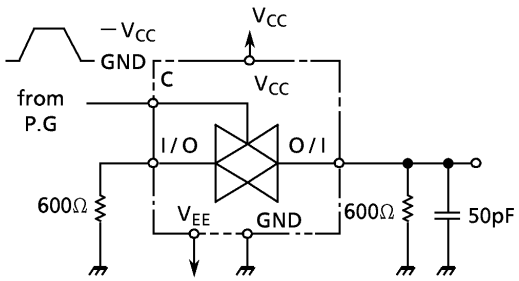
SWITCHING CHARACTERISTICS TEST CIRCUITS

1. t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

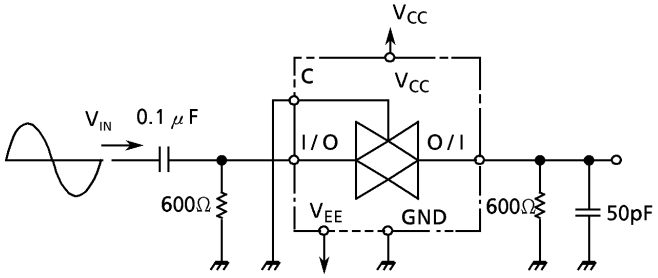




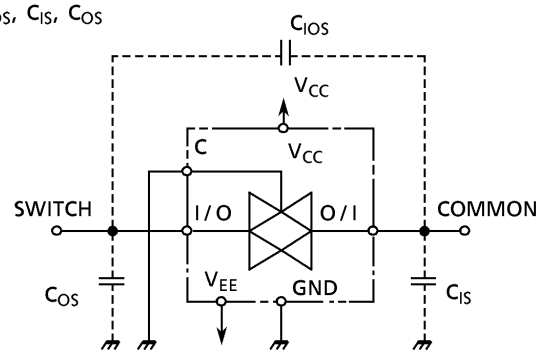
2. CROSS TALK (CONTROL INPUT – SWITCH OUTPUT)
fin = 1MHz duty = 50% tr = tf = 6ns



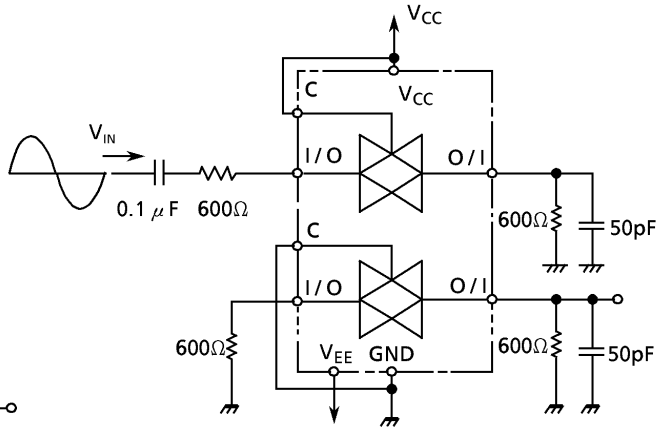
3. FEEDTHROUGH ATTENUATION



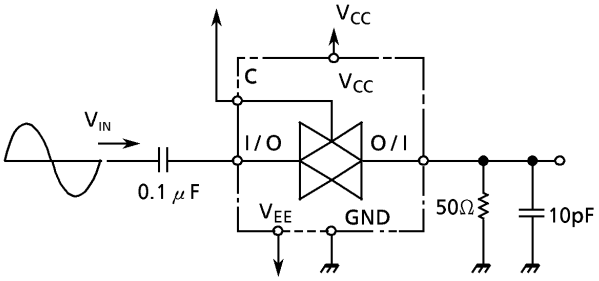
4. C_{IOS}, C_{IS}, C_{OS}



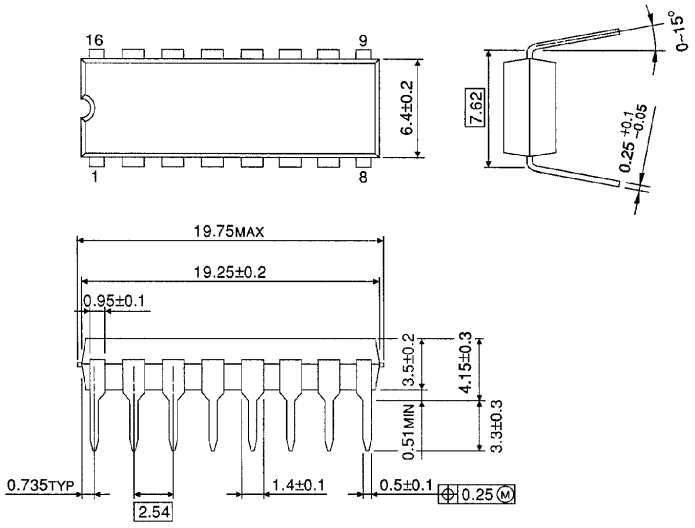
5. CROSS TALK (BETWEEN ANY TWO SWITCHES)



6. FREQUENCY RESPONSE (SWITCH ON)

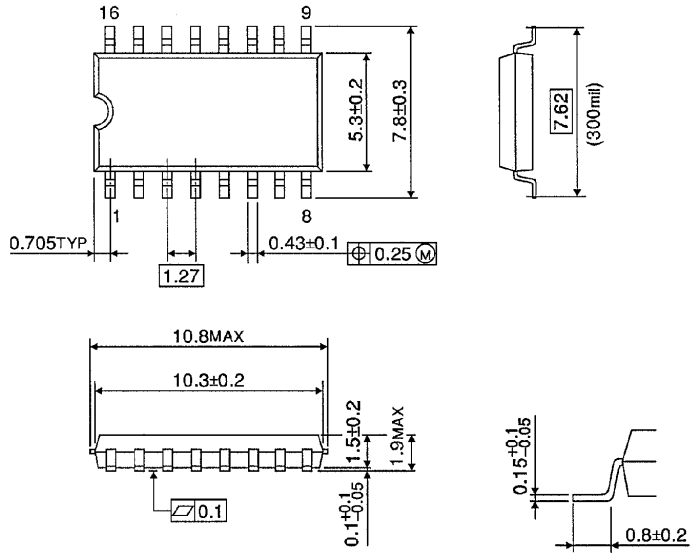


DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

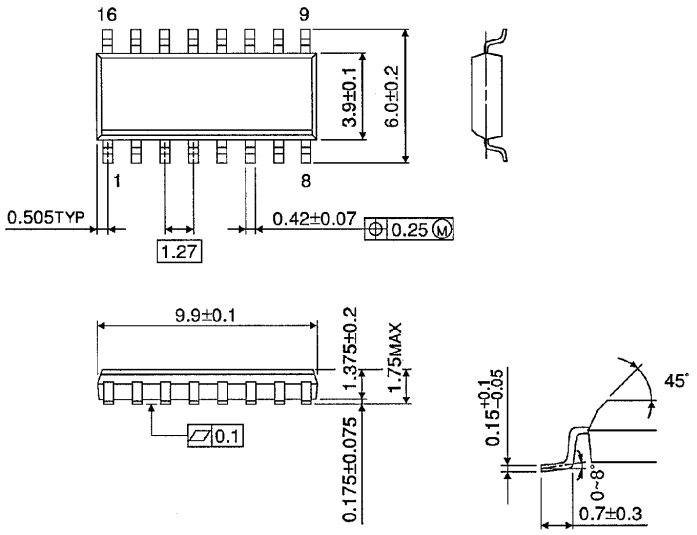
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

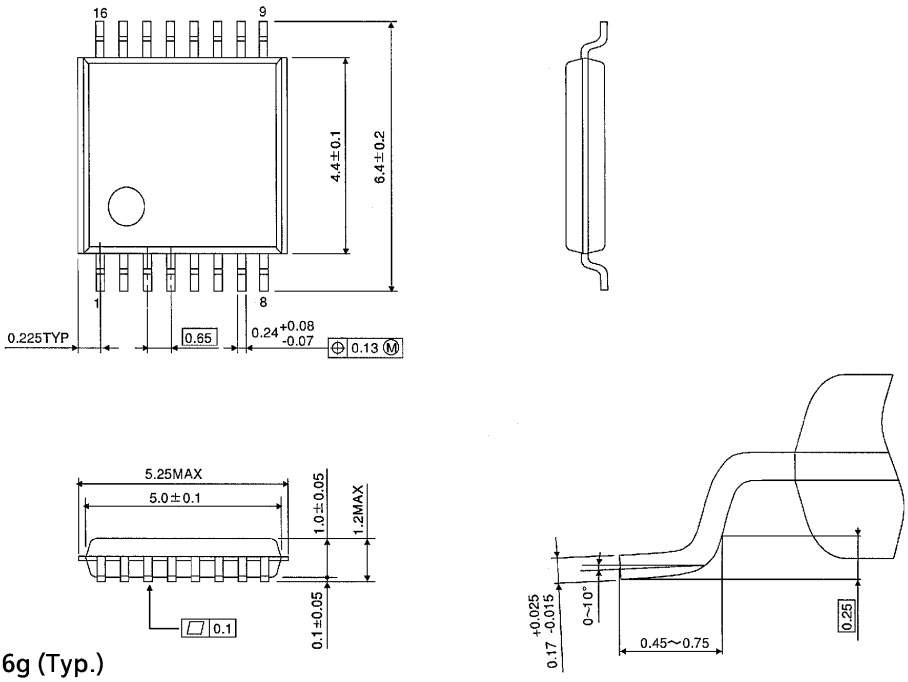
SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)