

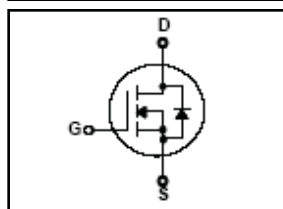
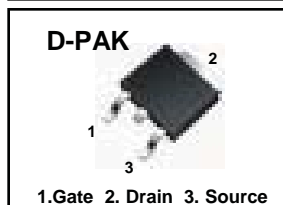
HCD70R1K4P

700V N-Channel Super Junction MOSFET

$BV_{DSS} = 700\text{ V}$
 $R_{DS(on)Typ} = 1.15\ \Omega$
 $I_D = 4.0\text{ A}$

FEATURES

- Originative New Design
- Superior Avalanche Rugged Technology
- Robust Gate Oxide Technology
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Unrivalled Gate Charge : 7.5 nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)} : 1.15\ \Omega$ (Typ.) @ $V_{GS}=10\text{V}$
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	700	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	4.0	A
	Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	2.8	A
I_{DM}	Drain Current – Pulsed (Note 1)	12.0	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	130	mJ
I_{AR}	Avalanche Current (Note 1)	2.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.2	mJ
dv/dt	Peak Diode Recovery dv/dt	50	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	21	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	6.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$	--	1.15	1.4	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	700	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 700 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	10	μA
		$V_{DS} = 560 \text{ V}, T_J = 125^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	± 100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$	--	280	--	pF
C_{oss}	Output Capacitance		--	30	--	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 350 \text{ V}, I_D = 4 \text{ A},$ $R_G = 25 \Omega$	--	15	40	ns
t_r	Turn-On Rise Time		--	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	70	ns
t_f	Turn-Off Fall Time		--	20	50	ns
Q_g	Total Gate Charge	$V_{DS} = 560 \text{ V}, I_D = 4 \text{ A}$ $V_{GS} = 10 \text{ V}$	--	7.5	10	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	2.5	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	4	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	12	
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 4 \text{ A}, V_{GS} = 0 \text{ V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 4 \text{ A}, V_{GS} = 0 \text{ V}$	--	150	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100 \text{ A}/\mu\text{s}$	--	0.85	--	μC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=16.2\text{mH}, I_{AS}=4\text{A}, V_{DD}=50\text{V}, R_G=25\Omega,$ Starting $T_J=25^\circ\text{C}$

Typical Characteristics

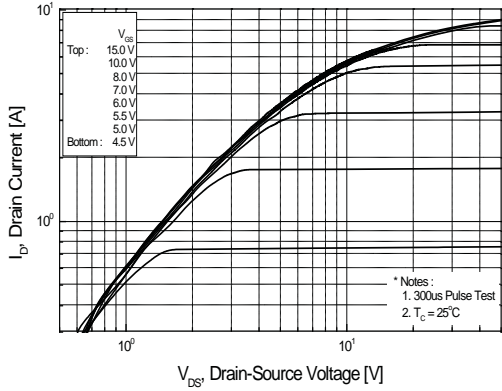


Figure 1. On Region Characteristics

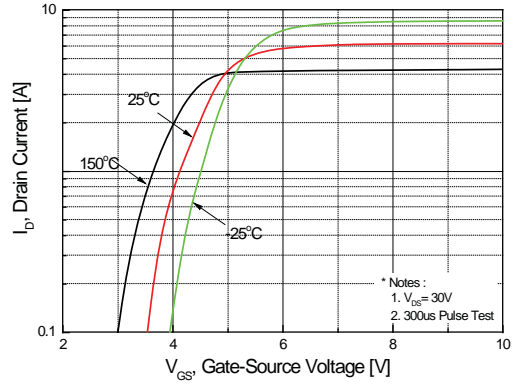


Figure 2. Transfer Characteristics

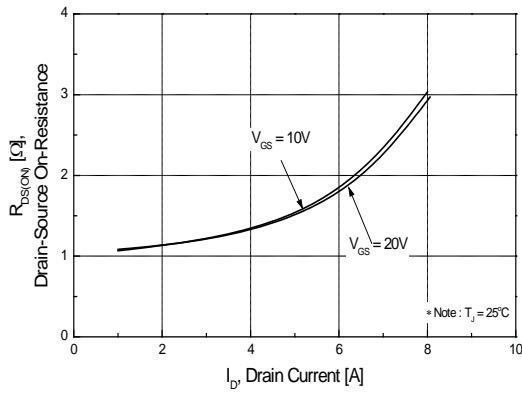


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

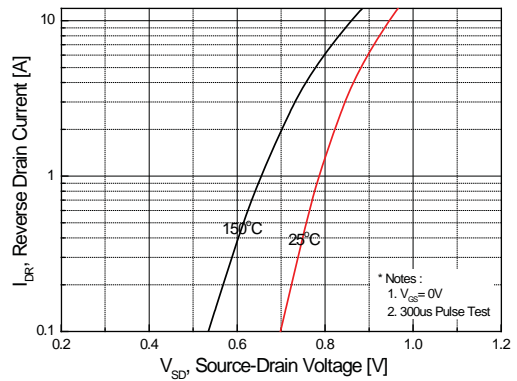


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

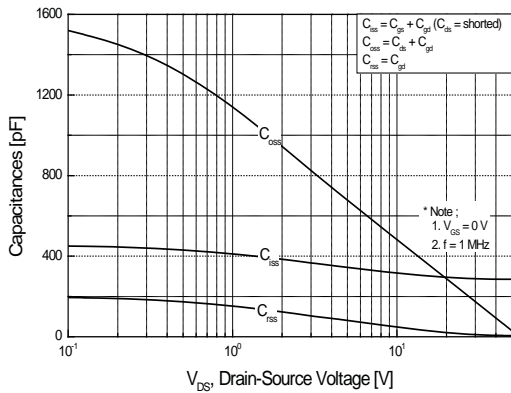


Figure 5. Capacitance Characteristics

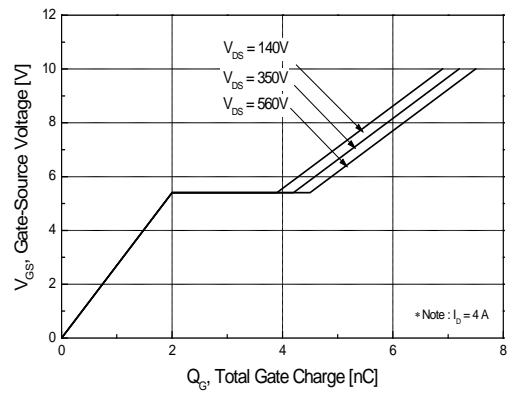


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

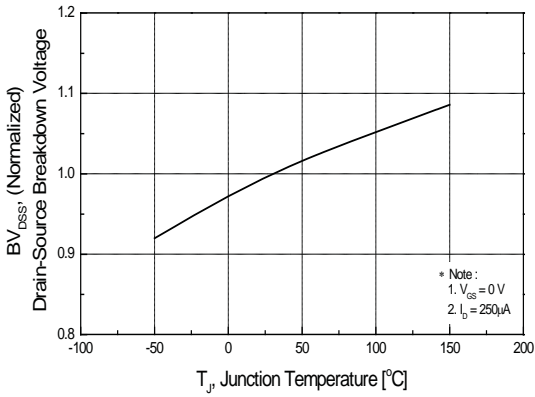


Figure 7. Breakdown Voltage Variation vs Temperature

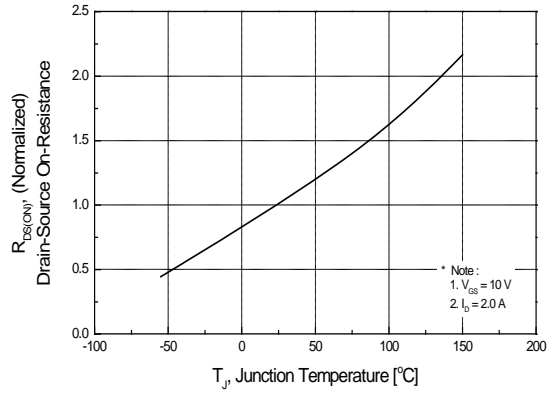


Figure 8. On-Resistance Variation vs Temperature

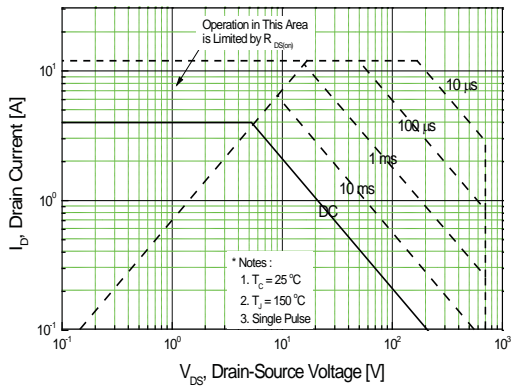


Figure 9. Maximum Safe Operating Area

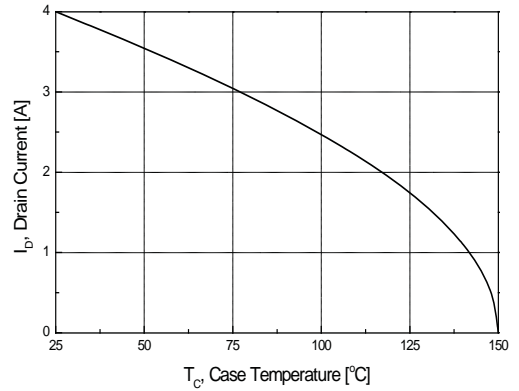


Figure 10. Maximum Drain Current vs Case Temperature

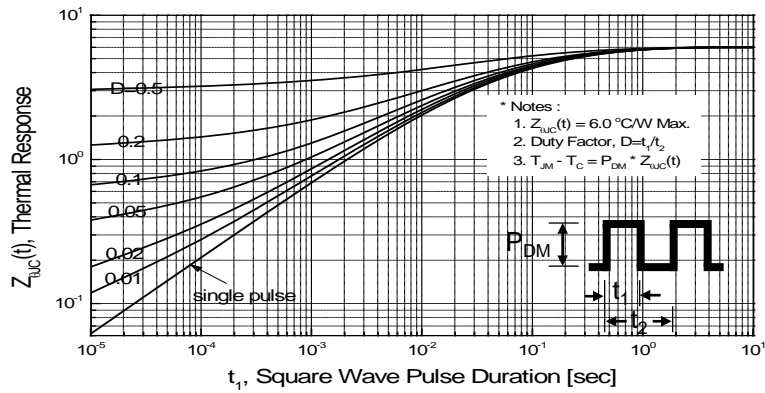


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform



Fig 13. Resistive Switching Test Circuit & Waveforms

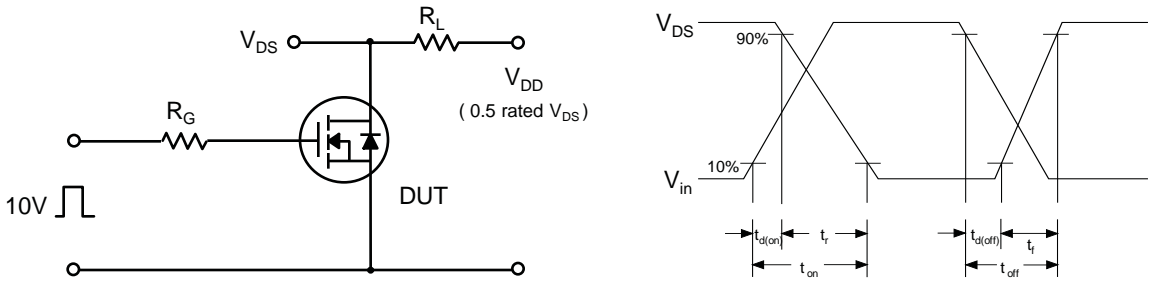


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

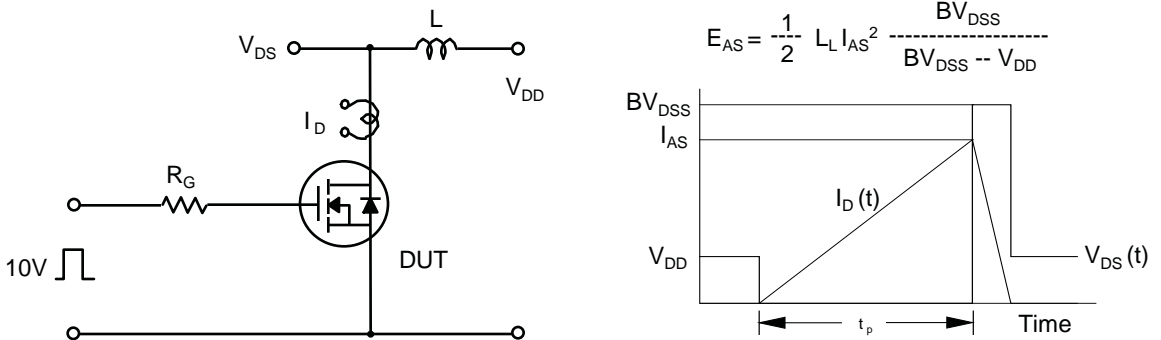
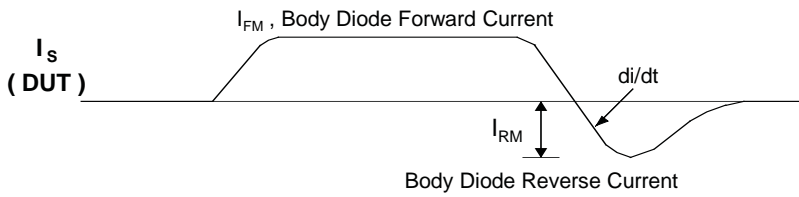
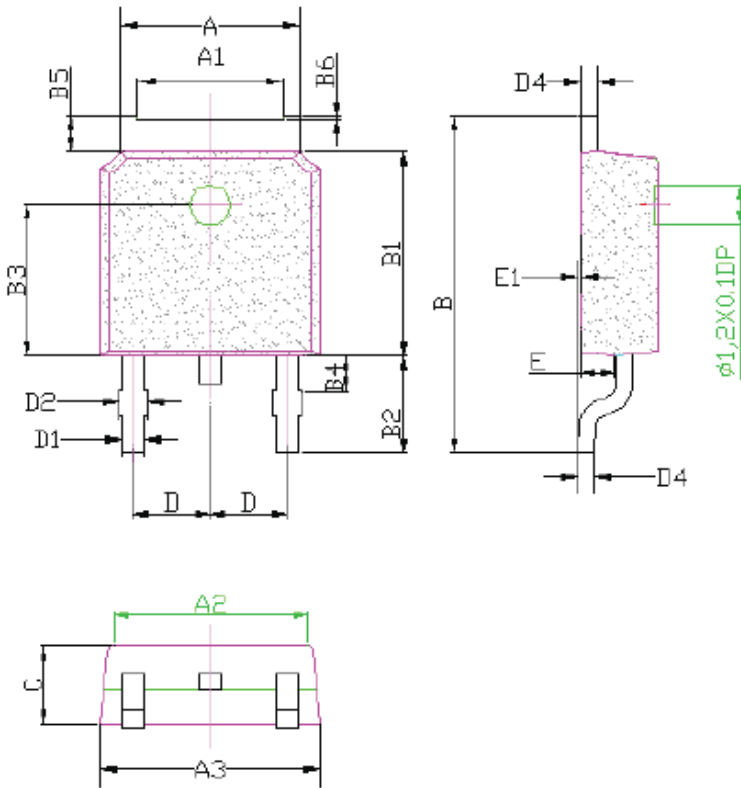


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252L)



DIM	MILLIMETERS
A	5.33 ± 0.2
A1	4.33 ± 0.2
A2	5.78 ± 0.1
A3	6.6 ± 0.2
B	10 ± 0.5
B1	6.1 ± 0.3
B2	2.85 ± 0.5
B3	4.5 ± 0.25
B4	1.0 ± 0.1
B5	1.05 ± 0.1
B6	0.1 ± 0.05
C	2.3 ± 0.2
D	2.286 ± 0.05
D1	0.62 ± 0.15
D2	0.75 ± 0.15
D3	0.5 ± 0.15
D4	0.5 ± 0.15
E	1.01 ± 0.2
E1	0.1 ± 0.05
DIA	$\odot 1.2$ (deep 0.1)

Unit :mm