Dual Channel Low Input Current, High Gain Optocouplers

Technical Data

HCPL-2730 HCPL-0730
HCPL-2731 HCPL-0731

Features

- **High Current Transfer Ratio – 1800% Typical**
- **Low Input Current Requirements – 0.5 mA**
- **Low Output Saturation Voltage – 0.1 V**
- **High Density Packaging**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **LSTTL Compatible**
- **High Output Current – 60 mA**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 Minute and 5000 V rms* for 1 minute
  CSA Approved
- **Available in 8 Pin DIP and SO-8 Footprint**
- **MIL-STD-1772 Version Available (HCPL-5730/5731)**
- **Surface Mount Gull Wing Option Available for 8-Pin DIP (Option 300)**

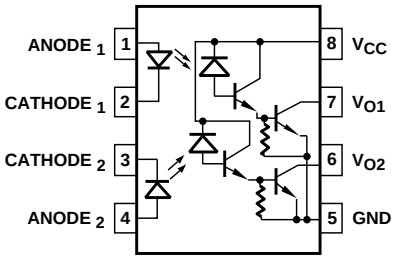
Applications

- **Digital Logic Ground Isolation**
- **Telephone Ring Detector**
- **Level Shifting**
- **EIA RS-232C Line Receiver**
- **Polarity Sensing**
- **Low Input Current Line Receiver - Long Line or Party Line**
- **Microprocessor Bus Isolation**
- **Current Loop Receiver**
- **Line Voltage Status Indicator -Low Input Power Dissipation**

Description

These dual channel optocouplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photo detectors. They provide extremely high current transfer ratio and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. In addition, V_{CC} may be as low as 1.6 V

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

*5000 V rms/1 minute withstand voltage rating is for Option 020 (HCPL-2730, HCLP-2731) products only.
A 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

without adversely affecting the parametric performance.

These dual channel optocouplers are available in an 8-Pin DIP and in an industry standard SO-8 package. The following is a cross reference table listing the 8-Pin DIP part number and the electrically equivalent SOIC-8 part number.

8-Pin DIP	SO-8
HCPL-2730	HCPL-0730
HCPL-2731	HCPL-0731

The SO-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

Guaranteed operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731/0731 have a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS, and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18 V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18 V.

The HCPL-2730/0730 are specified at an input current of 1.6 mA and have a 7 V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing at this input current.

Important specifications such as CTR, leakage current, and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation. Selection for lower input currents down to 250 µA is available upon request.

Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8		Widebody Package (400 mil)				Hermetic
Single Channel Package	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package	Minimum Input ON Current (I_F)	Minimum CTR	Absolute Maximum V_{CC}	Single and Dual Channel Packages HCPL-
6N139[1]	2731	0701[1]	0731	HCNW139[1]	0.5 mA	400%	18 V	
6N138[1]	2730	0700[1]	0730	HCNW138[1]	1.6 mA	300%	7 V	
HCPL-4701[1]	4731[1]	070A[1]	073A[1]		40 µA	800%	18 V	
					0.5 mA	300%	20 V	5701[1] 5700[1] 5731[1] 5730[1]

Note:
1. Technical data are on separate HP publications.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

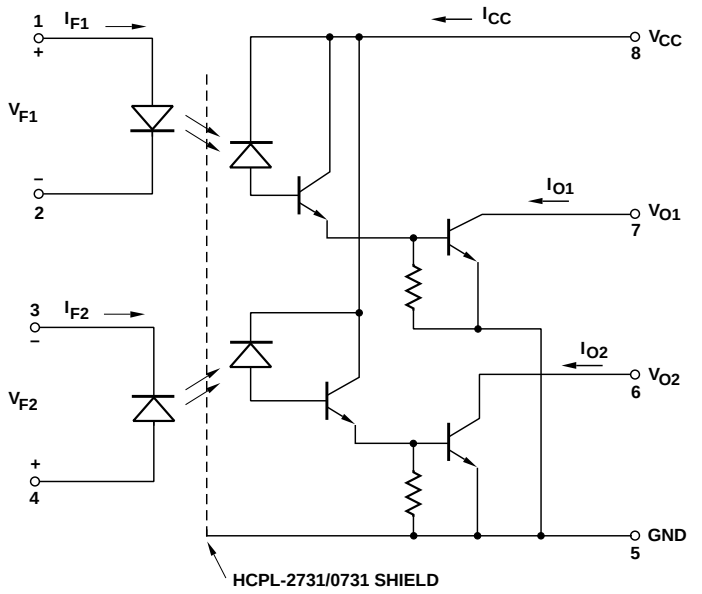
HCPL-2731#XXX

- 020 = 5000 V rms/1 Minute UL Rating Option.*
- 300 = Gull Wing Surface Mount Option, 50 per tube.**
- 500 = Tape and Reel Packaging Option, 1000 per reel.

Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

*For HCPL-2731 and HCPL-2730 only.
**Gull wing surface mount option applies to through hole parts only.

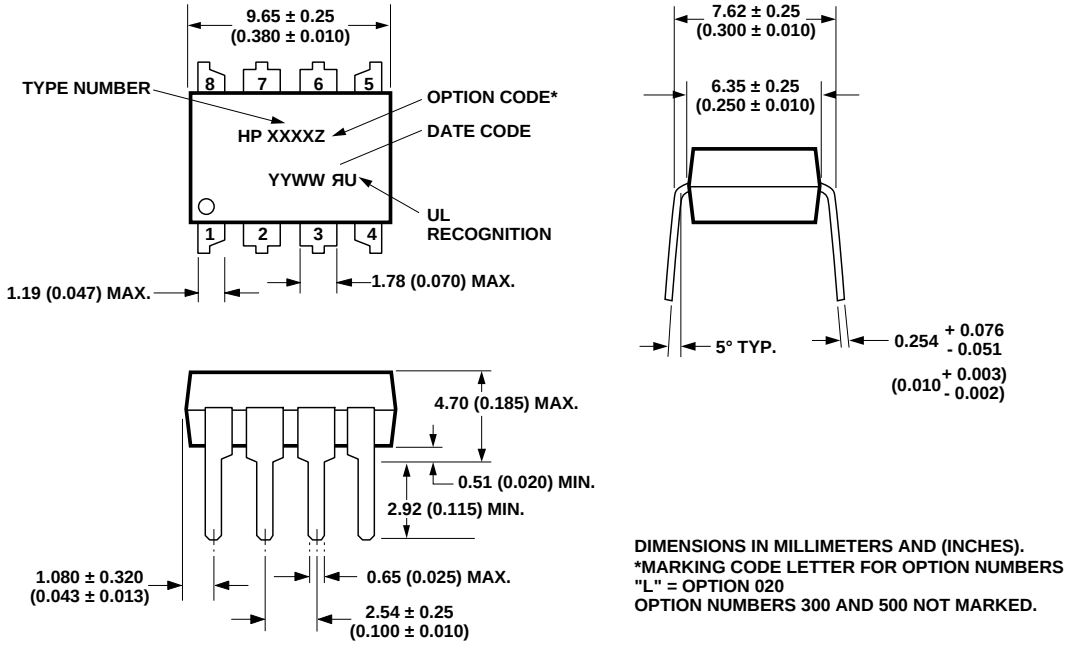
Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED (SEE NOTE 8)

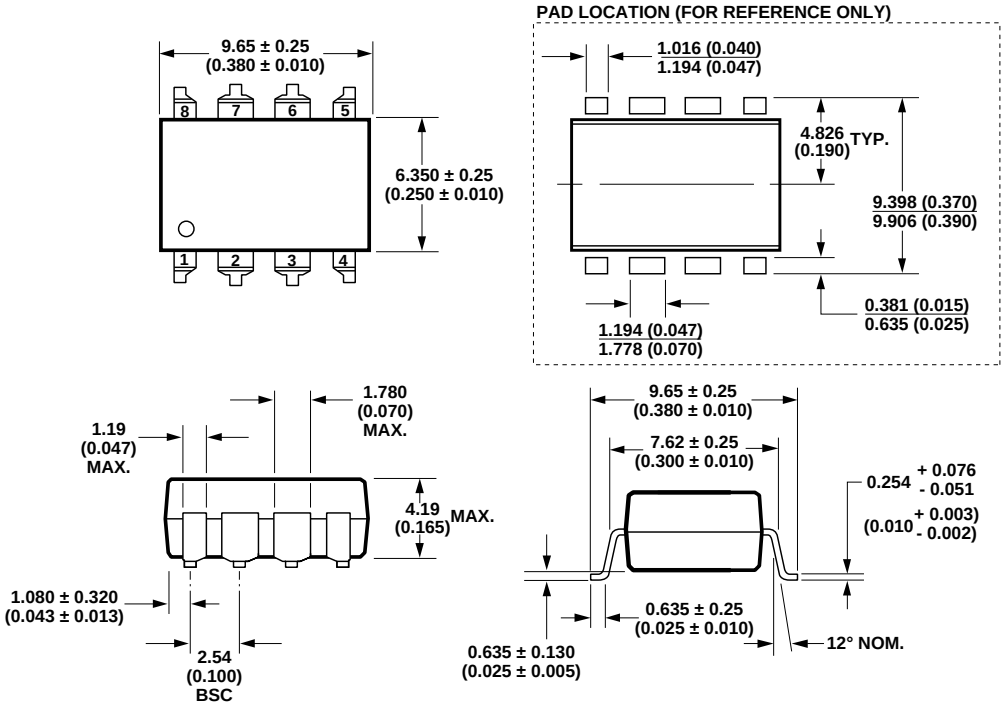
Package Outline Drawings

8-Pin DIP Package (HCPL-2731/HCPL-2730)



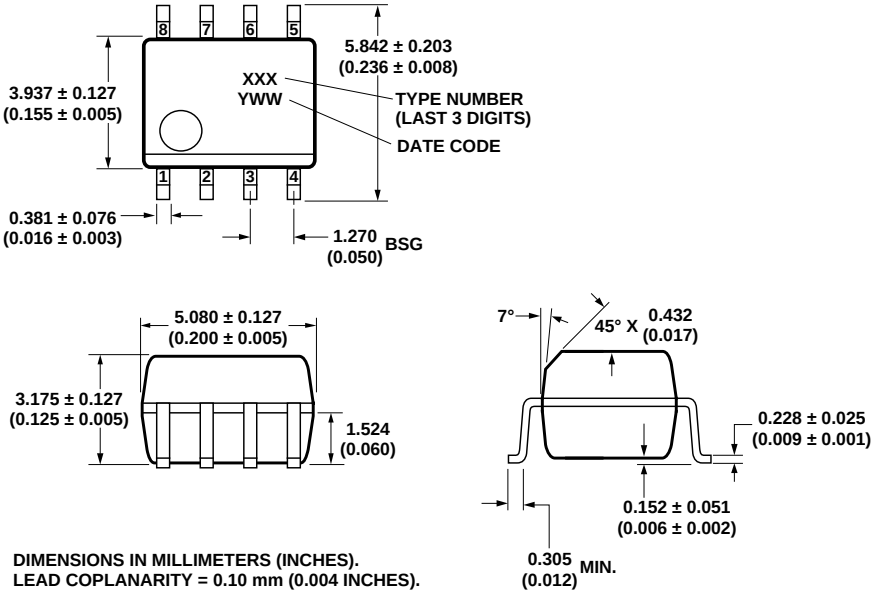
DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-2731/HCPL-2730)

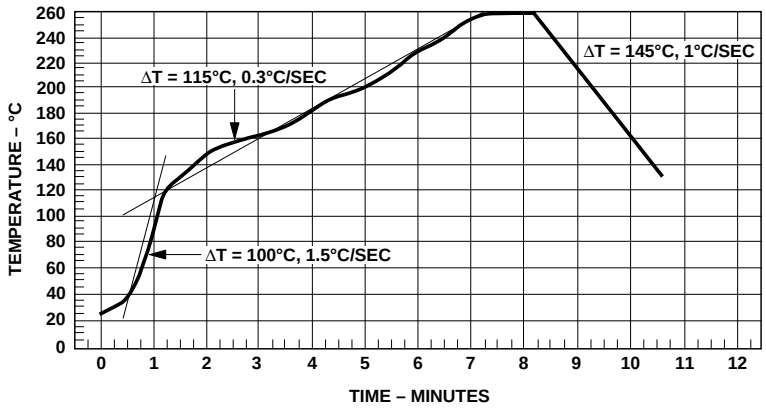


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

Small Outline SO-8 Package (HCPL-0731/HCPL-0730)



Solder Reflow Temperature Profile (HCPL-073X and Gull Wing Surface Mount Option 300 Parts).



Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The HCPL-2731/2730 have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation Related Specifications (HCPL-2731/2730/0731/0730)

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/ VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group DIN VDE 0110

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	85	°C
Average Forward Input Current	$I_{F(AVG)}$		20	mA
Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width)	I_{FPK}		40	mA
Reverse Input Voltage (Each Channel)	V_R		5	V
Input Power Dissipation (Each Channel)	P_I		35	mW
Output Current (Each Channel)	I_O		60	mA
Supply Voltage and Output Voltage (HCPL-2731, HCPL-0731) (V_{CC} - Pin 8-5, V_O - Pin 7,6-5) -Note 1	V_{CC}	-0.5	18	V
Supply Voltage and Output Voltage (HCPL-2730, HCPL-0730) (V_{CC} - Pin 8-5, V_O - Pin 7,6-5) -Note 1	V_{CC}	-0.5	7	V
Output Power Dissipation (Each Channel) -Note 12	P_O		100	mW
Total Power Dissipation (Each Channel)	P_T		135	mW
Lead Solder Temperature (for Through Hole Devices)	260°C for 10 sec., 1.6 mm below seating plane			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage (HCPL-2731/HCPL-0731)	V_{CC}	4.5	18	V
Power Supply Voltage (HCPL-2730/HCPL-0730)	V_{CC}	4.5	7	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	°C

Electrical Specifications

$0°C \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 18\ V$, $0.5\ mA \le I_{F(ON)} \le 12\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, unless otherwise specified. All Typicals at $T_A = 25°C$. (See note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR	2731 0731	400	1800	5000	%	$I_F = 0.5\ mA$	$V_{CC} = 4.5$ $V_O = 0.4\ V$	2, 3	2
			500	1600	2600		$I_F = 1.6\ mA$			
		2730/0730	300	1600	2600		$I_F = 1.6\ mA$			
Logic Low Output Voltage	V_{OL}	2731 0731		0.1	0.4	V	$I_F = 1.6\ mA$, $I_O = 8\ mA$	$V_{CC} = 4.5\ V$	1	
				0.1	0.4		$I_F = 5.0\ mA$, $I_O = 15\ mA$			
				0.2	0.4		$I_F = 12\ mA$, $I_O = 24\ mA$			
		2730/0730		0.1	0.4		$I_F = 1.6\ mA$, $I_O = 4.8\ mA$			
Logic High Output Current	I_{OH}	2731/0731		0.05	100	µA	$V_O = V_{CC} = 18\ V$	$I_F = 0\ mA$		2
		2730/0731		0.1	250		$V_O = V_{CC} = 7\ V$			
Logic Low Supply Current	I_{CCL}	2731/0731		1.2	3	mA	$V_{CC} = 18\ V$	$I_{F1} = I_{F2} = 1.6\ mA$ $V_{O1} = V_{O2} = Open$	5	
		2730/0730		0.9			$V_{CC} = 7\ V$			
Logic High Supply Current	I_{CCH}	2731/0731		0.005	20	µA	$V_{CC} = 18\ V$	$I_{F1} = I_{F2} = 0\ mA$, $V_{O1} = V_{O2} = Open$	5	
		2730/0730		0.004			$V_{CC} = 7\ V$			
Input Forward Voltage	V_F			1.4	1.7	V	$T_A = 25°C$		4	
					1.75		$I_F = 1.6\ mA$			
Input Reverse Breakdown Voltage	BV_R		5.0			V	$I_R = 10\ µA$, $T_A = 25°C$			2
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	$I_F = 1.6\ mA$			
Input Capacitance	C_{IN}			60		pF	$f = 1\ MHz$, $V_F = 0$			2

*All typical values at $T_A = 25°C$ and $V_{CC} = 5\ V$, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified. (See note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	2731 0731		25	100	µs	T_A = 25°C	6, 7, 8, 9	2
					120		I_F = 0.5 mA Rl = 4.7 kΩ		
		2730 2731 0730 0731		5	20		T_A = 25°C		
					25		I_F = 1.6 mA, Rl = 2.2 kΩ		
				0.5	2		T_A = 25°C		
					3		I_F = 12 mA, Rl = 270 Ω		
Propagation Delay Time to Logic High at Output	t_{PLH}	2731 0731		10	60	µs	T_A = 25°C	7, 8, 9	2
					90		I_F = 0.5 mA, Rl = 4.7 kΩ		
		2730 2731 0730 0731		10	35		T_A = 25°C		
					50		I_F = 1.6 mA, Rl = 2.2 kΩ		
				1	10		T_A = 25°C		
					15		I_F = 12 mA, Rl = 270 Ω		
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1000	10000		V/µs	I_F = 0 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}	10	2, 6, 7
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L$		1000	10000		V/µs	I_F = 1.6 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}		

*All typical values at T_A = 25°C and V_{CC} = 5 V, unless otherwise noted.

Package Characteristics

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		4, 9
Option 020		2730 2731	5000						4, 10
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 VDC RH ≤ 45%		4
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		11
Input-Input Insulation Leakage Current	I_{I-I}		0.005			µA	RH ≤ 45% V_{I-I} = 500 VDC		5
Input-Input Insulation Leakage Current	R_{I-I}			10^{11}		Ω			5
Capacitance (Input-Input)	C_{I-I}	2730 2731		0.03		pF			5
		0730 0731		0.25					

*All Typical values at T_A = 25°C unless otherwise noted.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:
1. Pin 5 should be the most negative voltage at the detector side.
2. Each channel.
3. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
4. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
7. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 110 Ω.
8. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 adjacent to the device is recommended.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 3000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, I_{I-O} < 5 µA).
11. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
12. Derate linearly above 65°C free-air temperature at a rate of 2.3 mW/°C for the SO-8 package.

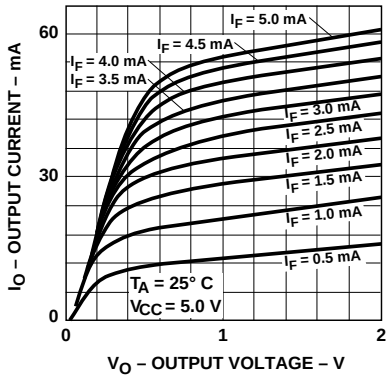


Figure 1. DC Transfer Characteristics.

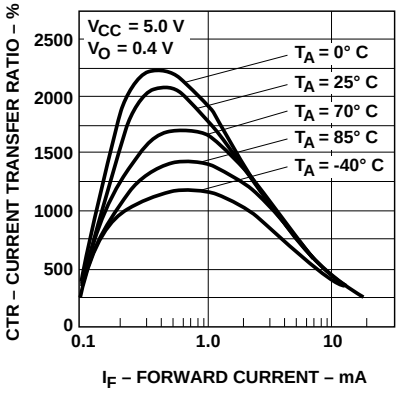


Figure 2. Current Transfer Ratio vs. Forward Current.

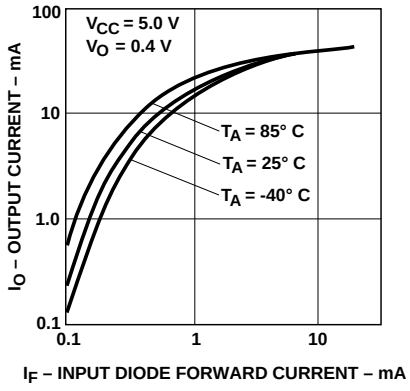


Figure 3. Output Current vs. Input Diode Forward Current.

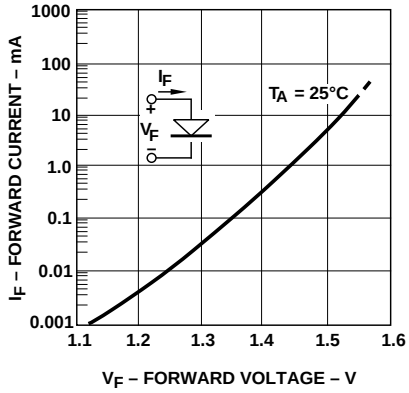


Figure 4. Input Diode Forward Current vs. Forward Voltage.

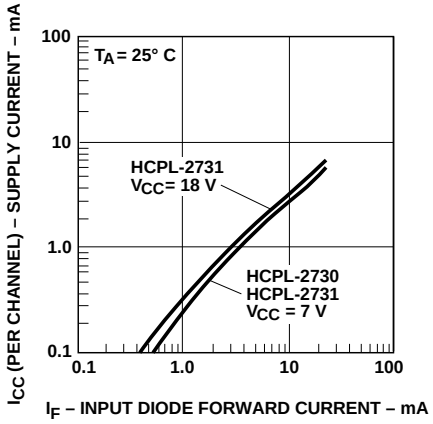


Figure 5. Supply Current per Channel vs. Input Diode Forward Current.

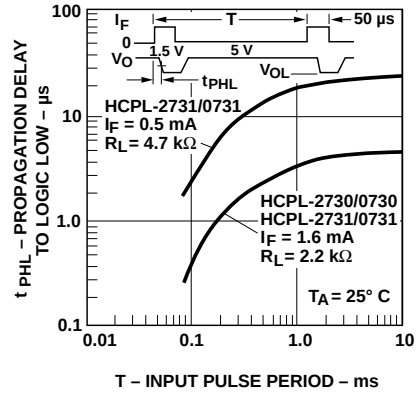


Figure 6. Propagation Delay to Logic Low vs. Pulse Period.

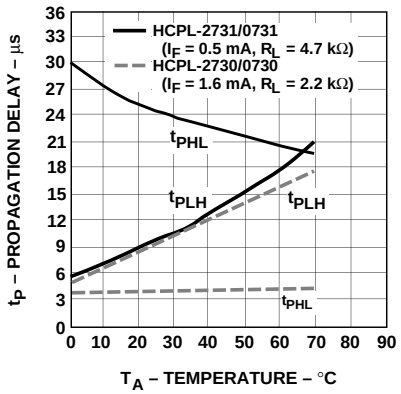


Figure 7. Propagation Delay vs. Temperature.

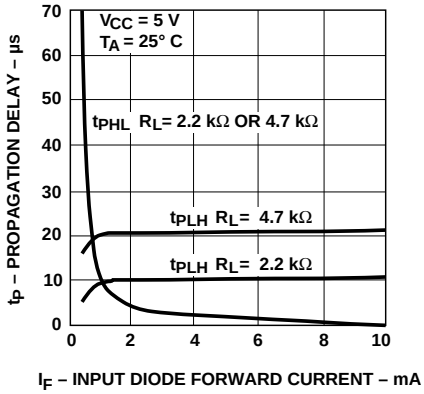


Figure 8. Propagation Delay vs. Input Diode Forward Current.

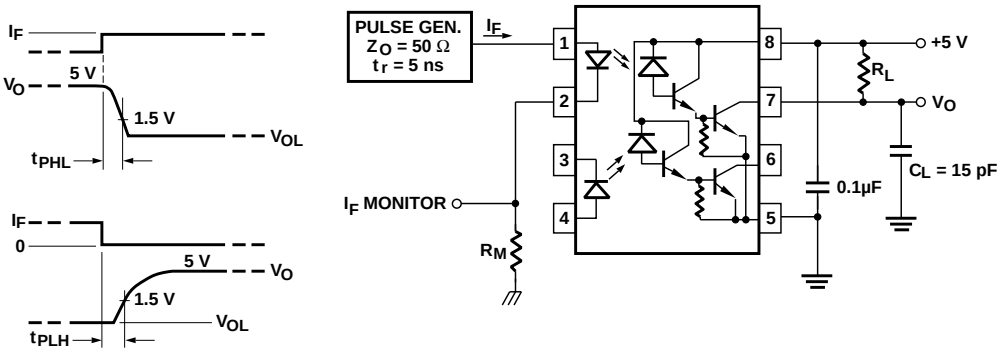


Figure 9. Switching Test Circuit.

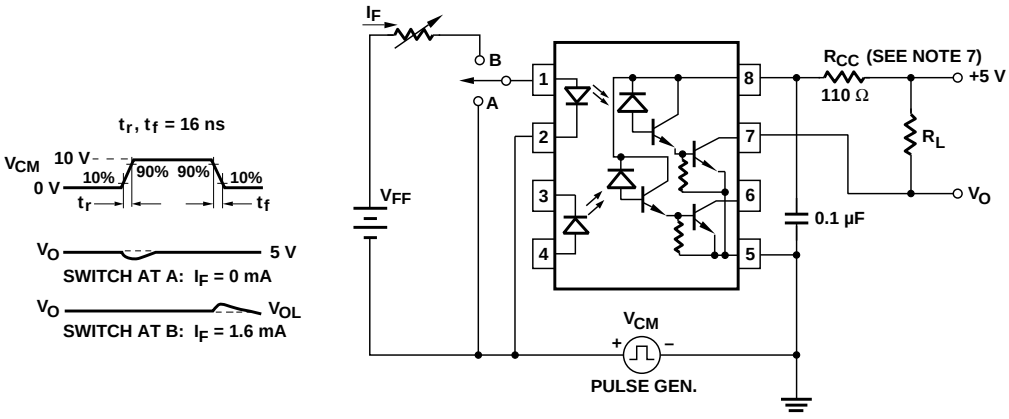


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.