



# HCPL0600, HCPL0601, HCPL0611, HCPL0630, HCPL0631, HCPL0661 High Speed-10 MBit/s Logic Gate Optocouplers

Single Channel: HCPL0600, HCPL0601, HCPL0611  
Dual Channel: HCPL0630, HCPL0631, HCPL0661

## Features

- Compact SO8 package
- Very high speed-10 MBit/s
- Superior CMR
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output (single channel devices)
- Wired OR-open collector
- U.L. recognized (File # E90700)
- VDE approval pending

## Applications

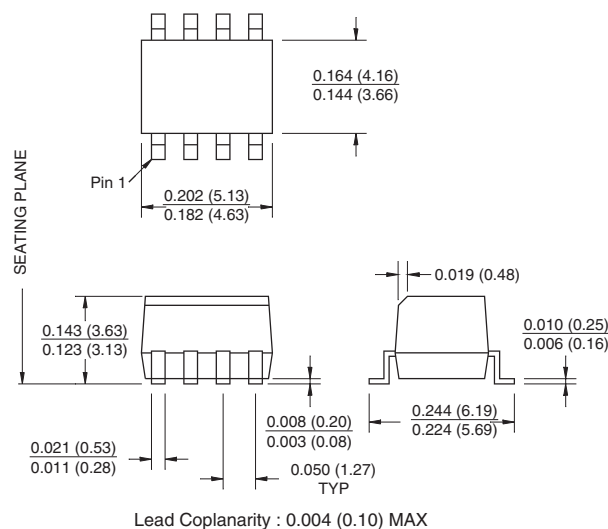
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing

- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

## Description

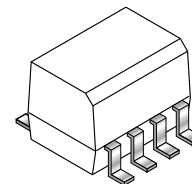
The HCPL06XX optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output (single channel devices). The devices are housed in a compact small-outline package. This output features an open collector, thereby permitting wired OR outputs. The HCPL0600 and HCPL0601 output consists of bipolar transistors on a bipolar process while the HCPL0611, HCPL0630 and HCPL0631 output consists of bipolar transistors on a CMOS process for reduced power consumption. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection.

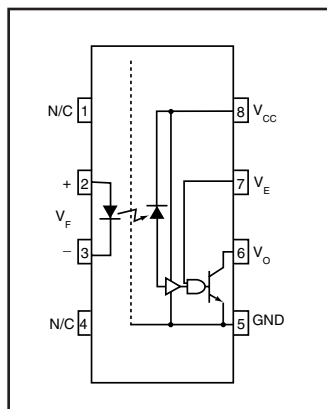
## Package Dimensions



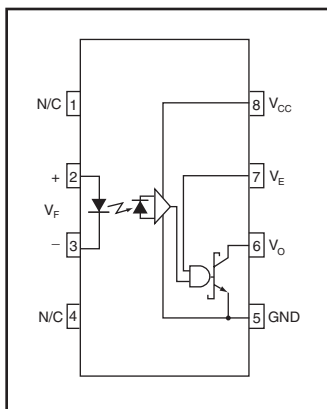
## NOTE

All dimensions are in inches (millimeters)

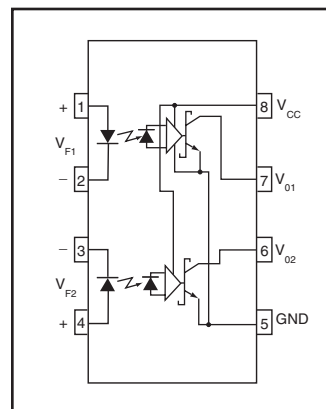




Single-channel circuit drawing (HCPL0600 and HCPL0601)



Single-channel circuit drawing (HCPL0611)



Dual-channel circuit drawing (HCPL0630, HCPL0631 and HCPL0661)

**TRUTH TABLE (Positive Logic)**

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H*	NC*	L*
L*	NC*	H*

\*Dual channel devices or single channel devices with pin 7 not connected.  
 A 0.1  $\mu$ F bypass capacitor must be connected between pins 8 and 5. (See note 1)

### Absolute Maximum Ratings (No derating required up to 85°C)

Parameter		Symbol	Value	Units	
Storage Temperature		$T_{STG}$	-40 to +125	°C	
Operating Temperature		$T_{OPR}$	-40 to +85	°C	
<b>EMITTER</b> DC/Average Forward Input Current (each channel)	Single Channel	$I_F$	50	mA	
	Dual Channel				
Enable Input Voltage Not to exceed VCC by more than 500 mV		Single Channel	$V_E$	5.5	V
Reverse Input Voltage (each channel)			$V_R$	5.0	V
Power Dissipation	Single Channel	$P_I$	45	mW	
	Dual Channel				
<b>DETECTOR</b> Supply Voltage			$V_{CC}$ (1 minute max)	7.0	V
Output Current (each channel)			$I_O$	50	mA
Output Voltage (each channel)			$V_O$	7.0	V
Collector Output Power Dissipation	Single Channel	$P_O$	85	mW	
	Dual Channel				

### Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Input Current, Low Level	$I_{FL}$	0	250	μA
Input Current, High Level	$I_{FH}$	*6.3	15	mA
Supply Voltage, Output	$V_{CC}$	4.5	5.5	V
Enable Voltage, Low Level	$V_{EL}$	0	0.8	V
Enable Voltage, High Level	$V_{EH}$	2.0	$V_{CC}$	V
Operating Temperature	$T_A$	-40	+85	°C
Fan Out (TTL load)	N		8	TTL Loads
Output Pull-up	$R_L$	330	4K	Ω

\*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less

**Electrical Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Unless otherwise specified.)

**Individual Component Characteristics**

Parameter	Test Conditions	Symbol	Min	Typ**	Max	Unit
<b>EMITTER</b> Input Forward Voltage	( $I_F = 10\text{ mA}$ )	$V_F$			1.8	V
	$T_A = 25^{\circ}\text{C}$				1.75	
Input Reverse Breakdown Voltage	( $I_R = 10\ \mu\text{A}$ )	$B_{VR}$	5.0			V
Input Capacitance	( $V_F = 0, f = 1\text{ MHz}$ )	$C_{IN}$				pF
Input Diode Temperature Coefficient	( $I_F = 10\text{ mA}$ )	$\Delta V_F/\Delta T_A$				mV/ $^{\circ}\text{C}$
<b>DETECTOR</b> High Level Supply Current	( $V_E = 0.5\text{ V}$ )	Single Channel			10	mA
	( $I_F = 0\text{ mA}, V_{CC} = 5.5\text{ V}$ )	Dual Channel			15	
Low Level Supply Current	( $V_E = 0.5\text{ V}$ )	Single Channel			13	mA
	( $I_F = 10\text{ mA}, V_{CC} = 5.5\text{ V}$ )	Dual Channel			21	
Low Level Enable Current	( $V_{CC} = 5.5\text{ V}, V_E = 0.5\text{ V}$ )	Single Channel			-1.6	mA
High Level Enable Current	( $V_{CC} = 5.5\text{ V}, V_E = 2.0\text{ V}$ )	Single Channel			-1.6	mA
High Level Enable Voltage	( $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$ )	Single Channel	$V_{EH}$	2.0		V
Low Level Enable Voltage	( $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$ )(Note 2)	Single Channel	$V_{EL}$		0.8	V

**Switching Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_F = 7.5\text{ mA}$  Unless otherwise specified.)

AC Characteristics	Test Conditions	Device	Symbol	Min	Typ	Max	Unit
Propagation Delay Time to Output High Level	(Note 3) ( $T_A = 25^{\circ}\text{C}$ )	All	$T_{PLH}$	20		75	ns
	( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ ) (Fig. 12)					100	
Propagation Delay Time to Output Low Level	(Note 4) ( $T_A = 25^{\circ}\text{C}$ )	All	$T_{PHL}$	25		75	ns
	( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ ) (Fig. 12)					100	
Pulse Width Distortion	( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ ) (Fig. 12)	All	$ T_{PHL} - T_{PLH} $			35	ns
Output Rise Time (10-90%)	( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ )(Note 5) (Fig. 12)	All	$t_r$		50		ns
Output Fall Time (90-10%)	( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ )(Note 6) (Fig. 12)	All	$t_f$		12		ns
Enable Propagation Delay Time to Output High Level	(I <sub>F</sub> = 7.5 mA, V <sub>EH</sub> = 3.5 V) ( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ ) (Note 7) (Fig. 13)	HCPL0600	$t_{ELH}$		20		ns
		HCPL0601					
		HCPL0611					
Enable Propagation Delay Time to Output Low Level	(I <sub>F</sub> = 7.5 mA, V <sub>EH</sub> = 3.5 V) ( $R_L = 350\ \Omega, C_L = 15\text{ pF}$ ) (Note 8) (Fig. 13)	HCPL0600	$t_{EHL}$		20		ns
		HCPL0601					
		HCPL0611					
Common Mode Transient Immunity (at Output High Level)	(R <sub>L</sub> = 350 $\Omega$ ) ( $T_A = 25^{\circ}\text{C}$ ) (I <sub>F</sub> = 0 mA, V <sub>OH</sub> (Min.) = 2.0 V) (Note 9)(Fig. 14)	HCPL0600	$ V_{CMH} $				V/ $\mu\text{s}$
		HCPL0601		5000			
		HCPL0611		25,000			
Common Mode Transient Immunity (at Output Low Level)	(R <sub>L</sub> = 350 $\Omega$ ) ( $T_A = 25^{\circ}\text{C}$ ) (I <sub>F</sub> = 7.5 mA, V <sub>OL</sub> (Max.) = 0.8 V) (Note 10)(Fig. 14)	HCPL0600	$ V_{CMH} $				V/ $\mu\text{s}$
		HCPL0601		5000			
		HCPL0611		25,000			

**Transfer Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
High Level Output Current	( $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$ ) ( $I_F = 250\ \mu\text{A}$ , $V_E = 2.0\text{ V}$ ) (Note 2)	$I_{OH}$			100	$\mu\text{A}$
Low Level Output Voltage	( $V_{CC} = 5.5\text{ V}$ , $I_F = 5\text{ mA}$ ) ( $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$ ) (Note 2)	$V_{OL}$			0.6	V
Input Threshold Current	( $V_{CC} = 5.5\text{ V}$ , $V_O = 0.6\text{ V}$ , $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$ )	$I_{FT}$			5	mA

**Isolation Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  Unless otherwise specified.)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-Output Insulation Leakage Current	(Relative humidity = 45%) ( $T_A = 25^\circ\text{C}$ , $t = 5\text{ s}$ ) ( $V_{I-O} = 3000\text{ VDC}$ ) (Note 11)	$I_{I-O}$			1.0*	$\mu\text{A}$
Withstand Insulation Test Voltage	( $R_H < 50\%$ , $T_A = 25^\circ\text{C}$ ) (Note 11) ( $t = 1\text{ min.}$ )	$V_{ISO}$	2500			$V_{RMS}$
Resistance (Input to Output)	( $V_{I-O} = 500\text{ V}$ ) (Note 11)	$R_{I-O}$		$10^{12}$		$\Omega$
Capacitance (Input to Output)	( $f = 1\text{ MHz}$ ) (Note 11)	$C_{I-O}$		0.6		pF

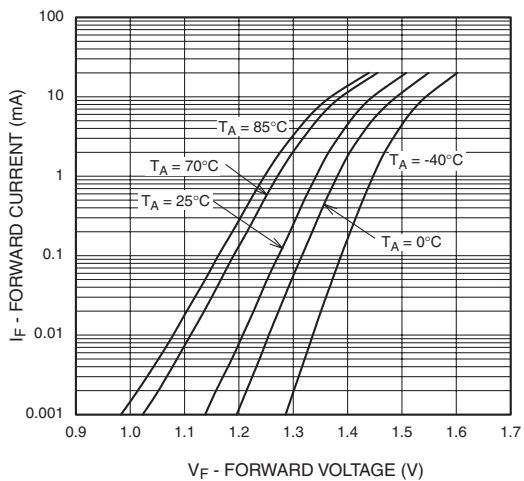
\*\* All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**NOTES**

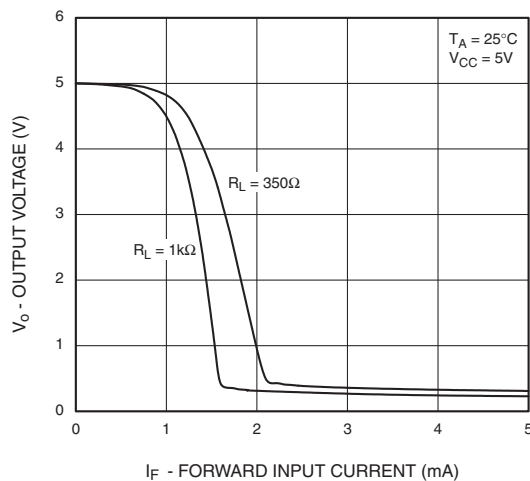
1. The  $V_{CC}$  supply to each optoisolator must be bypassed by a  $0.1\ \mu\text{F}$  capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package  $V_{CC}$  and GND pins of each device.
2. Enable Input - No pull up resistor required as the device has an internal pull up resistor.
3.  $t_{PLH}$  - Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4.  $t_{PHL}$  - Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
5.  $t_r$  - Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
6.  $t_f$  - Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
7.  $t_{ELH}$  - Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
8.  $t_{EHL}$  - Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
9.  $CM_H$  - The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e.,  $V_{OUT} > 2.0\text{ V}$ ). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
10.  $CM_L$  - The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e.,  $V_{OUT} < 0.8\text{ V}$ ). Measured in volts per microsecond (V/ $\mu\text{s}$ ).
11. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.

## Typical Performance Curves (HCPL0600 and HCPL0601 only)

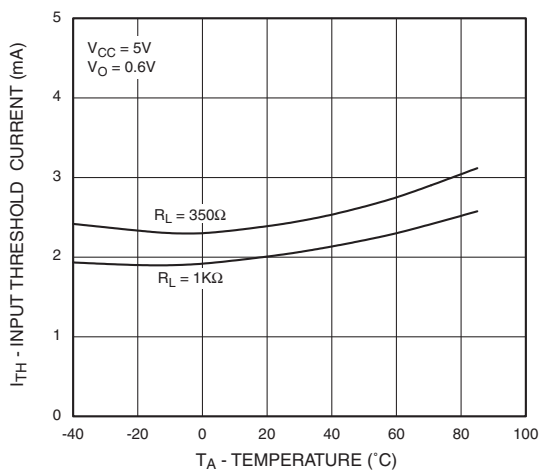
**Fig. 1 Forward Current vs. Input Forward Voltage**



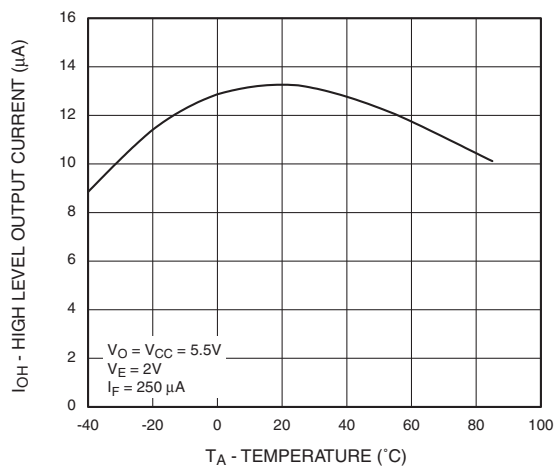
**Fig. 2 Output Voltage vs. Forward Current**



**Fig. 3 Input Threshold Current vs. Temperature**

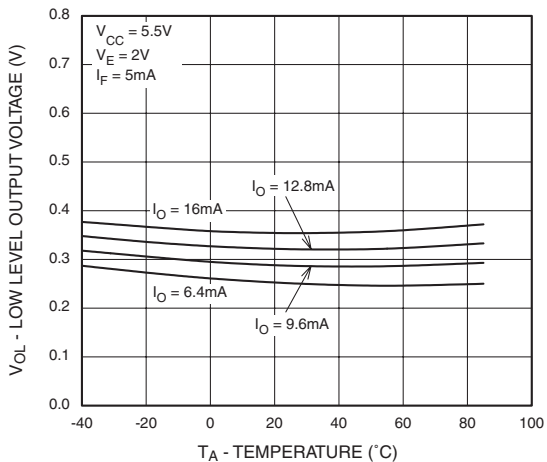


**Fig. 4 High Level Output Current vs. Temperature**

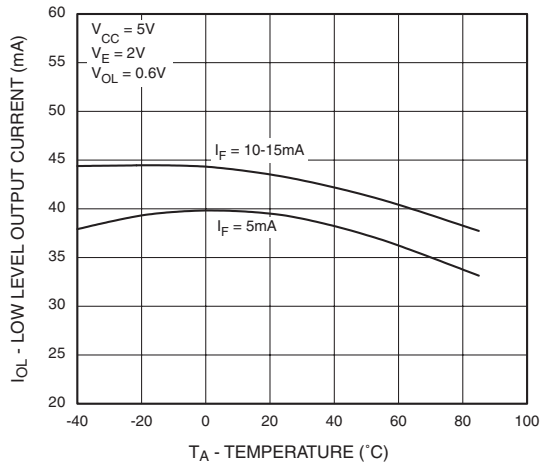


## Typical Performance Curves (HCPL0600 and HCPL0601 only)

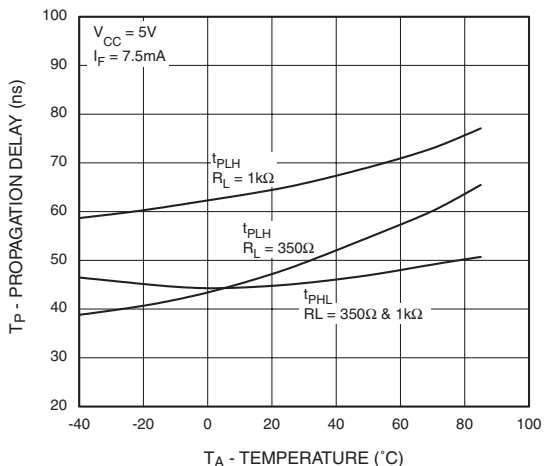
**Fig. 5 Low Level Output Voltage vs. Temperature**



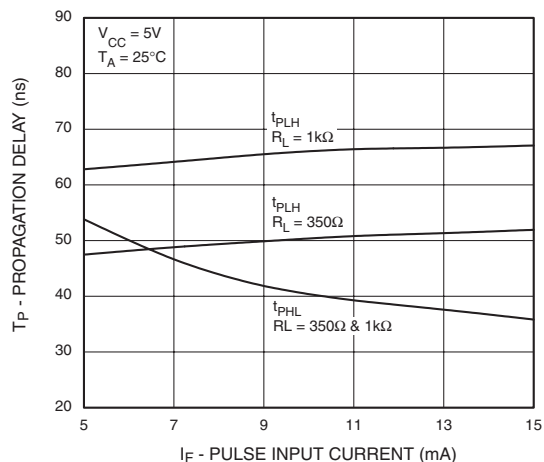
**Fig. 6 Low Level Output Current vs. Temperature**



**Fig. 7 Propagation Delay vs. Temperature**

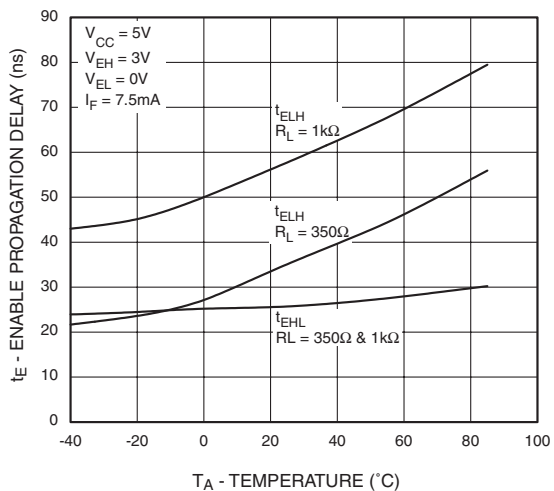


**Fig. 8 Propagation Delay vs. Pulse Input Current**

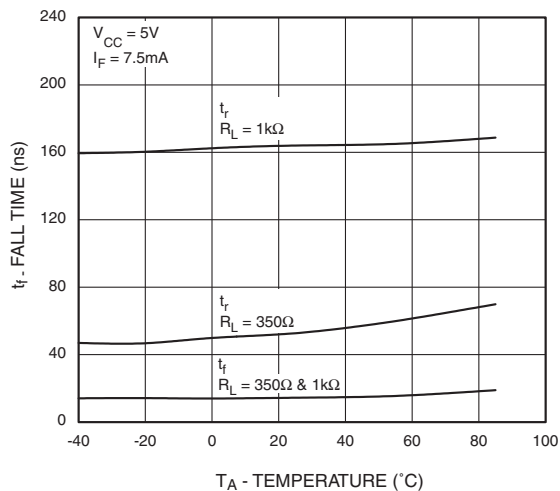


## Typical Performance Curves (HCPL0600 and HCPL0601 only)

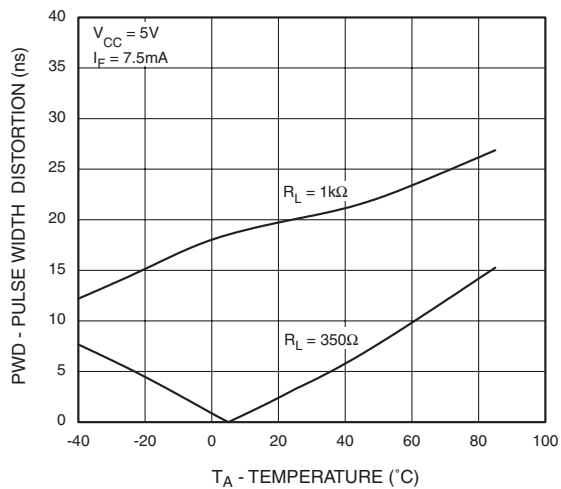
**Fig. 9 Typical Enable Propagation Delay vs. Temperature**



**Fig. 10 Typical Rise and Fall Time vs. Temperature**



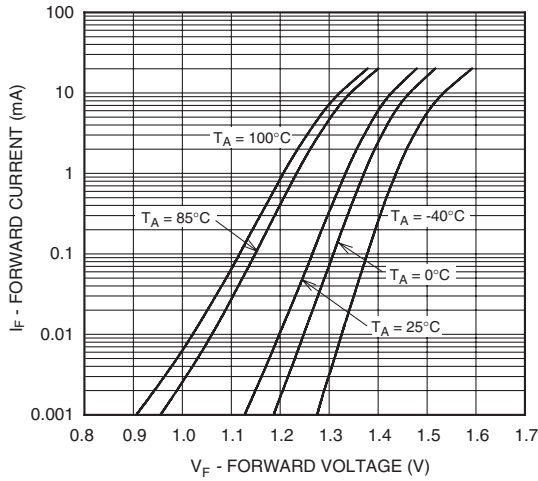
**Fig. 11 Typical Pulse Width Distortion vs. Temperature**



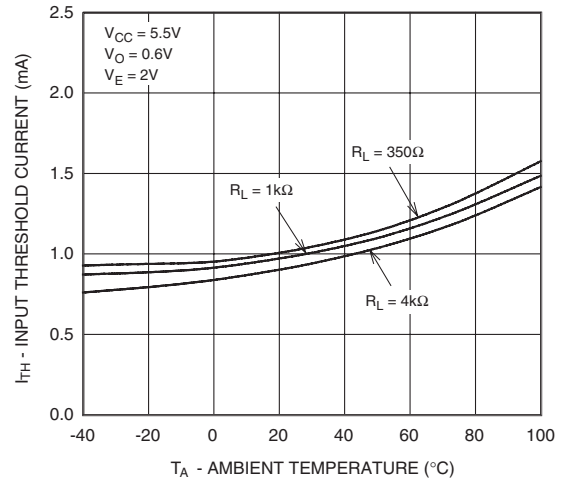


## Typical Performance Curves (HCPL0611, HCPL0630, HCPL0631 and HCPL0661 only)

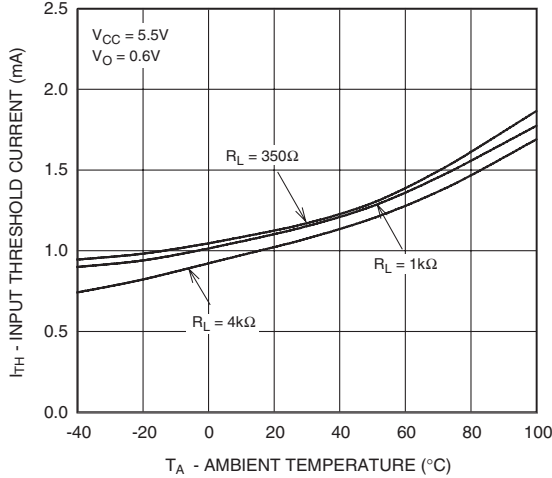
**Fig. 12 Input Forward Current vs. Forward Voltage**



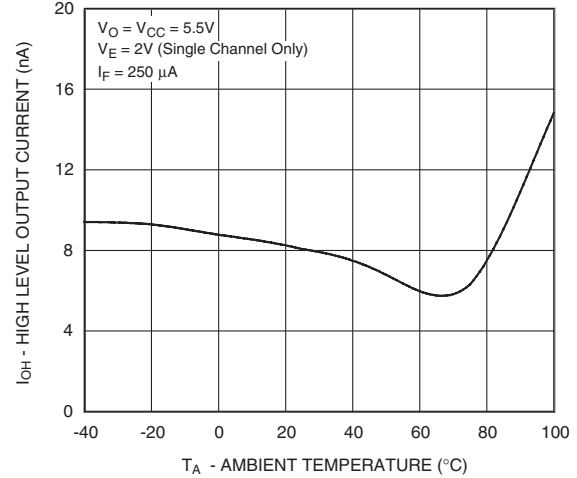
**Fig. 13 Input Threshold Current vs. Ambient Temperature (HCPL0611 only)**



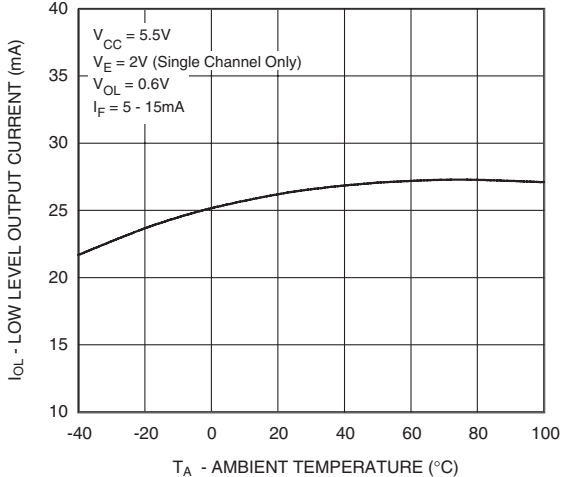
**Fig. 14 Input Threshold Current vs. Ambient Temperature (HCPL0630, HCPL0631 and HCPL0661 only)**



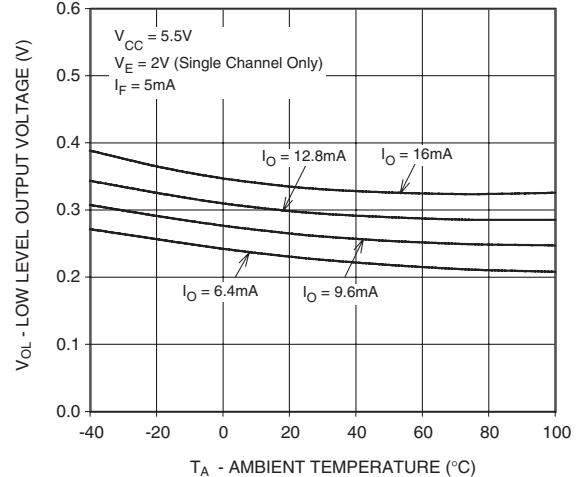
**Fig. 15 High Level Output Current vs. Ambient Temperature**



**Fig. 16 Low Level Output Current vs. Ambient Temperature**

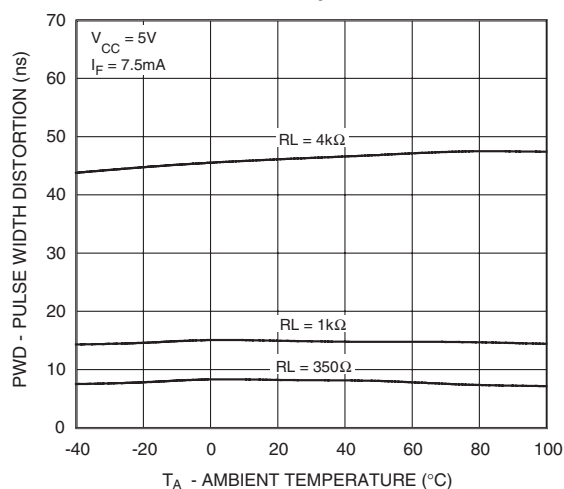


**Fig. 17 Low Level Output Voltage vs. Ambient Temperature**

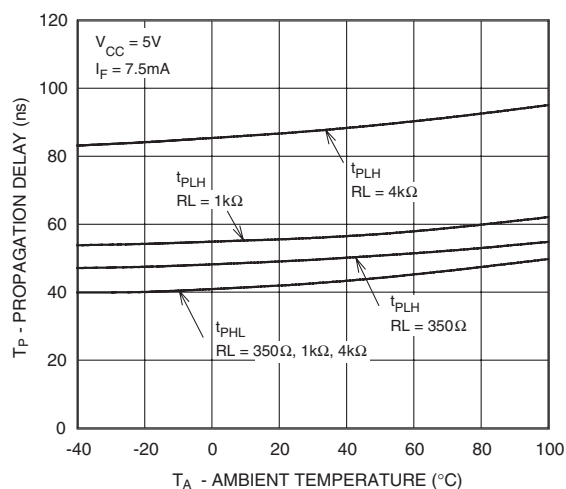


### Typical Performance Curves (HCPL0611, HCPL0630, HCPL0631 and HCPL0661 only)

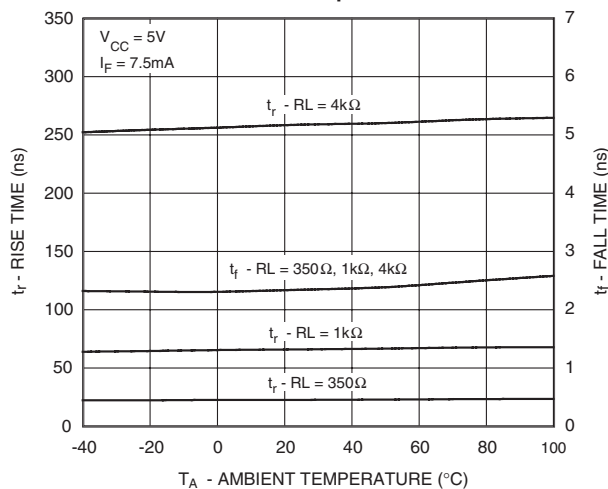
**Fig. 18 Pulse Width Distortion vs. Ambient Temperature**



**Fig. 19 Propagation Delay vs. Ambient Temperature**



**Fig. 20 Rise and Fall Times vs. Ambient Temperature**



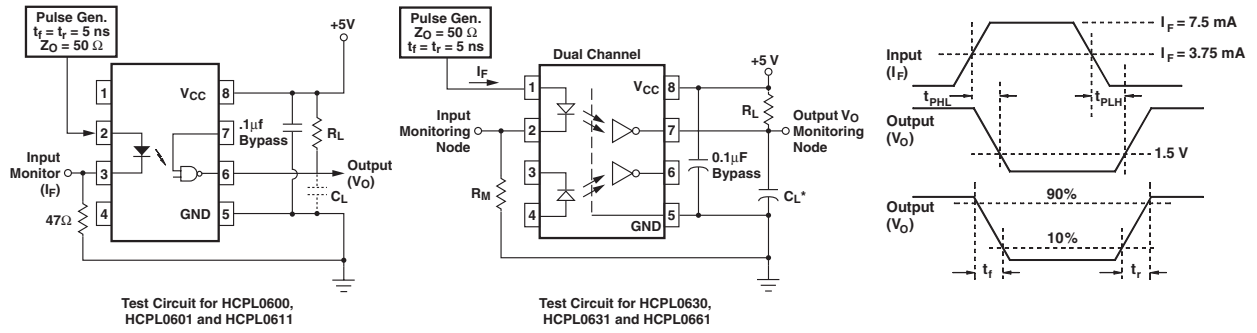


Fig. 21 Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$ .

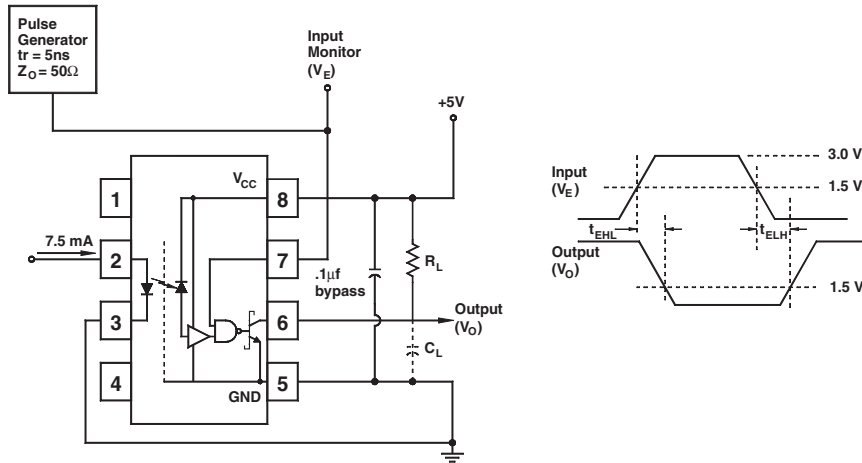
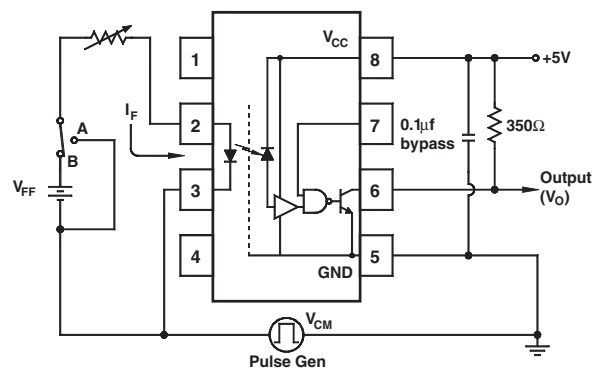


Fig. 22 Test Circuit  $t_{EHL}$  and  $t_{ELH}$ .



Test Circuit for HCPL0600, and HCPL0601

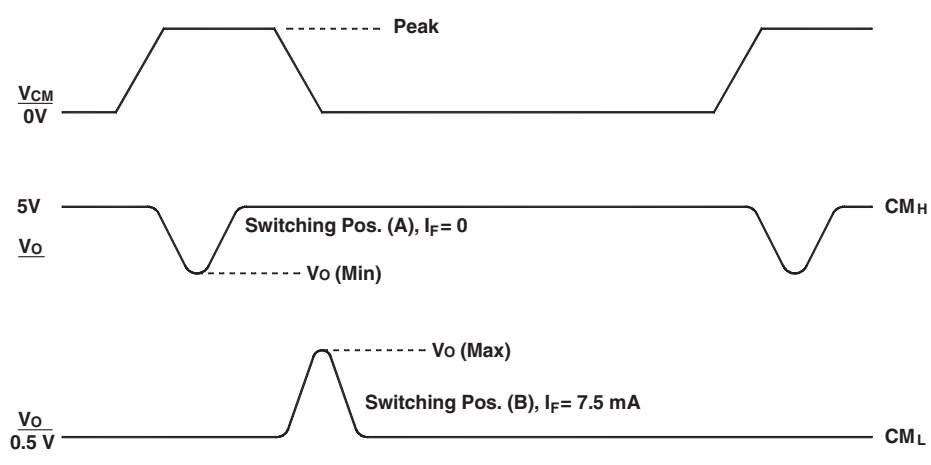
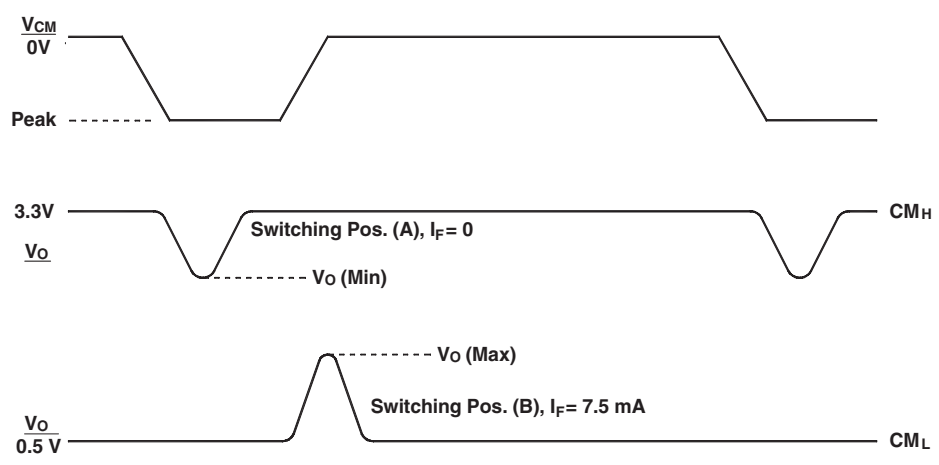
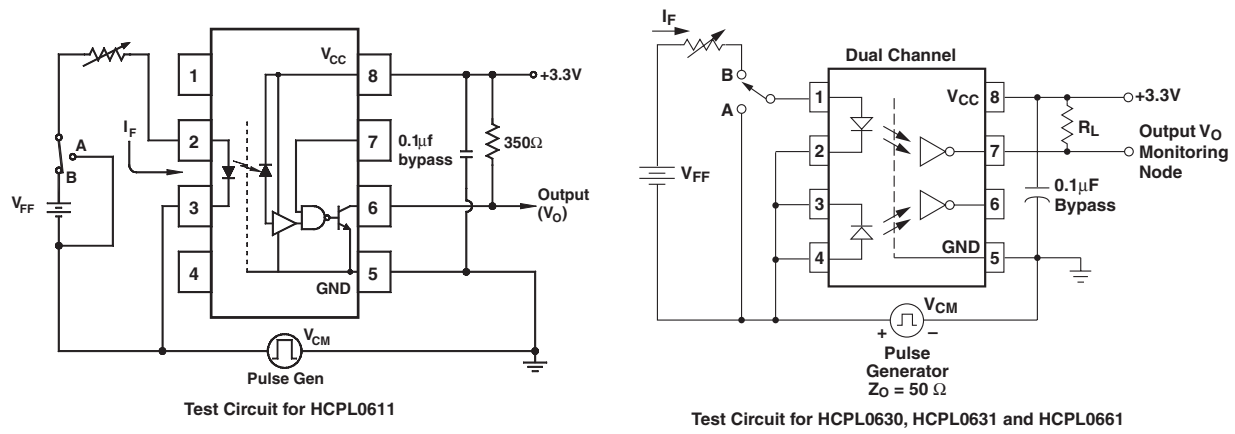
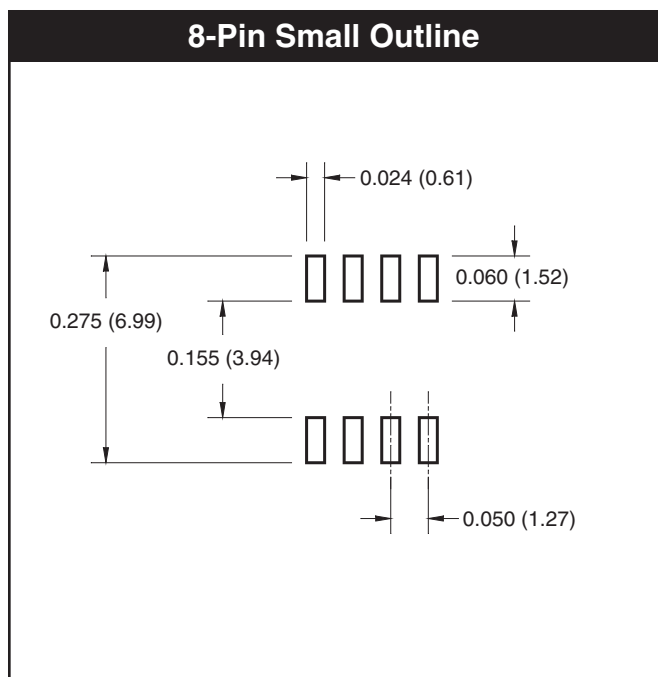


Fig. 23 Test Circuit Common Mode Transient Immunity (HCPL0600 and HCPL0601)



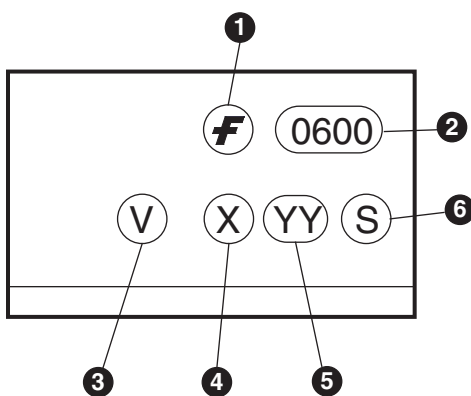
**Fig. 24 Test Circuit Common Mode Transient Immunity (HCPL0611, HCPL0630, HCPL0631 and HCPL0661)**



## Ordering Information

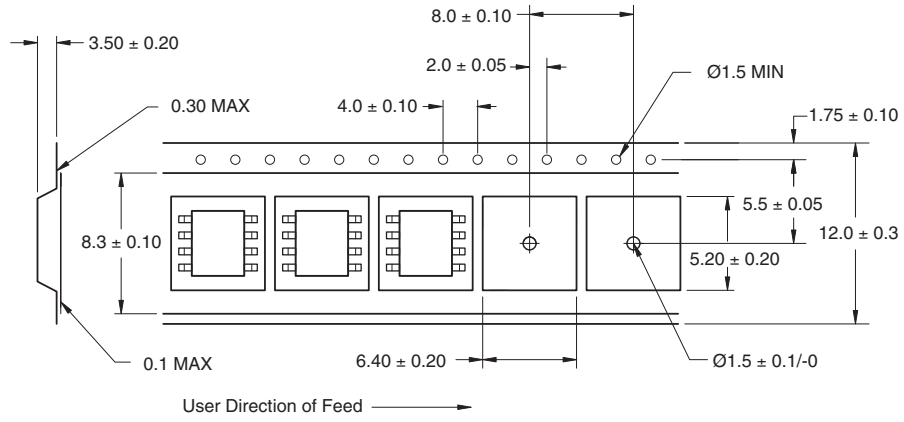
Option	Order Entry Identifier	Description
No Suffix	HCPL0600	Shipped in tubes (50 units per tube)
V	HCPL0600V	VDE0884 (pending approval)
R1	HCPL0600R1	Tape and Reel (500 units per reel)
R1V	HCPL0600R1V	VDE0884 (pending approval), Tape and Reel (500 units per reel)
R2	HCPL0600R2	Tape and Reel (2500 units per reel)
R2V	HCPL0600R2V	VDE0884 (pending approval), Tape and Reel (2500 units per reel)

## Marking Information

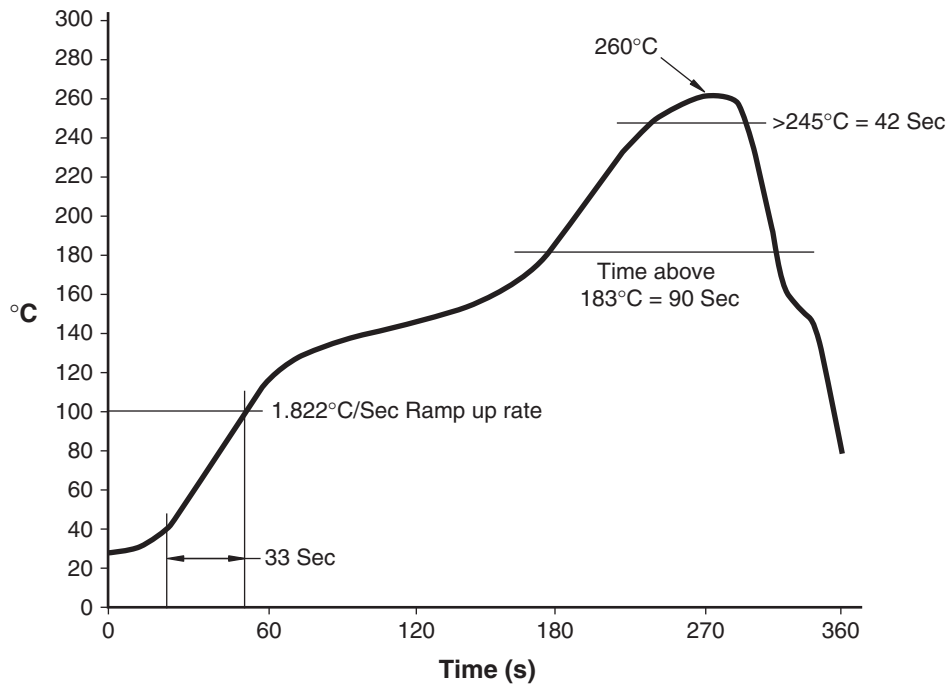


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

### Carrier Tape Specifications



### Reflow Profile





## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-8
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SyncFET™
Bottomless™	FPS™	MICROCOUPLER™	QFET®	TinyLogic®
Build it Now™	FRFET™	MicroFET™	QS™	TINYOPTO™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TruTranslation™
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	UHC™
DOME™	HiSeC™	MSX™	RapidConfigure™	UltraFET®
EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UniFET™
E <sup>2</sup> CMOS™	i-Lo™	OCX™	μSerDes™	VCX™
EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	Wire™
FACT™	IntelliMAX™	OPTOLOGIC®	SMART START™	
FACT Quiet Series™		OPTOPLANAR™	SPM™	
Across the board. Around the world.™		PACMAN™	Stealth™	
The Power Franchise®		POP™	SuperFET™	
Programmable Active Droop™		Power247™	SuperSOT™-3	
		PowerEdge™	SuperSOT™-6	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I16