



Single-Channel: 6N137M, HCPL2601M, HCPL2611M Dual-Channel: HCPL2630M, HCPL2631M High-Speed 10 MBit/s Logic Gate Optocouplers

Features

- Very High Speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Fan-out of 8 Over -40°C to +85°C
- Logic Gate Output
- Strobable Output
- Wired OR-open Collector
- U.L. Recognized (File # E90700, Vol. 2)

Applications

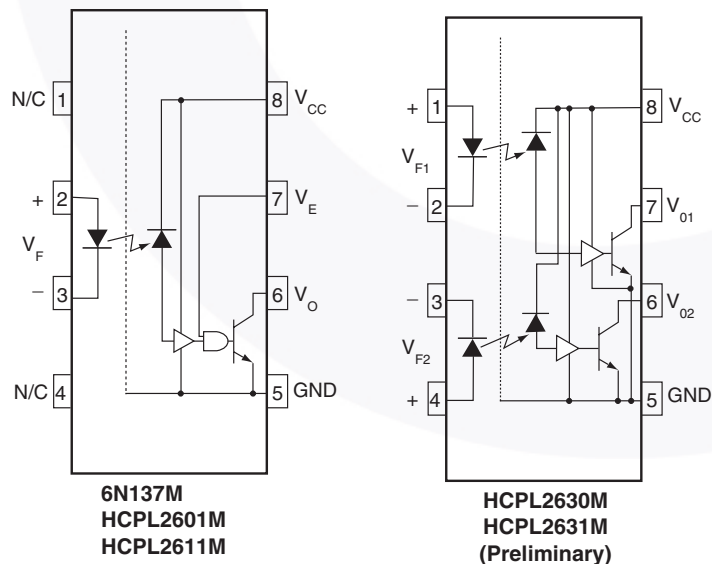
- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5 V CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer-peripheral Interface

Description

The 6N137M, HCPL2601M, HCPL2611M single-channel and HCPL2630M, HCPL2631M dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The switching parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The HCPL2601M and HCPL2631M has a minimum CMR of 5 kV/μs. The HCPL2611M has a minimum CMR of 10 kV/μs.

Schematics



A 0.1μF bypass capacitor must be connected between pins 8 and 5⁽¹⁾.

Figure 1. Schematics

Package Outlines

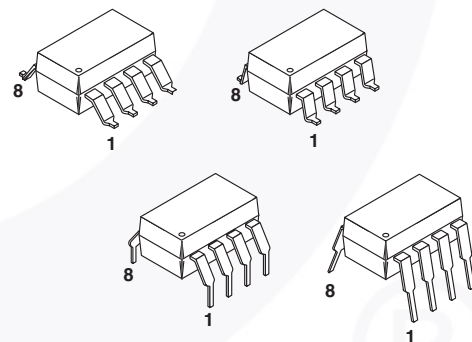


Figure 2. Package Options

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Safety and Insulation Ratings for 8-Pin DIP White

As per DIN_EN/IEC 60747-5-2. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 V _{RMS}		I-IV		
	For Rated Mains Voltage < 300 V _{RMS}		I-IV		
	For Rated Mains Voltage < 450 V _{RMS}		I-III		
	For Rated Mains Voltage < 600 V _{RMS}		I-III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V _{PR}	Input to Output Test Voltage, Method b, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	1,669			
	Input to Output Test Voltage, Method a, V _{IORM} × 1.5 = V _{PR} , Type and Sample Test with t _m = 60 s, Partial Discharge < 5 pC	1,335			
V _{IORM}	Max Working Insulation Voltage	890			V _{PEAK}
V _{IOTM}	Highest Allowable Over Voltage	6,000			V _{PEAK}
	External Creepage	8.0			mm
	External Clearance	7.4			mm
	External Clearance (for Option T, 0.4" Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values, Maximum Values Allowed in the Event of a Failure				
T _S	Case Temperature	150			°C
I _{S,INPUT}	Input Current	200			mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7%)	300			mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V	10 ⁹			Ω

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter		Value	Units
T_{STG}	Storage Temperature		-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature		-40 to +100	$^\circ\text{C}$
T_{SOL}	Lead Solder Temperature		260 for 10 s	$^\circ\text{C}$
Emitter				
I_F	DC/Average Forward	Single Channel	50	mA
	Input Current	Dual Channel (Each Channel)	30	
V_E	Enable Input Voltage Not to Exceed V_{CC} by more than 500 mV	Single Channel	5.5	V
V_R	Reverse Input Voltage	Each Channel	5.0	V
P_I	Power Dissipation	Single Channel	100	mW
		Dual Channel (Each Channel)	45	
Detector				
V_{CC} (1 minute max)	Supply Voltage		7.0	V
I_O	Output Current	Single Channel	50	mA
		Dual Channel (Each Channel)	50	
V_O	Output Voltage	Each Channel	7.0	V
P_O	Collector Output	Single Channel	85	mW
	Power Dissipation	Dual Channel (Each Channel)	60	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	4.5	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Ambient Operating Temperature	-40	+85	$^\circ\text{C}$
N	Fan Out (TTL load)		8	

*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit	
EMITTER							
V_F	Input Forward Voltage	$I_F = 10\text{ mA}$ $T_A = 25^\circ\text{C}$			1.8	V	
				1.4	1.75		
B_{VR}	Input Reverse Breakdown Voltage	$I_R = 10\ \mu\text{A}$	5.0			V	
C_{IN}	Input Capacitance	$V_F = 0, f = 1\text{ MHz}$		60		pF	
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	$I_F = 10\text{ mA}$		-1.4		mV/ $^\circ\text{C}$	
DETECTOR							
I_{CCH}	High Level Supply Current	$V_{CC} = 5.5\text{ V}, I_F = 0\text{ mA}, V_E = 0.5\text{ V}$	Single Channel		6	10	mA
			Dual Channel		10	15	
I_{CCL}	Low Level Supply Current		Single Channel	$V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$	8	13	mA
			Dual Channel				
I_{EL}	Low Level Enable Current	$V_{CC} = 5.5\text{ V}, V_E = 0.5\text{ V}$		-0.7	-1.6	mA	
I_{EH}	High Level Enable Current	$V_{CC} = 5.5\text{ V}, V_E = 2.0\text{ V}$		-0.5	-1.6	mA	
V_{EH}	High Level Enable Voltage	$V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}$	2.0			V	
V_{EL}	Low Level Enable Voltage	$V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}^{(3)}$			0.8	V	

Switching Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $I_F = 7.5\text{ mA}$ unless otherwise specified)

Symbol	AC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit	
T_{PLH}	Propagation Delay Time to Output HIGH Level	$R_L = 350\ \Omega, C_L = 15\text{ pF}^{(4)}$ (Fig. 14) $T_A = 25^\circ\text{C}$		20	40	75	ns
						100	
T_{PHL}	Propagation Delay Time to Output LOW Level	$T_A = 25^\circ\text{C}^{(5)}$ $R_L = 350\ \Omega, C_L = 15\text{ pF}$ (Fig. 14)		25	40	75	ns
						100	
$ T_{PHL} - T_{PLH} $	Pulse Width Distortion	$R_L = 350\ \Omega, C_L = 15\text{ pF}$ (Fig. 14)		1	35	ns	
t_r	Output Rise Time (10% to 90%)	$R_L = 350\ \Omega, C_L = 15\text{ pF}^{(6)}$ (Fig. 14)		30		ns	
t_f	Output Rise Time (90% to 10%)	$R_L = 350\ \Omega, C_L = 15\text{ pF}^{(7)}$ (Fig. 14)		10		ns	
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	$I_F = 7.5\text{ mA}, V_{EH} = 3.5\text{ V}, R_L = 350\ \Omega, C_L = 15\text{ pF}^{(8)}$ (Fig. 15)		15		ns	
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	$I_F = 7.5\text{ mA}, V_{EH} = 3.5\text{ V}, R_L = 350\ \Omega, C_L = 15\text{ pF}^{(9)}$ (Fig. 15)		15		ns	
$ ICM_H $	Common Mode Transient Immunity (at Output HIGH Level)	$T_A = 25^\circ\text{C}, IV_{CM} = 50\text{ V}$ (Peak), $I_F = 0\text{ mA}, V_{OH}$ (Min.) = $2.0\text{ V}, R_L = 350\ \Omega^{(10)}$ (Fig. 16)	6N137M, HCPL2630M		10,000		V/ μs
			HCPL2601M, HCPL2631M	5000	10,000		
$ ICM_L $	Common Mode Transient Immunity (at Output LOW Level)	$R_L = 350\ \Omega, I_F = 7.5\text{ mA}, V_{OL}$ (Max.) = $0.8\text{ V}, T_A = 25^\circ\text{C}^{(11)}$ (Fig. 16)	6N137M, HCPL2630M		10,000		V/ μs
			HCPL2601M, HCPL2631M	5000	10,000		
		$ IV_{CM} = 400\text{ V}$	HCPL2611M	10,000	15,000		

Electrical Characteristics (Continued)

Transfer Characteristics ($T_A = -40$ to $+85^\circ\text{C}$ unless otherwise specified)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{OH}	HIGH Level Output Current	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, $I_F = 250\ \mu\text{A}$, $V_E = 2.0\text{ V}^{(2)}$			100	μA
V_{OL}	LOW Level Output Current	$V_{CC} = 5.5\text{ V}$, $I_F = 5\text{ mA}$, $V_E = 2.0\text{ V}$, $I_{CL} = 13\text{ mA}^{(2)}$		0.4	0.6	V
I_{FT}	Input Threshold Current	$V_{CC} = 5.5\text{ V}$, $V_O = 0.6\text{ V}$, $V_E = 2.0\text{ V}$, $I_{OL} = 13\text{ mA}$		3	5	mA

Isolation Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^\circ\text{C}$, $t = 5\text{ s}$, $V_{I-O} = 3000\text{ VDC}^{(12)}$			1.0*	μA
V_{ISO}	Withstand Insulation Test Voltage	$RH < 50\%$, $T_A = 25^\circ\text{C}$, $I_{I-O} \leq 10\ \mu\text{A}$, $t = 1\text{ min.}^{(12)}$	5000			V_{RMS}
R_{I-O}	Resistance (Input to Output)	$V_{I-O} = 500\text{ V}^{(12)}$		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)	$f = 1\text{ MHz}^{(12)}$		1		pF

*All Typical at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

Notes:

- The V_{CC} supply to each optoisolator must be bypassed by a $0.1\ \mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
- Each channel.
- Enable Input – No pull up resistor required as the device has an internal pull up resistor.
- t_{PLH} – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- t_{PHL} – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- t_{ELH} – Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- t_{EHL} – Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OUT} > 2.0\text{ V}$). Measured in volts per microsecond (V/ μs).
- CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., $V_{OUT} < 0.8\text{ V}$). Measured in volts per microsecond (V/ μs).
- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

For Single-Channel Devices: 6N137M, HCPL2601M, and HCPL2611M

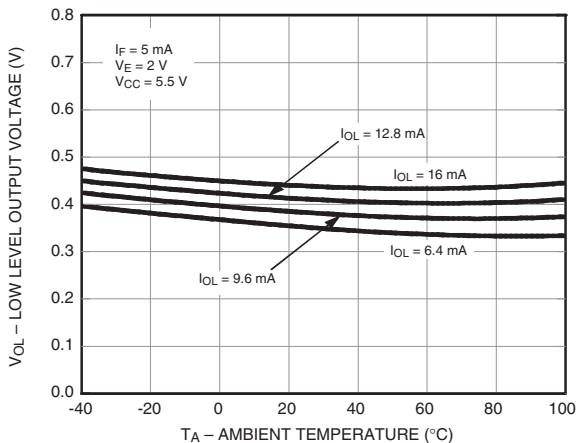


Figure 3. Low Level Output Voltage vs. Ambient Temperature

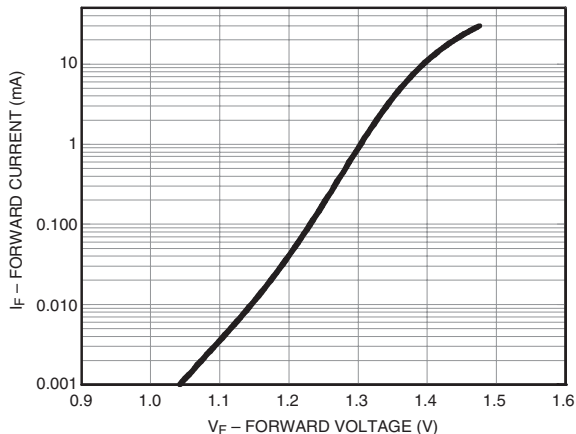


Figure 4. Input Diode Forward Voltage vs. Forward Current

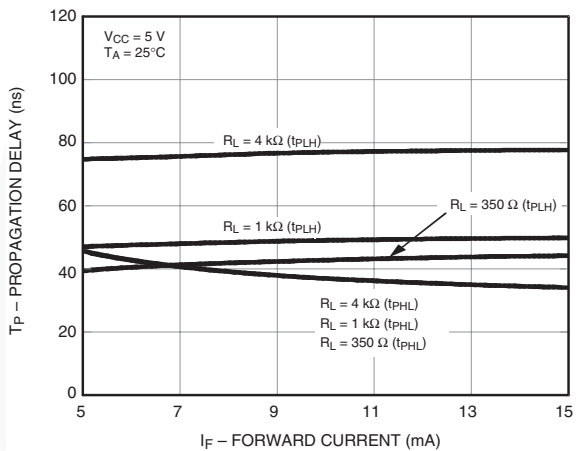


Figure 5. Switching Time vs. Forward Current

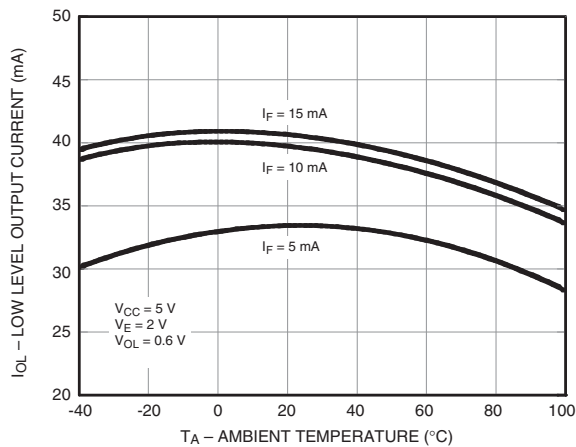


Figure 6. Low Level Output vs. Ambient Temperature

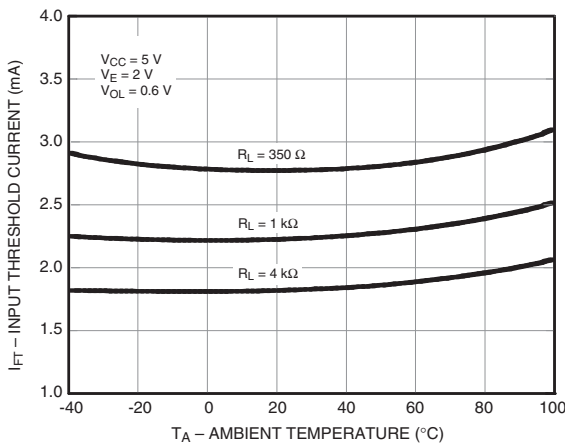


Figure 7. Input Threshold Current vs. Ambient Temperature

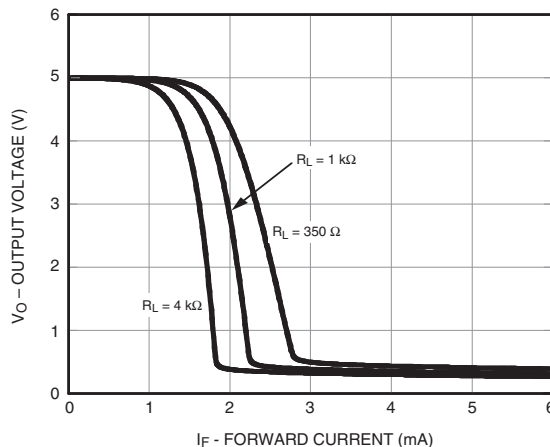


Figure 8. Output Voltage vs. Input Forward Current

Typical Performance Curves (Continued)

(For Single-Channel Devices: 6N137M, HCPL2601M, HCPL2611M)

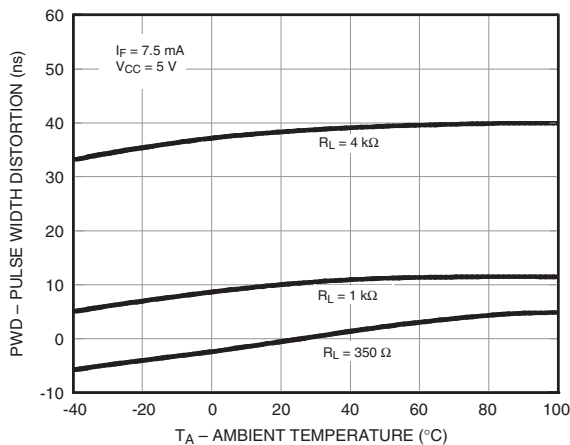


Figure 9. Pulse Width Distortion vs. Temperature

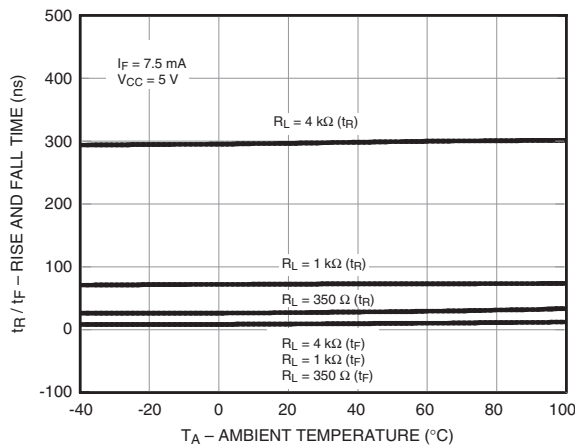


Figure 10. Rise and Fall Time vs. Temperature

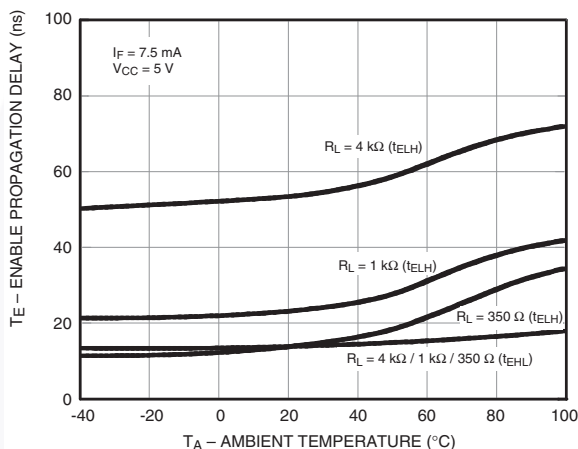


Figure 11. Enable Propagation Delay vs. Temperature

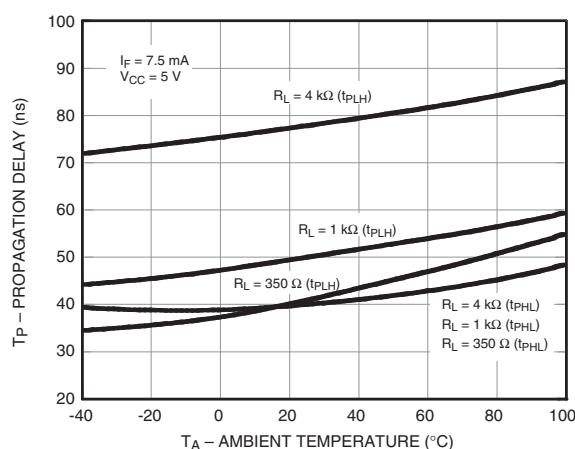


Figure 12. Switching Time vs. Temperature

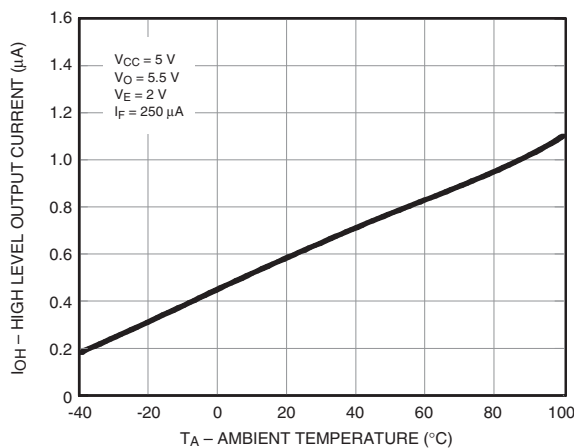


Figure 13. High Level Output Current vs. Temperature

Typical Performance Curves (Continued)

For Dual-Channel Devices: HCPL2630M and HCPL2631M

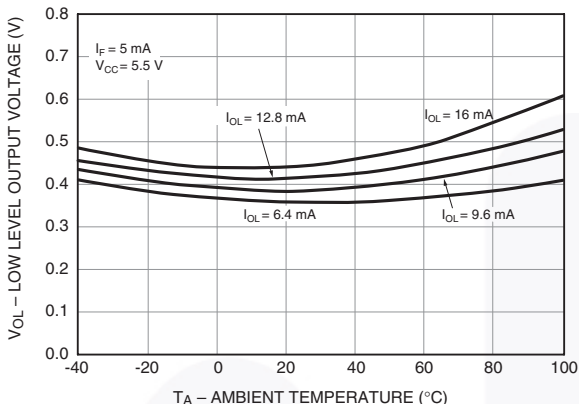


Figure 14. Low Level Output Voltage vs. Ambient Temperature

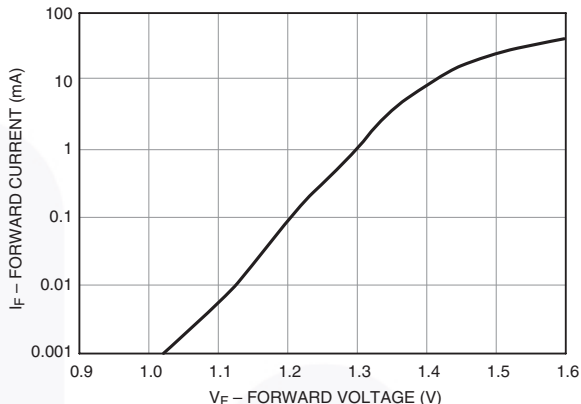


Figure 15. Input Diode Forward Voltage vs. Forward Current

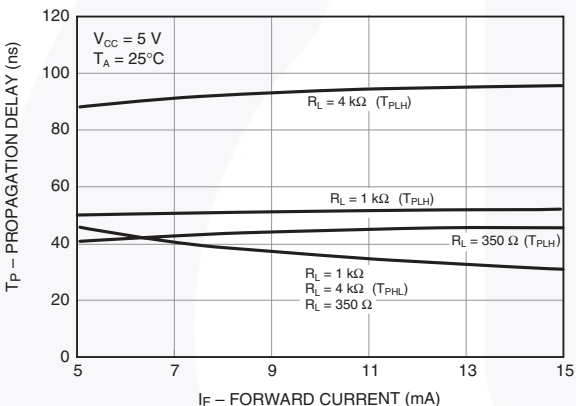


Figure 16. Switching Time vs. Forward Current

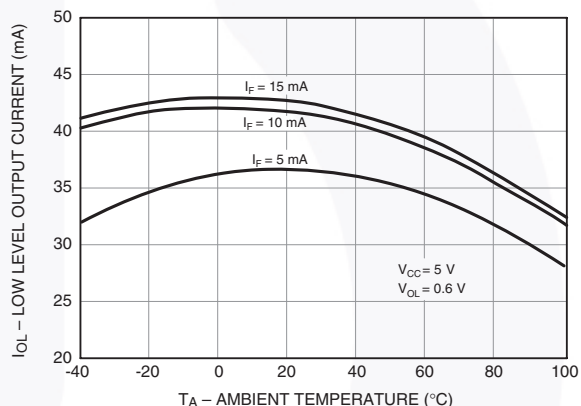


Figure 17. Low Level Output Current vs. Ambient Temperature

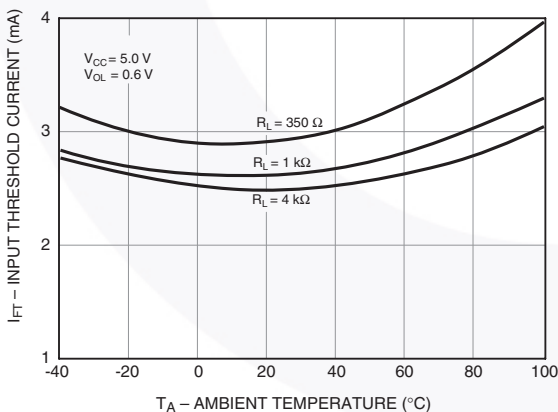


Figure 18. Input Threshold Current vs. Ambient Temperature

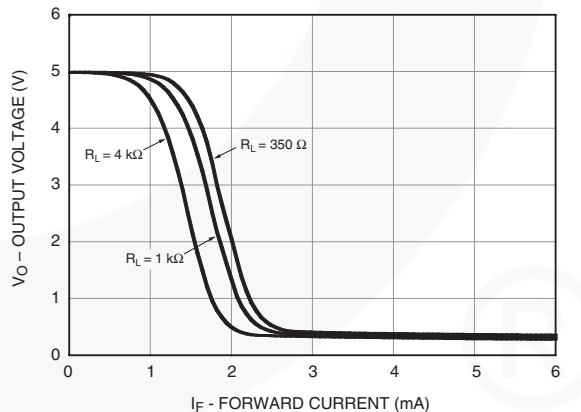


Figure 19. Output Voltage vs. Input Forward Current

Typical Performance Curves (Continued)

For Dual-Channel Devices: HCPL2630M and HCPL2631M

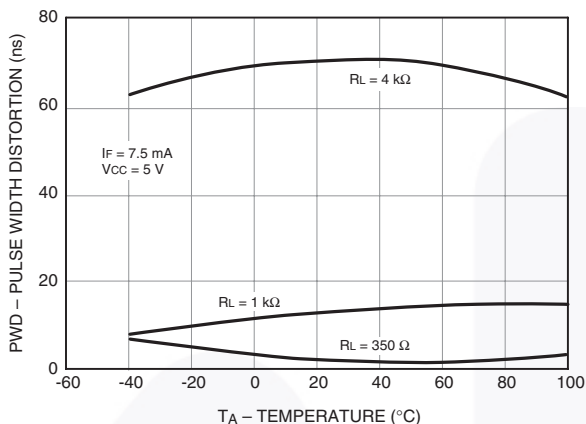


Figure 20. Pulse Width Distortion vs. Temperature

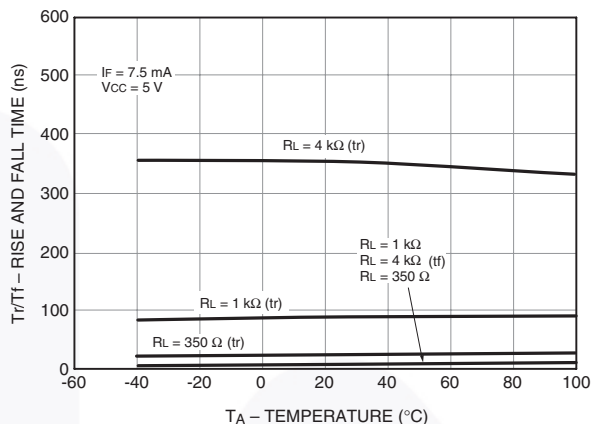


Figure 21. Rise and Fall Time vs. Temperature

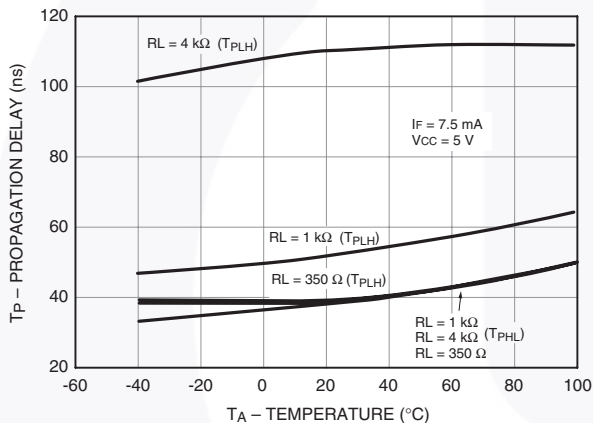


Figure 22. Switching Time vs. Temperature

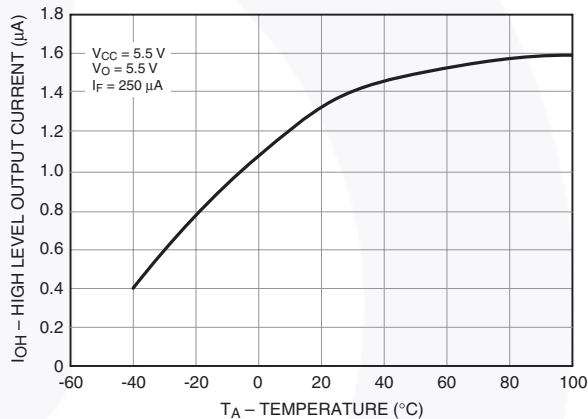


Figure 23. High Level Output Current vs. Temperature

Test Circuits

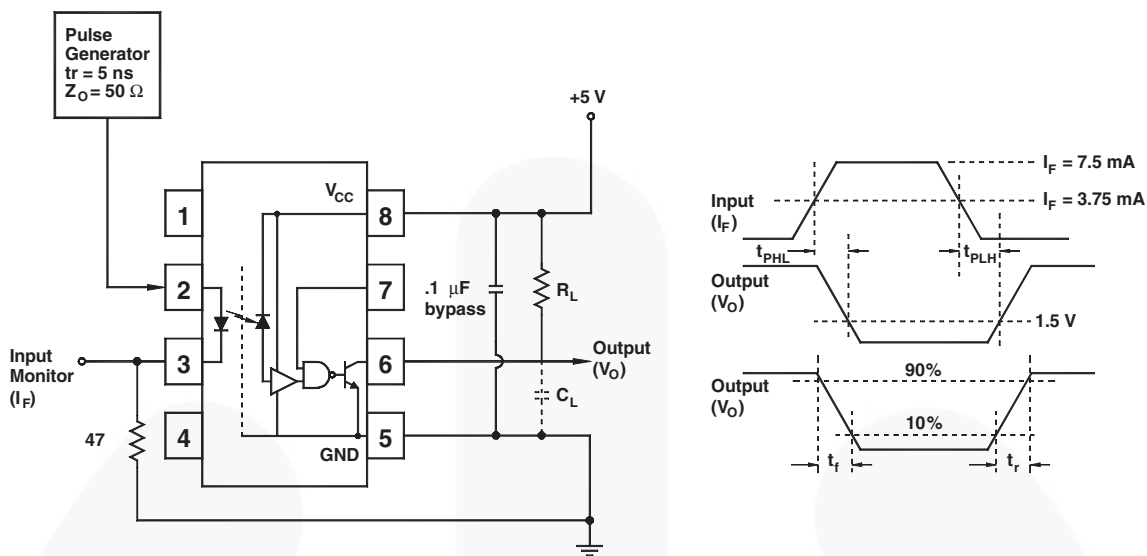


Figure 24. Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f

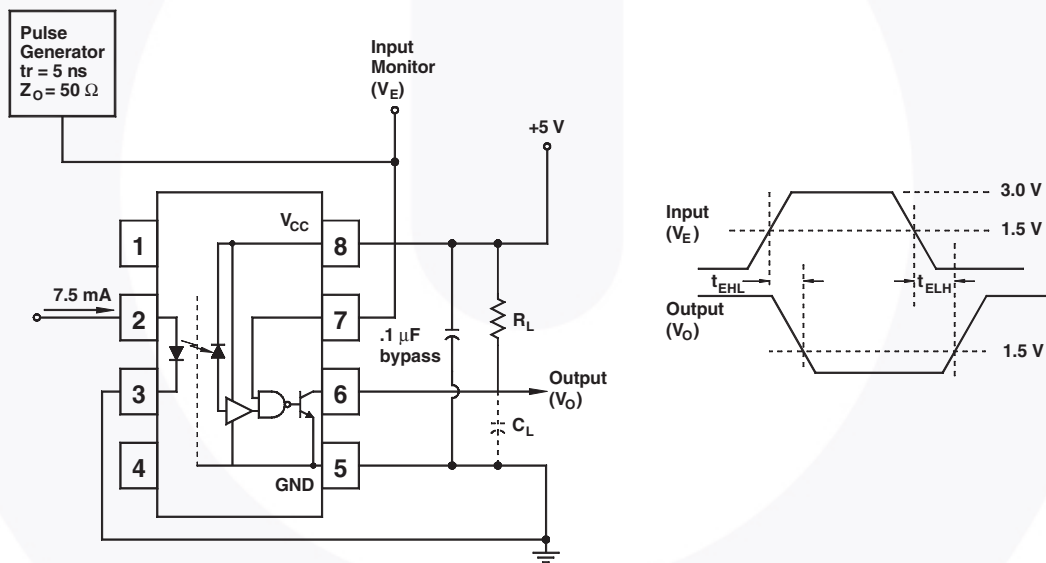


Figure 25. Test Circuit t_{EHL} and t_{ELH}

Test Circuits (Continued)

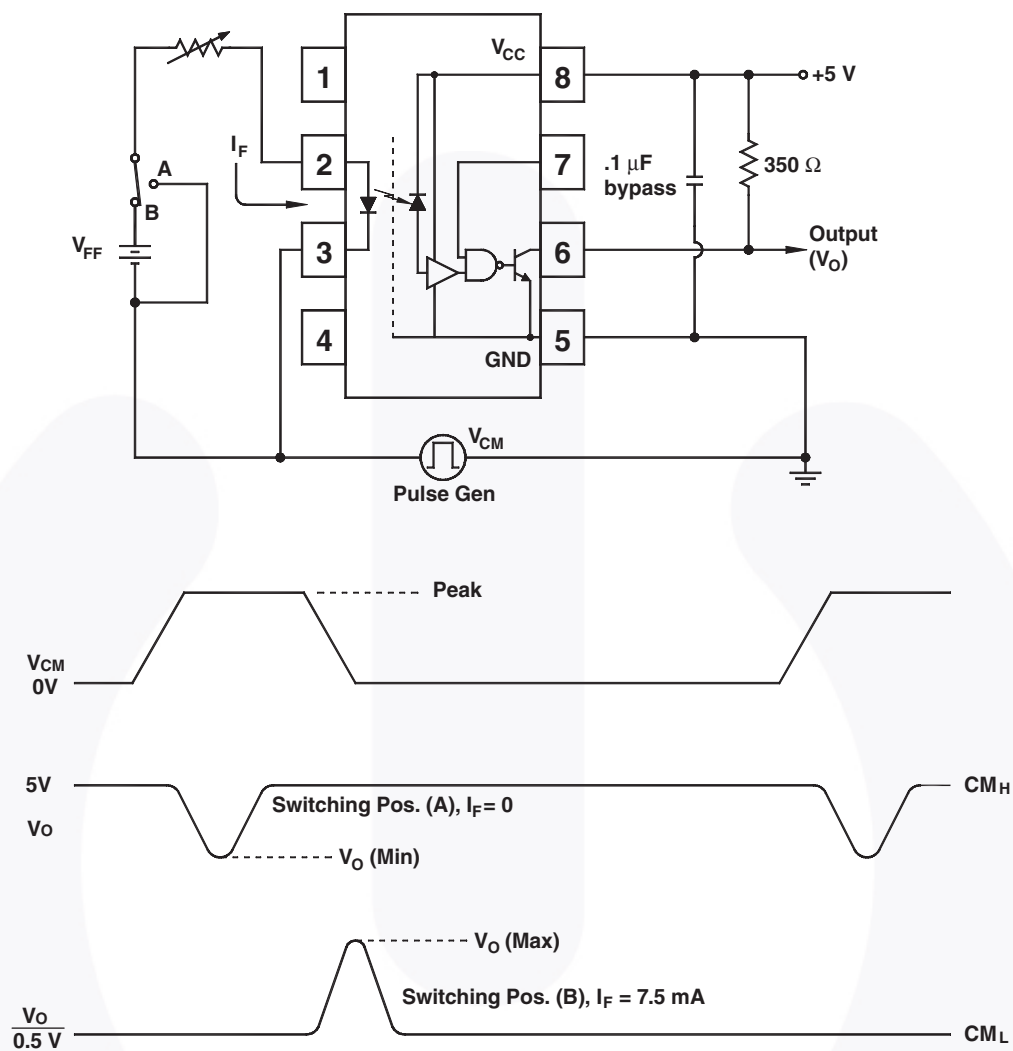
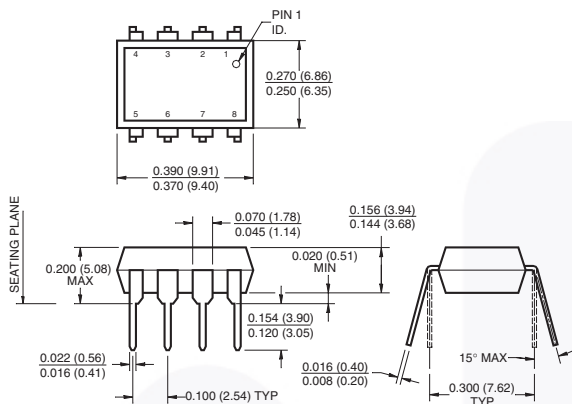


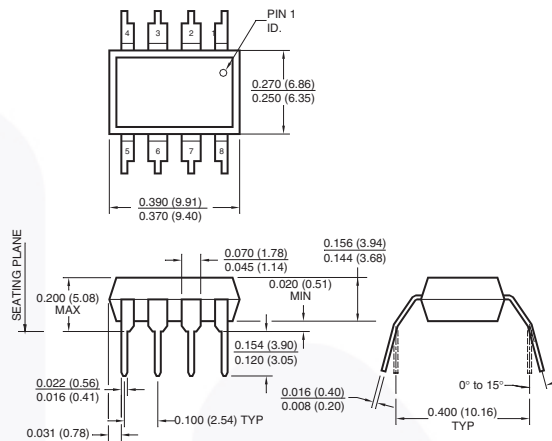
Figure 26. Test Circuit Common Mode Transient Immunity

Package Dimensions

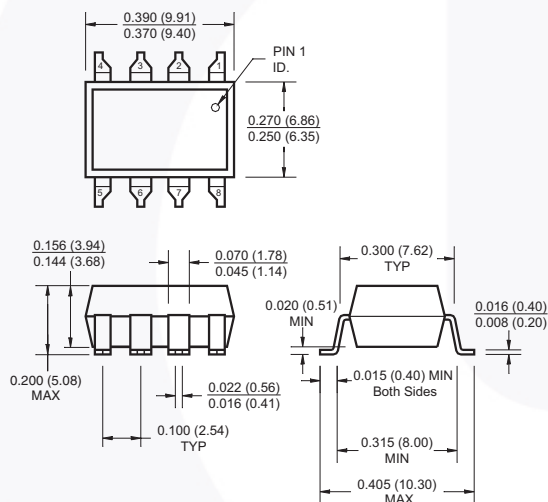
Through Hole



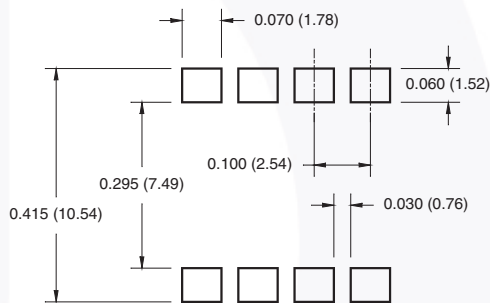
0.4" Lead Spacing (Option TV) (Pending)



Surface Mount – 0.3" Lead Spacing (Option S)



8-Pin Surface Mount DIP – Land Pattern (Option S)



Note:

All dimensions are in inches (millimeters)

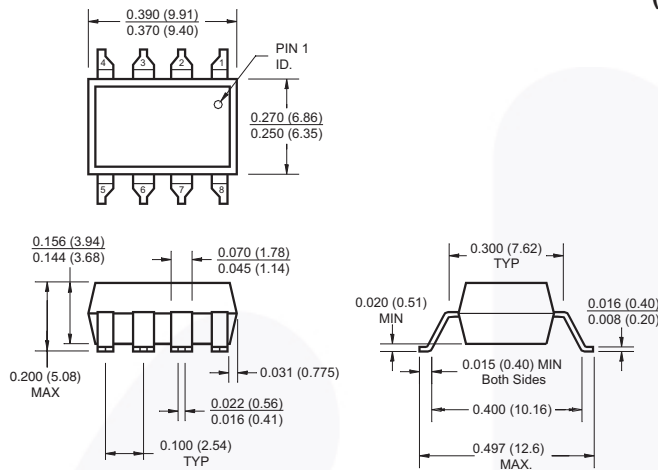
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

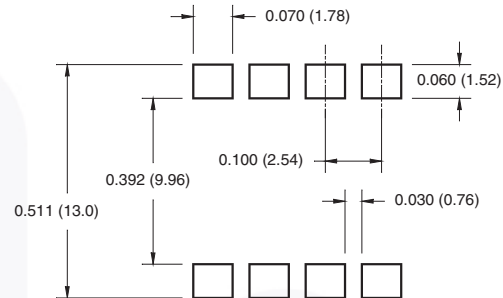
<http://www.fairchildsemi.com/packaging/>

Package Dimensions (Continued)

Surface Mount – 0.4" Lead Spacing (Option TS)



8-Pin Surface Mount DIP – Land Pattern (Option TS)



Note:

All dimensions are in inches (millimeters)

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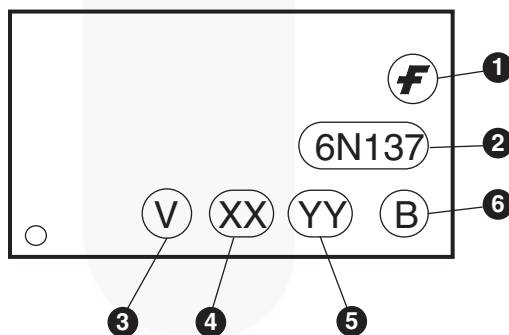
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Ordering Information

Option	Example Part Number	Description
No Suffix	6N137M	Standard Through Hole Device, 50 pcs per tube
S	6N137SM	Surface Mount Lead Bend
SD	6N137SDM	Surface Mount; Tape and Reel
V	6N137VM	DIN_EN/IEC60747-5-2 (VDE)
TV	6N137TVM	DIN_EN/IEC60747-5-2 (VDE), 0.4" lead spacing
SV	6N137SVM	DIN_EN/IEC60747-5-2 (VDE), surface mount
SDV	6N137SDVM	DIN_EN/IEC60747-5-2 (VDE), surface mount, tape and reel
TS	6N137TSM	Surface Mount, 0.4" lead spacing
TSV	6N137TSVM	Surface Mount, 0.4" lead spacing, IEC60747-5-2 approval pending (VDE)
TSR2	6N137TSR2M	Surface Mount, Tape and Reel, 0.4" lead spacing
TSR2V	6N137TSR2VM	Surface Mount, Tape and Reel, 0.4" lead spacing, IEC60747-5-2 approval pending (VDE)

Marking Information



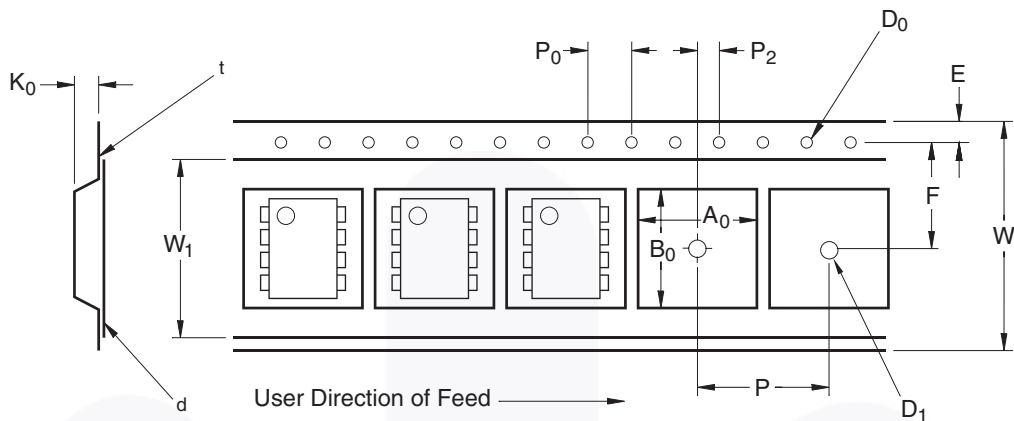
Definitions	
1	Fairchild logo
2	Device number
3	DIN_EN/IEC60747-5-2 (VDE) mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '13'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Note:

'HCPL' devices are marked only with the numerical characters (for example, HCPL2630 is marked as '2630').

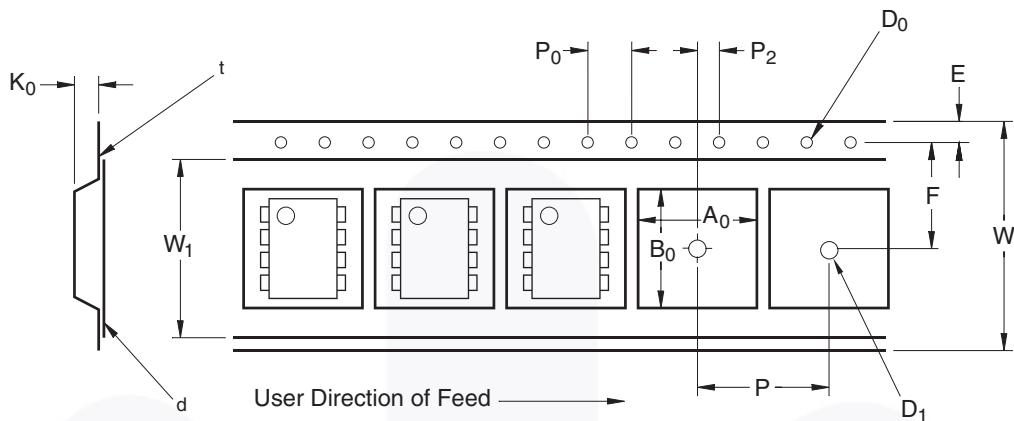
The 'M' suffix on the part number is an order identifier only. It is used to identify orders for the white package version. The 'M' does not appear on the device's top mark.

Carrier Tape Specifications (Option SD)



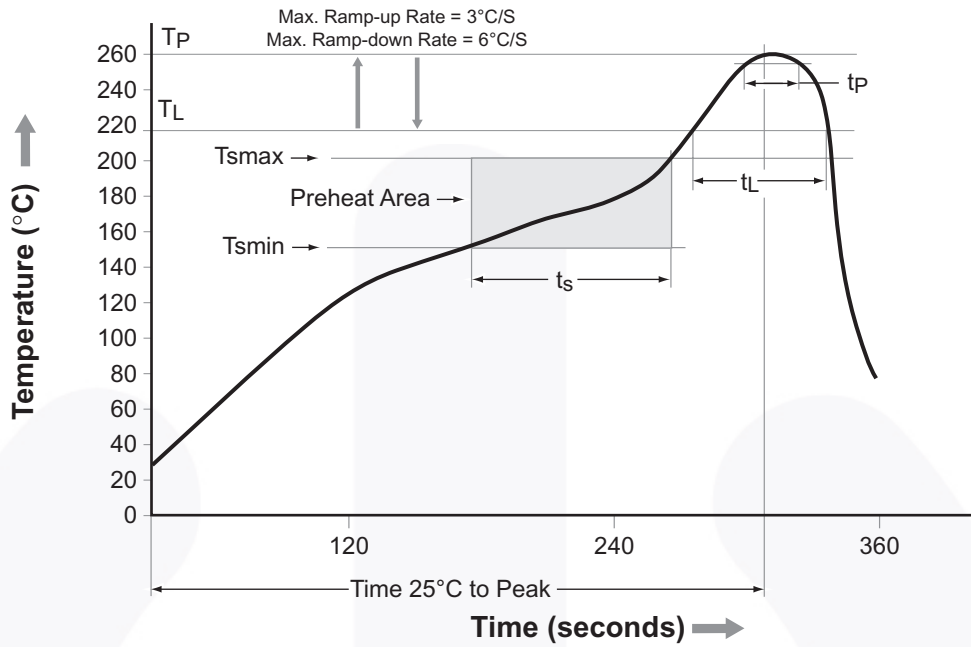
Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ± 0.20
B_0		10.30 ± 0.20
K_0		4.90 ± 0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 maximum
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Carrier Tape Specifications (Option TSR2)



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P ₀	Sprocket Hole Pitch	4.0 ± 0.1
D ₀	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P ₂		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A ₀	Pocket Dimensions	12.80 ± 0.1
B ₀		10.35 ± 0.1
K ₀		5.7 ± 0.1
W ₁	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile








Profile Feature	Pb-Free Assembly Profile
Temperature Minimum (T _{smin})	150°C
Temperature Maximum (T _{smax})	200°C
Time (t _s) from (T _{smin} to T _{smax})	60 to 120 seconds
Ramp-up Rate (t _L to t _p)	3°C/second maximum
Liquidous Temperature (T _L)	217°C
Time (t _L) Maintained Above (T _L)	60 to 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t _p) within 5°C of 260°C	30 seconds
Ramp-down Rate (T _P to T _L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum



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Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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