August 2019

SemiHow
Know-How for Semiconductor

HCS60R350S

600V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)}$ X Q_g)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

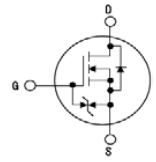
Key Parameters

Parameter	Value	Unit
BV_{DSS} @$T_{j,max}$	650	V
I_D	11	A
$R_{DS(on),\ max}$	0.35	Ω
$Qg_{,\ Typ}$	22.6	nC

Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

Package & Internal Circuit

TO-220FS	SYMBOL
	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C = 25℃)	11 *	A
	Drain Current - Continuous (T_C = 100℃)	7 *	A
I_{DM}[1)]	Drain Current - Pulsed	33 *	A
E_{AS}[2)]	Single Pulsed Avalanche Energy	141	mJ
I_{AR}	Avalanche Current	1.8	A
dv/dt	MOSFET dv/dt ruggedness, VDS=0…400V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…400V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	30	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.1	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient , Max.	80	℃/W

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 370 μA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.8 A	-	0.305	0.35	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1mA	600	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0	-	-	1	μA
		V_{DS} = 600 V, T_C = 150℃	-	-	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1.0 MHz	-	990	-	pF
C_{oss}	Output Capacitance		-	25	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.4	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 300 V, I_D = 4.8 A, R_G = 25 Ω (Note 3,4)	-	28	-	ns
t_r	Turn-On Rise Time		-	20	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	114	-	ns
t_f	Turn-Off Fall Time		-	17	-	ns
$Q_{g(}$	Total Gate Charge	V_{DS} = 480 V, I_D = 4.8 A, V_{GS} = 10 V (Note 3,4)	-	22.6	-	nC
Q_{gs}	Gate-Source Charge		-	4.6	-	nC
Q_{gd}	Gate-Drain Charge		-	6.4	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	33	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 4.8 A	-	-	1.3	V
trr	Reverse Recovery Time	V_R = 400 V, I_F = 4.8 A di_F/dt = 100 A/μs	-	250	-	ns
Qrr	Reverse Recovery Charge		-	2.6	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=1.8A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
4. Essentially Independent of Operating Temperature

Typical Characteristics

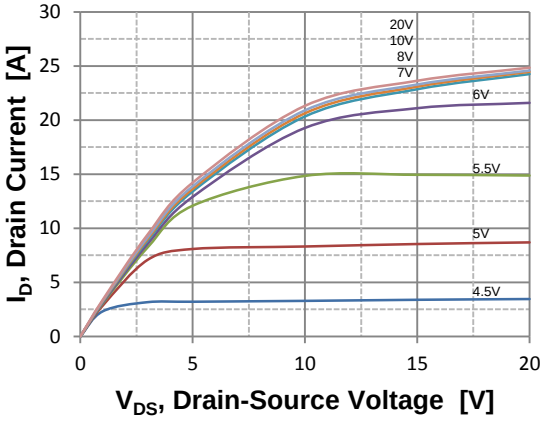


Figure 1. On Region Characteristics

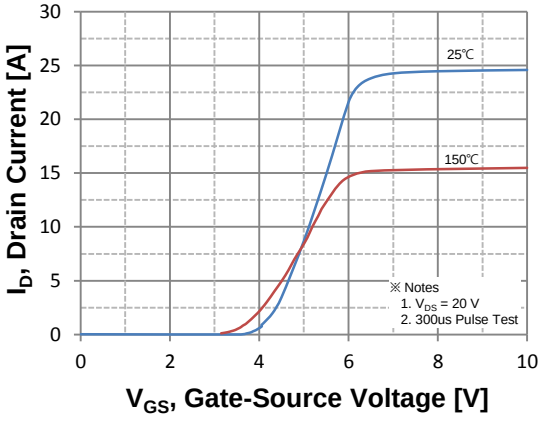


Figure 2. Transfer Characteristics

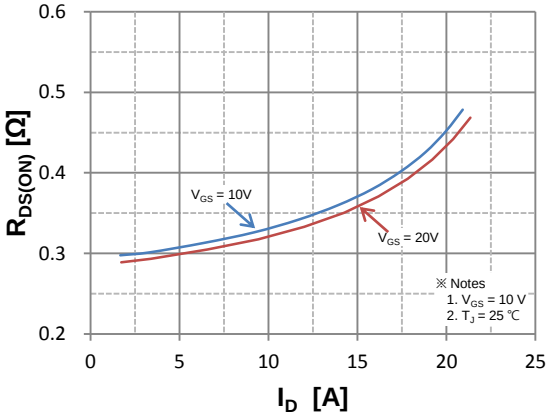


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

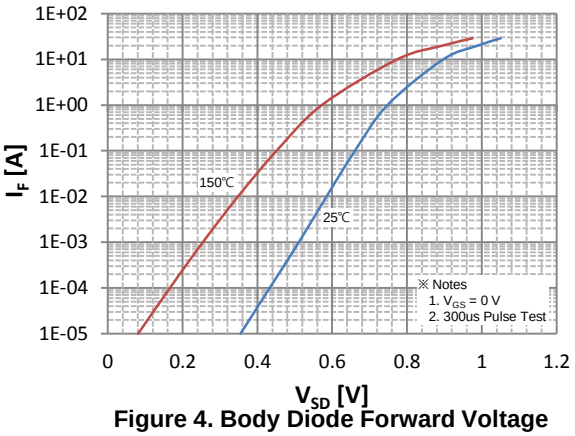


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

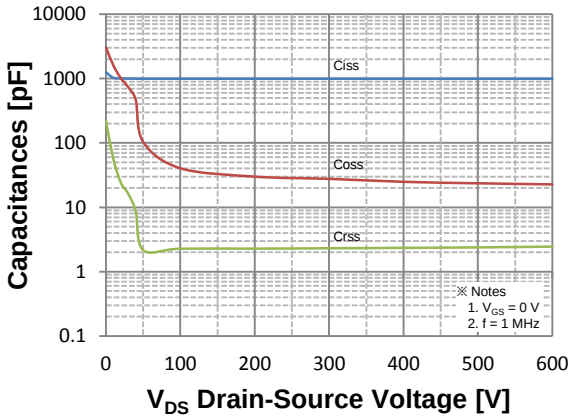


Figure 5. Capacitance Characteristics

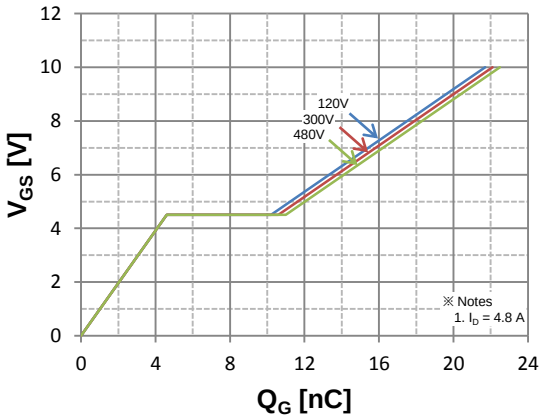


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

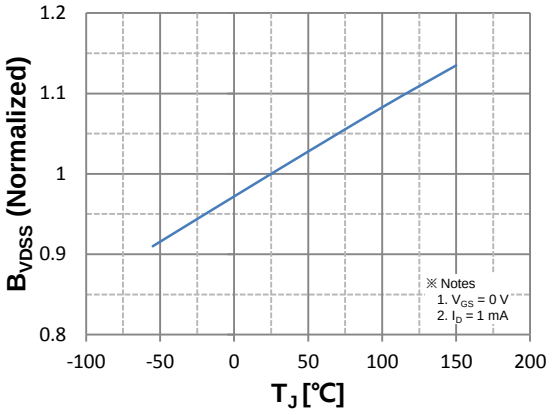


Figure 7. Breakdown Voltage Variation vs. Temperature

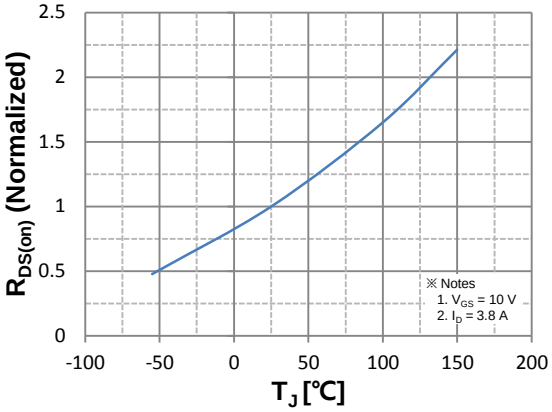


Figure 8. On-Resistance Variation vs. Temperature

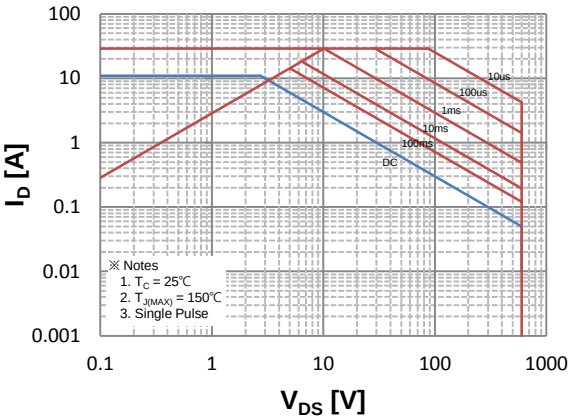


Figure 9. Maximum Safe Operating Area

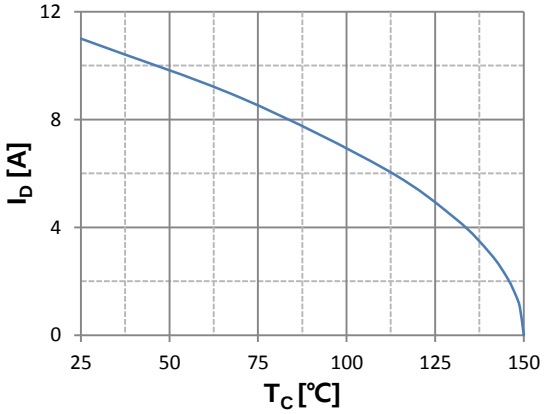


Figure 10. Maximum Drain Current vs. Case Temperature

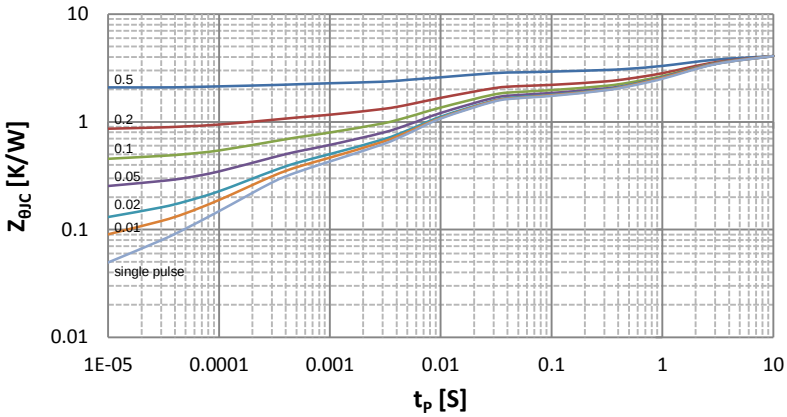


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

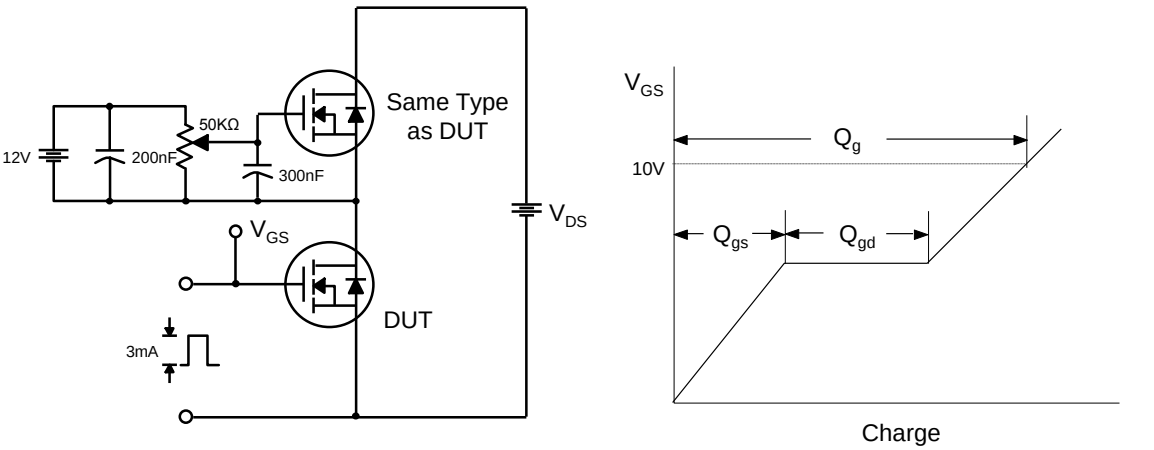


Fig 13. Resistive Switching Test Circuit & Waveforms

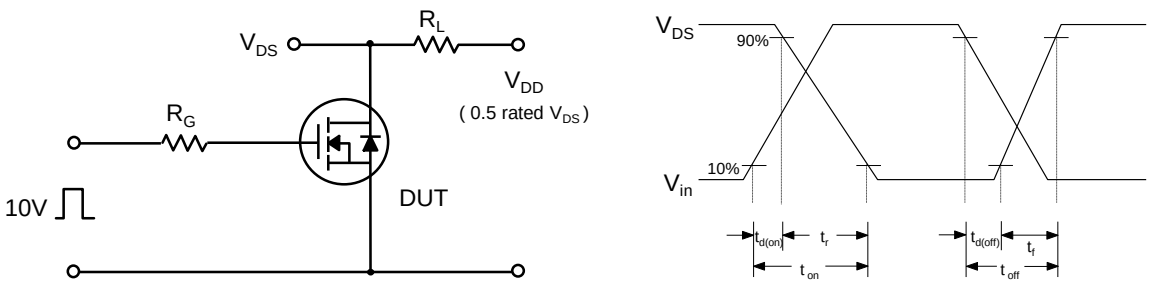


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

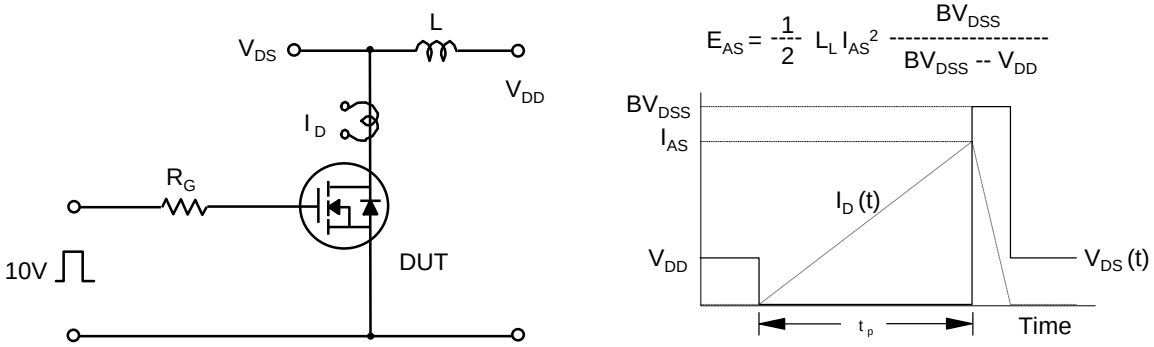
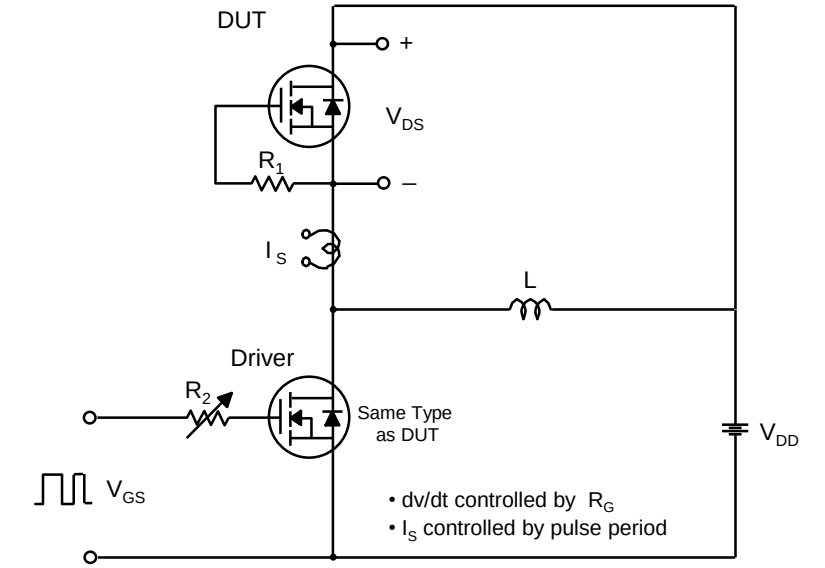
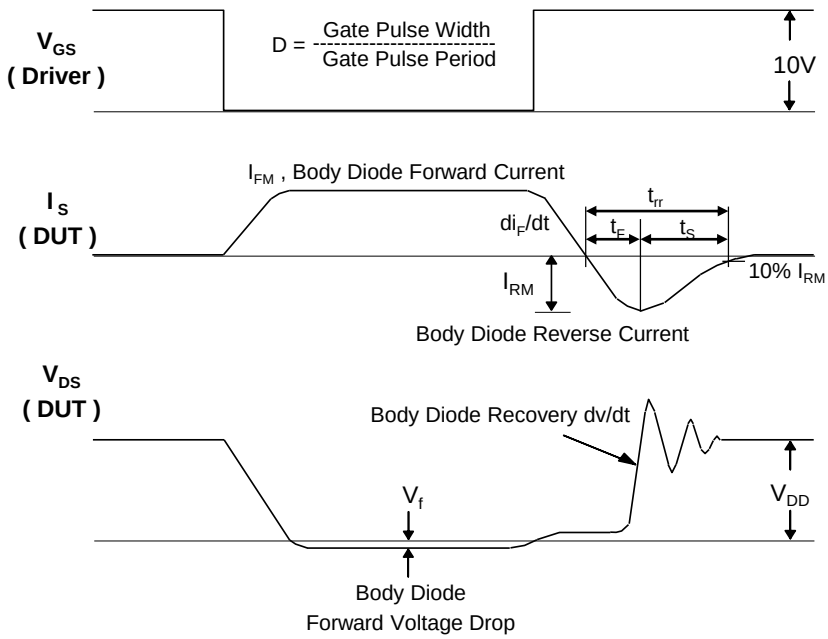


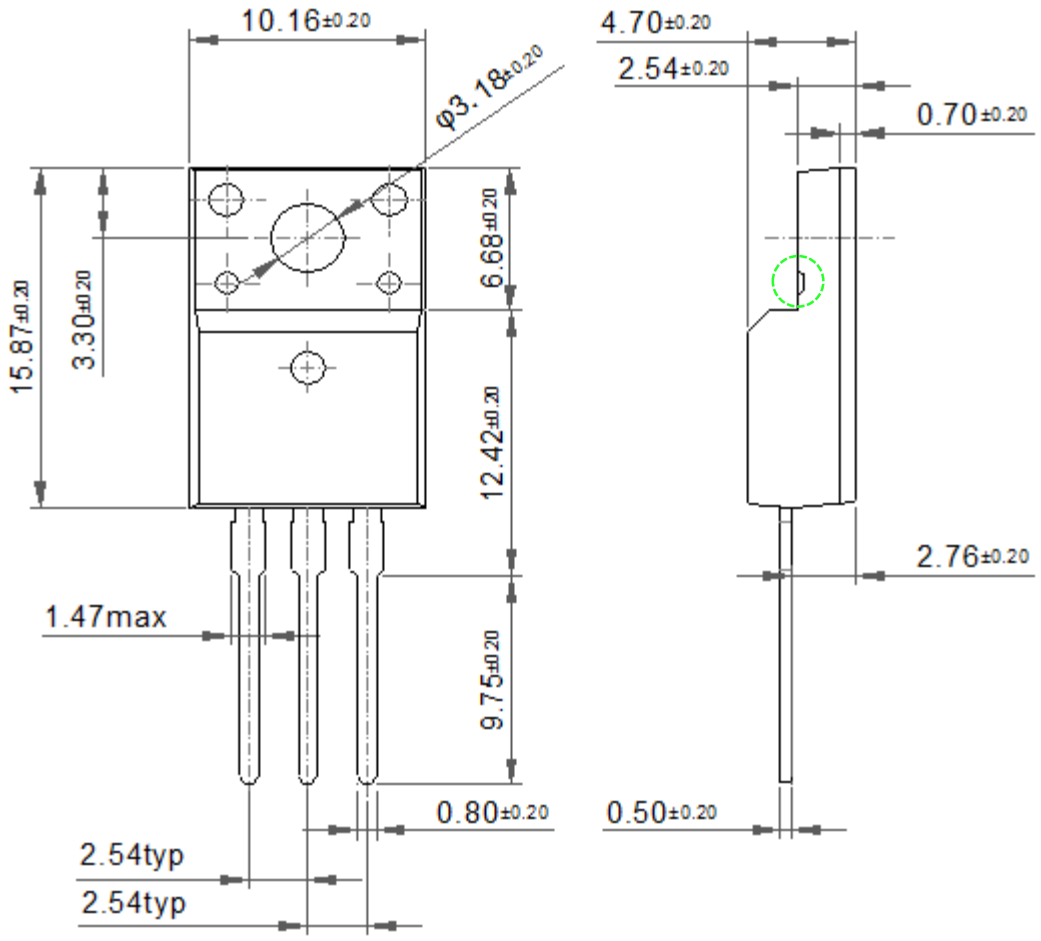
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimension

TO-220FS-FM(Full Mold)



Revision History

VERSION	DESCRIPTION	DATE	APPROVED
0	Initiate specification	20190507	HS Jo
1	Cap 조건 100V → 400V, TRR 수치 변경	20190620	HS Jo
2	S/W 특성 수치 변경 (Rg 30옴→3옴으로 변경하면서 낮아짐)	20190828	HS Jo
3			
4			
5			
6			
7			
8			
9			
10			