HCTS161AMS

Radiation Hardened Synchronous Counter

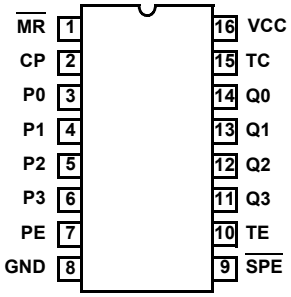
FN2144
Rev 2.00
September 1995

Features

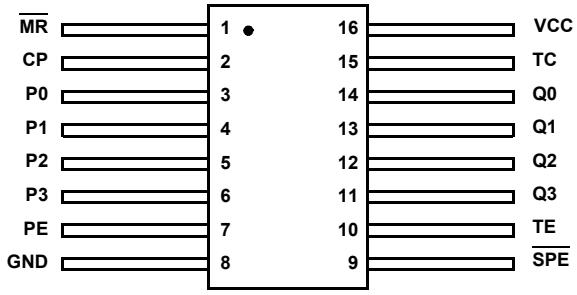
- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- Minimum LET for SEU Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55^{o}C to +125^{o}C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  -VIL = 0.8V Max
  -VIH = VCC/2V Min
- Input Current Levels Ii $\leq$ 5μA at VOL, VOH

Pinouts

**16 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T16, LEAD FINISH C**
TOP VIEW



**16 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F16, LEAD FINISH C**
TOP VIEW



Description

The Intersil HCTS161AMS high-reliability high-speed presettable four-bit binary synchronous counter features asynchronous reset and look-ahead carry logic. The HCTS161AMS has an active-low master reset to zero, $\overline{MR}$. A low level at the synchronous parallel enable, $\overline{SPE}$, disables counting and allows data at the preset inputs (P0 - P3) to load the counter. The data is latched to the outputs on the positive edge of the clock input, CP. The HCTS161AMS has two count enable pins, PE and TE. TE also controls the terminal count output, TC. The terminal count output indicates a maximum count for one clock pulse and is used to enable the next cascaded stage to count.

The HCTS161AMS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCTS161AMS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS161ADMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead SBDIP
HCTS161AKMSR	-55^{o}C to +125^{o}C	Intersil Class S Equivalent	16 Lead Ceramic Flatpack
HCTS161AD/Sample	+25^{o}C	Sample	16 Lead SBDIP
HCTS161AK/Sample	+25^{o}C	Sample	16 Lead Ceramic Flatpack
HCTS161AHMSR	+25^{o}C	Die	Die

Absolute Maximum Ratings

Supply Voltage (VCC). . . . . -0.5 to +7.0V
Input Voltage Range, All Inputs . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10sec) . . . . . $+265^oC$
Junction Temperature (TJ) . . . . . $+175^oC$
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package.	$73^oC/W$	$24^oC/W$
Ceramic Flatpack Package	$114^oC/W$	$29^oC/W$

Maximum Package Power Dissipation at $+125^oC$ Ambient
SBDIP Package. 0.68W
Ceramic Flatpack Package 0.44W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package. . . . . $13.7mW/^oC$
Ceramic Flatpack Package . . . . . $8.8mW/^oC$

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC). . . . . +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) . . . . . 100ns Max
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	40	µA
			2, 3	$+125^oC$, -55^oC	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V , (Note 2)	1	$+25^oC$	4.8	-	mA
			2, 3	$+125^oC$, -55^oC	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	$+25^oC$	-4.8	-	mA
			2, 3	$+125^oC$, -55^oC	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	V

NOTES:

1. All voltages reference to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay CP to Qn	TPLH1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPHL1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	29	ns
Propagation Delay CP to TC	TPLH2	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	31	ns
	TPHL2	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	33	ns
Propagation Delay TE to TC	TPLH3	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	21	ns
	TPHL3	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	25	
			10, 11	+125°C, -55°C	2	29	
Propagation Delay $\overline{MR}$ to Q	TPHL4	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	38	ns
			10, 11	+125°C, -55°C	2	45	ns
Propagation Delay $\overline{MR}$ to TC	TPHL5	VCC = 4.5V, VIH = 3.0V, VIL = 0V	9	+25°C	2	44	ns
			10, 11	+125°C, -55°C	2	51	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0, VIL = 0.0V, f = 1MHz	+25°C	-	231	pF
			+125°C, -55°C	-	285	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0, VIL = 0.0V, f = 1MHz	+25°C	-	10	pF
			+125°C, -55°C	-	10	pF
Pulse Width Time CP	TW	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	16	-	ns
			+125°C, -55°C	24	-	ns
Pulse Width Time $\overline{MR}$	TW	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	20	-	ns
			+125°C, -55°C	30	-	ns
Setup Time Pn to CP	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	10	-	ns
			+125°C, -55°C	15	-	ns
Setup Time PE to CP or TE	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	13	-	ns
			+125°C, -55°C	20	-	ns
Setup Time SPE to CP	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	12	-	ns
			+125°C, -55°C	18	-	ns
Hold Time Pn to CP	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	5	-	ns
			+125°C, -55°C	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Hold Time TE or PE to CP	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	3	-	ns
			+125°C, -55°C	3	-	ns
Hold Time SPE to CP	TSU	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	3	-	ns
			+125°C, -55°C	3	-	ns
Recovery Time	TREC	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	15	-	ns
			+125°C, -55°C	22	-	ns
Maximum Frequency	FMAX	VCC = 4.5V, VIH = 4.5, VIL = 0.0V,	+25°C	0	30	MHz
			+125°C, -55°C	0	20	MHz

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5, VIL = 0V, VOUT = 0.4V	+25°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5, VIL = 0V, VOUT = VCC -0.4V	+25°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V , IOL = 50μA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V , IOL = 50μA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, IOH = -50μA	+25°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, VIL = 0.8V, IOH = -50μA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V , (Note 2)	+25°C	-	-	V
Propagation Delay CP to Qn	TPHL1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	ns
	TPLH1	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	ns
Propagation Delay CP to TC	TPHL2	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	33	ns
	TPLH2	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	31	ns
Propagation Delay TE to TC	TPHL3	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	ns
	TPLH3	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	21	ns
Propagation Delay $\overline{MR}$ to Q	TPHL4	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	45	ns
Propagation Delay $\overline{MR}$ to TC	TPHL5	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	51	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic “1”, and VO ≤ 0.5V is recognized as a logic “0”.

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 15	1 - 10	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 15	8	-	1 - 7, 9, 10, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 6, 8	11 - 15	1, 3, 5, 7, 9, 10, 16	2	-

NOTES:

1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 15	8	1 - 7, 9, 10, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

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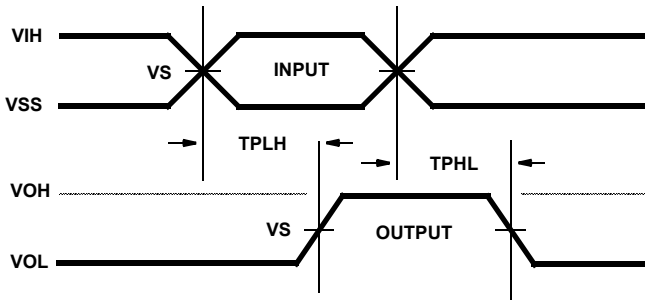
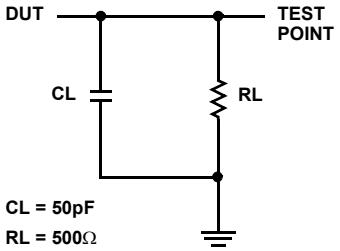
Propagation Delay Timing Diagram



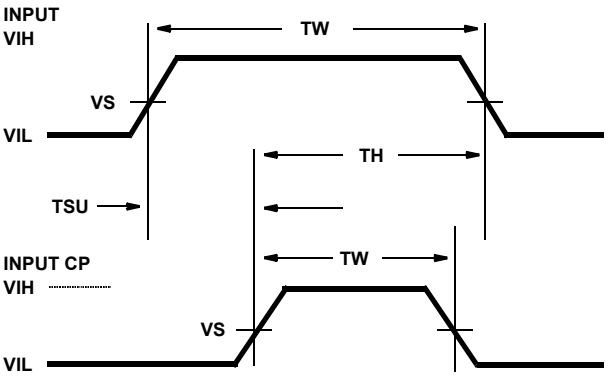
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger

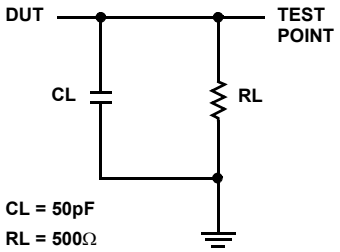


TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
86 x 104mils
2.19 x 2.65mm

METALLIZATION:
Type: AlSi
Metal Thickness: 11kÅ ± 1kÅ

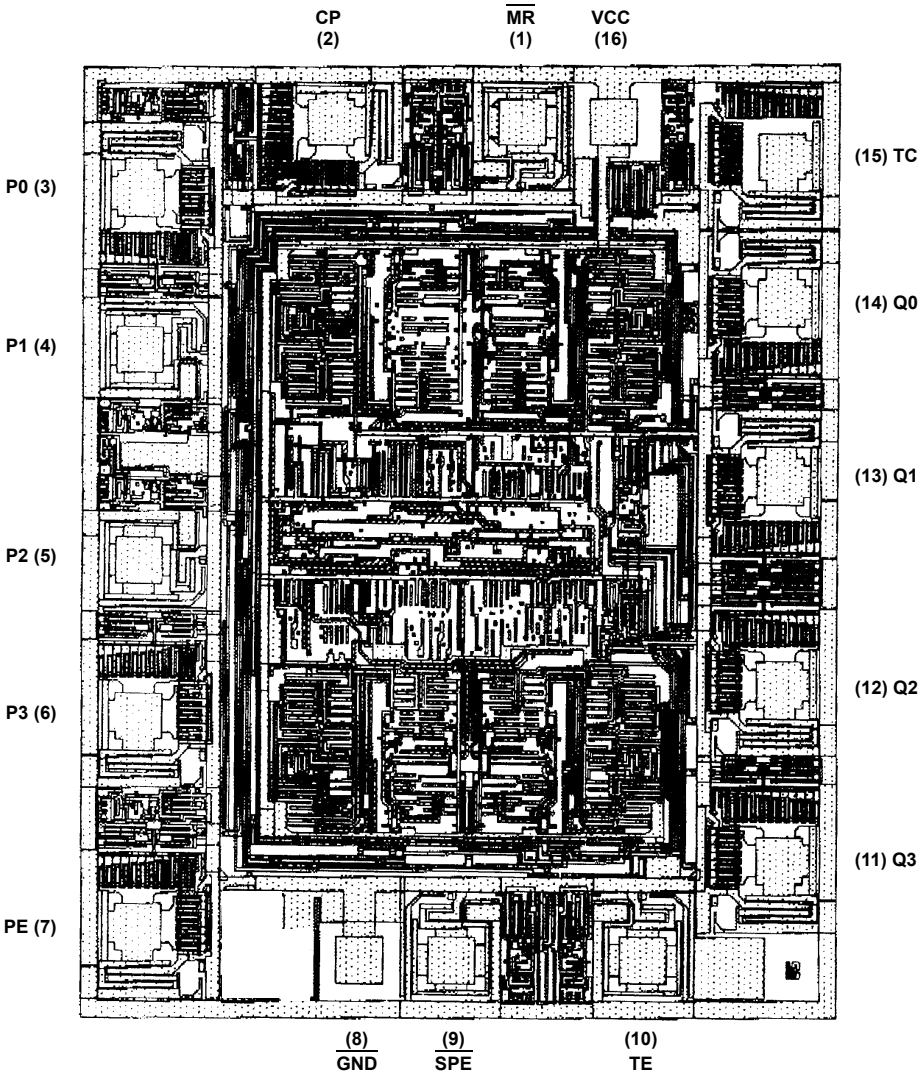
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCTS161AMS



NOTE: The die diagram is a generic plot form a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS161A is TA14446A.