

# HCTS574MS

Radiation Hardened Octal D-Type Flip-Flop, Three-State, Positive Edge Triggered

FN2359 Rev.2.00 August 1995

#### **Features**

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm<sup>2</sup>/mg
- Single Event Upset (SEU) Immunity < 2 x 10<sup>-9</sup> Errors/ Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10<sup>12</sup> RAD (Si)/s
- Dose Rate Upset >10<sup>10</sup> RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver O11utputs 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5µA at VOL, VOH

# Description

The Intersil HCTS574MS is a Radiation Hardened non-inverting octal D-type, positive edge triggered flip-flop with three-stateable outputs. The HCTS574MS utilizes advanced CMOS/SOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable  $(\overline{\text{OE}})$  controls the three-state outputs and is independent of the register operation. When the output enable is high, the outputs are in the high impedance state.

The HCTS574MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

The HCTS574MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

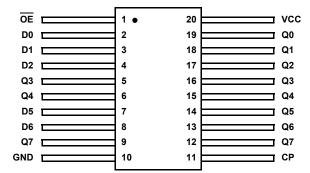
#### **Pinouts**

20 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T20 TOP VIEW

20 VCC OE 1 D0 2 19 Q0 D1 3 18 Q1 D2 4 Q2 17 D3 5 16 Q3 15 Q4 D4 6 D5 7 14 Q5 D6 8 13 Q6 D7 9 12 Q7 11 CP GND 10

20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F20

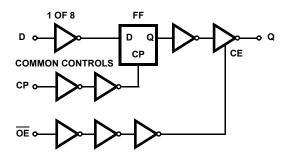
**TOP VIEW** 



# Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS574DMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead SBDIP
HCTS574KMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead Ceramic Flatpack
HCTS574D/Sample	+25°C	Sample	20 Lead SBDIP
HCTS574K/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
HCTS574HMSR	+25°C	Die	Die

# Functional Diagram



## **TRUTH TABLE**

INPUTS			OUTPUTS
ŌE	СР	Qn	
L		Н	Н
L	_	L	L
L	L	Х	Q0
L	Н	Х	Q0
Н	Х	Х	Z

H = High Level, L = Low Level, X = Immaterial, Z = High Impedance

= Transition from Low to High Level
Q0 = The level of Q before the indicated input conditions were established

## **Absolute Maximum Ratings**

Supply Voltage (VCC)	0.5V to +7.0V
Input Voltage Range, All Inputs	0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output	±25mA
(All Voltage Reference to the VSS Terminal)	
Storage Temperature Range (TSTG)	65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

## **Reliability Information**

Thermal Resistance	$\theta_{\sf JA}$	$\theta_{JC}$
SBDIP Package	72°C/W	24°C/W
Ceramic Flatpack Package	107°C/W	28°C/W
Maximum Package Power Dissipation at +125	5°C Ambien	t
SBDIP Package		0.69W
Ceramic Flatpack Package		0.47W
If device power exceeds package dissipation	capability, pi	rovide heat
sinking or derate linearly at the following rate:		
SBDIP Package	1	3.9mW/°C
Ceramic Flatpack Package		9.3mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

## **Operating Conditions**

Supply Voltage (VCC)+4.5V to +5.5V	Input Low Voltage (VIL)
Rise and Fall Times at 4.5V VCC(TR, TF) 500ns Max.	Input High Voltage (VIH)
Operating Temperature Range (T <sub>A</sub> )55°C to +125°C	

#### TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

	GROUP (NOTE 1) A SUB-		LIM	IITS			
PARAMETER	SYMBOL	CONDITIONS	GROUPS	TEMPERATURE	MIN	MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	μА
		VIIN - VCC OI GIND	2, 3	+125°C, -55°C	-	750	μА
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
(SIIIK)		VOOT = 0.4V, VIL = 0V	2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V,	1	+25°C	-7.2	-	mA
(Gource)		VIL = 0V	2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50μA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50μA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = 50μA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = 50μA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	μΑ
Current		GND	2, 3	+125°C, -55°C	-	±5.0	μА
Three-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 5.5V	1	+25°C	-	±1	μА
Leakage Current		voo, voo - 3.3v	2, 3	+125°C, -55°C	-	±50	μА
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

## NOTES:

- 1. All voltages reference to device GND.
- 2. For functional tests  $VO \ge 4.0V$  is recognized as a logic "1", and  $VO \le 0.5V$  is recognized as a logic "0".



TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

		(NOTES 1, 2)	GROUP A SUB-		LIM	IITS	
PARAMETER	SYMBOL	CONDITIONS	GROUPS	TEMPERATURE	MIN	MAX	UNITS
Clock to Q	TPLH, TPHL	VCC = 4.5V	9	+25°C	2	29	ns
	11111		10, 11	+125°C, -55°C	2	36	ns
Enable to Ouptput	TPZL	VCC = 4.5V	9	+25°C	2	32	ns
			10, 11	+125°C, -55°C	2	39	ns
	TPZH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	32	ns
Disable to Output	TPLZ, TPHZ	VCC = 4.5V	9	+25°C	2	23	ns
	11 112		10, 11	+125°C, -55°C	2	28	ns

#### NOTES:

- 1. All voltages referenced to device GND.
- 2. AC measurements assume RL =  $500\Omega$ , CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS** 

					LIM	IITS	
PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	MIN	MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, FQ = 1MHz	1	+25°C	-	39	pF
Dissipation			1	+125°C, -55°C	-	57	pF
Input Capacitance	CIN	VCC = 5.0V, FQ = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
Time	IILH		1	+125°C, -55°C	-	18	ns
Max Operating Frequency	FMAX	VCC = 4.5V	1	+25°C	-	30	MHz
rrequency			1	+125°C, -55°C	-	20	MHz
Setup Time Data to Clock	TSU	VCC = 4.5V	1	+125°C, -55°C	12	-	ns
CIOCK			1	+125°C, -55°C	18	-	ns
Hold Time Data to Clock	TH	VCC = 4.5V	1	+125°C, -55°C	5	-	ns
Clock			1	+125°C, -55°C	5	-	ns
Pulse Width Clocks	TW	VCC = 4.5V	1	+125°C, -55°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

## NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.



TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

		(NOTEC 4.2)		200K RAD LIMITS		
PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	MIN	MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50μA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50μA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	μА
Three-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 5.5V	+25°C	-	±50	μА
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3)	+25°C	-	-	-
Clock to Q	TPLH, TPHL	VCC = 4.5V	+25°C	2	36	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	39	ns
	TPZH	VCC = 4.5V	+25°C	2	32	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	28	ns

## NOTES:

- 1. All voltages referenced to device GND.
- 2. AC measurements assume RL =  $500\Omega$ , CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
- 3. For functional tests  $VO \ge 4.0V$  is recognized as a logic "1", and  $VO \le 0.5V$  is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μΑ
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

#### **TABLE 6. APPLICABLE SUBGROUPS**

CONFORMANCE GROUPS	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)	100%/5004	1, 7, 9	ICC, IOL/H



TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS		CONFORMANCE GROUPS METHOD GROUP A SUBGROUPS		READ AND RECORD
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Po	ostburn-In)	100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B Subgroup B-5		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
Subgroup B-6		Sample/5005	1, 7, 9	
Group D	•	Sample/5005	1, 7, 9	

#### NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

#### **TABLE 7. TOTAL DOSE IRRADIATION**

CONFORMANCE		TE	ST	READ AND	RECORD
GROUPS	METHOD	PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

## NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

#### TABLE 8. STATIC BURN-IN AND DYNAMIC BURN-IN TEST CONNECTIONS

				OSCILLATOR	
OPEN	GROUND	1/2 VCC = 3V $\pm$ 0.5V	$\text{VCC = 6V} \pm 0.5\text{V}$	50kHz	25kHz
STATIC BURN	-IN I TEST CONNECTIONS	S (Note 1)		-	
12 - 19	1 - 11	-	20	-	-
STATIC BURN	-IN II TEST CONNECTION	S (Note 1)			
12 - 19	10	-	1 - 9, 11, 20	-	-
DYNAMIC BUF	RN-IN TEST CONNECTION	IS (Note 2)			
-	1, 10	12 - 19	20	11	2 - 9

### NOTES:

- 1. Each pin except VCC and GND will have a resistor of 10K $\Omega$  ± 5% for static burn-in.
- 2. Each pin except VCC and GND will have a resistor of  $680\Omega \pm 5\%$  for dynamic burn-in.

**TABLE 9. IRRADIATION TEST CONNECTIONS** 

OPEN	GROUND	$\text{VCC} = 5\text{V} \pm 0.5\text{V}$
12 - 19	10	1 - 9, 11, 20

NOTE: Each pin except VCC and GND will have a resistor of  $47K\Omega \pm 5\%$  for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.



# Intersil Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

#### NOTES:

- 1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
- 2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
- 3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
- 4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
- 5. Data Package Contents:
  - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity)
  - · Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
  - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test
    equipment, etc. Radiation Read and Record data on file at Intersil.
  - · X-Ray report and film. Includes penetrometer measurements.
  - · Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
  - Lot Serial Number Sheet (Good units serial number and lot number).
  - · Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
  - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.



# AC Timing Diagrams

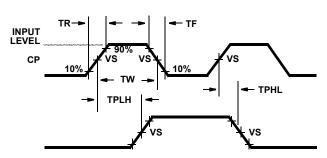


FIGURE 1. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

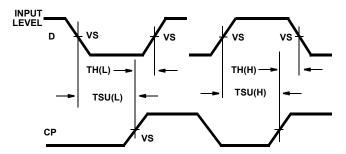


FIGURE 2. DATA SET-UP AND HOLD TIMES

#### **AC VOLTAGE LEVELS**

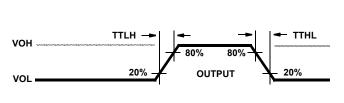
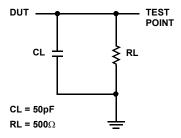


FIGURE 3. OUTPUT TRANSITION TIME

PARAMETER	нстѕ	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

# **AC Load Circuit**



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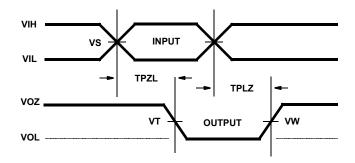
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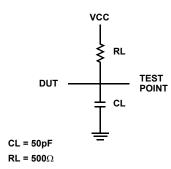
# Three-State Low Timing Diagrams



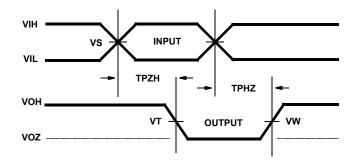
#### THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	нстѕ	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
vw	0.90	V
GND	0	V

# Three-State Low Load Circuit



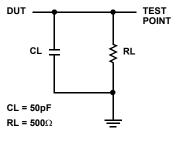
# Three-State High Timing Diagrams



#### THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	нстѕ	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

# Three-State High Load Circuit



## Die Characteristics

## **DIE DIMENSIONS:**

101 x 85 mils

#### **METALLIZATION:**

Type: SiAI

Metal Thickness: 11kÅ ± 1kÅ

## **GLASSIVATION:**

Type: SiO<sub>2</sub>

Thickness:  $13k\text{\AA} \pm 2.6k\text{\AA}$ 

## **WORST CASE CURRENT DENSITY:**

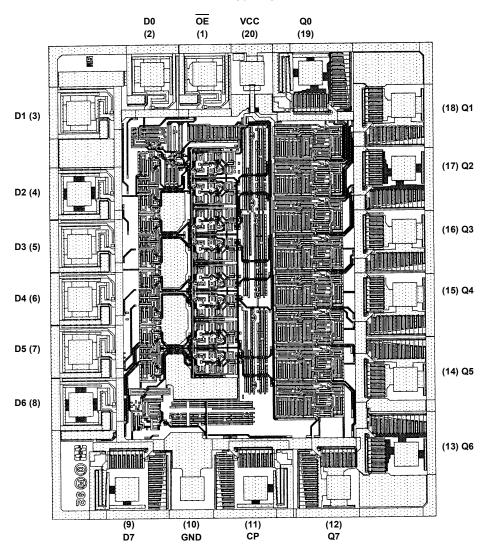
 $<2.0 \times 10^5 \text{A/cm}^2$ 

## **BOND PAD SIZE:**

 $100 \mu m~x~100 \mu m$  4 mils x 4 mils

# Metallization Mask Layout

## HCTS574MS



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS574 is TA14460A.

