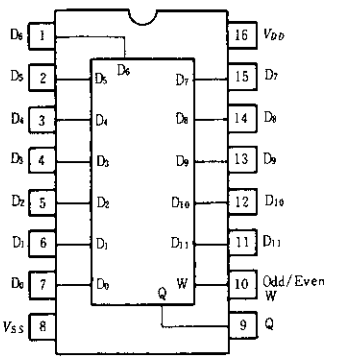
12-bit Parity Tree

The HD14531B 12-bit parity tree consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other HD14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

■ PIN ARRANGEMENT

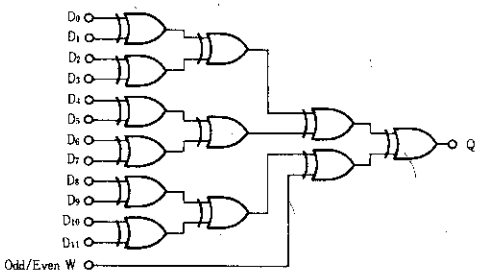


(Top View)

■ FEATURES

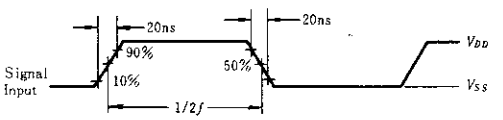
- Noise Immunity = 45% of V_{DD} typ.
- Supply Voltage Range = 3 to 18V
- All Outputs Buffered
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Quiescent Current = 5nA/pkg typ. @5V
- Variable Word Length

■ LOGIC DIAGRAM

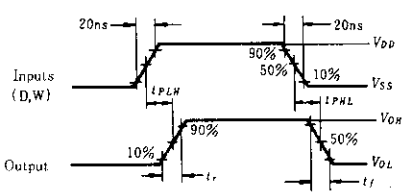


$Q = D_0 \oplus D_1 \oplus D_2 \oplus \cdots \oplus D_{11} \oplus W$

● POWER DISSIPATION SIGNAL WAVEFORM



● DYNAMIC SIGNAL WAVEFORMS



■ TRUTH TABLE

Inputs								Output
W	D_{11}	D_{10}	·····	D_2	D_1	D_0	Decimal(0ctal) Equivalent	Q*
0	0	0	·····	0	0	0	0 (0)	0
0	0	0	·····	0	0	1	1 (1)	1
0	0	0	·····	0	1	0	2 (2)	1
0	0	0	·····	0	1	1	3 (3)	0
0	0	0	·····	1	0	0	4 (4)	1
0	0	0	·····	1	0	1	5 (5)	0
0	0	0	·····	1	1	0	6 (6)	0
0	0	0	·····	1	1	1	7 (7)	1
⋮	⋮	⋮	·····	⋮	⋮	⋮	⋮	⋮
1	1	1	·····	0	0	0	8184(17770)	0
1	1	1	·····	0	0	1	8185(17771)	1
1	1	1	·····	0	1	0	8186(17772)	1
1	1	1	·····	0	1	1	8187(17773)	0
1	1	1	·····	1	0	0	8188(17774)	1
1	1	1	·····	1	0	1	8189(17775)	0
1	1	1	·····	1	1	0	8190(17776)	0
1	1	1	·····	1	1	1	8191(17777)	1

* 0=Even Parity, 1=Odd Parity

■ ELECTRICAL CHARACTERISTICS

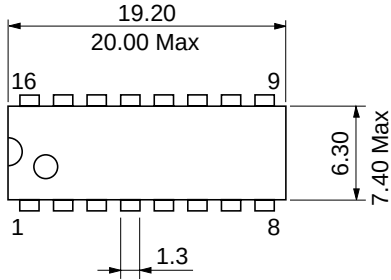
Characteristic	Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5$ or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5$ or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5$V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
		5.0	$V_{OH}=4.6$V	−0.2	—	−0.16	−0.36	—	−0.12	—	
		10	$V_{OH}=9.5$V	−0.5	—	−0.4	−0.9	—	−0.3	—	
		15	$V_{OH}=13.5$V	−1.4	—	−1.2	−3.5	—	−1.0	—	
	I_{OL}	5.0	$V_{OL}=0.4$V	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5$V	1.3	—	1.1	2.25	—	0.9	—	
		15	$V_{OL}=1.5$V	3.6	—	3.0	8.8	—	2.4	—	
Input Current	I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	μA
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	I_T	5.0	Dynamic $+I_{DD}$, per Gate $C_L=50$pF, $f=1$kHz	—	—	—	0.25	—	—	—	μA
		10		—	—	—	0.50	—	—	—	
		15		—	—	—	0.75	—	—	—	

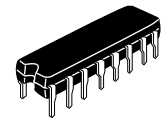
* To calculate total supply current at frequency other than 1kHz.
@$V_{DD}=5.0$V $I_T=(0.25\mu A/kHz)f+I_{DD}$, @$V_{DD}=10$V $I_T=(0.50\mu A/kHz)f+I_{DD}$, @$V_{DD}=15$V $I_T=(0.75\mu A/kHz)f+I_{DD}$

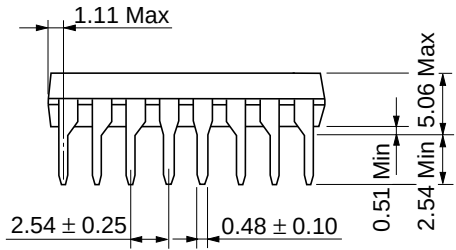
■ SWITCHING CHARACTERISTICS ($C_L=50$pF, $Ta=25$℃)

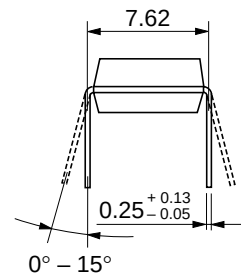
Characteristic		Symbol	V_{DD}(V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Data to Q	t_{PLH}, t_{PHL}	5.0	—	440	1320	ns
			10	—	175	525	
			15	—	120	360	
	Odd/Even to Q		5.0	—	250	750	
			10	—	100	300	
			15	—	70	210	

Unit: mm









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