HD153011

2-7 RLL ENDEC built-in VFO

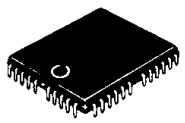
Description

The HD153011 is a 2-7 RLL ENDEC built-in VFO IC developed for magnetic disks. This device decodes a 2-7 RLL signal read from a magnetic disk into an NRZ signal, and encodes an NRZ signal to be written to a magnetic disk into a 2-7 RLL signal.

Features

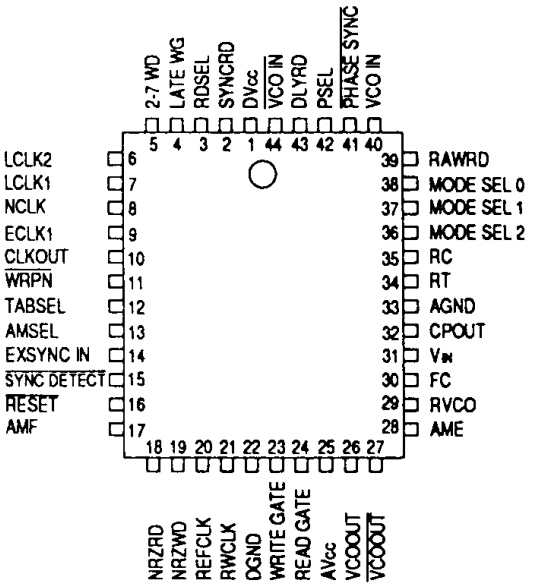
- Can correspond to 15 Mbps of data transfer rate
- Can decode and encode in IBM 2-7 RLL method
- Write precompensation function
- Selectable internal delay or external delay line with write precompensation
- Address mark generation and detection for DC erase and illegal patterns
- Detection of 4T (1000) sync field pattern
- 2-7 RLL signal can be active high or active low
- Undefined NRZ read data output disable immediately after read gate assertion
- Non-adjusting PLL (Decode window center adjust mode is provided)
- Selectable window-center adjusting mode or non-adjusting mode
- PLL characteristic frequency ωn and damping rate ζ are defined without 2-7 RLL signal cycle (3T to 8T)
- Two phase detector modes, phase comparison and frequency phase comparison
- Can switch normal gain mode to/from high gain mode and can switch loop filter constant
- Fix VCO center frequency by inputting the power-on reset signal at power on
- Built-in oscillation timing capacitance of VCO
- TTL compatible I/O's
- Package: MSP-44 suitable for compact surface mounting
- High-speed and low-power dissipation are accomplished owing to Hi-Bi CMOS process (300 mW Typ)
- 5 V single power supply

HD153011



(MP-44)

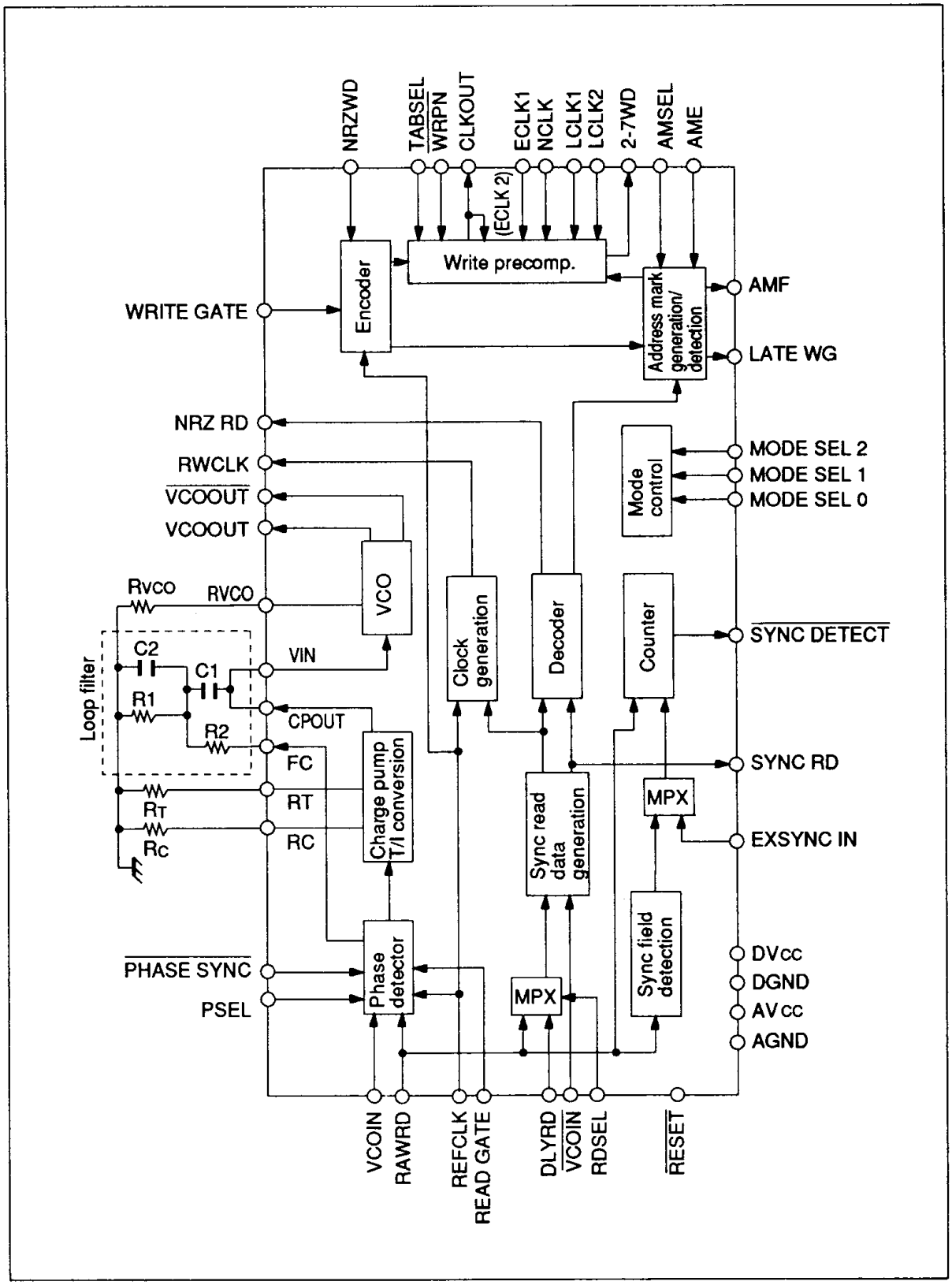
Pin Arrangement



(Top view)

Ordering Information

Type No.	Package
HD153011	MP-44



Block Diagram

Table 1 Pin Description

Pin Name	Pin No	Type	Function
WRITE GATE	23	IN	Setting this pin high allows a data write; NRZ data to be written to the disk is converted into a 2-7 code for output. Set WRITE GATE high to write a soft-sector address mark and low for address detection.
$\overline{\text{PHASE SYNC}}$	41	IN	A low on this pin allows the clock phase to be synchronized with 4T (1000) SYNC pattern (High Gain) during a data read from the disk. After synchronization, negating this pin sets the PLL in phase comparison mode (Normal Gain). This pin is usually connected to the $\overline{\text{SYNC DETECT}}$ pin.
PSEL	42	IN	Selects the polarity of the 2-7 code read from the disk which is input to the RAWRD and DLYRD pins. Read Data Polarity / PSEL Pin Active High / High Active Low / Low
VCOIN	40	IN	Connected to VCOOUT. Inputs PLL feed-back signal synchronous with a data read from the disk.
$\overline{\text{VCOIN}}$	44	IN	Connected to $\overline{\text{VCOOUT}}$. A clock-pulse input to this pin activates the clock sync and decoder circuits.
RAWRD	39	IN	Inputs a 2-7 code which was read from the disk. The leading edge of the input signal is the flux reversal timing. The PLL uses this leading edge for phase sync.
REFCLK	20	IN	Provides the reference clock signal with a frequency twice the data transfer rate. The VCO synchronizes with this clock when not reading data. REFCLK is also used as a data write clock.
READ GATE	24	IN	Setting this pin high allows a data read; a 2-7 code read from the disk is converted into an NRZ signal for output. This signal activates the counter clock and internal circuits and enables NRZ signal output. The PLL also initiates phase synchronization with a 2-7 code. Set READ GATE high for 7-2 illegal pattern detection.
DLYRD	43	IN	Setting the RDSEL pin Low inputs a 2-7 code to the sync read data generation circuit. Since this pin is independant of the PLL, the shift of window center caused by the PLL phase error and gate delay error can be adjusted by controlling the phase using external delay elements.

Table 1 Pin Description (cont)

RDSEL	3	IN	Determines what signal will be input to the sync read data generation circuit. RDSEL: High → 2-7 code input from RAWRD; Low → 2-7 code input from DLYRD For details, see in "Functional Description"
$\overline{\text{RESET}}$	16	IN	Initializes internal logic by setting this pin Low at power on. The VCO output clock frequency is set to the center frequency. This pin is held high during normal operation.
EXSYNC IN	14	IN	Inputs a High level that is output from an external sync field detection circuit during detection of a 4T (1000) pattern (at soft-sector/external circuit mode). If the High level is detected for a 2-byte period, SYNC DETECT is asserted Low. Before returning High, this Low is maintained for the period set by MODE SEL 0-2. When EXSYNC IN is set Low while $\overline{\text{SYNC DETECT}}$ is Low, SYNC DETECT returns to the High state.
MODE SEL 0 MODE SEL 1 MODE SEL 2	38 37 36	IN IN IN	These three pins set the operation mode of the IC.

Mode SEL 2	Mode SEL 1	Mode SEL 0	SYNC pattern detection mode	SYNC DETECT output period
L	L	L	Built-in sync field detection circuit	6 bytes
L	L	H		8 bytes
L	H	L		8 bytes
L	H	H	External sync field detection circuit	6 bytes
H	L	L		8 bytes
H	L	H	READ GATE*1	6 bytes
H	H	L		8 bytes
H	H	H		8 bytes

Notes:

*1. With a hard-sector format, the $\overline{\text{SYNC DETECT}}$ signal becomes active low at the first trailing edge of the RAWRD signal, while READ GATE is asserted.

*2 The DC erase method can be used in hard-sector mode.

Table 1 Pin Description (cont)

AME (Address mark enable)	28	IN	Used with DC Erase mode. Set this pin High to write a soft-sector address mark or to detect an address mark. When writing an address mark, DC Erase will continue as long as AME and WRITE GATE are both held High. For an address mark detect, hold AME High and WRITE GATE Low when a DC Erase has continued for 30 REF CLOCK periods, signal AMF (Address Mark Found) will be asserted at the end of the DC Erase period. For hard-sector mode and 7-2 illegal pattern mode, this pin should be held Low.
AMSEL	13	IN	Selects the method of address mark generation and detection. AMSEL: High — Method of Address Mark Generation/Detection: DC erase AMSEL: Low — Method of Address Mark Generation/Detection: 7-2 illegal pattern* *: 7-2 illegal pattern: Not covered by the 2-7 code. 100000001001 (7 0's, 2 0's)
LCLK2	6	IN	Clock used for write precompensation. The phase of this clock must lag behind the normal clock, and the amount of lag must be larger than LCLK1. This pin is also used to switch to internal gate delay mode (WRPN = high, TABSEL = low, LCLK2 = high).*1 *1: See item in "Functional Description"
LCLK1	7	IN	Clock used for write precompensation. The phase of this clock must lag behind the normal clock. This clock is selected only when Table 2 is selected.
NCLK	8	IN	A reference clock used for write precompensation. This pin is connected to the CLKOUT pin in internal gate delay mode.
ECLK1	9	IN	Clock used for write precompensation. The phase of this clock must lead the normal clock (NCLK), but lag the CLKOUT signal.
TABSEL WRPN	12 11	IN IN	These pins select one of three types of write precompensation modes as follows:

LCLK 1	$\overline{\text{WRPN}}$	TABSEL	Table Selected	Precomp. Method
—	L	L	2	External delay element
—	L	H	1	External delay element
H	H	L	2	Internal delay element
—	H	H	—	No phase precomp.

Table 1 Pin Description (cont)

NRZWD	19	IN	Inputs an NRZ signal to be written to the disk. This signal must be input synchronously with the RWCLK signal. The HD153011 converts the input signal of this pin into a 2-7 code once.
NRZWD	18	OUT	Outputs NRZ data converted from a 2-7 code, during a data read. This signal is synchronized with the RWCLK signal.
RWCLK	21	OUT	When reading data, outputs a clock signal synchronous with the converted NRZRD and when writing data, outputs a clock signal divided by the reference clock (REFCLK). The disk controller must input NRZ read data synchronous with this clock signal, and input NRZ write data synchronous with this clock. Glitches from clock switching are removed from the RWCLK output signal.
VCOOUT	26	OUT	VCO output pin. Connected directly to the VCOIN pin.
$\overline{\text{VCOOUT}}$	27	OUT	VCO output pin. Connected directly to the $\overline{\text{VCOIN}}$ pin. This signal, which is an inverted VCOOUT signal, is generated from the same circuit as the VCOOUT signal, utilizing symmetrical characteristics of the internal VCO circuit.
SYNCRD	2	OUT	A 2-7 code latched by the VCO clock. The output of this pin is used to monitor the window margin when in non-adjusting mode without DLYRD. Otherwise it is used as a window center adjusting monitor pin to adjust the phase of DLYRD.
$\overline{\text{SYNC}}$ DETECT	15	OUT	• Soft-sector mode If a high level is detected for 2-byte period at the built-in sync field detection circuit output and the EXSYNC IN input, this pin is asserted Low. The pin returns to High after Low is maintained for the period set by MODE SEL 0-2. • Hard-sector mode When READ GATE is active High, this pin is asserted Low with RAWRD pulse timing. The pin returns to High after Low is maintained for the period set by MODE SEL 0-2. In both soft-sector DC Erase mode and hard-sector mode, this signal will go Low with the first assertion of READ GATE. It will remain Low until READ GATE is asserted again, at which time it is disabled and returns to a High level. This pin is usually connected with the $\overline{\text{PHASE SYNC}}$ pin.

Table 1 Pin Description (cont)

LATE WG	4	OUT	A clock that lags the rising edge of the WRITE GATE signal by 16 REFCLK cycles. During this period, 2-7 write data output signal returns to its original form.
AMF (Address Mark Found)	17	OUT	• DC erase mode AMF is held High when the DC erase period exceeds 30 REFCLK cycles with the AME signal High and WRITE GATE signal Low. AMF is set Low when AME is set Low. • 7-2 illegal mode AMF is held high if the 7-2 illegal pattern (100000001001) is detected while READ GATE is Low. AMF is set High when the READ GATE signal is set Low.
2-7WD	5	OUT	Outputs a 2-7 code that has been converted from the NRZ signal before writing.
CLKOUT	10	OUT	Outputs a reference clock signal used to perform write precompensation. Internally, this signal is used as the ECLK2 input.
FC	30	Part connector	Used to set the damping rate ζ of a loop filter, and independently set the damping rates in High Gain and in Normal Gain. • High Gain An internal transistor connected to FC is saturated, grounding FC. • Normal Gain An internal transistor connected to FC is shut off, putting FC into the high-impedance.
RC	35	Part connector	Used for resisitor to set the charge pump output current at High Gain. The resistor value determines the gain of the charge pump.
RT	34	Part connector	Used for resistor to set the sampling feedback gain of the T/I conversion circuit to 1 (ideal value). The value is determined depending on transfer rate.
CPOUT	32	Part connector	Output pin that sources current to an external loop filter. This pin is usually connected to the V_{IN} pin and to an external loop filter.
V_{IN}	31	Part connector	Voltage input pin for the built-in VCO. VCO oscillation frequency is changed depending on the voltage applied to this pin. When the RESET signal is enabled, VCO bias voltage generated internally is applied to V_{IN} via an analog switch. VCO then oscillates at the center frequency. This pin is usually connected to CPOUT.

Table 1 Pin Description (cont)

RVCO	29	Part connec-tor	Used for resistor to set the VCO center frequency. It is determined depending on the transfer rate.
DVcc	1	Power supply	Vcc pin for digital circuits
DGND	22	Power supply	GND pin for digital circuits
AVcc	25	Power	Vcc pin for analog circuits
AGND	33	Power supply	GND pin for analog circuits

Functional Description

NRZ signal to 2-7 code conversion

a. An NRZ signal to be written to a magnetic disk is converted into a 2-7 code.
b. The Conversion table is shown below.

NRZ to/from Code Conversion Table

NRZ	2-7 Code
01	0100
101	100100
1101	00100100
00	1000
100	001000
1100	00001000
111	000100

Note: The disk controller must output a "0 0" sync pattern.

c. Write precompensation of converted 2-7 code. (described later).

2-7 code to NRZ signal conversion

a. A 2-7 code read from a magnetic disk is converted into an NRZ signal.
b. The conversion table is shown above.
c. Read clock is output as the sync clock of an NRZ read signal.

Write precompensation

a. A converted 2-7 write code is write precompensated according to Table 1 or 2.
2-7 code string example:

n m
100..... 01 00.... 01
before current after

n: The number of 0's between the current "1" and before "1".
m: The number of 0's between the current "1" and after "1".

b. Tables 2 and 3 are selected depending on the input state of the TABSEL pin:

Table 2 for High level, Table 2 for Low level.
(Table 2)

n/m	2	3	4	5	6	7
2	N	E_2	E_2	E_2	E_2	E_2
3	L_2	E_1	E_1	E_1	E_1	E_1
4	L_2	E_1	E_1	E_1	E_1	E_1
5	L_2	E_1	E_1	E_1	E_1	E_1
6	L_2	E_1	E_1	E_1	E_1	E_1
7	L_2	E_1	E_1	E_1	E_1	E_1

(Table 3)

n/m	2	3	4	5	6	7
2	N	E_1	E_2	E_2	E_2	E_2
3	L_1	N	E_1	E_1	E_1	E_1
4	L_2	L_1	N	N	E_1	E_1
5	L_2	L_1	N	N	N	N
6	L_2	L_1	L_1	N	N	N
7	L_2	L_1	L_1	N	N	N

c. The amount of write precompensation depends on the phase difference between the CLKOUT reference output clock and the externally-supplied clock, and on the internal gate delay.

E_2: CLKOUT output signal phase
E_1: ECLK1 input signal phase
N: NCLK input signal phase
L_1: LCLK1 input signal phase
L_2: LCLK2 input signal phase

The relation among the five clocks is:

$E_2 > E_1 > N > L_1 > L_2$

← Phase lead Phase lag →

d. Write precompensation is enabled when $\overline{WRPN}$ is Low.
e. Write precompensation is disabled when $\overline{WRPN}$ and TABSEL are High.
f. When $\overline{WRPN}$ is High and TABSEL is Low, internal gate delay write precompensation is performed according to Table 3. The clock is supplied to an internal gate from the NCLK pin. Normally the NCLK is connected to the CLKOUT pin.

LCLK 2	$\overline{WRPN}$	TABSEL	Table Selected	Precompensation Method
—	L	L	2	External delay element
—	L	H	1	External delay element
H	H	L	2	Internal gate delay element
—	H	H	—	No precompensation

Address generation (DC erase) generation

a. When the WRITE GATE signal is asserted, 2-7 write signal transitions halt when the AME signal (address mark enable) is active.
b. The address mark continues to be written, even when AME is active.

Address mark (DC erase) detection

When the 2-7 write signal remains unchanged for 16 bits of data or more, address mark detection signal AMF is asserted following the next address mark. The AMF signal is then negated after the AME signal is negated.

Address mark (7-2 illegal pattern) generation

During WRITE GATE signal assertion, the NRZ write signal "174X" (X means arbitrary bit) which is transmitted first is converted into a 7-2 illegal pattern, after which an address mark is written. This operation is done once for each WRITE GATE assertion.

Address mark (7-2 illegal pattern) detection

If a 7-2 illegal pattern appears during a data read, address mark detection signal AMF is asserted. Then after negating the READ GATE signal, the AMF signal is negated. At that time. NRZRD converts the illegal pattern into "17CX" and outputs it.

Sync field detection

a. READ GATE active mode (read gate mode, DC erase mode)

In READ GATE active mode, the READ GATE can be asserted during the sync field. After the READ GATE is asserted, $\overline{SYNC\ DETECT}$ is asserted Low at the first 2-7 code pulse timing. The Low is maintained for the period set by MODE SEL 0-2 before returning High. This operation is done once for each READ GATE assertion.

b. 4T cycle detection mode 1 (7-2 illegal pattern mode, DC Erase mode)

In this mode, an internal 4T cycle detection circuit is used. When a 4T(1000) pattern is detected after the assertion of READ GATE, then $\overline{SYNC\ DETECT}$ will pulse Low for the time period set by MODE SEL 0-2. This operation is performed once for each assertion of READ GATE.

c. 4T cycle detection mode 2 (7-2 illegal pattern mode, DC Erase mode)

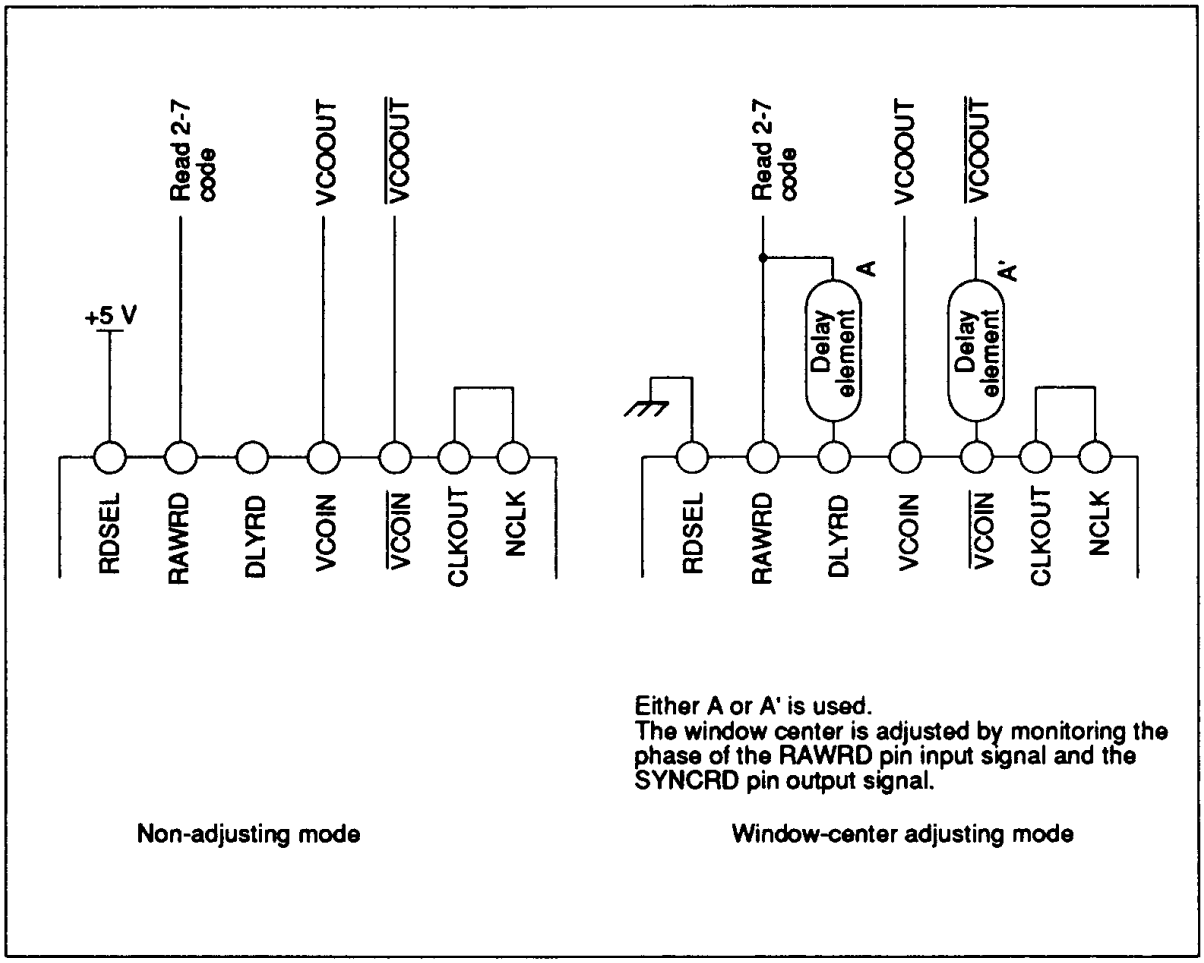
In this mode, an external 4T cycle detection circuit is used. The output from this circuit, which should go High when a 4T cycle pattern is being detected, is applied to the EXSYNC IN pin. After READ GATE has been asserted, a High on EXSYNC IN for a two-byte 4T pattern detection period will cause $\overline{SYNC\ DETECT}$ to pulse low for the time period set by MODE SEL 0-2. With DC Erase mode, this operation is performed once for each assertion of READ GATE.

Sync read data generation and TEST mode

The 2-7 read code to be input to the sync read data generation circuit is selected by the RDSEL pin.

RDSEL	Sync Read Data Generation Circuit Input	DLYRD Pin	$\overline{VCOIN}$ Pin	SYNCRD Pin	RWCLK Pin	$\overline{SYNC\ DETECT}$ Pin	VCOOUT Pin	$\overline{VCOOUT}$ Pin
H	RAWRD	Disable	$\overline{VCOIN}$	SYNCRD	RWCLK	$\overline{SYNC\ DETECT}$	VCOOUT	$\overline{VCOOUT}$
L	DLYRD	DLYRD						

Each pin functions depending on the setting as shown in the preceding page.
When a window center is adjusted by external delay element, RDSEL must be set Low. If not adjusted, RDSEL must be set High. (See the figures shown below.)



Non-adjusting mode

Either A or A' is used.
The window center is adjusted by monitoring the phase of the RAWRD pin input signal and the SYNCRD pin output signal.

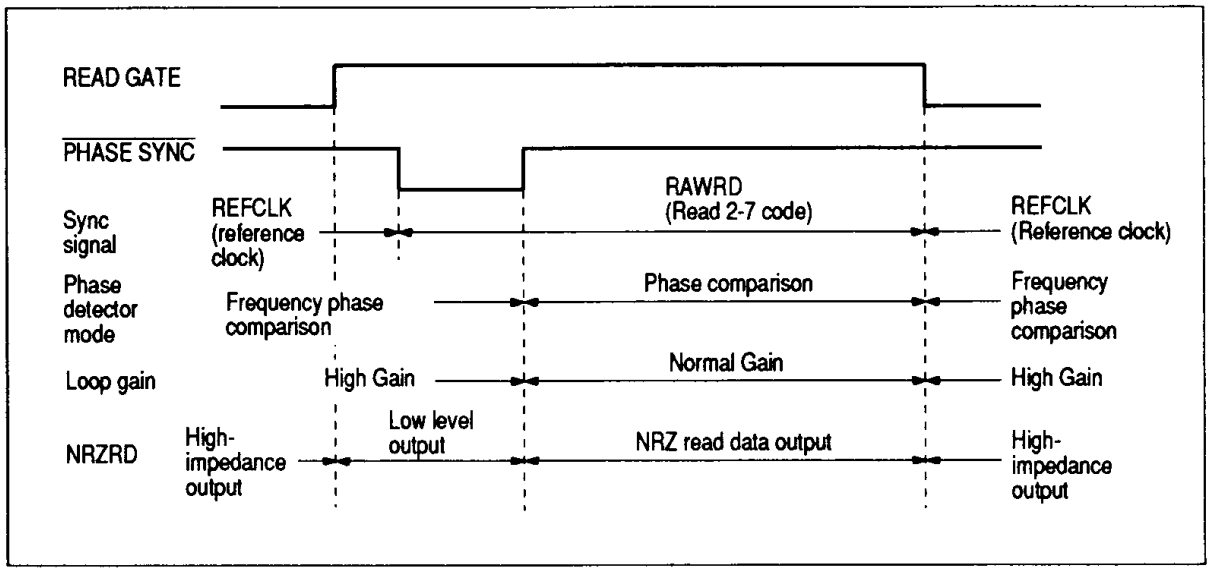
Window-center adjusting mode

Polarity of 2-7 read code

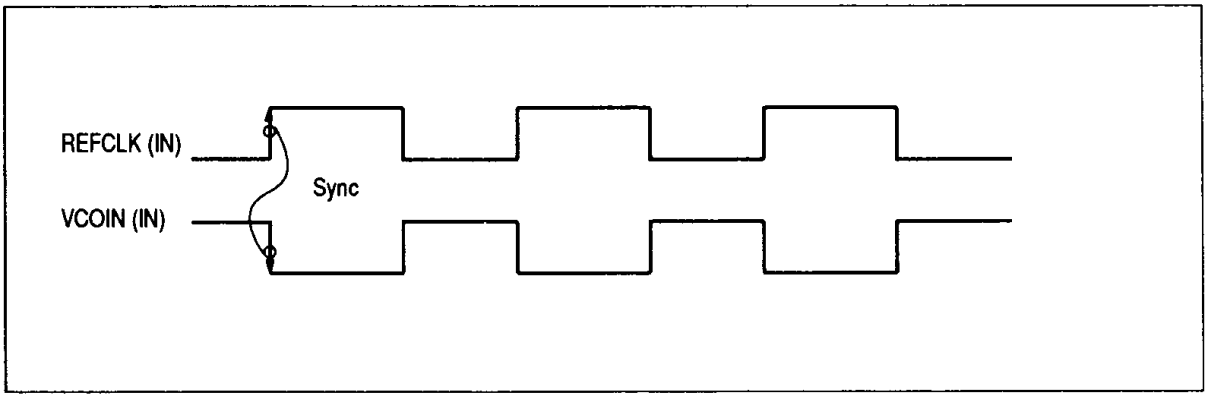
2-7 read code can be active Low or active High depending on the PSEL setting as shown below.

PSEL	2-7 Read Code	Applicable pin
H	Active High	RAWRD, DLYRD
L	Active Low	

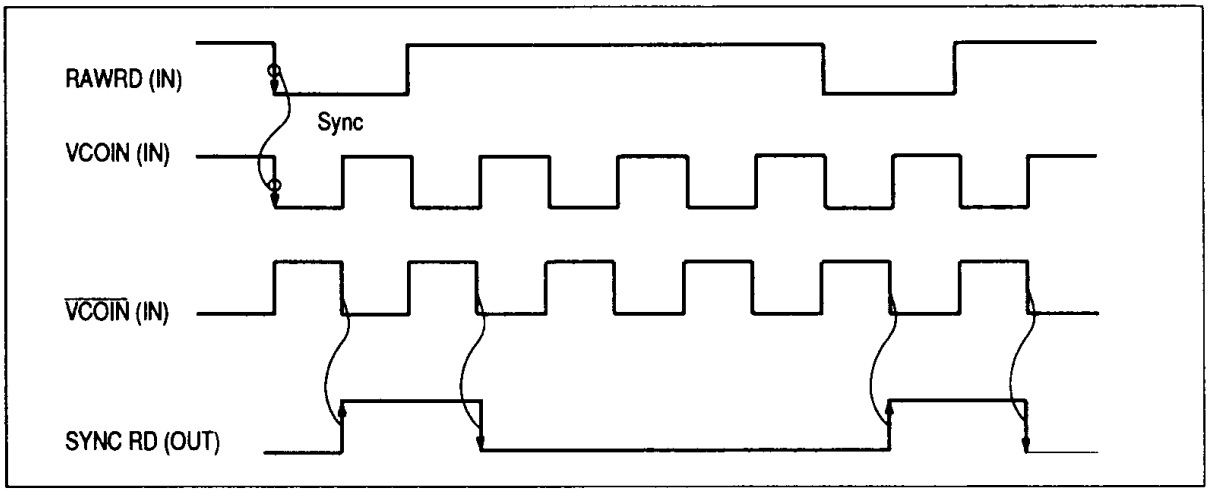
PLL Function



The PLL characteristics are changed through the READ GATE and $\overline{\text{PHASE SYNC}}$ signals



REFCLK (Reference clock) synchronization (PSEL: "L")

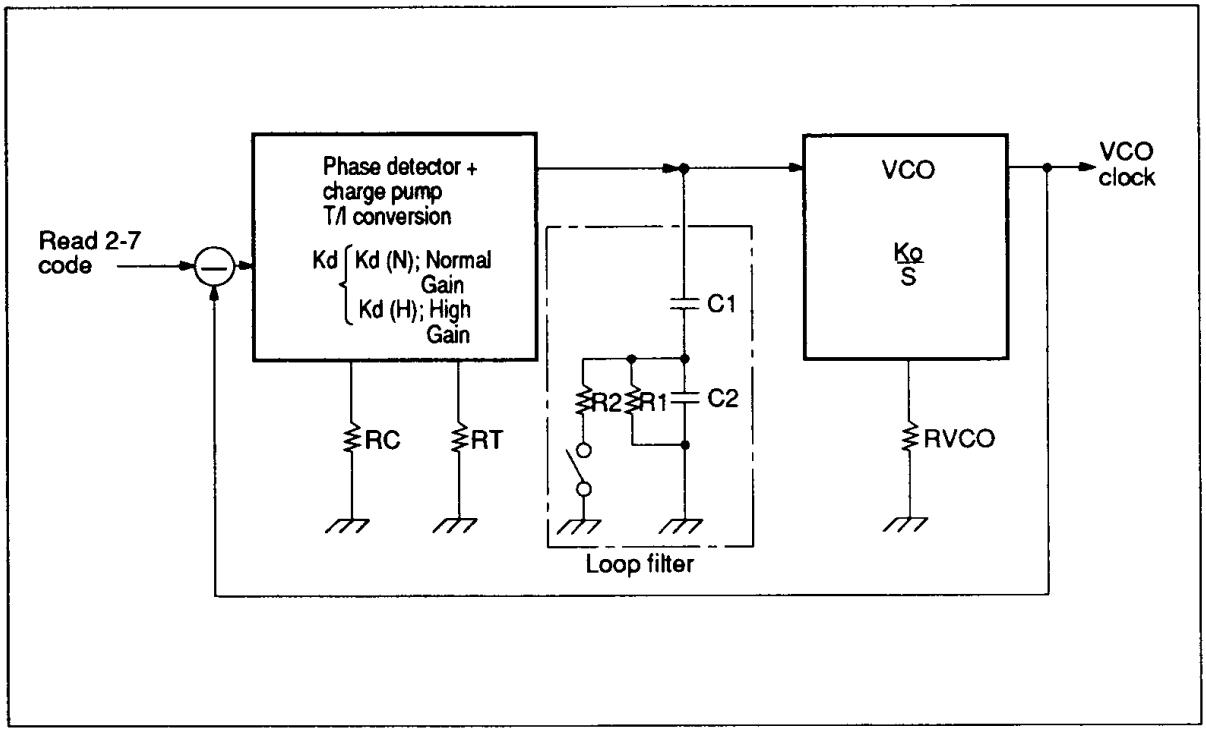


RAWRD (2-7 read code) synchronization (PSEL: "L")

PLL Constant Setting Procedure

In cases of High Gain and Normal Gain, the built-in PLL can independently set the damping rate of frequencies other than the characteristic frequency ωn. This is accomplished with the charge pump's output current switch function and the loop filter's constant switch funtion, both of which are internal to the PLL. Owing to a built-in sampling servo circuit, the characteristic frequency ωn and damping rate ζ can always be regulated, regardless of the pulse cycle (flux reversal cycle) of a 2-7 code read from a disk. These functions stabilize the PLL so that optimum response characteristics are attained.

The HD153011 internal PLL is shown below.



PLL Block Diagram

a. Kd [A/rad]
Gain of (phase detector + charge pump, T/I conversion)

Kd (N): Gain at Normal Gain
Kd (H): Gain at High Gain

b. F (S)
Transfer function of loop filter

$$F(S) = \frac{S \cdot (C1 + C2) \cdot R + 1}{S \cdot C1 \cdot (S \cdot C2 \cdot R + 1)}$$

Where R $\begin{cases} R1: & \text{At Normal Gain} \\ R1//R2: & \text{At High Gain} \end{cases}$

c. Ko [rad/S•V]
Gain of VCO

d. ωn
PLL characteristic frequency

$$\omega n\ (N) = \left(\frac{Kd\ (N) \cdot Ko}{C1}\right)^{1/2}\ [rad/s]: \text{Normal Gain}$$

$$\omega n\ (H) = \left(\frac{Kd\ (H) \cdot Ko}{C1}\right)^{1/2}\ [rad/s]: \text{High Gain}$$

e. ζ
PLL damping rate

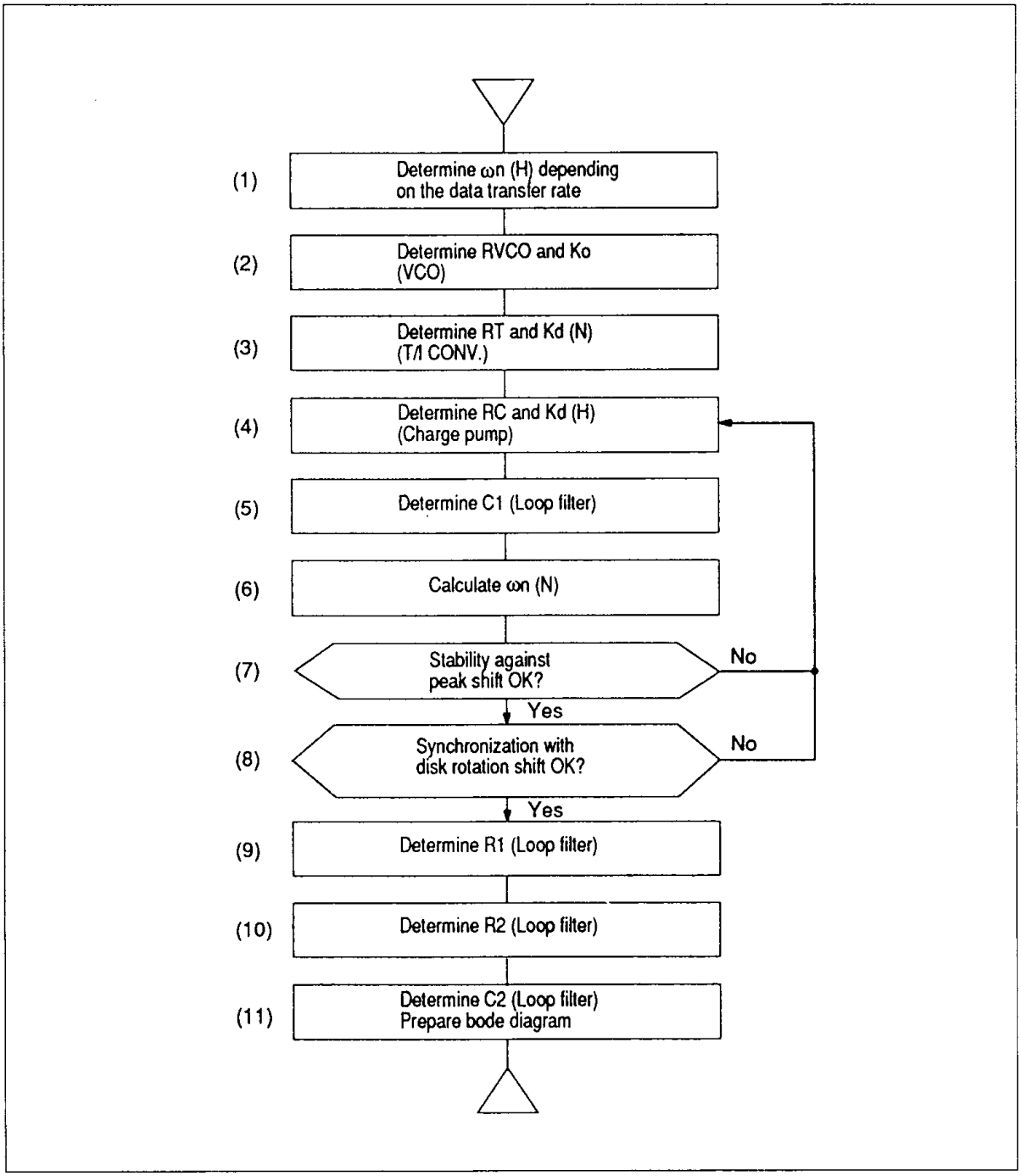
$$\begin{cases} \zeta\ (N) = \dfrac{(C1 + C2) \cdot R1}{2} \cdot \omega n\ (N): \text{Normal Gain} \\ \zeta\ (H) = \dfrac{(C1 + C2) \cdot (R1\ //\ R2)}{2} \cdot \omega n\ (H): \text{High Gain} \end{cases}$$

f. RC, RT
Resistors that determine phase detector gain.

g. C1, C2, R1, R2
Capacitors and resistors of the loop filter.

h. RVCO
A resistor that determines the VCO oscillation frequency and gain.

The values described in (a) to (h) and the PLL constant are determined according to the flowchart shown on the next page.



PLL Constant Setting Flowchart

1. Data transfer rate and High-Gain characteristic frequency ωn (H)

a. Determine the phase lead-in time Taq depending on the data transfer rate. Taq must be set High Gain period (6 bytes/8 bytes) or below.

[Example] If the lead-in is 5 bytes and if the data transfer rate is 15 Mbps, then

$$Taq = \frac{1}{15\ Mbps} \times 8\ bit \times 5\ Byte \cong 2.7\ \mu s$$

b. Determine the High–Gain characteristics frequency ωn (H) which is required to set the phase lead-in timer Taq. according to figure 1.
However, the ωn (H) should be set 1.17 times as much as that from figure 1, considering variations of ICs and parts.

[Example] When Taq = 2.7 μs, then ωn = 2.0 Mrad/s

ωn (H) = ωn x 1.17 = 2.0 x 1.17 = 2.34 [Mrad/s]

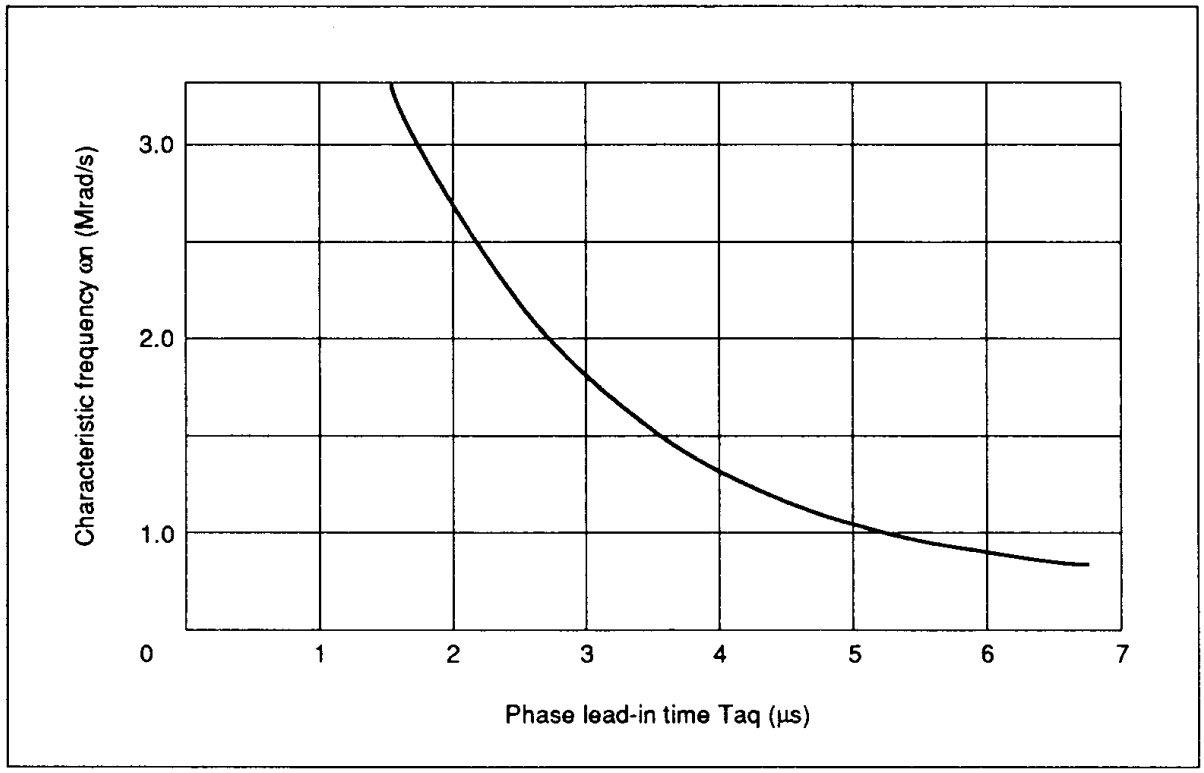


Figure 1 The Relation between Phase Lead-in Time Taq and Characteristic Frequency ωn

2. External resistor Rvco of VCO and gain Ko

a. The oscillator frequency fvco of the VCO must be set to twice the data transfer rate. Rvco is determined using the following expression.

$$Rvco(\Omega) = \frac{K1}{fvco\ (Hz)} \qquad (K1 = 9.0 \times 10^{10})$$

[Example] When the data transfer rate is 15 Mbps, the VCO oscillates at 30 MHz (15 MHz x 2). Therefore,

$$Rvco = \frac{9.0 \times 10^{10}}{3 \times 10^{7}} = 3\ [k\Omega]$$

b. Determine the gain Ko of the VCO.

$$Ko = \frac{K2}{\sqrt{Rvco}}\ [rad/s \cdot V] \qquad (K2 = 1.04 \times 10^{10})$$

[Example] When Rvco = 3 kΩ, then

$$Ko = \frac{1.04 \times 10^{10}}{\sqrt{3 \times 10^{3}}} = 190\ [Mrad/s \cdot V]$$

3. Determine the external resistor RT of the T/I converter and the normal gain phase detector gain Kd (N).

a. RT is determined by the transfer rate to optimize T/I converter operation.

$$RT\ (\Omega) = \frac{K3}{fvco\ (Hz)} \quad (K3 = 3.0 \times 10^{11})$$

[Example] When fvco = 30 MHz, then

$$RT = \frac{3.0 \times 10^{11}}{3 \times 10^{7}} = 10[k\Omega]$$

b. Determine the Normal Gain phase detector gain Kd (N.)

$$Kd\ (N) = \frac{K4}{\pi \cdot RT}\ [A/rad] \qquad (K4 = 0.28)$$

[Example] When RT = 10 kΩ, then

$$Kd\ (N) = \frac{0.28}{\pi \times 10 \times 10^{3}} = \frac{28}{\pi}\ [\mu A/rad]$$

4. Determine the external resistance RC and phase detector gain Kd (H).

a. RC determines the charge pump output current. It must be set within the following range.

$$250\ (\Omega) \leq Rc \leq 1\ [k\Omega]$$

RC should first be set to 470 Ω, and changed after process (7) or (8).

b. Determine the phase detector gain Kd (H) at High Gain.

$$Kd\ (H) = \frac{0.90}{8\ \pi\ Rc}\ [A/rad]$$

[Example] When Rc = 470 Ω, then

$$Kd\ (H) = \frac{239}{\pi}\ [\mu A/rad]$$

5. Determine C1 of the loop filter.

$$C1 = \frac{Ko \cdot Kd\ (H)}{\omega n\ (H)^2}$$

[Example] When Ko = 190 Mrad/s•V,
Kd (H) = 239/π [μA/rad],
When ωn (H) = 2.34 Mrad/s, then

$$C1 = \frac{190 \times 10^{6} \times 239 \times 10^{-6}}{\pi \times (2.34 \times 10^{6})^2}$$

$$\cong 2640 \rightarrow 2700\ [pF]$$

6. Determine the characteristic frequency ωn (N) at Normal Gain.

$$\omega n\ (N) = \sqrt{\frac{Ko \cdot Kd\ (N)}{C1}}$$

[Example] When Ko = 190 Mrad/s• V, Kd (N) = 28/π [μA/rad], C1 = 2700 pF,

$$\omega n\ (N) = \sqrt{\frac{190 \times 10^{6} \times 28 \times 10^{-6}}{\pi \times 2700 \times 10^{-12}}}$$

$$= 792\ [Krad/s]$$

7. Stability against peak shift

Determine if the following inequality holds using the step function response.

$$1 - (1 - \omega n\ (N)\ t)\ \exp(-\omega n\ (N)\ t) \leq K5$$

(Determined with respect to the specification.)

$$\text{Where } K5 = \frac{\text{VCO shift (rad) or (ns)}}{\text{Peak shift (rad) or (ns)}}$$

If the inequality does not hold, return to (4) and reduce RC.

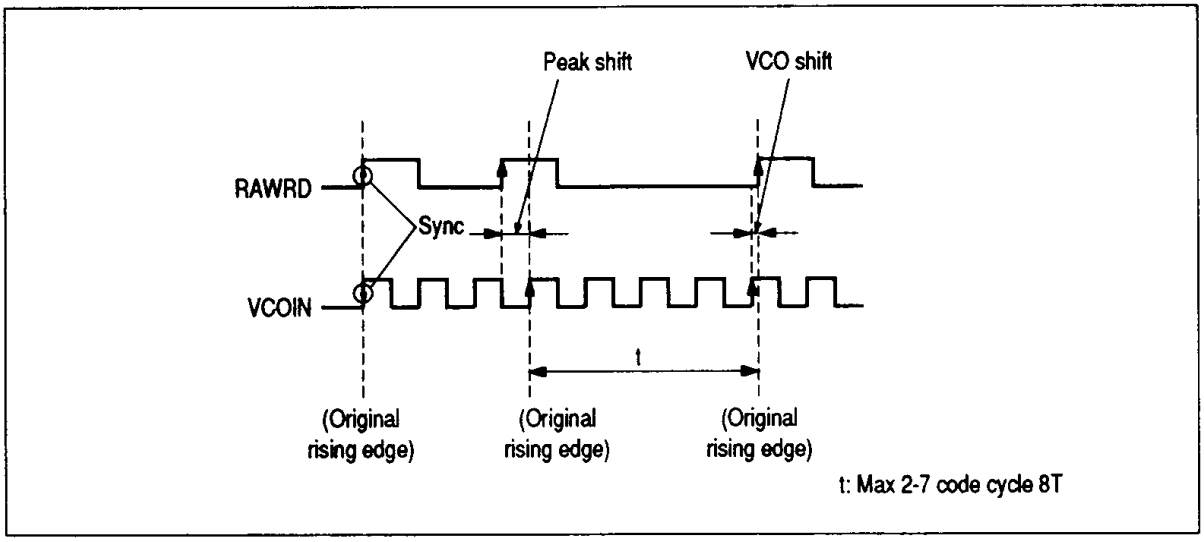
[Example] The VCO shift must be 4 ns or less when the data transfer rate is 15 Mbps and the peak shift is 10 ns. Therefore, the followings are obtained,

$$K5 = 0.4 \quad t = \frac{1}{30\ MHz} \times 8 = 267\ ns$$

Then when ωn (N) = 792 Krad/s is assigned,

$1 - (1 - 792 \times 10^{3} \times .267 \times 10^{-9}) \exp(-792 \times 10^{3} \times 267 \times 10^{-9}) = 0.36$

can be obtained, providing the inequality. At this time, the VCO is shifted by 3.6 ns.

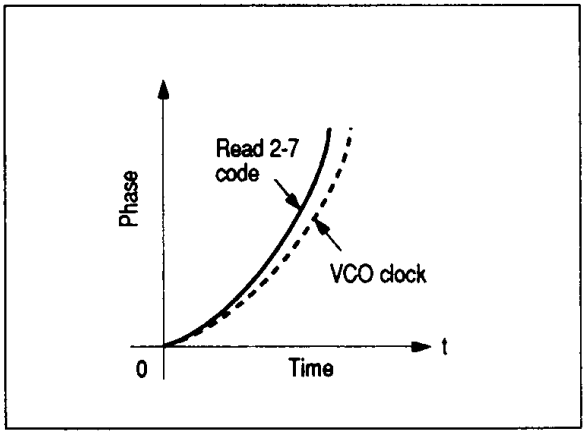


8. Synchronization with disk rotation change

With Normal Gain, the VCO must synchronize with the disk rotation change. Suppose that the change in disk rotation is approximately linear within a sector. If disk rotation speed changes ω% during the time T [s] in which one sector passes, the following inequality must hold in order for the VCO clock synchronization error to be v [s] or less.

$$\omega\,(N) > \sqrt{\frac{0.01 \times \omega}{v \cdot T}}$$

If the inequality is not valid, return to (4) and reexamine with RC increased.



[Example] Rotation change within one sector (one track = 32 sectors): 0.5%
Phase difference: 1 ns or less
When the VCO clock synchronizes with the above conditions, the inequality holds.

$$\omega\,(N) = 792[\text{Krad/s}] > \sqrt{\frac{0.01 \times 0.5}{1 \times 10^{-9} \times 520 \times 10^{-6}}}$$
$$= 98\ [\text{Krad/s}]$$

9. Determine R1 of the loop filter.

The damping rate ζ (N) with Normal Gain is set at 1.00 in depending on the stability of a circuit. At this time, R = R1 and

$$R = R1 = \frac{2 \cdot \zeta\,(N)}{(C1 + C2) \cdot \omega n\,(N)}$$

Considering C1 ≫ C2, $R1 \cong \dfrac{2 \cdot \zeta\,(N)}{C1 \cdot \omega n\,(N)}$

[Example] When C1 = 2700 [pF],
ωn (N) = 792 [Krad/s]

$$R1 = \frac{2}{2700 \times 10^{-12} \times 792 \times 10^{3}}$$
$$= 935 \rightarrow 910\ [\Omega]$$

10. Determine R2 of the loop filter.

The High Gain damping rate ζ (H) is set at 0.72, depending on the high synchronization capability of a circuit. At this time, R = R1/R2 and

$$R = \left(\frac{1}{R2} + \frac{1}{R1}\right)^{-1} = \frac{2 \cdot \zeta\,(H)}{C1 \cdot \omega n\,(H)}$$

$$R2 = \left(\frac{C1 \cdot \omega n\ (H)}{2 \cdot \zeta\ (H)} - \frac{1}{R1} \right)^{-1}$$

[Example] When C1 = 2700 [pF],
$\omega(H)$ = 234 [Mrad/s], R1 = 910 [Ω]

$$R2 = \left(\frac{2700 \times 10^{-12} \times 2.34 \times 10^{6}}{2 \times 0.72} - \frac{1}{910} \right)^{-1}$$
$$= 304 \rightarrow 300\ [\Omega]$$

11. Prepare the bode diagram and determine C2 of the loop filter

a. Bode diagram preparation
The Open-loop transfer function G (S) is

$$G(S) = \frac{Ko \cdot Kd}{C1} \cdot \frac{1}{S^2} \cdot \frac{1 + S \cdot (C1 + C2) \cdot R}{1 + S \cdot C2 \cdot R}$$

Therefore, a bode diagram is drawn with the following proceedure.

i. Draw a – 40 dB/dec straight line through (ωn, 0).
ii. Draw a – 20 dB/dec straight line through $\omega = 1/(C1 + R2) \cdot R$.
iii. Determine the unity gain frequency $\omega 0$ (N) and $\omega 0$ (H) from the graph.

b. Determine C2 of the loop filter.
C2 reduces the gain of the circuit in the high-frequency area. The break frequency $\omega 2$, which lags behind – 40 dB/dec, is calculated

$$\omega 2 = \frac{1}{C2 \cdot R}$$

as

If $\omega 2$ is large, VCO is apt to synchronize with a high-frequency component (jitter etc.), and if $\omega 2$ is small, the circuit phase margin is reduced, and secondary approximate calculation error is

$$C2 = \frac{0.65}{C1 \cdot R1^2 \cdot \omega o(N)^2}$$

increased. Therefore, C2 must be set around the value shown below.

ωo (N): Unity gain frequency at Normal Gain

$$C2 = \frac{1}{2700\ pF \times 910^2 \times (1.55 \times 10^6)^2}$$
$$= 121\ pF \rightarrow 120\ [pF]$$

[Example] When ωo (N) = 1.55 [Mrad/s], Continue preparing the bode diagram (process (a)).
C2 lags to – 40 dB/dec ((a) – (iv) $\omega = 1/C2R$

$$R = \begin{cases} R1\text{: Normal Gain} \\ R1//R2\text{: High Gain} \end{cases}$$

Note:"R" in item (11) indicates that the value differs between High Gain and Normal Gain.

[Example] Figure 2 is a bode diagram made according to the above procedure, using the constant that corresponds to the maximum data transfer rate of 15 Mbps.

Transfer Rate	R_{VCO}	R_C	R_T	C_1	C_2	R_1	R_2
10 Mbps	4.5 kΩ	470 Ω	15 kΩ	4700 pF	220 pF	910 Ω	240 Ω
12.5 Mbps	3.6 kΩ	470 Ω	12 kΩ	3300 pF	150 pF	910 Ω	270 Ω
15 Mbps	3.0 kΩ	470 Ω	10 kΩ	2700 pF	120 pF	910 Ω	300 Ω

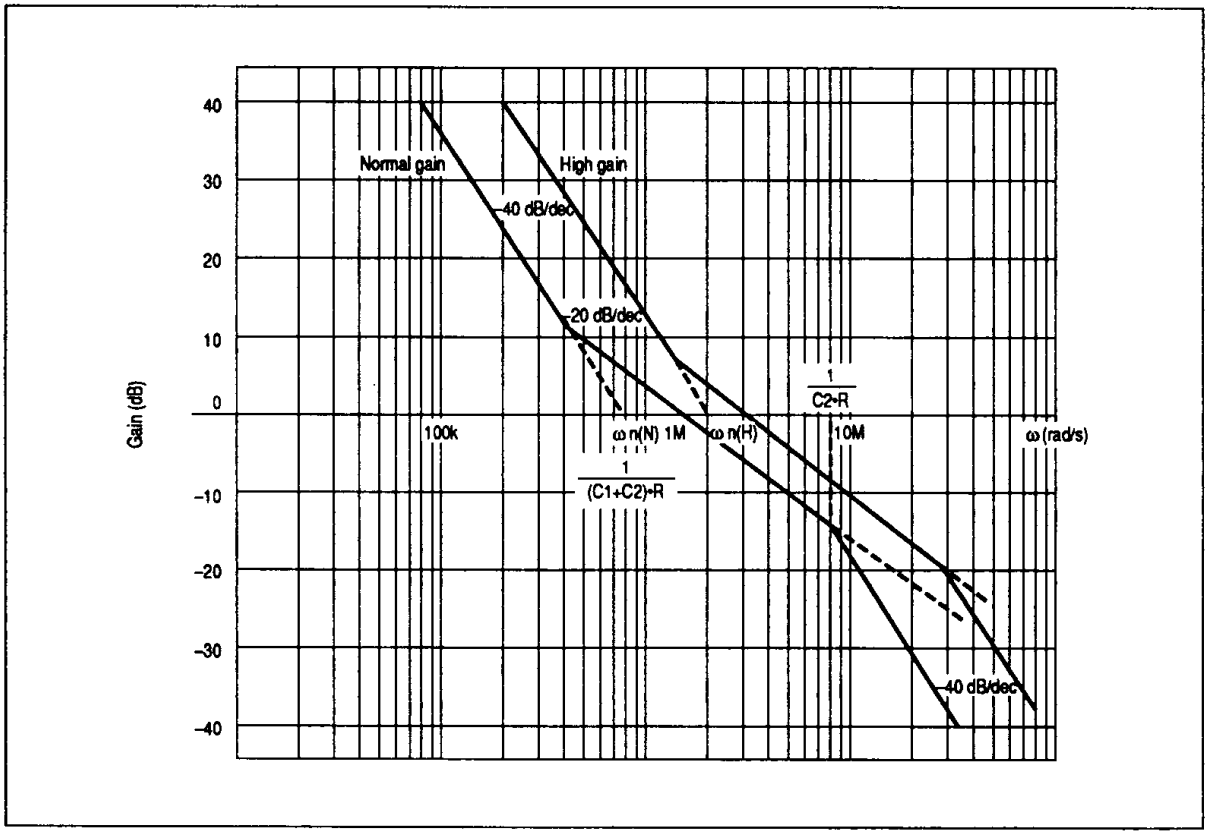


Figure 2 Bode Diagram Example when Maximum Transfer Rate is 15 Mbps

Table 4 Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit	Applicable Pin
Supply voltage	Vcc	7	V	AVcc, DVcc
Input Voltage	V_I	5.5	V	*1
Output Voltage	Vo	5.5	V	*2
Current dissipation	P_T	550	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	−55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes: *1 VCOIN, RAWRD, REFCLK, READ GATE, DLYRD, $\overline{\text{VCOIN}}$, RDSEL, $\overline{\text{RESET}}$, EXSYNC IN, MODE SEL 0, MODE SEL 1, MODE SEL 2, AME, AMSEL, LCLK2, LCLK1, NCLK, ECLK1, TABSEL, $\overline{\text{WRPN}}$, NRZWD, WRITE GATE, PHASE SYNC, PSEL

*2 SYNCRD, $\overline{\text{SYNC DETECT}}$, LATE WG, AMF, 2-7WD, CLKOUT, NRZRD, RWCLK, VCOOUT, $\overline{\text{VCOOUT}}$

Output Voltage of Three-state Output Pin (Disable)

Item	Symbol	Rating	Unit	Applicable Pin
Output voltage (high level)	Vo (off)	5.5	V	NRZRD, AMF

Note: AMF is a three-state output only during a 7-2 illegal pattern

Table 5 Electrical Characteristics

DC Characteristics (T_a = 0 to + 70°C unless otherwise specified, V_{CC} = 5.0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin
Supply voltage	V_{CC}	4.75	5.0	5.25	V		DVcc, AVcc
Input voltage	V_{IH}	2.0			V		*1
	V_{IL}			0.8	V		
Input current	I_{IH}			20	μA	V_{CC} = 5.25 V, V_I = 2.7 V	
	I_{IL}			-400	μA	V_{CC} = 5.25 V, V_I = 0.4 V	
Output voltage	V_{OH}	2.7			V	V_{CC} = 4.75 V, I_{OH} = -400μA	*2
	V_{OL}			0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA	
Output short current	I_{OS}	-20		-120	mA	V_{CC} = 5.25 V	
Input clamp voltage	V_{IK}			-1.5	V	V_{CC} = 4.75 V, I_{IN} = -18 mA	*1
Off-state output current	I_{OZH}			20	μA	V_{CC} = 5.25 V, V_O = 2.7 V	NRZRD
	I_{OZL}			-20	μA	V_{CC} = 5.25 V, V_O = 0.4 V	
Current dissipation	I_{CC}		65	100	mA	V_{CC} = 5.25 V, Max transfer rate = 15 Mbps	DVcc, AVcc
Charge pump output current	I_{CI}		-1.9		mA	V_{CC} = 5.0 V, Vcpout = 2.15 V, R_C = 470Ω	CPOUT
	I_{CD}		1.9		mA	V_{CC} = 5.0 V, Vcpout = 2.15 V, R_C = 470Ω	
T/I conversion output current	I_{TI}		-14		μA	V_{CC} = 5.0 V, Vcpout = 2.15 V, Input signal phase difference = + π/2[rad], R_T = 10kΩ when transfer rate = 15 Mbps	CPOUT
	I_{TD}		14		μA	V_{CC} = 5.0 V, Vcpout = 2.15 V, Input signal phase difference = + π/2[rad], R_T = 10kΩ when transfer rate = 15 Mbps	
	I_{TO}		0		μA	V_{CC} = 5.0 V, Vcpout = 2.15 V, Input signal phase difference = + π/2[rad], R_T = 10kΩ when transfer rate = 15 Mbps	

Notes: *1. VCOIN, RAWRD, REFCLK, READ GATE, DLYRD, $\overline{\text{VCOIN}}$, RDSEL, $\overline{\text{RESET}}$, EXSYNC IN, MODE SELO, MODE SEL 1, MODE SEL 2, AME, AMSEL, LCLK2, LCLK1, NCLK, $\overline{\text{ECLK1}}$, $\overline{\text{TABSET}}$, $\overline{\text{WRPN}}$, NRZWD, WRITE GATE, $\overline{\text{PHASE SYNC}}$, PSEL

*2. SYNCRD, $\overline{\text{SYNC DETECT}}$, LATE WG, AMF, 2-7WD, CLKOUT, NRZRD, RWCLK, $\overline{\text{VCOOUT}}$, VCOOUT

AC Characteristics (1) (V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Remarks
Data transfer rate				15	Mbps			
$\overline{\text{Reset}}$ time	t_{RS}	50			ns		$\overline{\text{RESET}}$	Figure 3
NRZ read data set-up time	t_{SNR}	25			ns	Max transfer rate 15 Mbps	NRZRD	Figure 4
NRZ read data hold time	t_{HNR}	25			ns	Max transfer rate 15 Mbps		
Input read data pulse width	t_W	16	33	50	ns	Max transfer rate 15 Mbps	RAWRD	Figure 5
Decode time	t_{DD}		12		VCO clock			Figure 6
Write clock to read clock	t_{WTR}			5	VCO clock		RWCLK	Figure 7
Read clock to write clock	t_{RTW}			5	REFCLK			
NRZ write data set-up time	t_{SNW}	10			ns		NRZWD	Figure 8
NRZ write data hold time	t_{HNW}	10			ns		$\overline{\text{REFCLK}}$	
Encode time	t_{ED}		12		REFCLK	No write precomp.		Figure 9
			21			Write precomp.		

Table 5 Electrical Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Remarks
Write gate to late write gate	t_{LWG}	30		32	REFCLK			Figure 10
	t_{RWG}			20	ns			
Address mark write enable time	t_{AML}			2	REFCLK			Figure 11
Address mark write disable time	t_{AMH}			2				DC erase
Address mark detection time	t_{AMR}	30		32	REFCLK			Figure 12
Address mark detection rise time	t_{AFH}			30	ns			DC erase
Address mark detection fall time	t_{AFL}			30	ns			
$\overline{\text{SYNC DETECT}}$ fall time	t_{SDO}		1		RAW READ DATA		$\overline{\text{SYNC DETECT}}$	Figure 13
$\overline{\text{SYNC DETECT}}$time hard-selector mode)	t_{SDH}		26		RAW READ DATA	Set to 6 bytes		
			32			Set to 8 bytes		
$\overline{\text{SYNC DETECT}}$ fall time	t_{SDD}		8		RAW READ DATA		$\overline{\text{SYNC DETECT}}$	Figure 14
$\overline{\text{SYNC DETECT}}$ time (soft-sector mode)	t_{SDS}		26		RAW READ DATA	Set to 6 bytes		
			32			Set to 8 bytes		
Internal delay E2	t_{E2}		–5		ns			Figure 15
E1	t_{E1}		–3		ns		Delay with	
L1	t_{L1}		3		ns		respect to	
L2	t_{L2}		5		ns		NCLK	
REFCLK duty		40	50	60	%			
Address mark write delay time	t_{AID}		12		REFCLK	No write precomp.		Figure 16
			21			write precomp.		7-2 illegal
Address mark detection rise time	t_{AIL}			14	VCOCLK			Figure 17 7-2 illegal
REFCLK rise time	t_{rR}			7	ns	REFCLK		Figure 18
REFCLK fall time	t_{fR}			7	ns			

AC Characteristics (2) (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
VCO maximum oscillation frequency		50			MHz	
VCO center frequency		28.5	30	31.5	MHz	Transfer rate: 15 Mbps
VCO upper-limit clamp frequency			45		MHz	
VCO lower-limit clamp frequency			15		MHz	
VCO gAIN			190		Mrad/S·V	
						Transfer rate: 15 Mbps, R_{VCO}: 3 kΩ
Phase detector gain		239/π			μA/rad	15 Mbps High Gain R_C = 470 Ω
		28/π			μA/rad	15Mbps Normal Gain R_T = 10 kΩ
Window center transaction			3.0		ns	15Mbps No Adjusting
			1.0			Adjusting
Phase lead-in time	taq			3.2	μs	15 Mbps, Under recommended constants
Capture range		± 10			%	15 Mbps High Gain
Lock range		± 10			%	15 Mbps Normal Gain

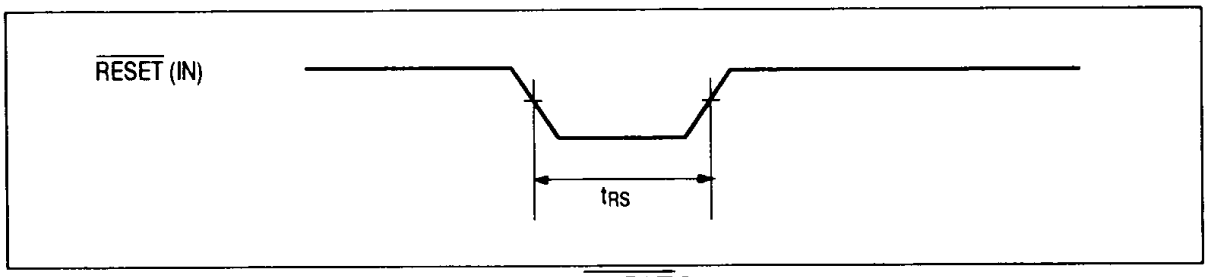


Figure 3 $\overline{\text{RESET}}$ Input

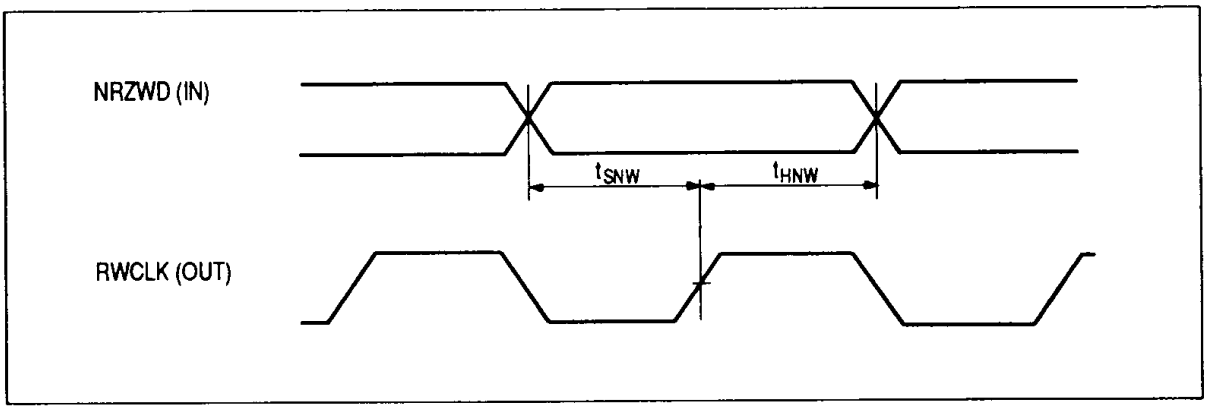


Figure 4 NRZ READ DATA Output

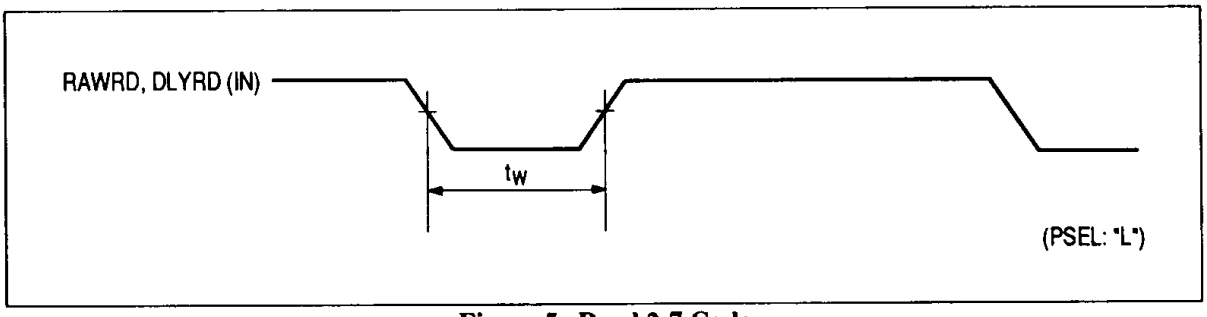


Figure 5 Read 2-7 Code

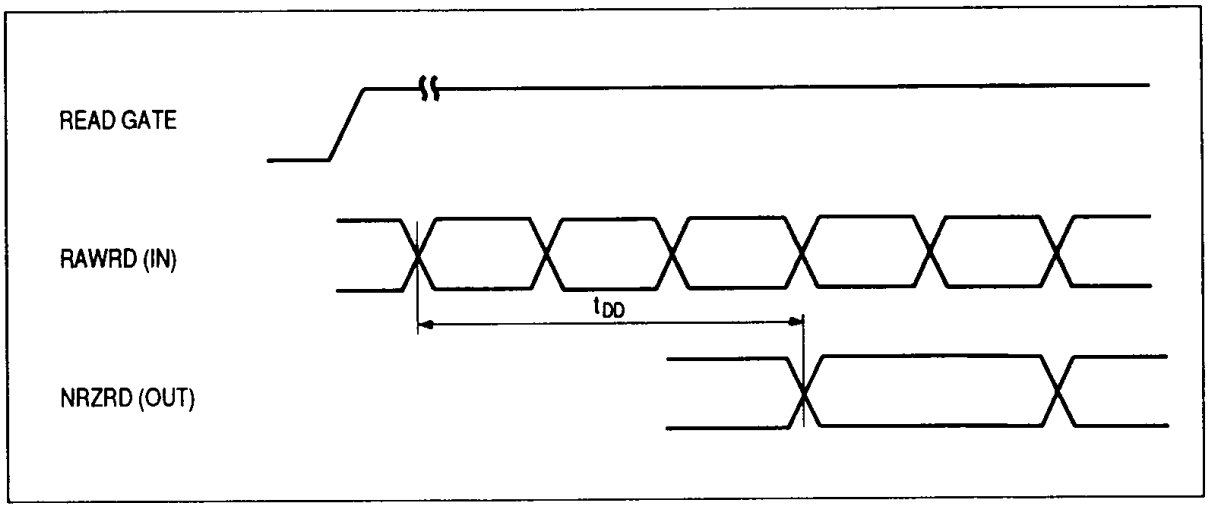


Figure 6 Decode

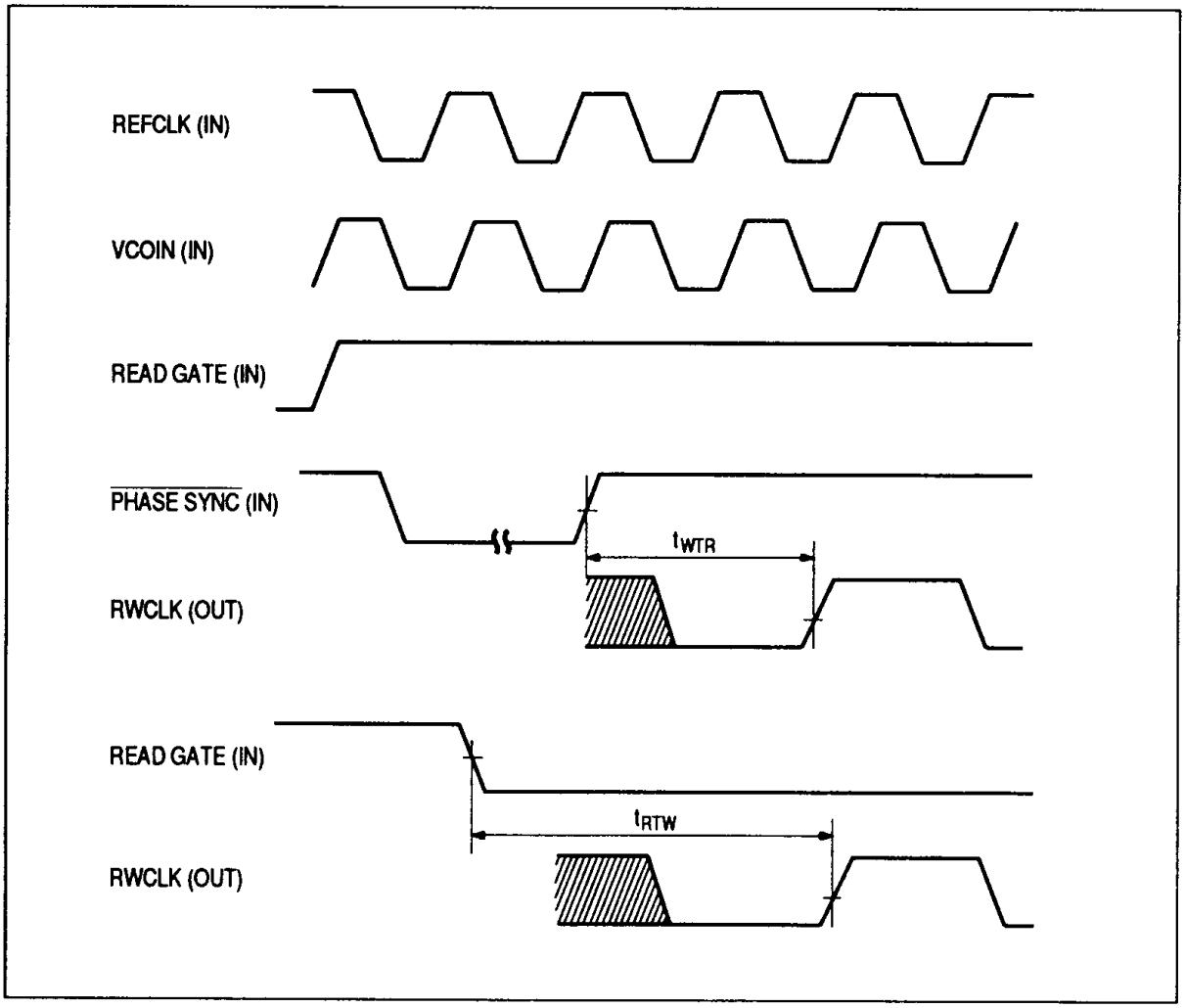


Figure 7 READ WRITE CLOCK

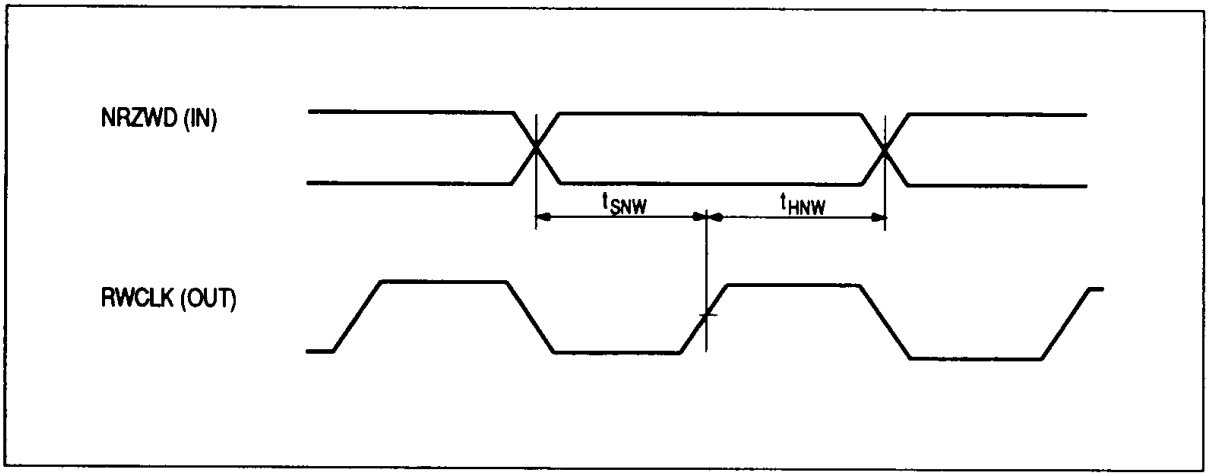


Figure 8 NRZ WRITE DATA Input

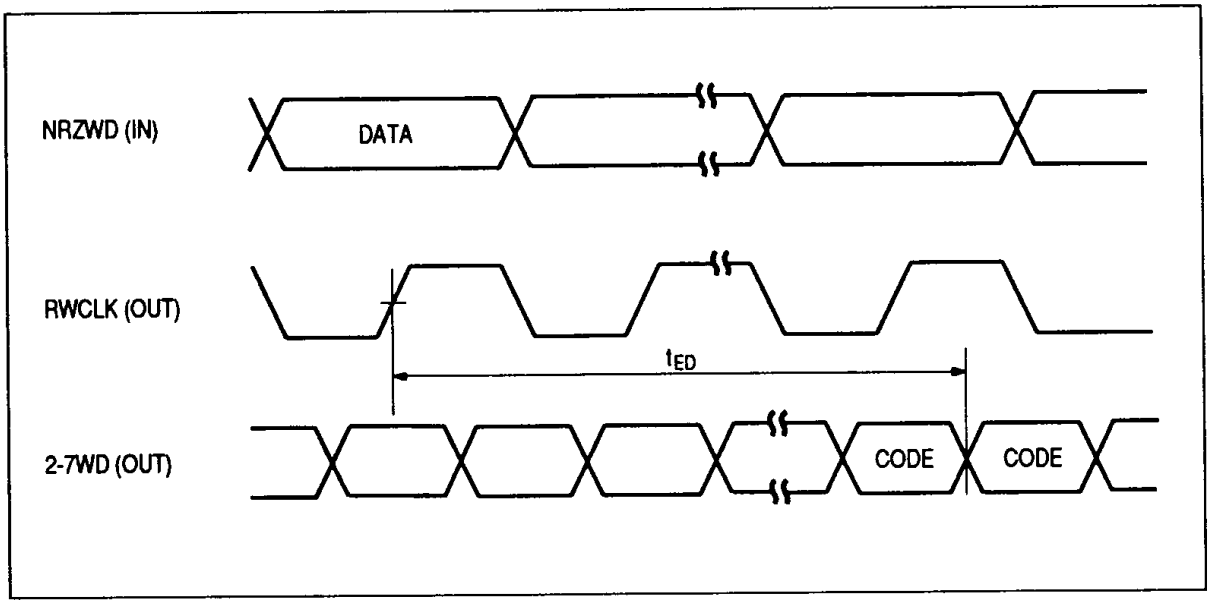


Figure 9 Encode

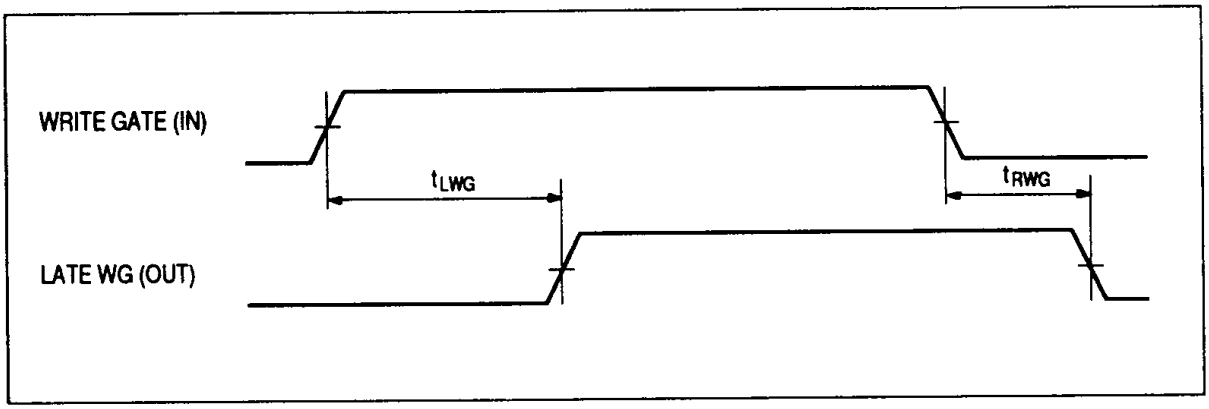


Fig 10 Late Write Gate

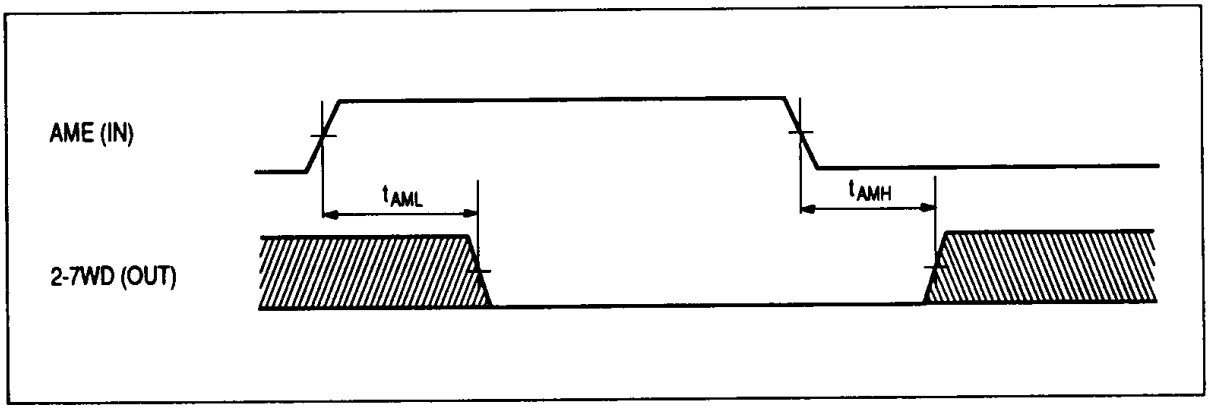


Figure 11 Address Mark Write (DC Erase)

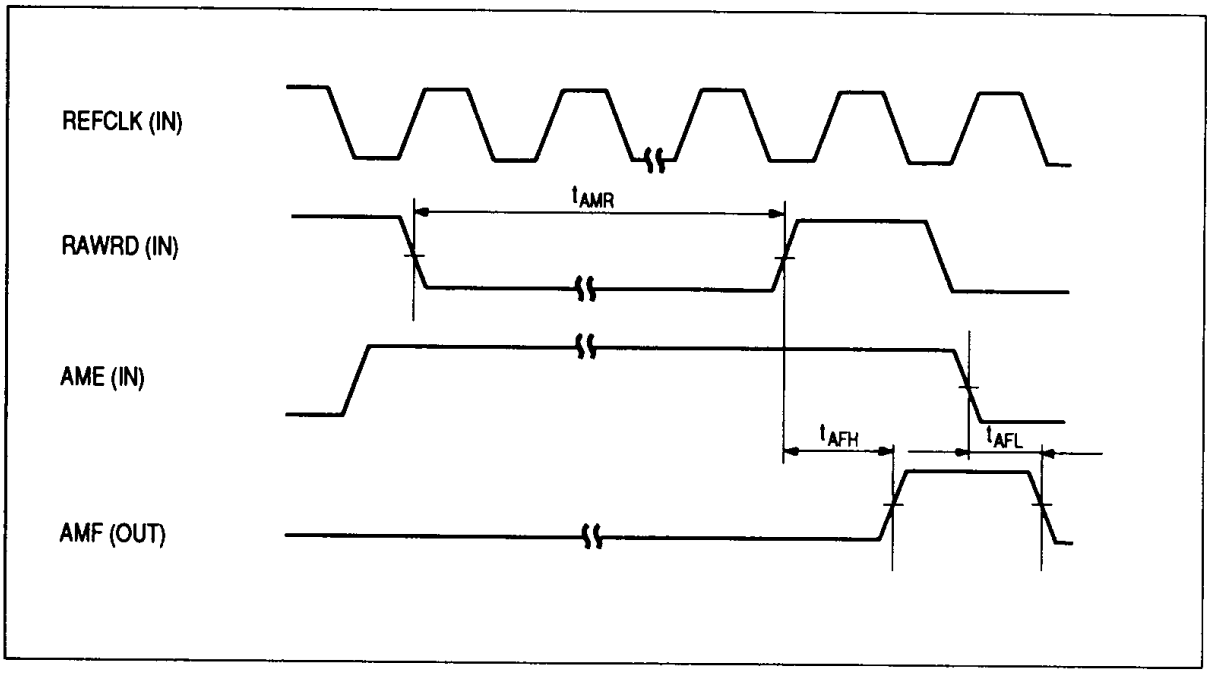


Figure 12 Address Mark Detection (DC Erase)

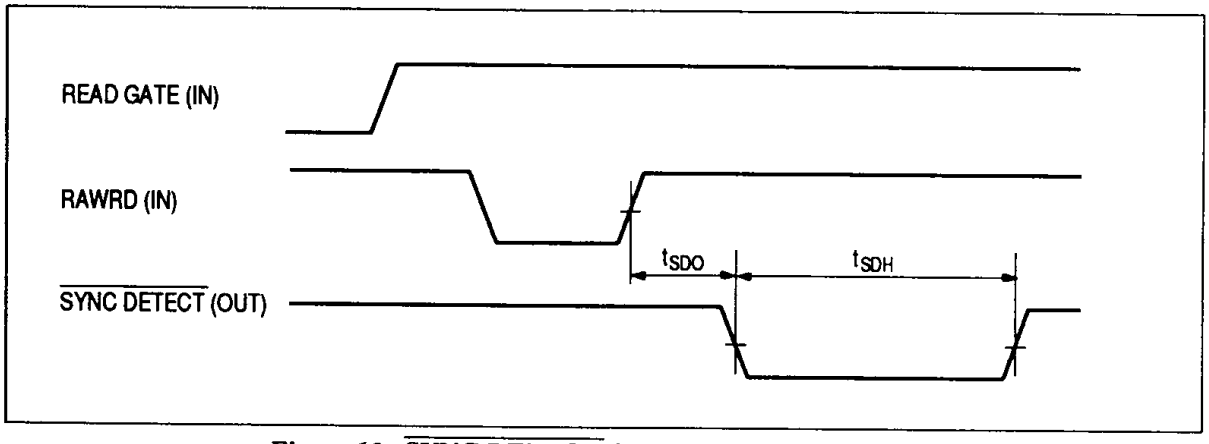


Figure 13 $\overline{\text{SYNC DETECT}}$ Output (Hard-sector Mode)

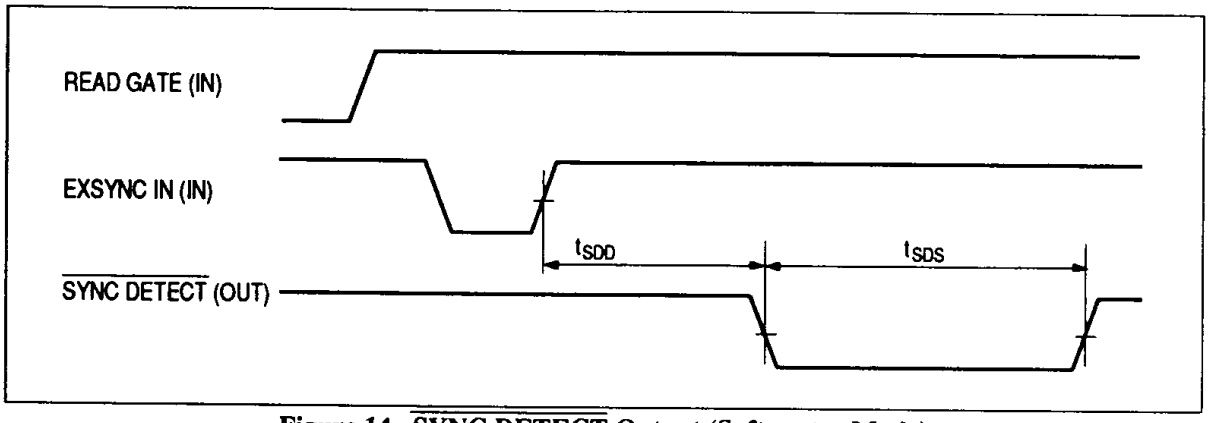


Figure 14 $\overline{\text{SYNC DETECT}}$ Output (Soft-sector Mode)

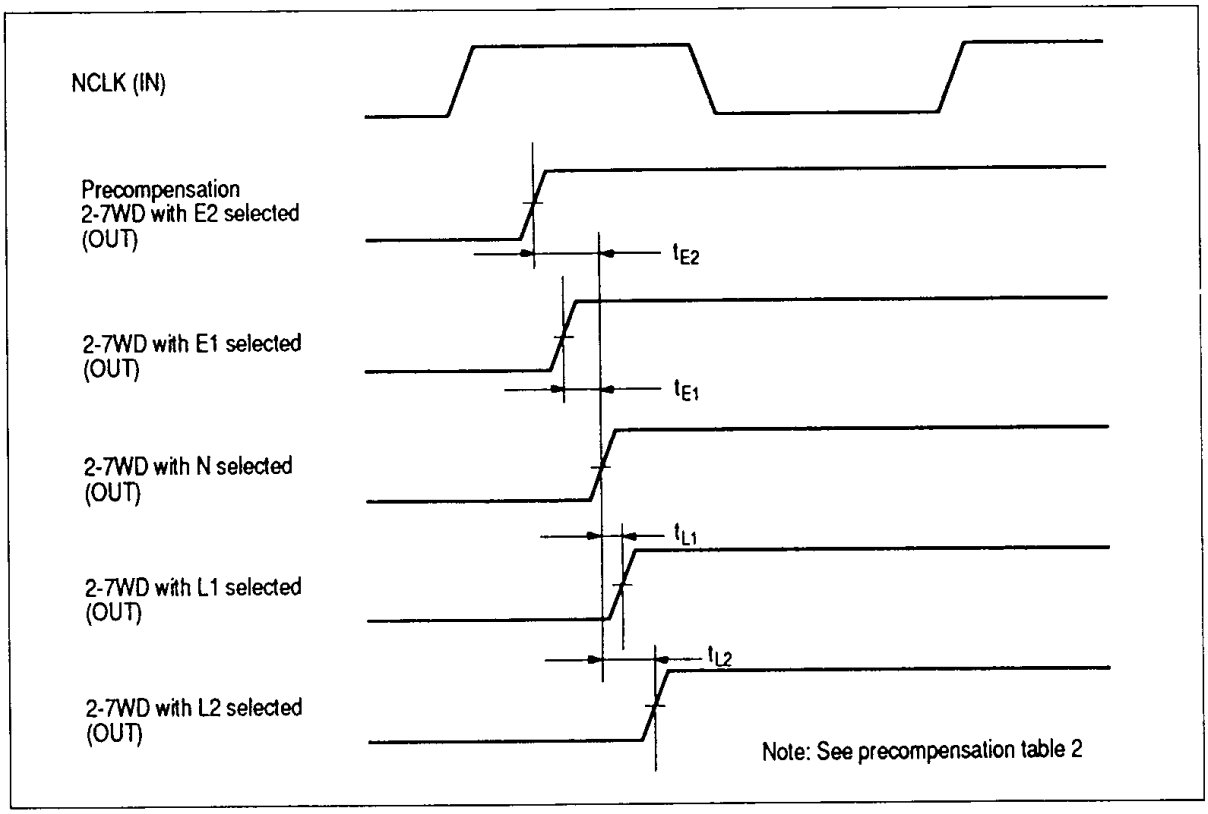


Figure 15 Write Precompensation in Internal Gate Delay Mode

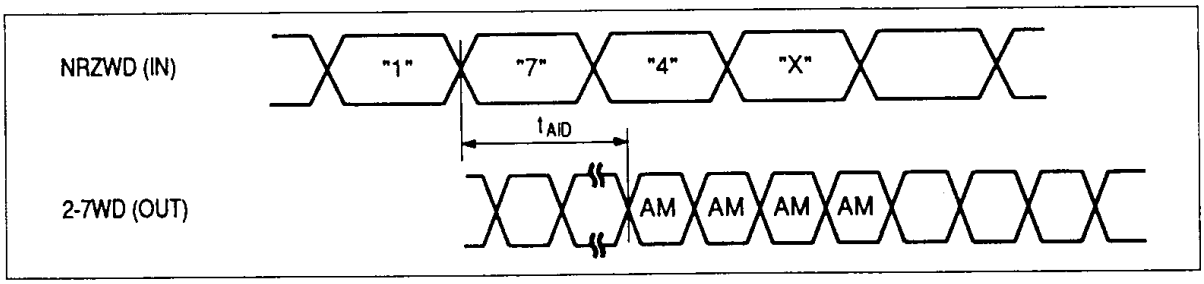


Figure 16 Address Mark Write (7-2 Illegal)

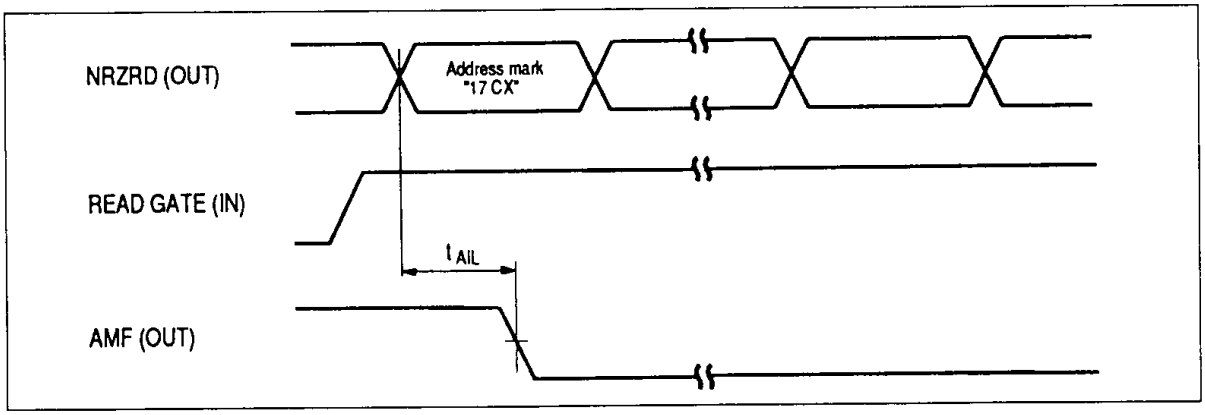


Figure 17 Address Mark Detection (7-2 Illegal)

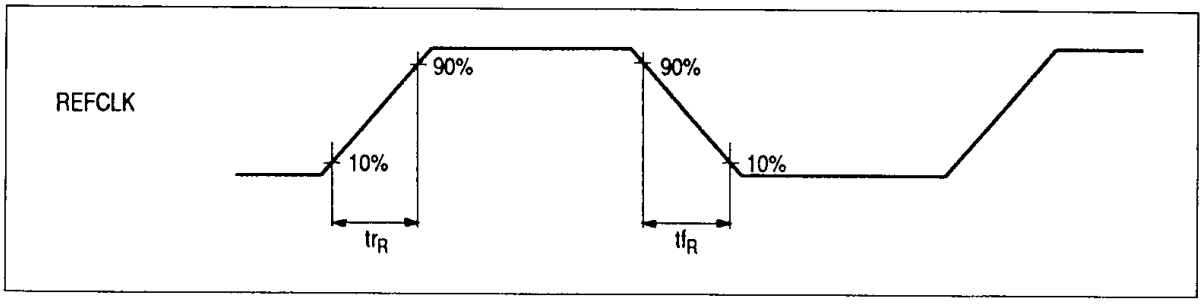


Figure 18 Reference Clock Rise and Fall Time

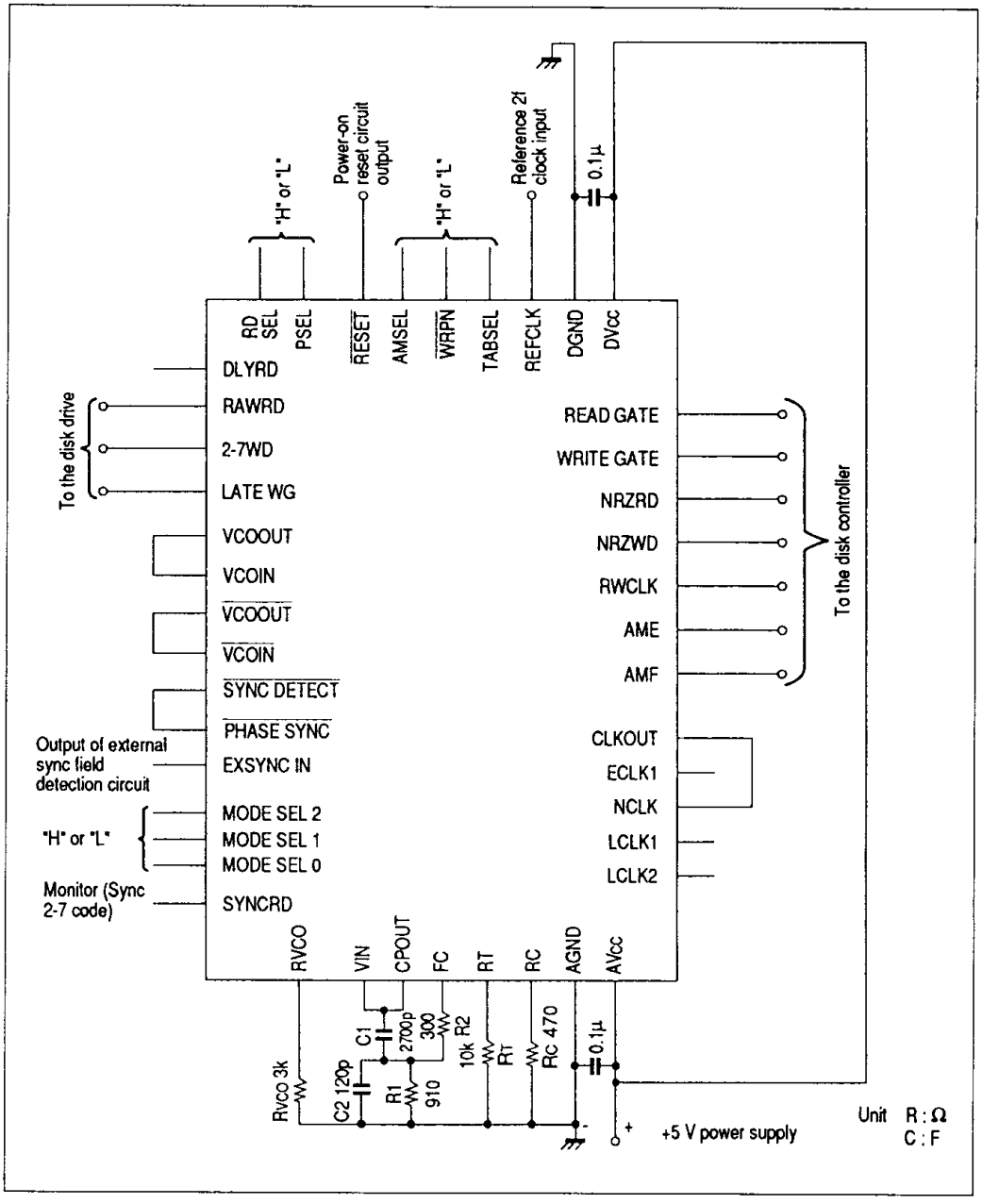
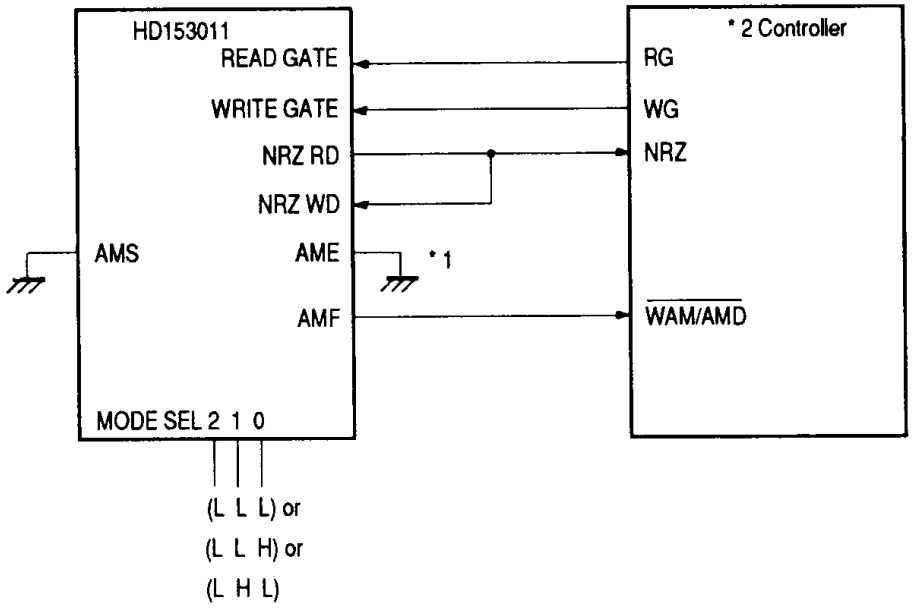


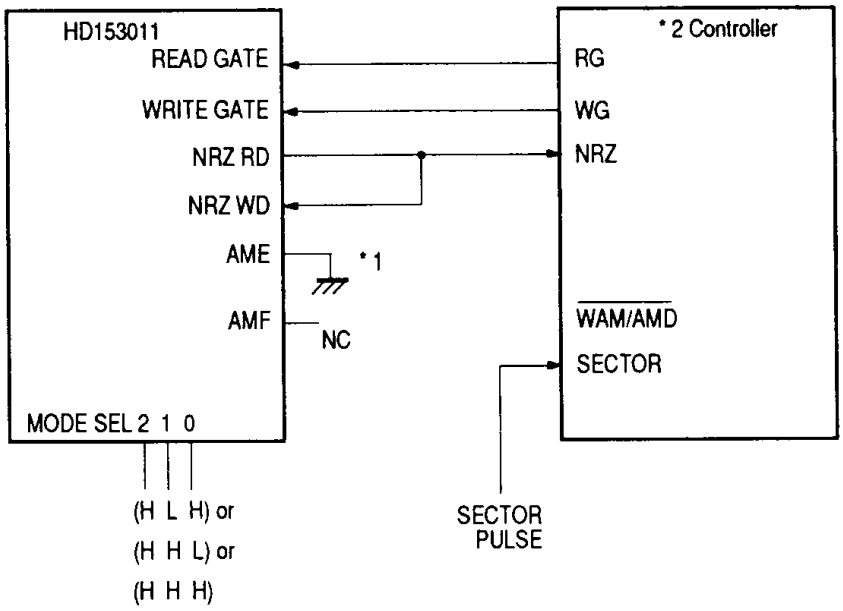
Figure 19 External Circuit Connection Example (15 Mbps)

HD153011 and Controller Connection Example

- Soft-sector mode (7-2 illegal pattern method) using internal sync pattern detection circuit



- Hard-sector mode



*1 AME should be held Low for hard-sector and soft-sector modes (7-2 illegal pattern method).

*2 Can connect directly with Adaptek AIC-6110, Shiras Logic CL-SH260/250 or equivalent controllers. This product supports soft-sector mode (DC Erase method). Controller connection methods should be investigated.

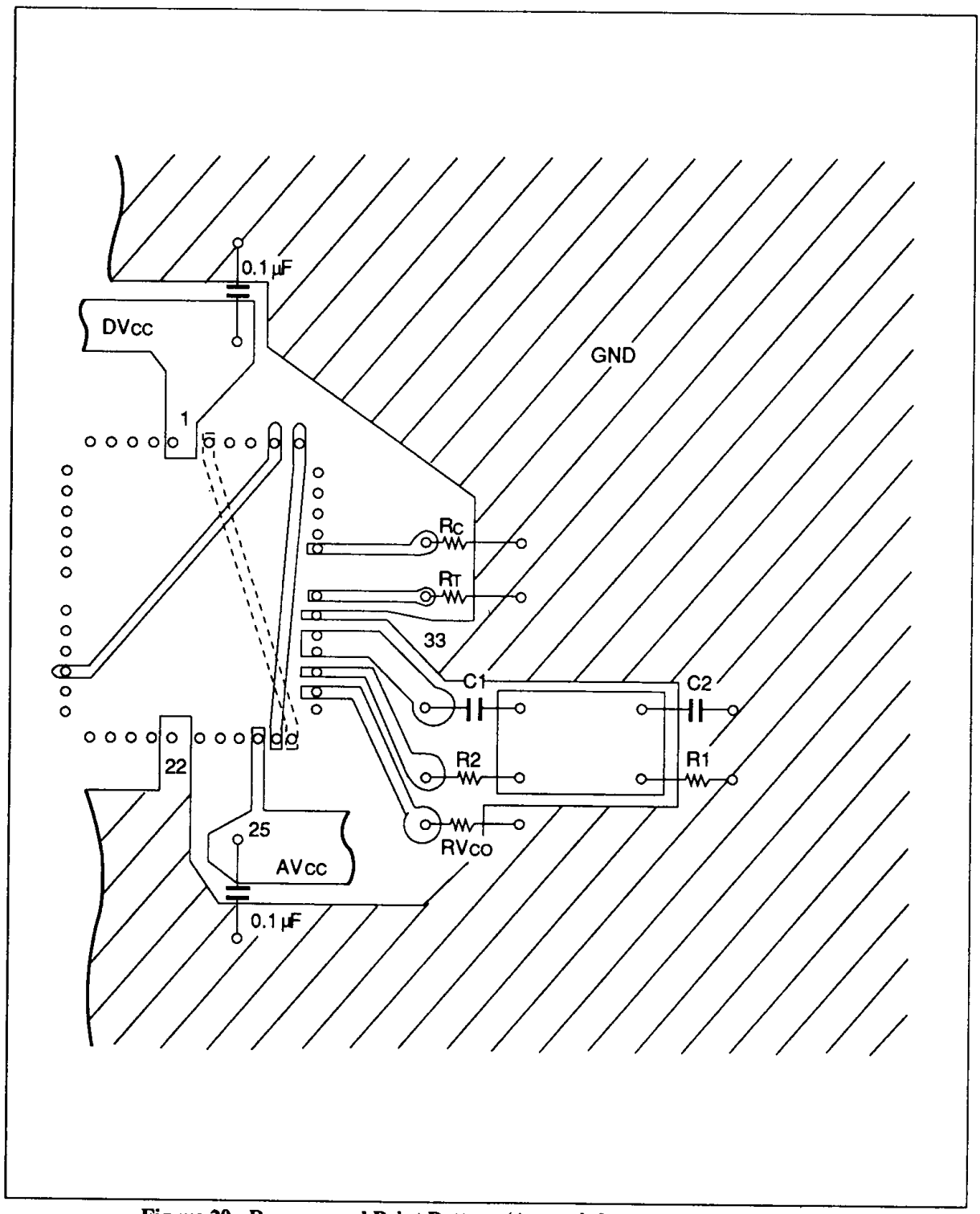


Figure 20 Recommend Print Pattern (Around the parts-connected pins)

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