

# HD153110

## Color Palette with Triple 8-bit DA Converter

The HD153110FS is a color palette with built-in triple 8-bit DA converter. Manufactured with Hitachi's Hi-BiCMOS process, this LSI realizes high speed, high density, low power consumption and minimizes the need for externally connected parts. Also, in addition to applications for existing CRTs, the provision of digital R, G and B outputs for color LCD ensure that the HD153110FS can easily accommodate future systems using full-color LCD. With color palette, advanced functions, small size and low cost, the HD153110FS is an essential component for advanced graphics systems.

### Ordering Information

Type No.	Max. Operating Freq.	Package
HD153110FS	50 MHz	80 pin plastic
HD153110FS-65	65 MHz	QFP (FP-80B)

### Features

- Displays 256 colors simultaneously from a total of 16,777,216 possible colors.
- Three 8-bit DA converters for RGB video output on a single chip
- Read mask function for display control
- Compatible with VGA\* graphics standard
- For each pixel, dynamic switching between 16,777,216-color simultaneous display mode and normal mode
- In addition to existing CRT applications, direct digital RGB outputs from the color lookup table (CLT) are provided for color LCD applications.
- Variable BLACK level (0 or 7.5 IRE)
- Switchable between 8-bit/6-bit mode; supports both 8-bit and 6-bit software.
- Dot rate maximum of 50/65 MHz
- TTL compatible I/O levels
- 28-pin DIP package

Note: VGA is a registered trademark of IBM.

Pin Arrangement

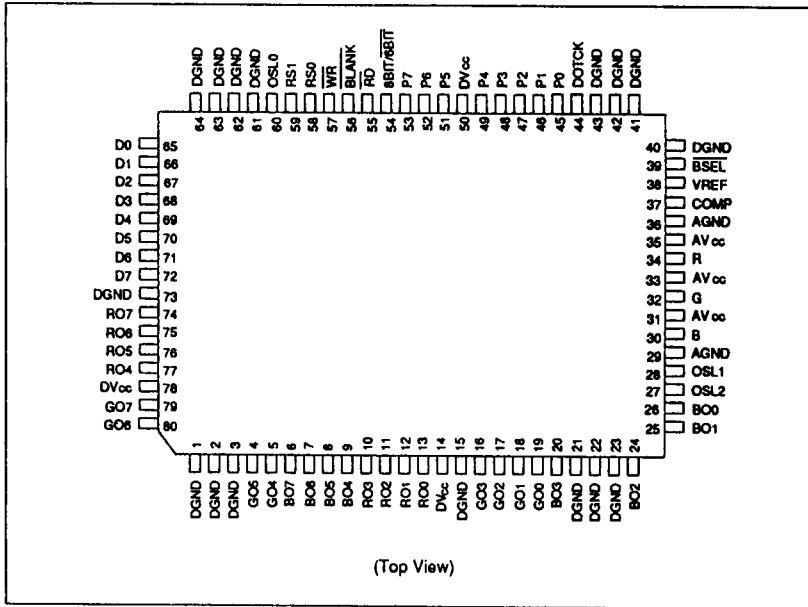


Figure 1

Block Diagram

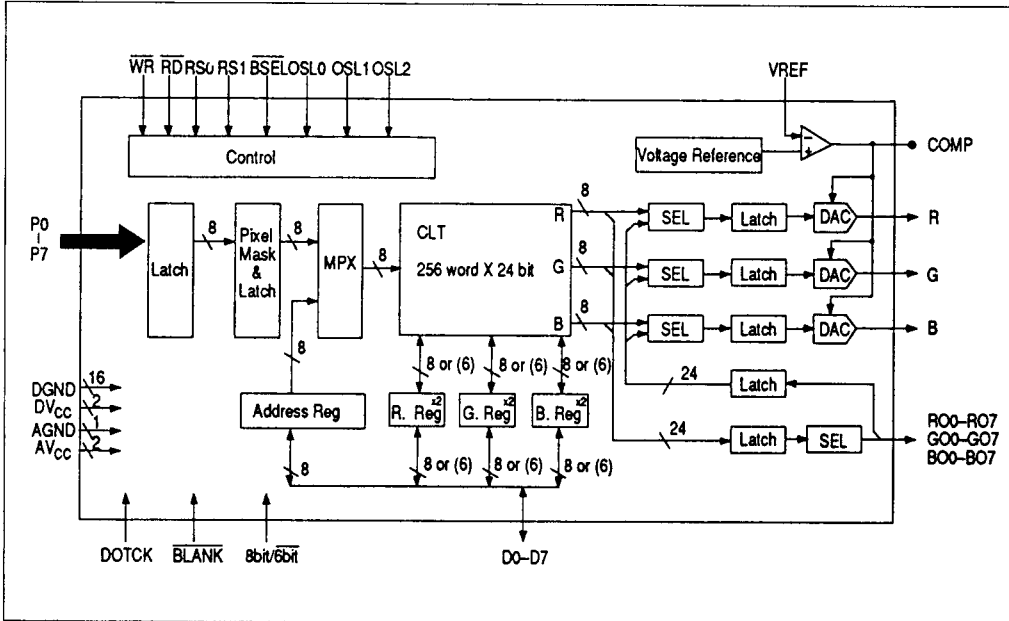


Figure 2 Block Diagram

Table 1 Pin Description

Pin Name	Pin Number	Description
P0 to P7	45 to 49, 51 to 53	CLT address inputs. P7 is MSB, P0 is LSB.
D0 to D7	65 to 72	Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB.
$\overline{RD}$	55	Read clock input. Strokes data from CLT or address, pixel mask, R, G or B registers during read operation.
$\overline{WR}$	57	Write clock input. Strokes data to CLT or address, pixel mask, R, G or B registers during write operation.
RS0, RS1	58, 59	Select inputs for CLT, address register or pixel mask register
RO0 to RO7 GO0 to GO7 BO0 to BO7	13 to 10, 77 to 74 19 to 16, 4, 5, 79, 80 26 to 24, 20 9 to 6	Palette (CLT) digital signal outputs. RO7, GO7 and BO7 are the MSBs and RO0, GO0, and BO0 are the LSBs.
VREF	38	Terminal for connecting reference resistor to set DAC analog output level
COMP	37	Terminal for connecting a phase-compensation capacitor
OSL0, OSL1, OSL2	60, 28, 27	Select inputs for digital signal outputs
R, G, B	34, 32, 30	DAC analog signal outputs
BLANK	56	Video blank input for activating blank signal levels at DAC analog outputs
8BIT/ $\overline{6BIT}$	54	Inputs for setting color palette resolution. 'H' for an 8-bit palette, 'L' for a 6-bit palette
BSEL	39	Input for selecting DAC BLANK level (0 or 7.5 IRE)
DOTCK	44	Reference clock input for digital and analog sections. On the rise of this signal, CLT and BLANK operations are processed and analog signal outputs become active.
DV <sub>CC</sub>	14, 50, 78	Digital power supply
DGND	1 to 3, 15, 21 to 23, 40 to 43, 61 to 64, 73	Digital GND
AV <sub>CC</sub>	31, 33, 35	Analog power supply
AGND	29, 36	Analog GND

## Functions

### Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see Table 2).

### Registers

**Address Register:** To perform read/write operations on the CLT, the CLT address must be set in the address register through D7 to D0 (D7 is the MSB and D0 is the LSB).

For a CLT write operation, write the CLT address via D7 to D0 with RS0 = '0' and RS1 = '0' (in order to select the address register, write mode).

To set up the address register for a CLT read operation, write the CLT address via D7 to D0 with RS0 = '1' and RS1 = '1' (in order to select the address register, read mode).

Also, the address register contents can be read as shown in figure 10 and figure 11.

**Pixel Mask Register:** The pixel mask register is used when displayed colors to be modified by altering the value input from video memory and

the contents of the CLT. The pixel mask register is set by writing a pixel mask value to D7 (MSB) to D0(LSB) with RS0 = '0' and RS1 = '1' (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) to P0(LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask '0' bits will cancel corresponding video memory value '1' bits. The following table shows the CLT address that is generated for a particular pixel mask register value and video memory value.

**RGB Registers:** There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 24-bit word.

To read or write data to the CLT, set RS0 = '1' and RS1 = '0' to select the appropriate RGB register while performing the read or write via data port D7 (MSB) to D0 (LSB). Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

**Table 2 Register Selection**

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

**Table 3 Pixel Mask Example**

	MSB				LSB			
Pixel mask register	1	0	1	0	1	1	0	1
Address input (P7 to P0)	Pd7	Pd6	Pd5	Pd4	Pd3	Pd2	Pd1	Pd0
CLT address value	Pd7	0	Pd5	0	Pd3	Pd2	0	Pd0

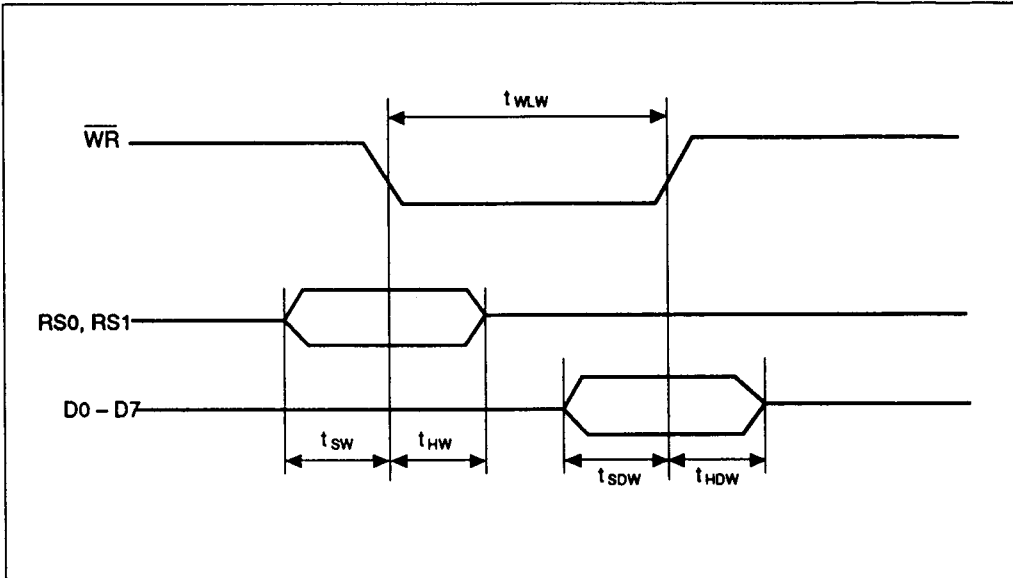


Figure 3 Write Timing

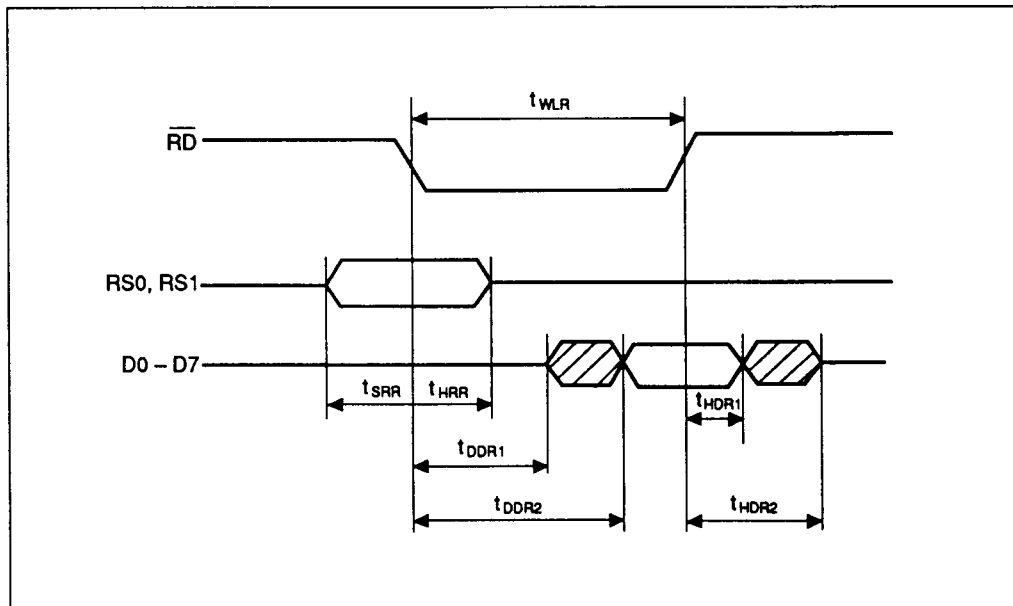
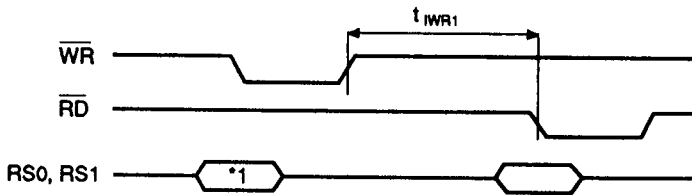


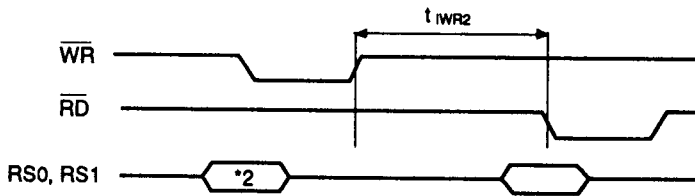
Figure 4 Read Timing

(a) Applies to all read-after-write operations except when the write operation is placing a read address in the address register.



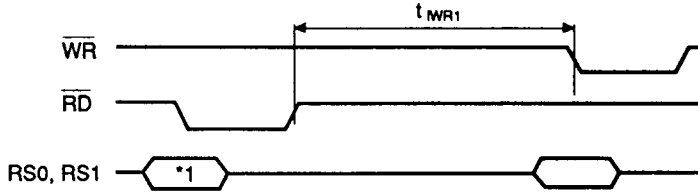
Note 1: This timing not valid when RS0 = 'H' and RS1 = 'H'

(b) Applies to the case when the write operation is placing a read address in the address register.



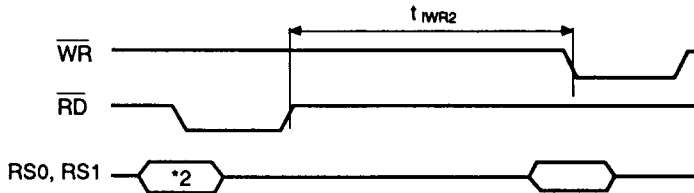
Note 2: This timing is valid when RS0 = 'H' and RS1 = 'H'

Figure 5 Read after Write



Note 1: This timing not valid for reading CLT Blue data or when RS0 = 'H' and RS1 = 'L'.

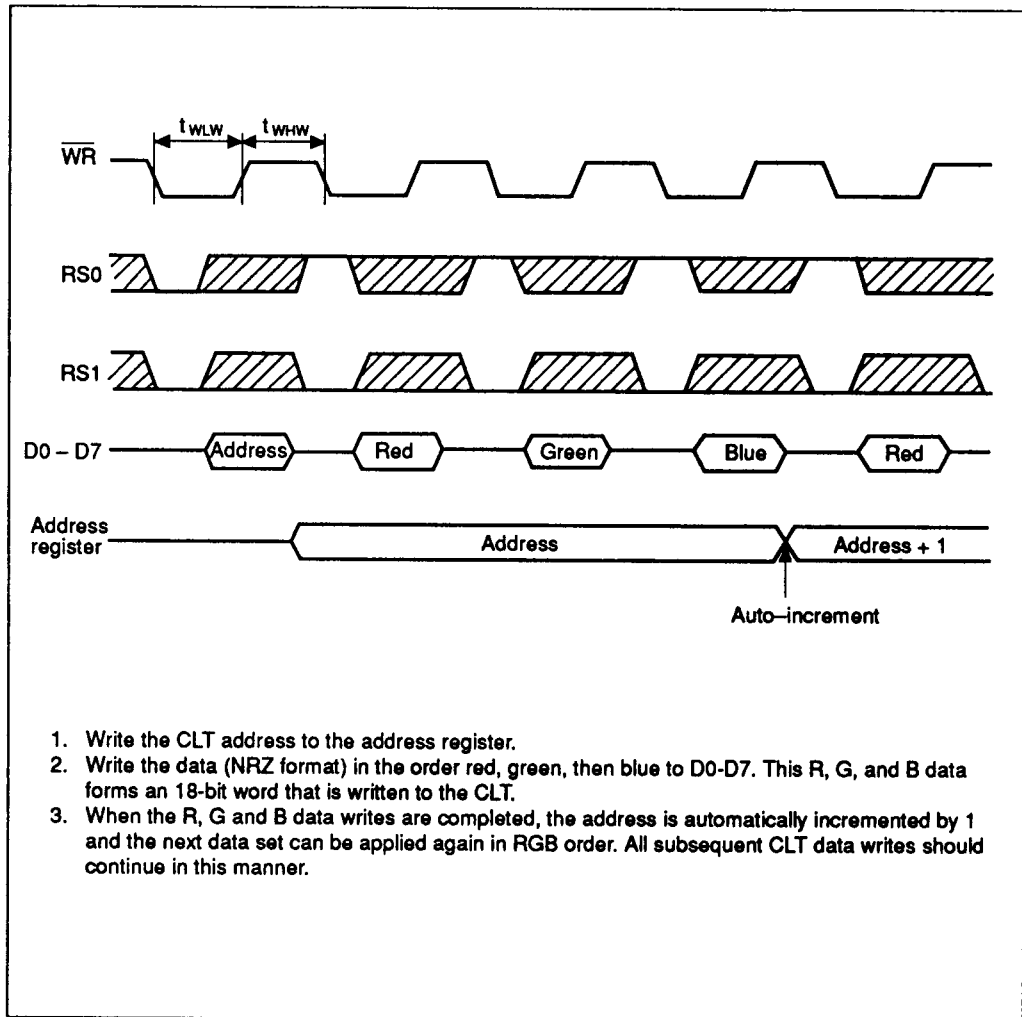
(b) Applies to the case where the read operation is for CLT Blue data.



Note 2: This timing is valid for reading CLT Blue data or when RS0 = 'H' and RS1 = 'L'.

Figure 6 Write after Read

2



1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0-D7. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by 1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

Figure 7 CLT Write



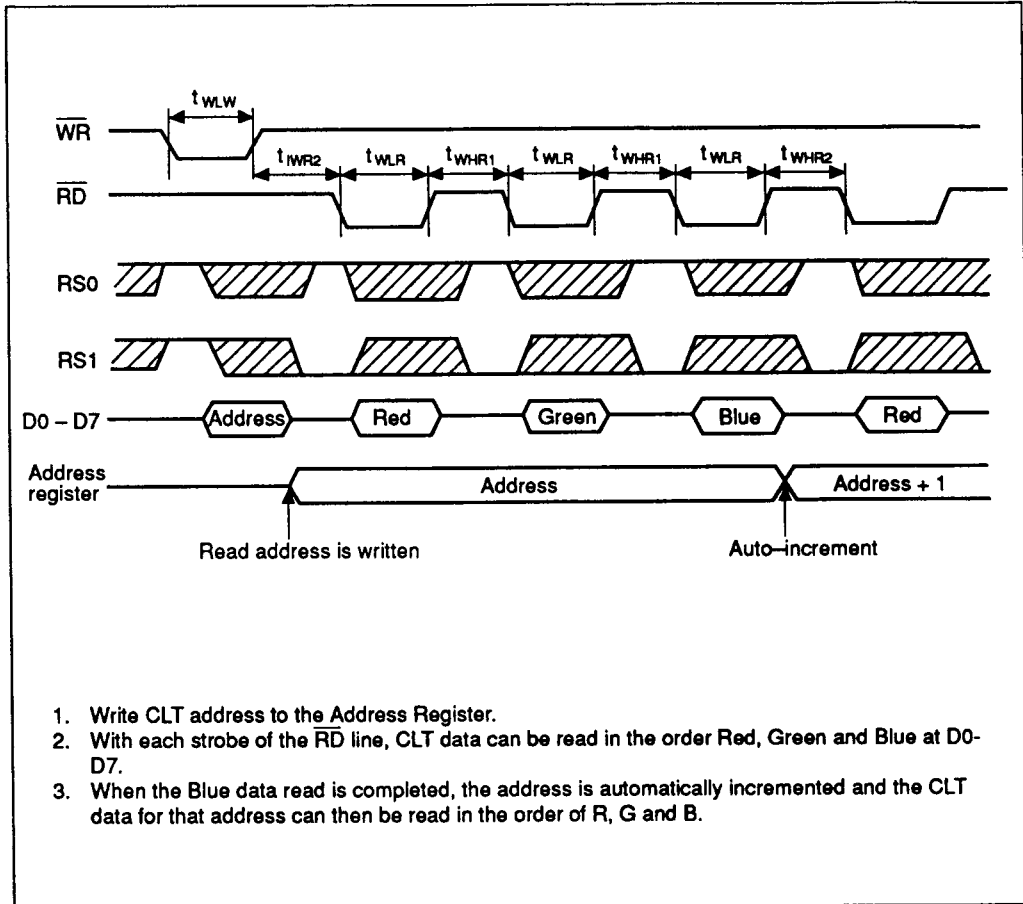


Figure 8 CLT Read

2

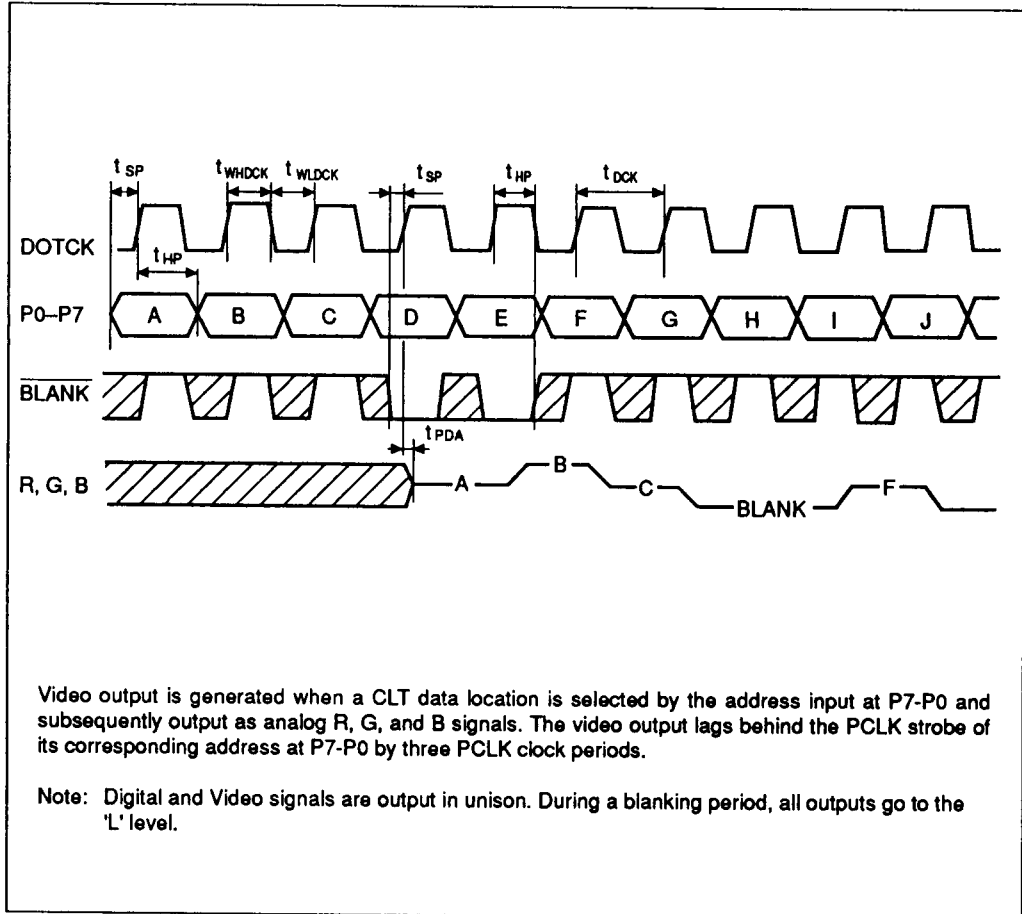


Figure 9 Video Output

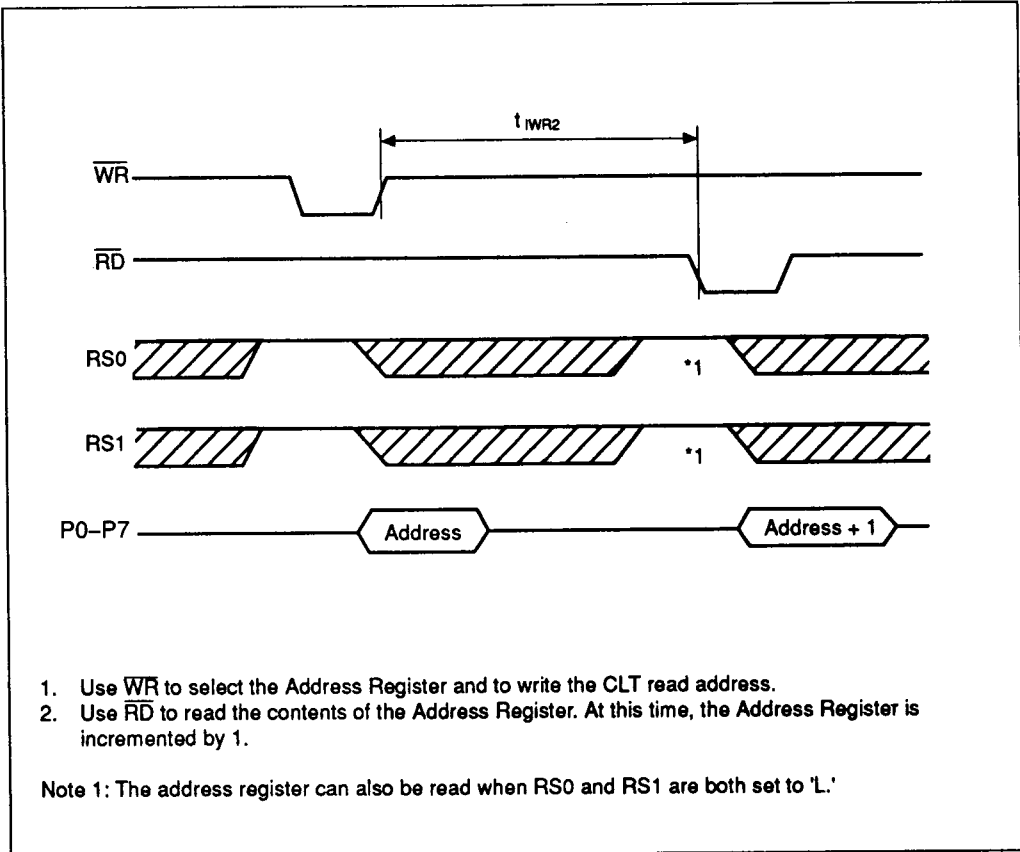


Figure 10 Address Register Read (1)

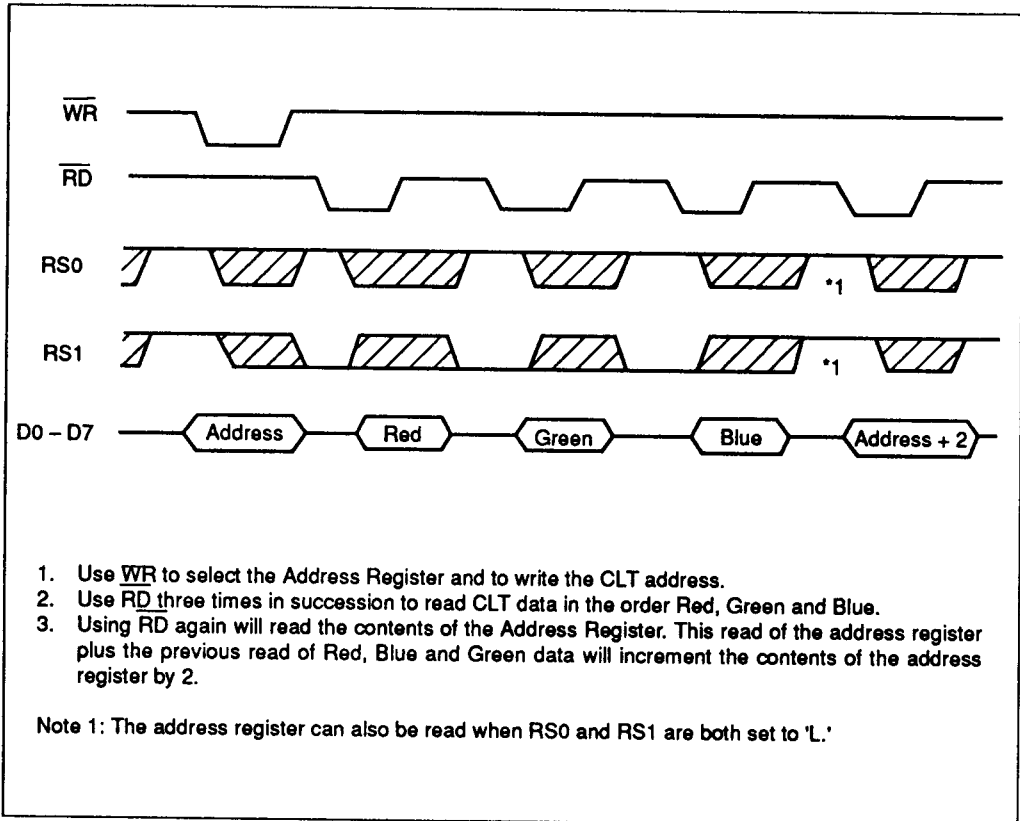


Figure 11 Address Register Read (2)

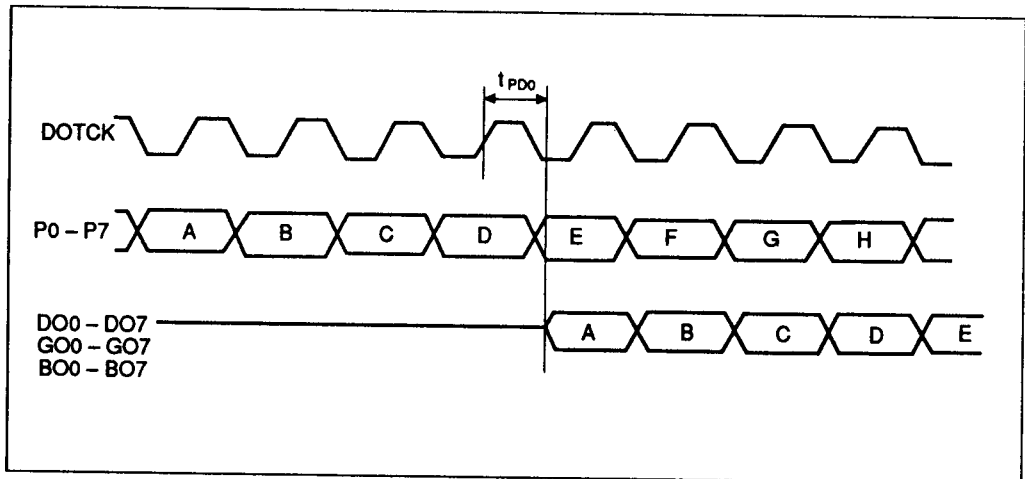


Figure 12 Digital Output

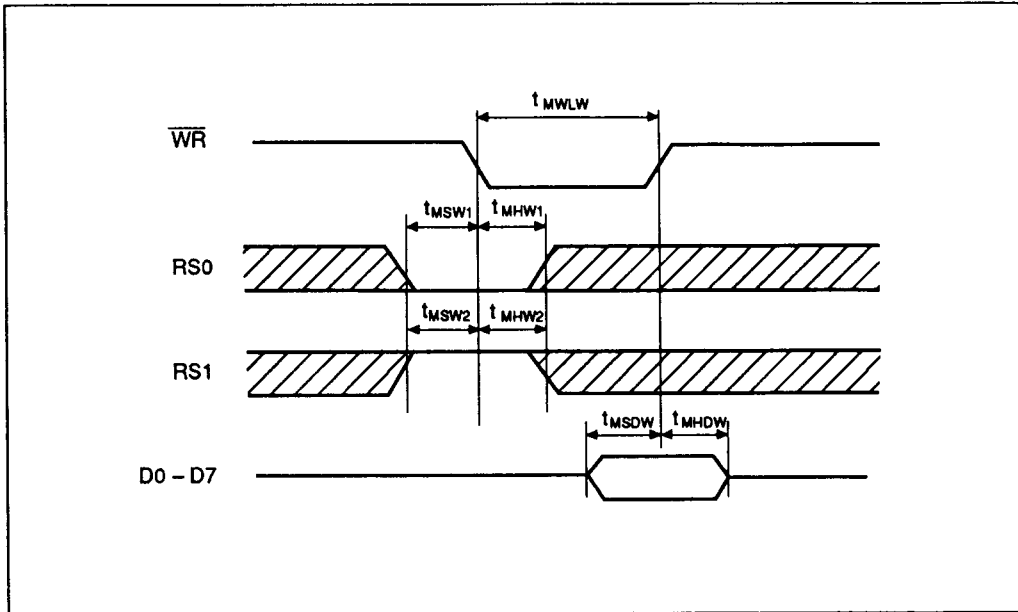


Figure 13 Pixel Mask Register Write

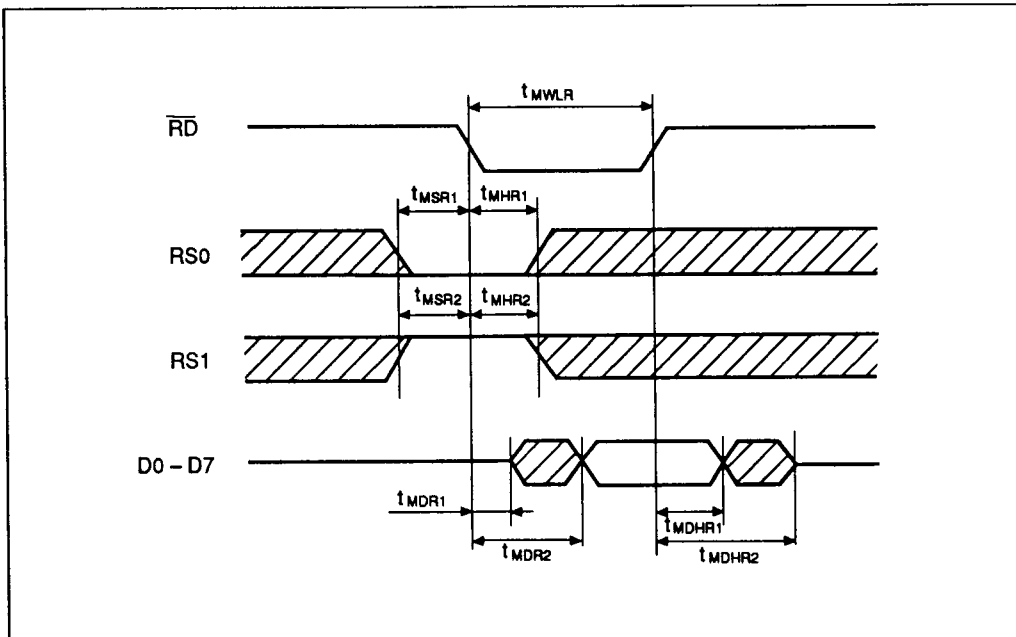
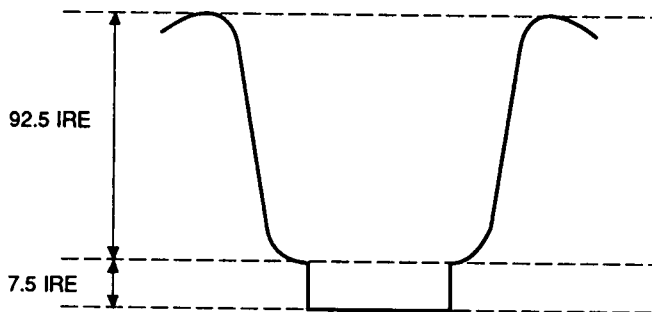


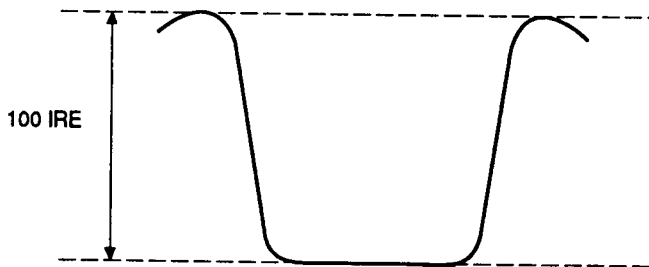
Figure 14 Pixel Mask Register Read

White level	0.698 V
Black level	0.054 V
Blank level	0.000 V



( $\overline{\text{BSEL}} = \text{'L'}$ ,  $R_{VREF} = 13 \text{ k}\Omega$ )

White level	0.698 V
Black/blank level	0.000 V



( $\overline{\text{BSEL}} = \text{'H'}$ ,  $R_{VREF} = 12 \text{ k}\Omega$ )

Figure 15 Video Output Waveforms

**Mode Switching**

HD153110 operating mode is switched as shown below. (8 bit/6bit='H')

When the 8 bit/6bit terminal is 'L' a 6-bit color palette can be used; when in 24-bit digital output mode, the digital outputs will be on the upper six bits of each 8-bit word and the lower two bits will be set 'L.'

**Table 4 Mode Switching**

OSL2	OSL1	OSL0	Operating Mode	Notes
L	L	L	DAC output mode	1
L	L	H	DAC direct Input (16,777,216-color simultaneous display mode)	1
L	H	L	Digital output 12-bit mode (R, G and B are output on upper 4 bits)	2
L	H	H	Prohibited (Digital output 24-bit mode)	3
H	L	L	Digital output 6-bit mode (Green output only)	2
H	L	H	Prohibited	
H	H	L	Digital output 24-bit mode	2
H	H	H	Prohibited	

- Notes: 1. Digital output is Hi-Z.  
 2. DAC outputs are off.  
 3. Both Digital and DAC outputs are active.



Register Correspondence with CLT

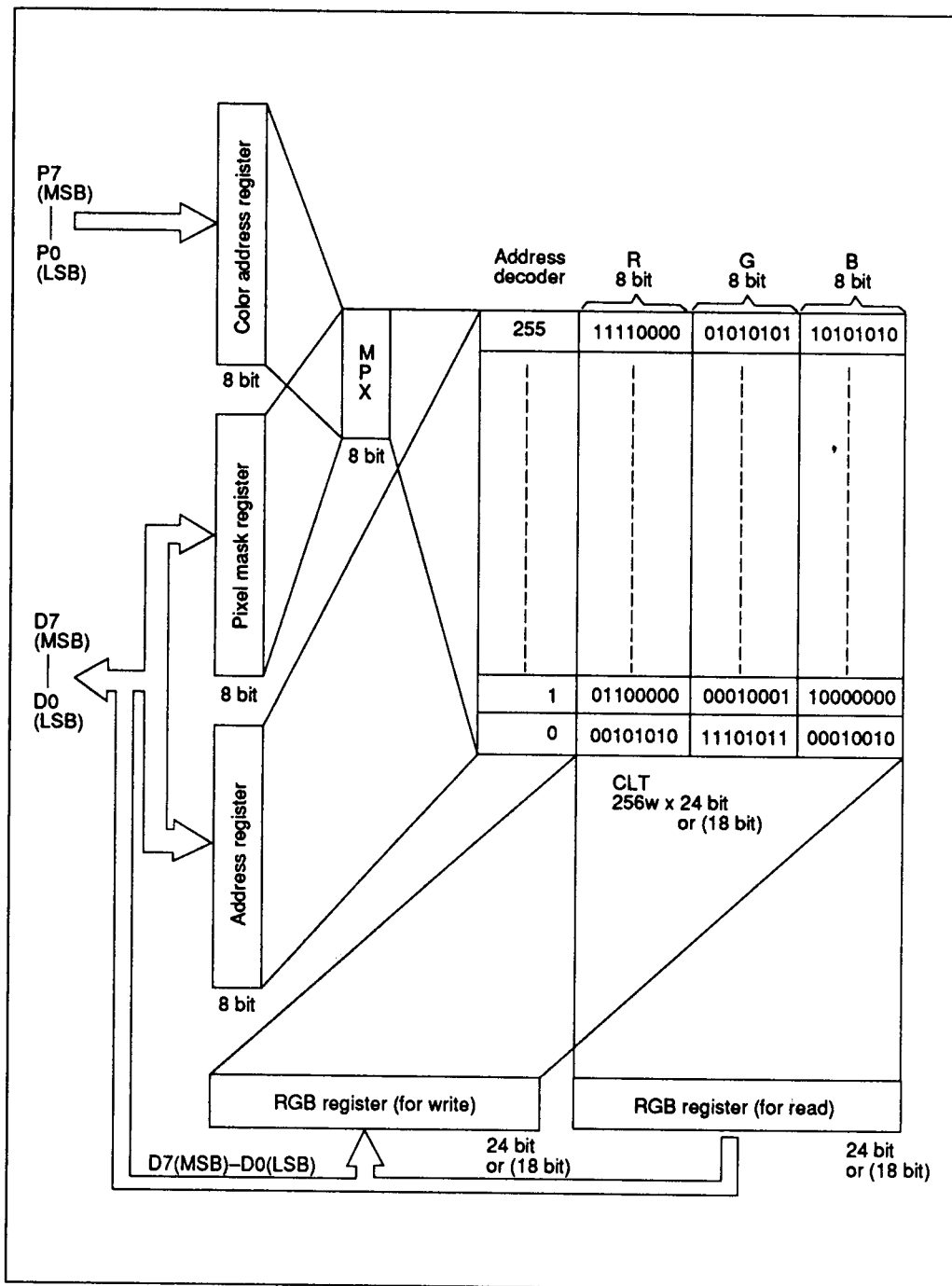
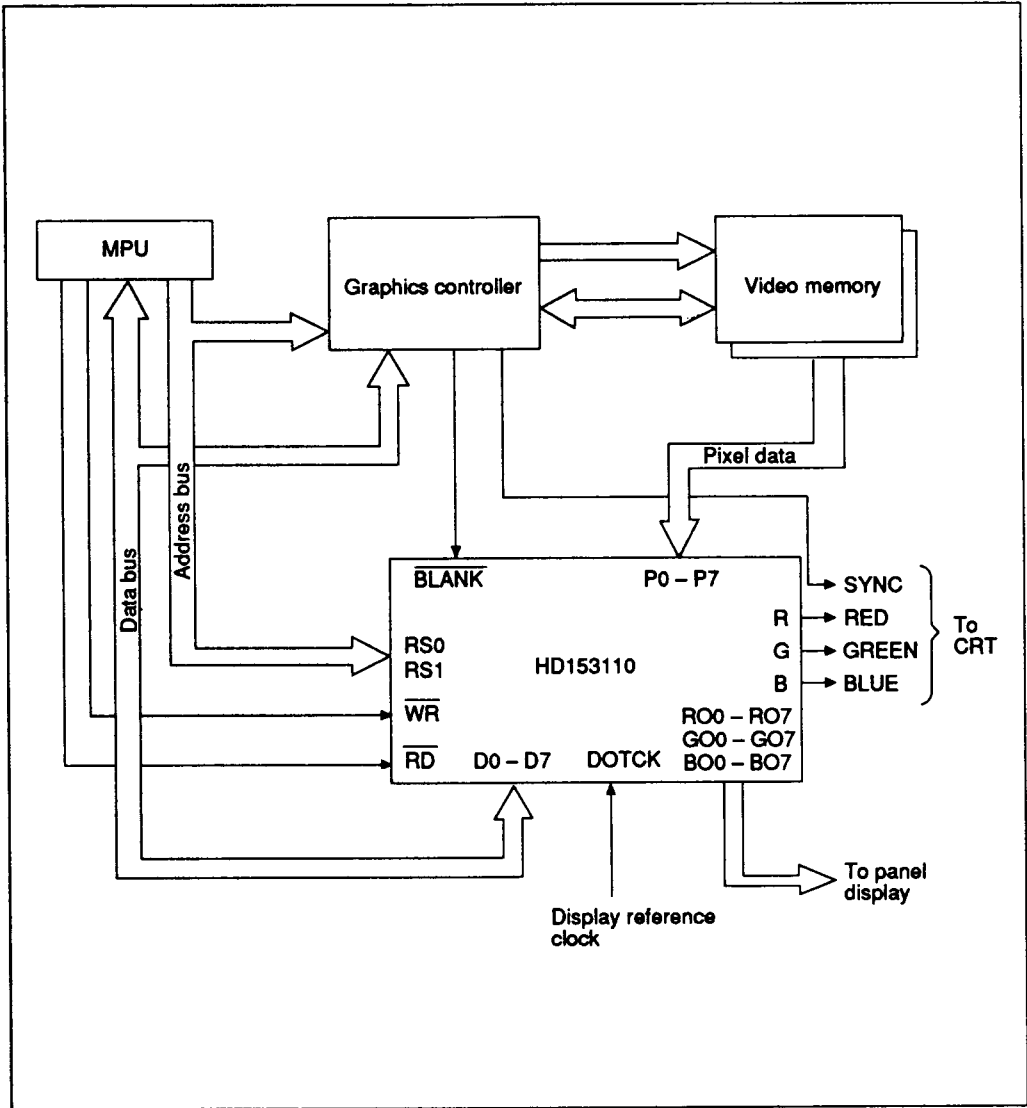


Figure 16 Register Correspondence with CLT





System Configuration Example



2

Figure 17 System Configuration Example

**Table 5 Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	7.0	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

**Electrical Characteristics**

**Table 6 DAC Section Electrical Characteristics ( $V_{cc}=5\text{ V}$ ,  $T_a=25^\circ\text{C}$ )**

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Resolution		8 (6)	8 (6)	8 (6)	bits	
Maximum operating frequency	$f_{CLK}$	—	—	50/65	MHz	
Analog output voltage	$V_A$ (Full)	-15	—	15	% of FSR	
( $R_{VREF} = 12\text{ k}\Omega$ )	$V_A$ (Zero)	-2	—	2	% of FSR	
Differential linearity	DLE	-1	—	+1	LSB	
Integral linearity	ILE	-1	—	+1	LSB	
Output rise time (20 – 80%)	$t_r$	—	—	10	ns	$C_L = 15\text{ pF}$
Output fall time (80 – 20%)	$t_f$	—	—	10	ns	$C_L = 15\text{ pF}$
Settling time	$t_s$	—	—	30	ns	$C_L = 15\text{ pF}$
Glitch energy	$E_G$	—	90	—	PVS	

( ) indicates 6-bit mode.

**Table 7 Digital Section DC Characteristics**  
(unless otherwise specified  $V_{CC} = 5\text{ V} \pm 5\%$ ;  $T_a = 0\text{ to }+70^\circ\text{C}$ )

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input "High" level voltage	$V_{IH}$	2.0	—	$V_{CC}$	V		
Input "Low" level voltage	$V_{IL}$	-0.3	—	0.8	V		
Input clamp voltage	$V_I$	—	—	-1.5	V	$V_{CC} = 4.75\text{ V}$ $I_{IN} = -18\text{ mA}$	

**Digital Section DC Characteristics**  
(unless otherwise specified  $V_{CC} = 5\text{ V} \pm 5\%$ ;  $T_a = 0\text{ to }+70\text{ }^\circ\text{C}$ ) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Output "High" level voltage	$V_{OH}$	2.7	—	—	V	$V_{CC} = 4.75\text{ V}$ $I_{OH} = -400\text{ }\mu\text{A}$	
Output "Low" level voltage	$V_{OL}$	—	—	0.5	V	$V_{CC} = 4.75\text{ V}$ $I_{OL} = 8\text{ mA}$	
Input current	$I_I$	—	—	1	mA	$V_{CC} = 5.25\text{ V}$ $V_I = 5.5\text{ V}$	
"High" level input current	$I_{IH}$	—	—	20	$\mu\text{A}$	$V_{CC} = 5.25\text{ V}$ $V_I = 2.7\text{ V}$	
"Low" level input current	$I_{IL}$	—	—	-400	$\mu\text{A}$	$V_{CC} = 5.25\text{ V}$ $V_I = 0.4\text{ V}$	
Supply current (1)	$I_{CC}(1)$	—	130	190	mA	$V_{CC} = 5.25\text{ V}$	1
Supply current (2)	$I_{CC}(2)$	—	110	160	mA	$V_{CC} = 5.25$	2

- Notes: 1. OSL0 = 'L', OSL1 = 'L', OSL2 = 'L'  
2. OSL0 = 'L', OSL1 = 'H', OSL2 = 'H'

**Table 8 Digital Section AC Characteristics ( $V_{CC} = 5\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C}$ )**

Item	Symbol	50 MHz		65 MHz		Unit	Remarks	Reference Figure
		Min	Max	Min	Max			
DOTCK cycle time	$t_{DCK}$	20	—	15.3	—	ns		9
DOTCK low level time	$t_{WLDCK}$	8	—	6	—	ns		9
DOTCK high level time	$t_{WHDC}$	8	—	6	—	ns		9
Data setup time	$t_{sp}$	6	—	5	—	ns		9
Data hold time	$t_{HP}$	6	—	5	—	ns		9
Data output delay time	$t_{PDA}$	—	30	—	30	ns	$C_L = 15\text{ pF}$	9
$\overline{WR}$ low level time	$t_{WLW}$	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ high level time	$t_{WHW}$	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		7
$\overline{RD}$ low level time	$t_{WLR}$	50	—	50	—	ns		8
$\overline{RD}$ high level time (1)	$t_{WHR1}$	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		8
$\overline{RD}$ high level time (2)	$t_{WHR2}$	$6 \times t_{DCK}$	—	$6 \times t_{DCK}$	—	ns		8
$\overline{WR}/\overline{RD}$ interval time (1)	$t_{WR1}$	$3 \times t_{DCK}$	—	$3 \times t_{DCK}$	—	ns		5, 6
$\overline{WR}/\overline{RD}$ interval time (2)	$t_{WR2}$	$6 \times t_{DCK}$	—	$6 \times t_{DCK}$	—	ns		5, 6, 8, 9



# HD153110

## Digital Section AC Characteristics ( $V_{CC} = 5\text{ V}$ , $T_a = 25\text{ }^\circ\text{C}$ ) (cont)

Item	Symbol	50 MHz		65 MHz		Unit	Remarks	Reference Figure
		Min	Max	Min	Max			
$\overline{WR}/RS0$ , RS1 setup time	$t_{SW}$	10	—	10	—	ns		3
$\overline{WR}/RS0$ , RS1 hold time	$t_{HW}$	10	—	10	—	ns		3
$\overline{RD}/RS0$ , RS1 setup time	$t_{SRR}$	10	—	10	—	ns		4
$\overline{RD}/RS0$ , RS1 hold time	$t_{HRR}$	10	—	10	—	ns		4
$\overline{WR}$ data setup time	$t_{SDW}$	10	—	10	—	ns		3
$\overline{WR}$ data hold time	$t_{HDW}$	10	—	10	—	ns		3
$\overline{RD}$ data output delay time (1)	$t_{DDR1}$	5	—	5	—	ns	$C_L = 15\text{ pF}$	4
$\overline{RD}$ data output delay time (2)	$t_{DDR2}$	—	40	—	40	ns	$C_L = 15\text{ pF}$	4
$\overline{RD}$ data output hold time (1)	$t_{HDR1}$	5	—	5	—	ns	$C_L = 15\text{ pF}$	4
$\overline{RD}$ data output hold time (2)	$t_{HDR2}$	—	20	—	20	ns	$C_L = 15\text{ pF}$	4
Digital output delay time	$t_{PDO}$	—	19	—	19	ns	$C_L = 15\text{ pF}$	12
$\overline{WR}$ low level time	$t_{MWLW}$	50	—	50	—	ns		13
$\overline{RD}$ low level time	$t_{MWLR}$	50	—	50	—	ns		14
$\overline{WR}/RS0$ , RS1 setup time	$t_{MSW1}$	10	—	10	—	ns		13
	$t_{MSW2}$	10	—	10	—	ns		13
$\overline{WR}/RS0$ , RS1 hold time	$t_{MHW1}$	10	—	10	—	ns		13
	$t_{MHW2}$	10	—	10	—	ns		13
$\overline{RD}/RS0$ , RS1 setup time	$t_{MSR1}$	10	—	10	—	ns		14
	$t_{MSR2}$	10	—	10	—	ns		14
$\overline{RD}/RS0$ , RS1 hold time	$t_{MHR1}$	10	—	10	—	ns		14
	$t_{MHR2}$	10	—	10	—	ns		14
$\overline{WR}$ data setup time	$t_{MSDW}$	10	—	10	—	ns		13
$\overline{WR}$ data hold time	$t_{MHDW}$	10	—	10	—	ns		13

Digital Section AC Characteristics ( $V_{CC} = 5\text{ V}$ ,  $T_a = 25\text{ }^\circ\text{C}$ ) (cont)

Item	Symbol	50 MHz		65 MHz		Unit	Remarks	Reference
		Min	Max	Min	Max			Figure
RD data output delay time	$t_{MDR1}$	5	—	5	—	ns	$C_L = 15\text{ pF}$	14
	$t_{MDR2}$	—	40	—	40	ns	$C_L = 15\text{ pF}$	14
RD data output hold time	$t_{MDHR1}$	5	—	5	—	ns	$C_L = 15\text{ pF}$	14
	$t_{MDHR2}$	—	20	— </td <td>20</td> <td>ns</td> <td><math>C_L = 15\text{ pF}</math></td> <td>14</td>	20	ns	$C_L = 15\text{ pF}$	14



Connection Example

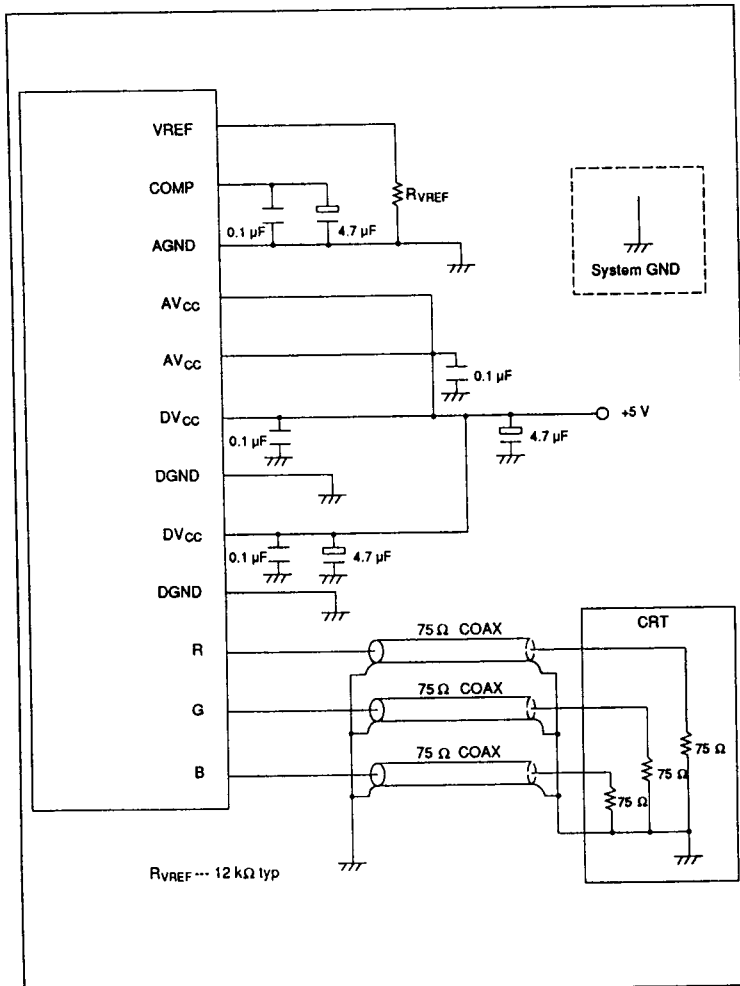


Figure 18 Connection Example