HD155004T

Built-in Prescaler PLL Frequency Synthesizer IC for Cellular Systems and DTS

HITACHI

ADE-207-244 (Z)
1st. Edition
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Description

The HD155004T is a PLL frequency synthesizer IC that was developed for cellular systems and DTS. The HD155004T includes a built-in prescaler for cellular intermediate frequencies, and thus can form a PLL system by attaching an external loop filter and VCO.

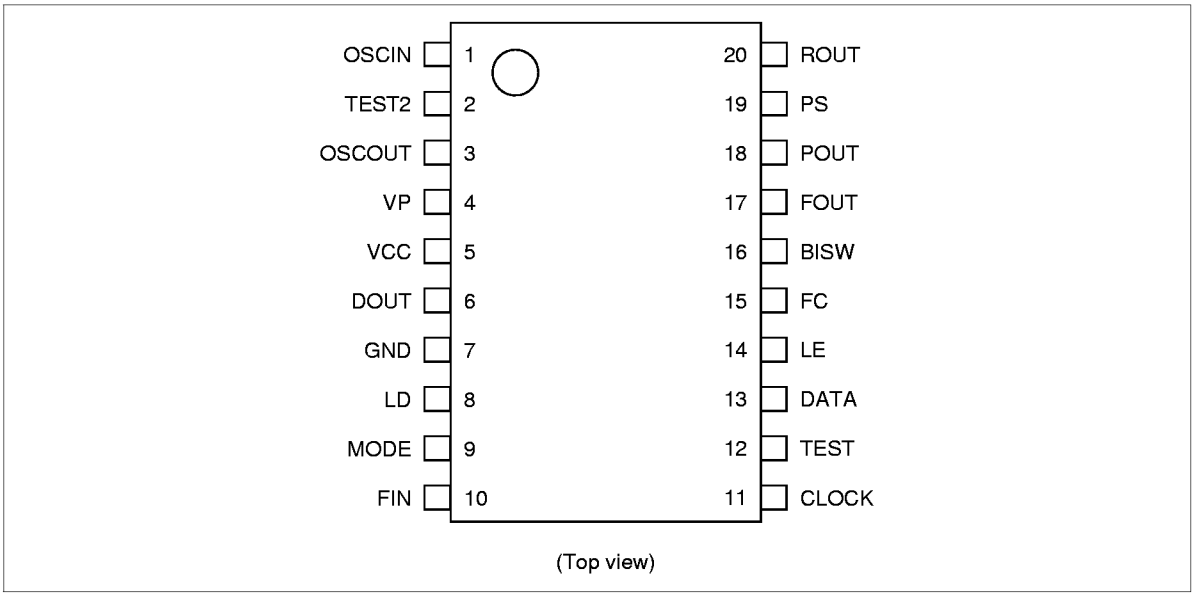
Functions

- Dual-modulus pulse swallow type PLL frequency synthesizer
- Power saving mode
- Lock detection function (selectable hysteresis characteristics)
- Optional mode (Serial control and lock detection)
- Divisors can be set by serial interface commands
- Built-in charge pump circuit
- Built-in analog switch for high speed lock-up

Features

- High speed prescaler (FIN Max = 130 MHz)
- Low current consumption
  - — Operational mode: 0.8 mA (Typ), 2.0 mA (Max)
  - — Power saving mode: 100 µA (Typ), 200 µA (Max)
- High charge pump current drivability
- TSSOP–20 (Thin Shrink Small Outline Package)

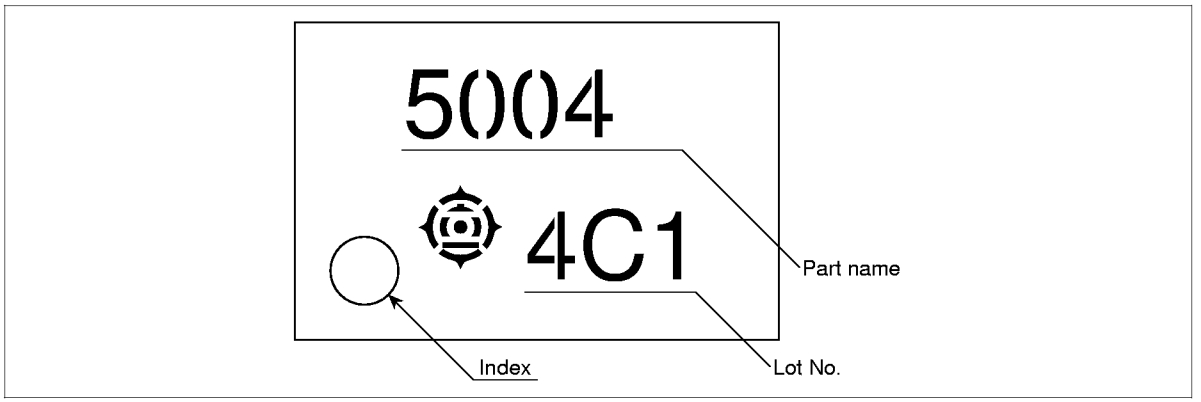
Pin Arrangement



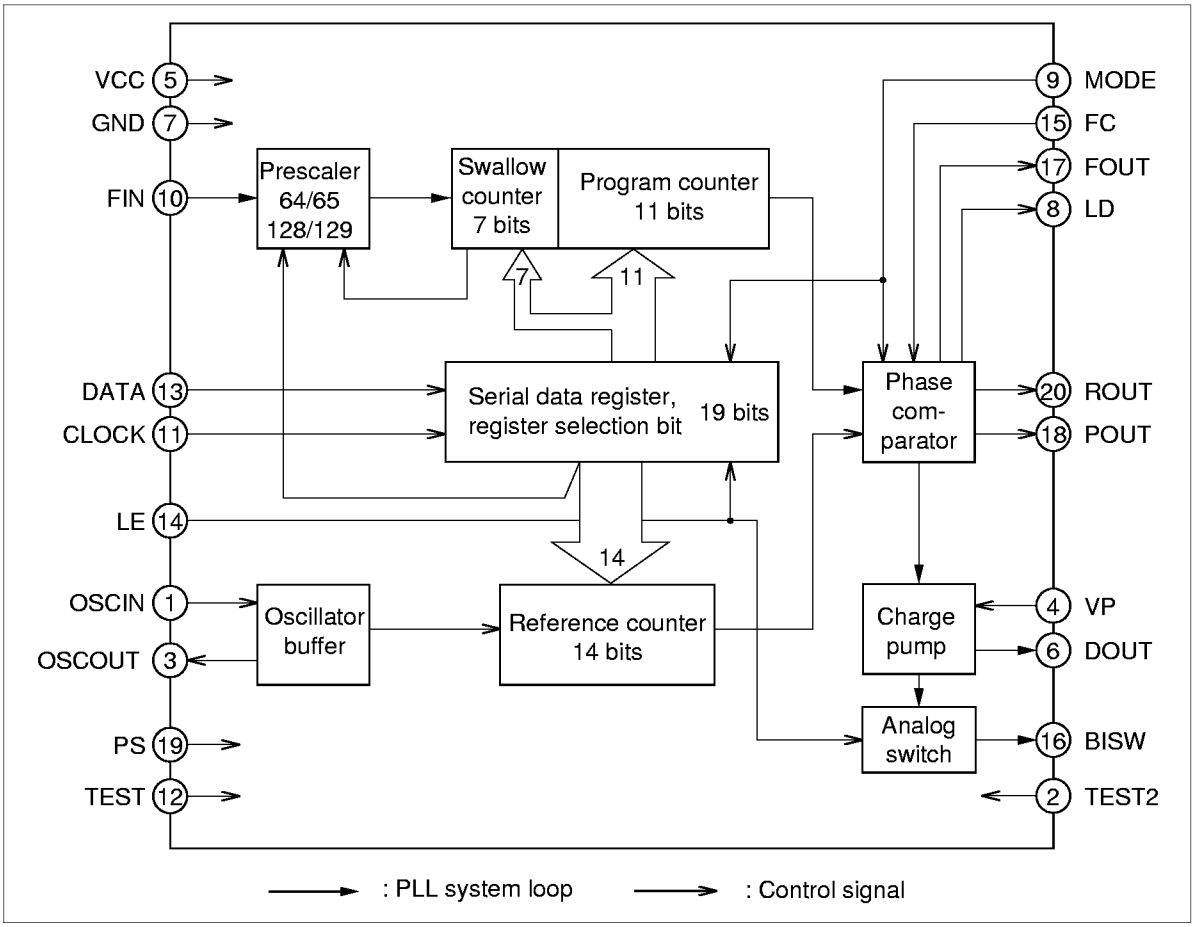
Pin Description

No.	Pin	I/O	Function	Pin Characteristics
1	OSCIN	Input	Reference oscillator input pin.	Oscillator
2	TEST2	Input	Test pin (Normally left open)	Pull-up
3	OSCOUT	Output	Reverse phase output pin for the OSCIN pin.	Oscillator
4	VP		DOUT pin power supply connection pin	
5	VCC		Power supply connection pin	
6	DOUT	Output	Charge pump output	Analog
7	GND		Ground pin	
8	LD	Output	Lock detection output pin	CMOS
9	MODE	Input	Normal/Optional setting pin	Pull-up
10	FIN	Input	VCO connection pin	Analog
11	CLOCK	Input	Synchronous clock pin for command input	CMOS
12	TEST	Input	Test pin (Normally left open)	Pull-up
13	DATA	Input	Command input data pin	CMOS
14	LE	Input	Command input enable pin	Pull-up
15	FC	Input	Phase comparator polarity setting pin	Pull-up
16	BISW	Output	Analog switch output pin for high speed lock-up	Analog
17	FOUT	Output	Internal counter monitor pin	CMOS
18	POUT	Output	Phase comparator output pin 1	Analog
19	PS	Input	Power saving mode setting pin	Pull-up
20	ROUT	Output	Phase comparator output pin 2	CMOS

Marking Specification



Block Diagram



Functional Description

To operate the HD155004T, the mode must be set from the mode pins, and the registers must be set by the control microcomputer.

Setting the Operating Mode: The HD155004T provides the operating modes shown in table 1. These operating modes are described in "Operating Modes."

Table 1 Setting the HD155004T Operating Mode

	MODE = H	MODE = L
PS = H	Normal active mode	Optional active mode
PS = L	Normal power saving mode	Optional power saving mode

Register Setting Values: The HD155004T is a dual-modulus pulse swallow type PLL frequency synthesizer. Therefore, the register settings can be derived from the following formulas.

1. When the prescaler divisor is 128/129:
$$f_{VCO} = f_{OSCIN} \times (PRG \times 128 + SWL) / REF$$
2. When the prescaler divisor is 64/65:
$$f_{VCO} = f_{OSCIN} \times (PRG \times 64 + SWL) / REF$$

f_{VCO} and f_{OSCIN} indicate the VCO and oscillator frequencies respectively, and PRG, SWL, and REF are the program, swallow, and reference counter division ratios. Note that PRG must be larger than SWL, and when the prescaler divisor is 64, SWL must be less than 64.

Setting the Registers: The HD155004T has four internal registers, and they are used to set the reference counter, the program counter, the swallow counter, and the prescaler divisors. These registers are set by the control microcomputer from the CLOCK, DATA, and LE pins. Figures 1 and 2 show the timing charts for these operations.

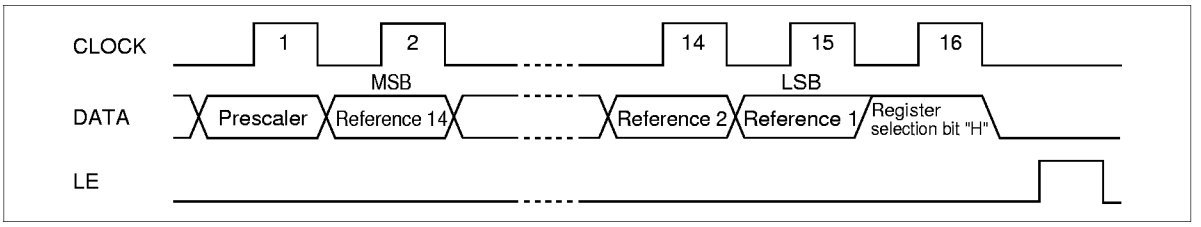


Figure 1 Setting the Prescaler and the Reference Counter Registers (Serial 16 bits)

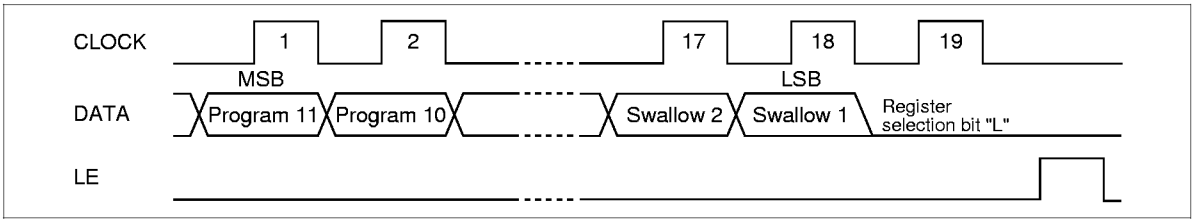


Figure 2 Setting the Program Counter and the Swallow Counter Registers (Serial 19 bits)

When setting these registers, the prescaler and the reference counter, and the program counter and the swallow counter, are set together as register pairs. These register pairs are selected by appending a register selection bit to the end of the setup data.

The register selection bit selects the prescaler and reference counter register, when this bit is high, and selects the program counter and swallow counter register when low.

The prescaler register (1 bit) sets the prescaler divisor, which is 64/65 when this bit is high, and 128/129 when low.

Note that the counter registers execute divide operations based on the set value as the divisor, i.e., they function as auto reload counters.

The value of the reference counter register must be between 16 and 16383, the value of the program counter register must be between 16 and 2047, and that of the swallow counter register, between 0 and 127.

Other Settings: The only other HD155004T setting is the FC pin, which determines the phase comparator's input polarity. When FC is high, if the reference counter output is delayed relative to the outputs of the program counter and the swallow counter (i.e., the VCO oscillator frequency is too high), then the charge pump output is set to low. When FC is low, the charge pump will be set to high in that case.

Operating Modes: The HD155004T provides four operating modes, which are selected by the MODE and PS pins. The MODE pin switches the HD155004T between the normal and optional modes. These modes differ in the register data loading timing from the LE pin, and in the LD pin lock detection conditions. MODE pin is usually pulled up and by making this pin open, the normal mode is selected.

1. Normal mode

Data loading controlled by the LE pin is based on the pin level: the register data is loaded when the LE pin is high.

The LD pin uses the phase comparator output without modification, and outputs that data. More accurately, when the charge pump is high impedance, LD will output a high level.

2. Optional mode

In optional mode, data loading by the LE pin is performed on signal edges. The OSCIN pin clock is used, and data is latched into the registers on the rising edge of the LE pin signal. A length of at least 3 OSCIN clock pulses is required by the LE pin. (See figure 3.)

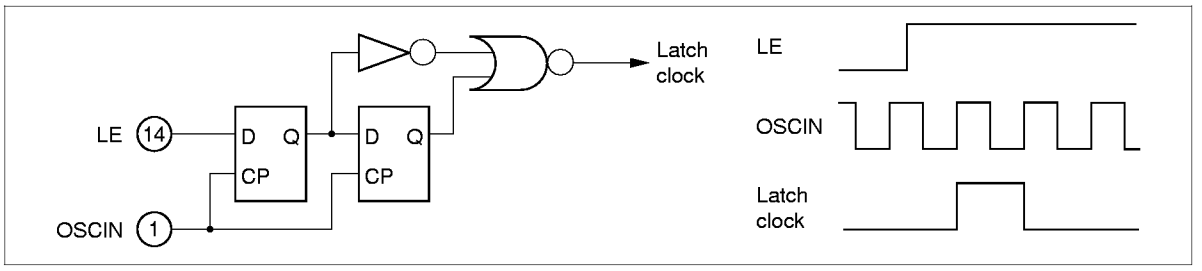


Figure 3 Register Latching in Optional Mode

The LD pin outputs the phase comparator output with hysteresis generated by counting the phase comparator output with a counter. (See figures 4 and 5.)

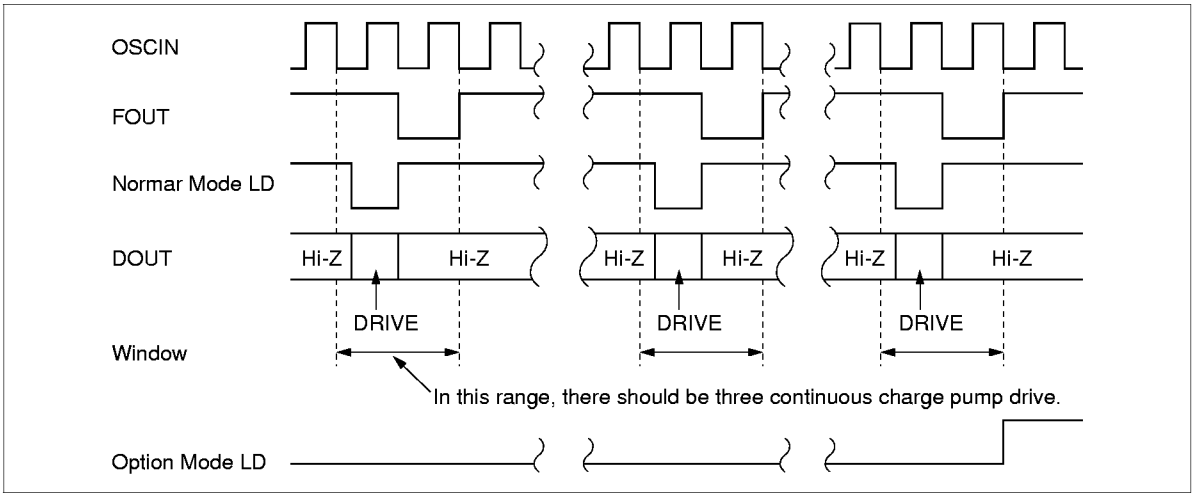


Figure 4 LD Rising Edge Timing

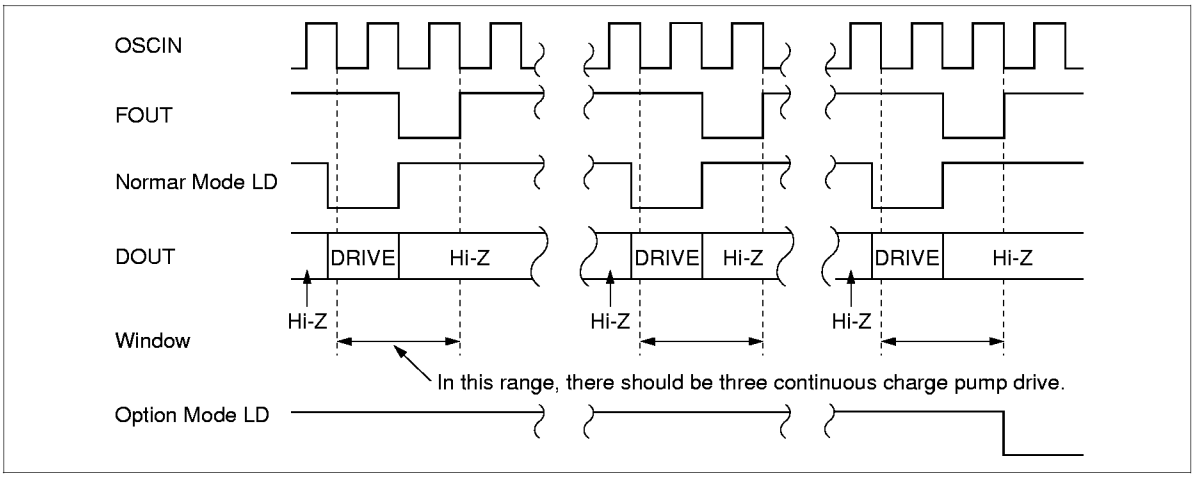


Figure 5 LD Falling Edge Timing

3. Power saving mode

In waiting mode, the operation of HD155004T can be stopped to reduce the current consumption by using the power saving mode. In power saving mode, the prescaler is stopped to keep the CMOS in waiting mode.

Since the CMOS logic blocks consume essentially no power when there is no clock input, clock input to the CMOS blocks is stopped in power saving mode.

Furthermore, the charge pump output goes to the high impedance state, and the loop filter holds the immediately preceding value. A point that requires attention when using power saving mode, is that although the CMOS blocks, for which only the clock is stopped, retain prior states, the prescaler circuits do

not retain their state. Thus there will be a slight phase difference created on return to active mode after exiting power saving mode.

Use of the BISW Pin: The HD155004T provides a built-in analog switch for changing the loop filter time constants to shorten the lock-up time. By connecting the BISW pin to the loop filter capacitor, either directly or through an appropriate resistance, the charge pump output can charge the loop filter capacity rapidly. This shortens the lock-up time. (See figure 6.)

To turn the analog switch on, the LE pin must be high.

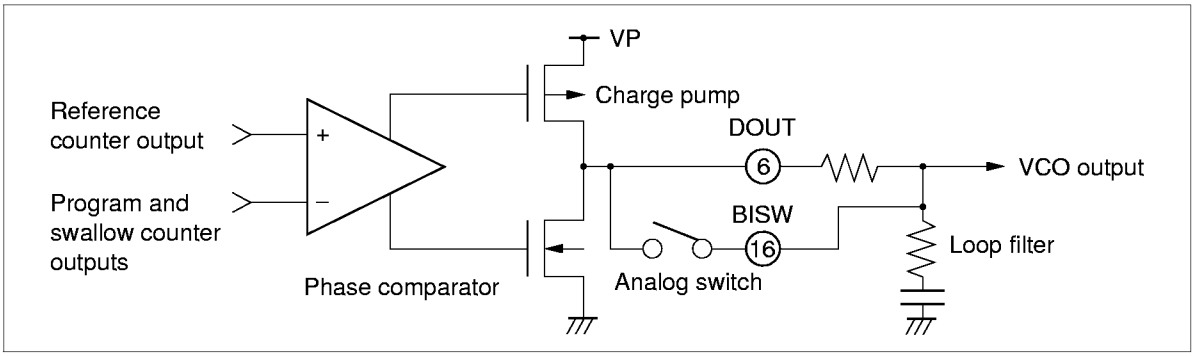


Figure 6 Analog Switch Usage Example

Use of the VP Pin: There are cases where, due to the characteristics of the VCO used, it is necessary to have the dynamic range of the charge pump output exceed the VCC voltage. The HD155004T provides the VP pin as a charge pump drive power supply, separate from the power supply for the prescaler and logic blocks. This pin is not connected to the VCC pin, and therefore the current consumption does not increase if there exist little difference between VCC and VP. (within ±0.3 V).

Please use the power supply that is little noise for the VP pin because the VP pin is charge pump drive.

Internal State Monitoring: The HD155004T provides three monitor pins.

1. FOUT

The FOUT pin is the monitor pin for the reference and program counters. Since these counters are auto-reload counters, the FOUT pin monitors the overflow signals. The FC pin determines which counter is monitored: the reference counter is monitored when FC is high, and the program counter when FC is low.

2. ROUT and POUT

The ROUT and POUT pins monitor the charge pump drive signals. The ROUT pin is the current sink side monitor (NMOS internally), and the POUT pin is the current source monitor (PMOS internally).

Use of the Monitor Pins: Of the monitor pins described above, the ROUT and POUT pins can be used as shown in the circuit in figure 7.

In this case, the external VPEX value should be within ±0.3 V for difference with VCC.

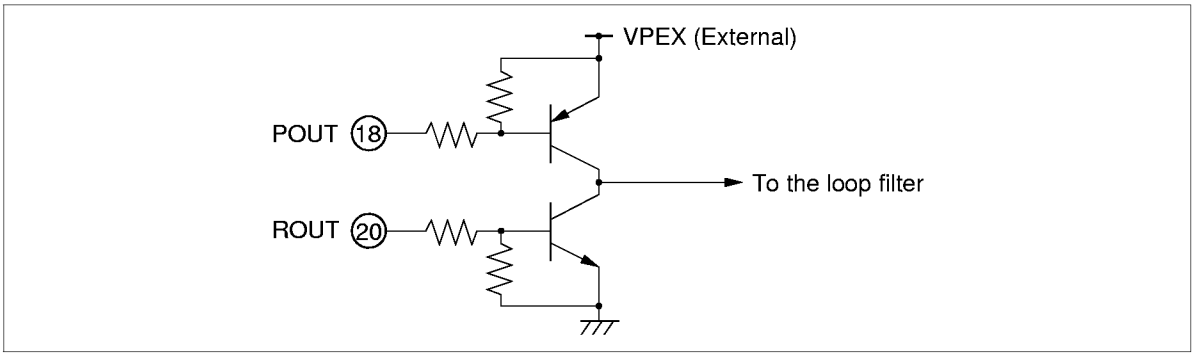


Figure 7 ROUT and POUT Pin Application Example

Absolute Maximum Ratings

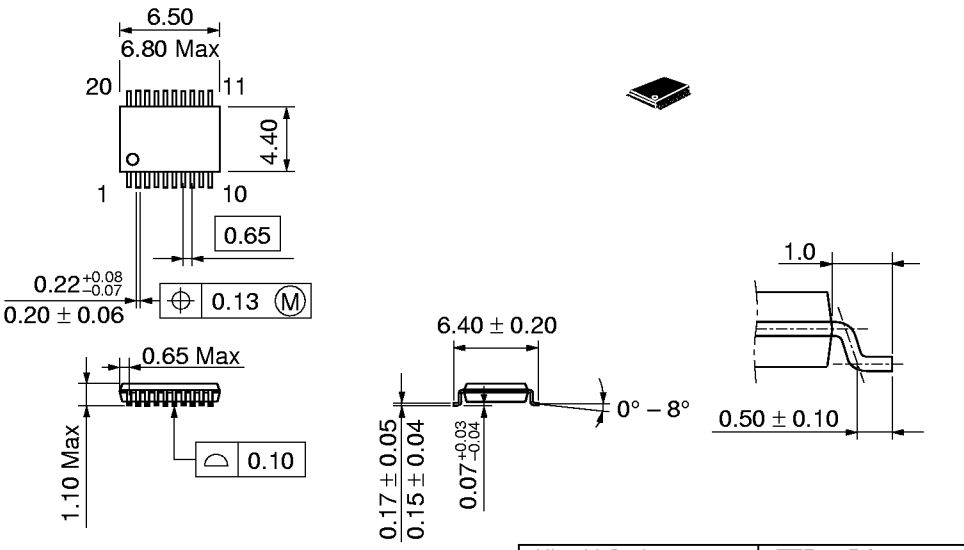
Item	Symbol	Rated Value	Unit
Power supply voltage (VCC)	Vcc	–0.3 to +6.0	V
Power supply voltage (VP)	Vp	Vcc to +6.0	V
Vcc-Vp max voltage difference	ΔV	±0.3	V
Pin voltage	Vt	–0.3 to Vcc+0.3 (6.0 Max)	V
Power dissipation	Pt	400	mW
Operating temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins
Power supply voltage	V_{CC}	2.7	3.0	3.6	V		5
Power supply voltage	V_P	V_{CC}–0.3	3.0	V_{CC}+0.3	V		4
Power supply current	I_{CC}	—	0.8	2.0	mA	V_{CC} = 3.0 V	5
Power saving mode current	I_{PS}	—	100	200	µA	V_{CC} = 3.0 V	
FIN operating frequency	f_{FIN}	10	—	130	MHz	V_{FIN} = 0 dBm	10
OSCIN operating frequency	f_{OSCIN}	0.1	—	20	MHz	V_{OSCIN} = 2 Vpp	1
FIN input voltage	V_{FIN}	–6	—	6	dBm	f_{FIN} = 100 MHz	10
OSCIN input voltage	V_{OSCIN}	0.5	—	V_{CC}	Vpp	f_{OSCIN} = 10 MHz	1
Input voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		9, 11, 13,
	V_{IL}	0	—	0.2 V_{CC}	V		14, 15, 19
Input leakage current	I_L	–1	—	1	µA	0 < V_{IL} < V_{CC}	11, 13
Pull-up resistance	R_{PU}	—	50	—	kΩ		9, 14, 15, 19
Output voltage	V_{OH}	V_{CC}–0.4	—	—	V	–I_{OH} = 0.4 mA	8, 17, 20
	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA	
DOUT output voltage	V_{DOH}	V_{CC}–0.4	—	—	V	–I_{DOH} = 2.0 mA	6
	V_{DOL}	—	—	0.4	V	I_{DOL} = 2.0 mA	
Analog switch on resistance	R_{SW}	—	50	—	Ω		16
POUT output voltage	V_{POUT}	—	—	0.4	V	I_{POUT} = 0.4 mA	18

Package Dimensions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g