HD155121F

RF Transceiver IC for GSM and PCN Dual band cellular systems

HITACHI

ADE-207-265A (Z)
2nd Edition
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Description

The HD155121F is a RF transceiver IC for GSM and PCN dual band cellular systems, and integrates most of the low power silicon functions of a transceiver. The HD155121F incorporates two bias circuits for RF LNAs, two first mixers, a second mixer, a programmable gain amplifier, and an IQ demodulator for the receiver, and an IQ modulator and offset PLL for the transmitter. Also, on chip are dividers for the phase splitter. Moreover the HD155121F includes control circuits to implement power saving modes. These functions can operate down to 2.7 V and are housed in a 48-pin LQFP SMD package.

Hence the HD155121F can form a small size transceiver handset for dual band by adding a dual PLL frequency synthesizer IC, power amplifiers and some external components.

The HD155121F is fabricated using a 0.6 μm double-polysilicon Bi-CMOS process.

Functions

Receiver(Rx)

- Low Noise Amplifier (LNA) bias circuit
- First mixer
- IF amplifier and second mixer
- Programmable Gain Amplifier (PGA)
- IQ demodulator with 90 degree phase splitter

Transmitter(Tx)

- IQ modulator with 90 degree phase splitter
- Offset PLL
  - — Down converter
  - — Phase comparator
  - — TXVCO driver

Others

- IF dividers
- Power saving control circuit
- IFVCO

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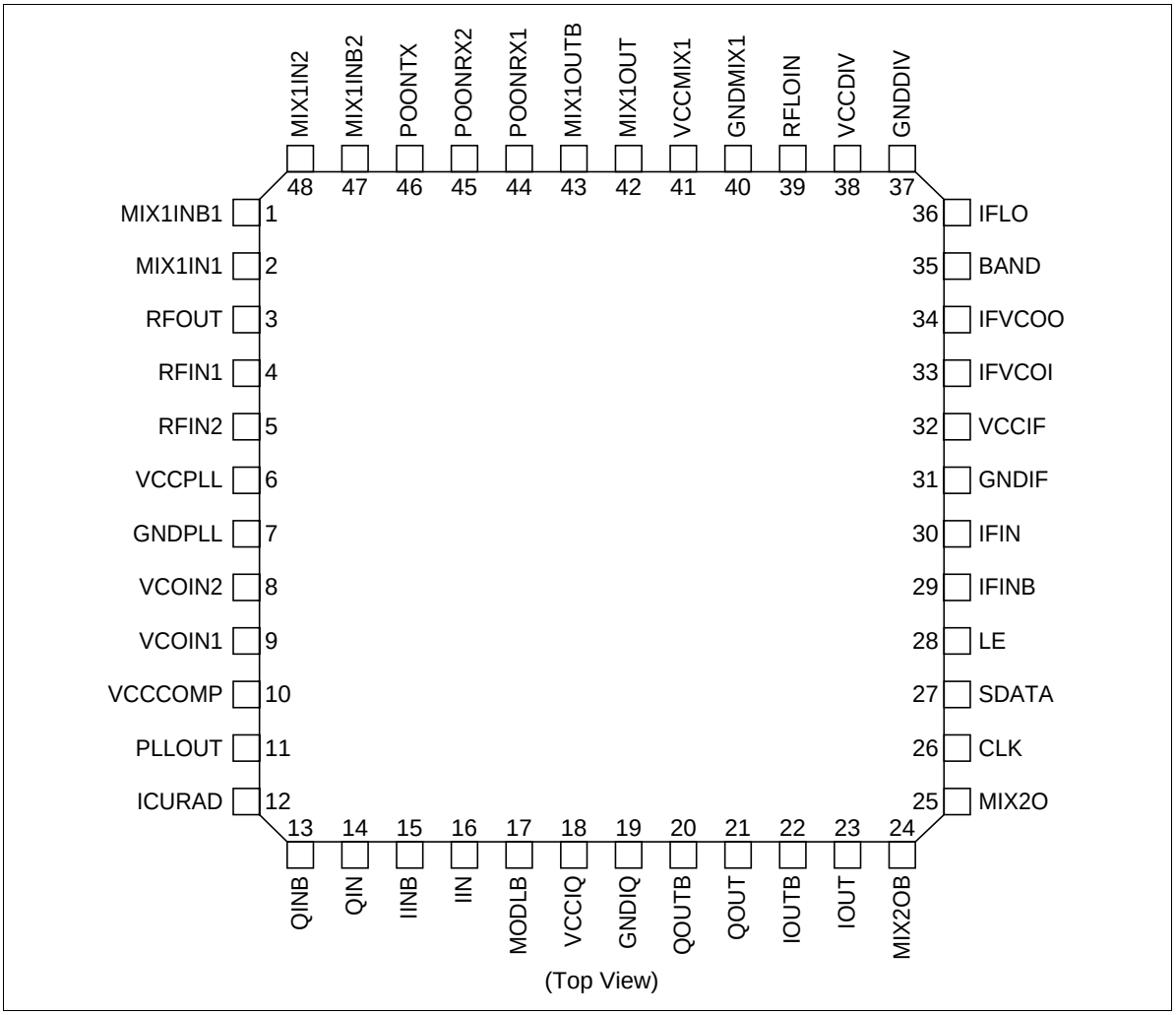
Features

- Highly integrated RF processing for hand-portables
- Operating supply voltage
  - — V_{CC} : 2.7 to 3.6 V
  - — Phase comparator and TXVCO driver circuit : 2.7 to 5.25 V
- Current consumption
  - — Rx mode (GSM) : 53 mA + LNA current
  - — Rx mode (PCN) : 52 mA + LNA current
  - — Tx mode (GSM) : 36 mA
  - — Tx mode (PCN) : 37 mA
  - — Idle mode :1 µA
- Operating temperature : –20 to +75 degree
- LQFP 48pin SMD (Low Profile Quad Flat Package)
- Wide operating frequencies

— Rx	RF	GSM	: 925 - 960 MHz
		PCN	: 1805 - 1880 MHz
	1st IF		: 225 MHz
	2nd IF		: 45 MHz
— Tx	RF	GSM	: 880 - 915 MHz
		PCN	: 1710 - 1785 MHz
	IF	GSM	: 270 MHz
		PCN	: 135 MHz

- Offset PLL architecture for Transmitter
- High dynamic range Programmable Gain Amplifier (PGA)

Pin Arrangement



(Top View)

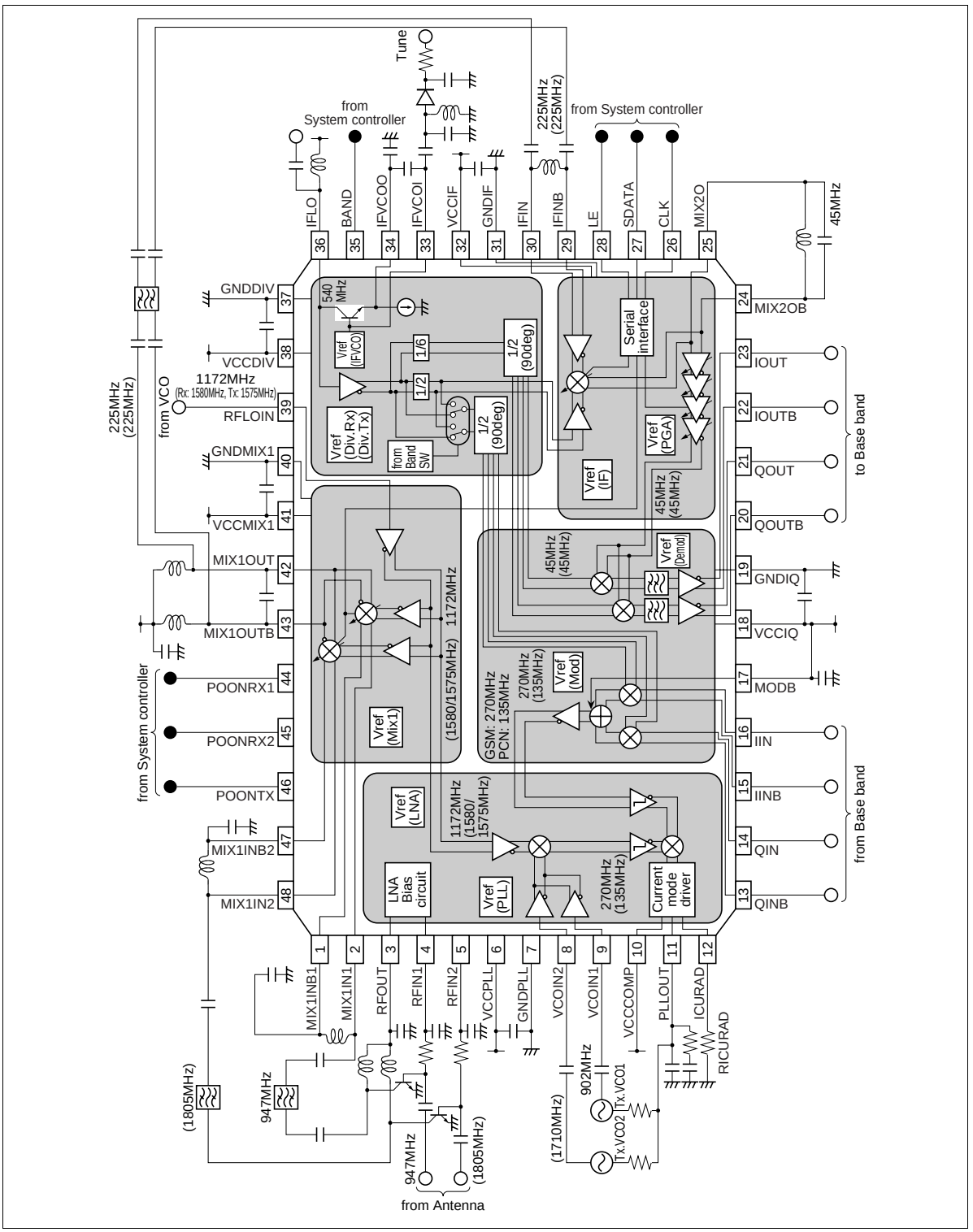
Pin Description

Pin No.	Pin Name	Description
1	MIX1INB1	Negative input for Mixer1 (GSM)
2	MIX1IN1	Positive input for Mixer1 (GSM)
3	RFOUT	Bias for the collector of LNA transistor
4	RFIN1	Bias for the base of LNA transistor (GSM)
5	RFIN2	Bias for the base of LNA transistor (PCN)
6	VCCPLL	V_{CC} for OPLL
7	GNDPLL	GND for OPLL
8	VCOIN2	TxVCO signal input (PCN)
9	VCOIN1	TxVCO signal input (GSM)
10	VCCCOMP	V_{CC} for phase comparator
11	PLLOUT	Current output to control and modulate the TxVCO
12	ICURAD	Phase comparator output current setting
13	QINB	Negative input of Q signal for modulator
14	QIN	Positive input of Q signal for modulator
15	IINB	Negative input of I signal for modulator
16	IIN	Positive input of I signal for modulator
17	MODLB	V_{CC} for modulator load bias
18	VCCIQ	V_{CC} for IQ modulator and demodulator
19	GNDIQ	GND for IQ modulator and demodulator
20	QOUTB	Negative output of Q signal for modulator
21	QOUT	Positive output of Q signal for modulator
22	IOUTB	Negative output of I signal for modulator
23	IOUT	Positive output of I signal for modulator
24	MIX2OB	Negative output for Mixer2
25	MIX2O	Positive output for Mixer2
26	CLK	Clock for serial data
27	SDATA	Serial data for Gain control
28	LE	Load enable for serial data
29	IFINB	Negative input for Mixer2
30	IFIN	Positive input for Mixer2
31	GNDIF	GND for Mixer2 and PGA
32	VCCIF	V_{CC} for Mixer2 and PGA
33	IFVCOI	Base of IFVCO transistor
34	IFVCOO	Emitter of IFVCO transistor

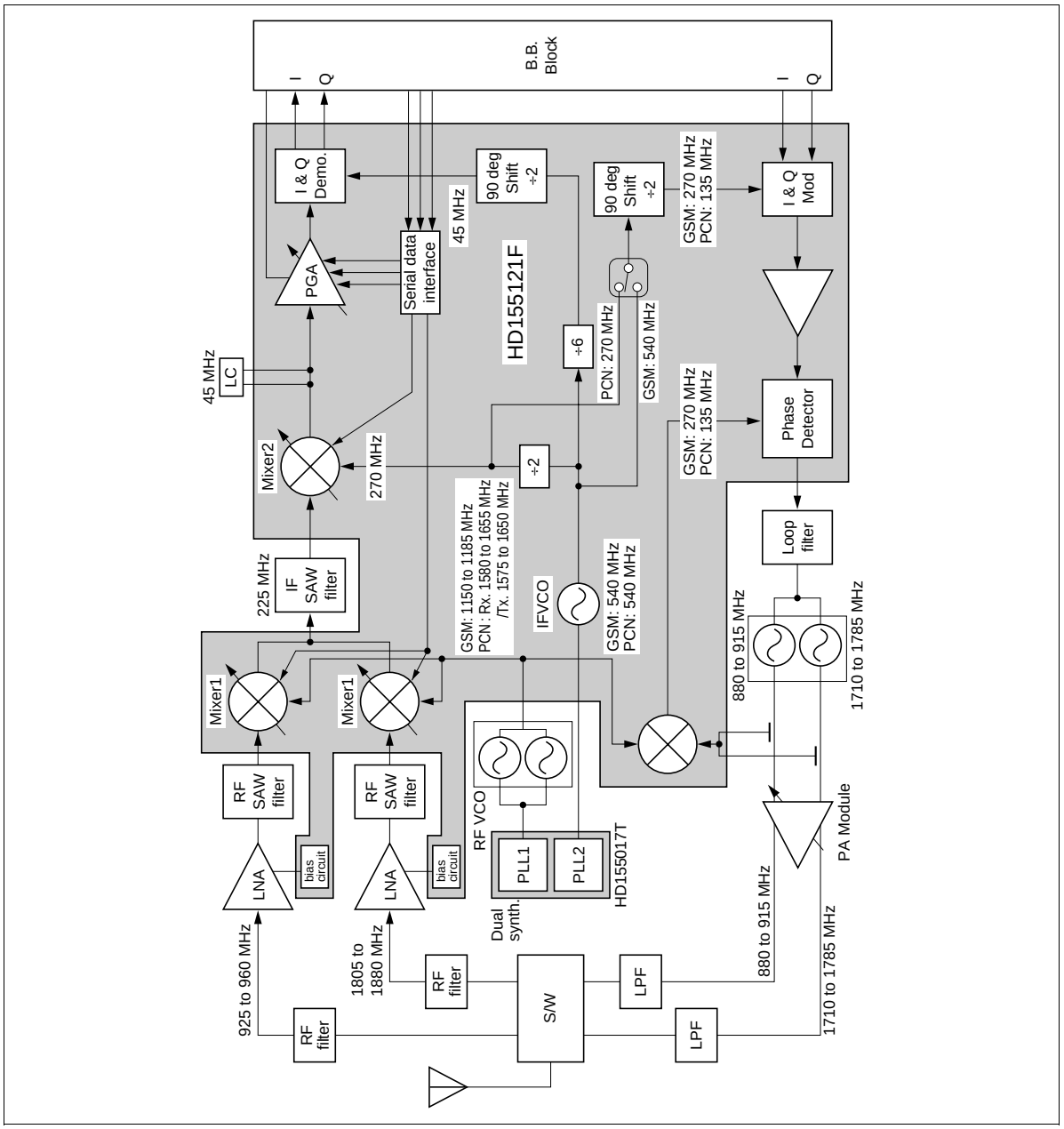
Pin Description (cont)

Pin No.	Pin Name	Description
35	BAND	Band control (Low: GSM, High: PCN)
36	IFLO	Output of IFVCO or Input of IF Local
37	GNDDIV	GND for Divider and IFVCO
38	VCCDIV	V_{cc} for Divider and IFVCO
39	RFLOIN	Input for RF Local
40	GNDMIX1	GND for Mixer1
41	VCCMIX1	V_{cc} for Mixer1
42	MIX1OUT	Positive output for Mixer1 (GSM/PCN)
43	MIX1OUTB	Negative output for Mixer1 (GSM/PCN)
44	POONRX1	Power save control for LNA and Mixer1
45	POONRX2	Power save control for Mixer2, PGA and demodulator
46	POONTX	Power save control for modulator and OPLL
47	MIX1INB2	Negative input for Mixer1 (PCN)
48	MIX1IN2	Positive input for Mixer1 (PCN)

Block Diagram



Configuration



Functional Operation

The HD155121F has been designed from system stand point and incorporated a large number of the circuit blocks necessary in the design of a digital cellular handset.

Receiver Operation

The HD155121F incorporates two LNA bias circuits for external RF transistors, whose NF and power gain can be better selected.

This circuit amplifies the RF signal after selection by the antenna filter before the signal enters the first mixer section. The RF signal is combined with a local oscillator (LO) signal to generate a wanted first IF signal in the 130 - 300 MHz range. The first mixer circuit uses a double-balanced Gilbert cell architecture, which has open collector differential outputs. If, at 225 MHz, a 800 Ω LC load is connected to the mixer's outputs then a SSB NF of 9.0 dB (GSM), 9.1 dB (PCN) with a gain of 9.5 dB (GSM), 8.5 dB (PCN) is realizable. The corresponding input compression point is –10.5 dBm (GSM), –12.5 dBm (PCN), which allows the device to be used within a GSM and EGSM and PCN system.

A filter is used after the first mixer to provide image rejection and the conditioned signal is then passed through an intermediate amplifier, before being down converted to a second IF in the range of 26 - 60 MHz.

The second mixer can generate a 45 MHz second IF, if a 270 MHz second local signal is used. The second mixer also uses the Gilbert cell architecture, but with internal resistive differential outputs of 300 Ω. If amplifier and second mixer has a SSB NF of 6.0 dB, a power gain of 13 dB and a input compression point of –22 dBm. In order to improve the blocking characteristics of the device an external LC resonator across the differential outputs of the second mixer is recommended.

First mixer and second mixer can switch the power gain. Switching gain step of first mixer is 12 dB, and such step of second mixer is 16 dB.

The signal is then passed to the PGA circuit, which has a dynamic range of more than 80 dB (–42 dB - +56 dB typ.) and is controlled by digital serial data, which is generated by the microprocessor. This gain step is 2 dB.

The signal is then down converted by a demodulator to I and Q. Internal divider circuits convert the IFLO signal to the same frequency as the second IF before passing this local signal through a phase splitter / shifter in order to generate the in phase and quadrature phase IQ components. The phase accuracy of the IQ demodulator is less than +/–1 degree and the amplitude mismatch is less than +/–0.5 dB. In order to accommodate different baseband interfaces the HD155121F IQ differential outputs have a voltage swing of 1.6 Vpp and DC offset of less than +/–60 mV. Within each output stage a second order Butterworth filter (fc = 210 kHz) is used to improve the blocking performance of the device.

In order to allow flexibility in circuit implementation the HD155121F can configured to use either a single-ended or balanced external circuitry and components.

Transmitter Operation

The transmitter chain converts differential IQ baseband signals to a suitable format for transmission by a power amplifier.

The common mode voltage range of the modulator inputs is 0.8 V to 1.2 V and they have 2.0 Vpp differential swing. The modulator circuit uses double-balanced mixers for the I and Q paths. The Local signals are generated by dividing the IFLO signals by 2, and then passed to the modulator through a phase splitter / shifter. The IF signals generated are then summed to produce a single modulated IF signal which is amplified and fed into the offset PLL block. Carrier suppression due to the mixer circuit is better than 31 dBc. If the common mode DC voltage of the I and Q inputs is adjusted, carrier suppression is better than 40 dBc easily. Side band suppression is better than 35 dBc without adjustment.

Within the offset PLL block there are a down converter, a phase comparator and a VCO driver. The down converter mixes the first local signal and the TXVCO signal to create a reference local signal for use in the offset PLL circuit. The phase comparator and the VCO driver generate an error current, which is proportional to the phase differential between the reference IF and the modulated IF signals. This current is used in a second order loop filter to generate a voltage, which in turn modulates the TXVCO. In order to optimize the PLL loop gain, the error current value can be modified by changing the value of an external resistor - ICURAD. In order to accommodate various control range of TXVCOs, the offset PLL circuit has been designed to operate with a supply voltage up to 5.25 V.

Operation Modes

The HD155121F has necessary control circuitry to implement the necessary states within the dual band system. Also provided is a power saving mode which reduces the current consumption of the device by powering down unnecessary function blocks. Three pins are assigned for power saving mode control, POONRX1, POONRX2 and POONTX. Also one pin is assigned for switching operational band, BAND. Table 1 shows the relationship between the pins and the required operating mode. These pins are controlled by the system controller.

As per GSM requirements the Tx and Rx sections do not operate simultaneously. For the receiver there is a calibration mode in which the LNA bias circuit and first mixer are switched off. During this period the gain of the PGA can be adjusted. Also the DC offsets of the IQ demodulator are measured and subsequently canceled.

In order to change between the Rx and Tx modes a state called "warm-up" is used to ensure that the local signals are not unduly affected. This method of switching between Tx and Rx ensures that lock is achieved first time.

Power saving is implemented through use of the idle mode. All function blocks of the HD155121F are switched off until such time as the system controller commands the device to power up again.

Table 1 Operating Modes with Power Saving

Mode		**Receive**		**Calibrate**	**Warm-up**	**Transmit**		**Idle**
Band		**GSM**	**PCN**	**—**	**—**	**GSM**	**PCN**	**—**
POONRX1 (44)		H	H	L	L	L	L	H
POONRX2 (45)		H	H	H	L	L	L	L
POONTX (46)		L	L	L	L	H	H	Don't care
BAND (35)		L	H	Don't care	Don't care	L	H	Don't care
Rx block	LNA bias (GSM)	ON	OFF	OFF	OFF	OFF	OFF	OFF
	LNA bias (PCN)	OFF	ON	OFF	OFF	OFF	OFF	OFF
	1st Mixer (GSM)	ON	OFF	OFF	OFF	OFF	OFF	OFF
	1st Mixer (PCN)	OFF	ON	OFF	OFF	OFF	OFF	OFF
	2nd Mixer	ON	ON	ON	OFF	OFF	OFF	OFF
	PGA	ON	ON	ON	OFF	OFF	OFF	OFF
	I/Q demodulator	ON	ON	ON	OFF	OFF	OFF	OFF
Tx block	Offset PLL	OFF	OFF	OFF	OFF	ON	ON	OFF
	I/Q modulator	OFF	OFF	OFF	OFF	ON	ON	OFF
Oscillator block	IF VCO	ON	ON	ON	ON	ON	ON	OFF
	Divider (Rx)	ON	ON	ON	OFF	OFF	OFF	OFF
	Divider (Tx)	OFF	OFF	OFF	OFF	ON	ON	OFF
	1st local buffer	ON	ON	ON	ON	ON	ON	OFF
	IF local buffer	ON	ON	ON	ON	ON	ON	OFF
Total current		53 mA	52 mA	34 mA	9.0 mA	36 mA	37 mA	1 μA

Absolute Maximum Ratings

Any stress in excess of the absolute maximum ratings can cause permanent damage to the HD155121F.

Item	Symbol	Rating	Unit
Power supply voltage (V_{CC})	V_{CC}	–0.3 to +4.0	V
Power supply voltage (V_{CCCOMP})	V_{CCCOMP}	–0.3 to +5.5	V
Pin voltage	V_T	–0.3 to V_{CC}+0.3 (4.0 Max)	V
Maximum power dissipation	P_T	400	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

DC Specifications (V_{CC} = 3 V, Ta = 25°C unless otherwise specified.)

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Power supply voltage (V_{CC})		2.7	3.0	3.6	V		
Power supply voltage (V_{CCCOMP})		2.7	3.0	5.25	V		
Power supply current (Rx.)	GSM	—	53.0	74.0	mA	V_{CC} = 3.0V, V_{CCCOMP} = 3.0V,	2
	PCN	—	52.0	73.0	mA	Mixer1, 2 = Gain1, PGA = bitNo26	
Power supply current (Tx.)	GSM	—	36.0	50.0	mA	V_{CC} = 3.0V, V_{CCCOMP} = 3.0V	2
	PCN	—	37.0	52.0	mA		
Power supply current (Warm-up)		—	9.0	12.5	mA	V_{CC} = 3.0V, V_{CCCOMP} = 3.0V	2
Power saving mode supply current		—	1.0	10.0	µA	V_{CC} = 3.0V, V_{CCCOMP} = 3.0V High level = VCC, Low level = 0V at mode control pin and serial data pin (POONRX1, RX2, TX, BAND, CLK (no clock signal), SDATA, LE)	2
Power up time (Rx.)		—	1.5	5.0	µsec	from PS mode	1
Power up time (Tx.)		—	0.2	0.5	µsec	from PS mode	1
Power on control voltage range (POONRX1, POONRX2, POONTX)		2.3	—	—	V		
Power off control voltage range (POONRX1, POONRX2, POONTX)		—	—	0.8	V		
I/Q common-mode output voltage		1.15	1.35	1.55	V		
I/Q maximum output swing (Single ended)		0.8	1.06	—	Vp-p	VIOUT, VIOUTB, VQOUT, VQOUTB	
I/Q output DC offset voltage		–60	0	60	mV	VIOUTDC – VIOUTBDC, VQOUTDC, VQOUTBDC	
I/Q common-mode input voltage		0.8	1.0	1.2	V		1
I/Q input swing (Single ended)		0.8	1.0	1.2	Vp-p	VIIN, VIINB, VQIN, VQINB	1
Serial data VH (CLK, SDATA, LE)		2.3	—	—	V		
Serial data VL (CLK, SDATA, LE)		—	—	0.8	V		
Band control VH (BAND)		2.3	—	—	V		
Band control VL (BAND)		—	—	0.8	V		
Input current (POONRX1, POONRX2, POONTX, BAND, CLK, SDATA, LE)		–10	0	10	µA		

Note: 1. These values are not tested in mass production.
2. Power supply current does not include the LNA bias current.

AC Specifications (V_{CC} = 3 V, Ta = 25°C unless otherwise specified.)

- LNA Bias circuit specifications

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
LNA transistor bias current	GSM	4.7	5.6	—	mA		
	PCN	4.7	5.6	—	mA		
Frequency	GSM	925	—	960	MHz		1
	PCN	1805		1880	MHz		
Power gain	GSM	—	19.4	—	dB	RF = 940 MHz	1
	PCN	—	13.4	—	dB	RF = 1842 MHz	
Noise figure	GSM	—	1.6	—	dB	RF = 940 MHz	1
	PCN	—	1.6	—	dB	RF = 1842 MHz	
3rd order input intercept point	GSM	—	–6.0	—	dBm		1
	PCN	—	–2.0	—	dBm		
3rd order output intercept point	GSM	—	13	—	dBm		1
	PCN	—	11	—	dBm		
1dB input compression point	GSM	—	–14.5	—	dBm		1
	PCN	—	–9.5	—	dBm		
1dB output compression point	GSM	—	3.9	—	dBm		1
	PCN	—	2.9	—	dBm		
Output (RF) Z	GSM	—	50	—	Ω	Output (GSM RF)	1
	PCN	—	50	—	Ω	Output (PCN RF)	
Input (RF) Z	GSM	—	50	—	Ω	Input (GSM RF)	1
	PCN	—	50	—	Ω	Input (PCN RF)	

Note: 1. These AC characteristics are shown for reference only and do not form part of the HD155121F component specification.

- Mixer1 specifications (Differential output load between pin42 and pin43 = 800 Ω)

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Frequency (RF)	GSM	925	—	960	MHz		1
	PCN	1805	—	1880	MHz		
Frequency (LO)	GSM	1125	—	1260	MHz		1
	PCN	1505	—	1680	MHz		
Frequency (IF)	—	200	225	300	MHz		1
RFLO input level	—	–8.0	—	—	dBm		
Conversion gain 1	GSM	6.5	9.5	12.5	dB	RF = 940MHz, LO = 1165MHz, IF = 225MHz	2
	PCN	5.5	8.5	11.5	dB	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
Conversion gain 2	GSM	–5.5	–2.5	0.5	dB	RF = 940MHz, LO = 1165MHz, IF = 225MHz	2
	PCN	–6.5	–3.5	–0.5	dB	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
Noise figure 1	GSM	—	9.0	10.5	dB	RF = 940MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	—	9.1	10.6	dB	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
Noise figure 2	GSM	—	15.0	16.5	dB	RF = 940MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	—	16.0	17.5	dB	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
3rd order input intercept point 1	GSM	–3.0	–1.0	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	–6.0	–4.0	—	dBm	RF1 = 1842.8MHz, RF2 = 1843.6MHz, LO = 1617MHz, IF = 225MHz	
3rd order input intercept point 2	GSM	1.0	3.0	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	–3.0	–1.0	—	dBm	RF1 = 1842.8MHz, RF2 = 1843.6MHz, LO = 1617MHz, IF = 225MHz	
3rd order output intercept point 1	GSM	6.5	8.5	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	2.5	4.5	—	dBm	RF1 = 1842.8MHz, RF2 = 1843.6MHz, LO = 1617MHz, IF = 225MHz	
3rd order output intercept point 2	GSM	–1.5	0.5	—	dBm	RF1 = 940.8MHz, RF2 = 941.6MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	–6.5	–4.5	—	dBm	RF1 = 1842.8MHz, RF2 = 1843.6MHz, LO = 1617MHz, IF = 225MHz	
1dB input compression point 1	GSM	–12.5	–10.5	—	dBm	RF = 940MHz, LO = 1165MHz, IF = 225MHz	2
	PCN	–14.5	–12.5	—	dBm	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
1dB input compression point 2	GSM	–8.5	–6.5	—	dBm	RF = 940MHz, LO = 1165MHz, IF = 225MHz	2
	PCN	–10.5	–8.5	—	dBm	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
1dB output compression point 1	GSM	–4.0	–2.0	—	dBm	RF = 940MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	–7.0	–5.0	—	dBm	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	
1dB output compression point 2	GSM	–12.0	–10.0	—	dBm	RF = 940MHz, LO = 1165MHz, IF = 225MHz	1, 2
	PCN	–15.0	–13.0	—	dBm	RF = 1842MHz, LO = 1617MHz, IF = 225MHz	

Note: 1. These values are not tested in mass production.
2. The loss (2.2 dB) of test circuit at Mixer1 output is calculated.

- Mixer2 specifications

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Frequency (IF1)		200	225	300	MHz		1
Frequency (LO2)		240	270	360	MHz	LO2 = IFLO/2	1
Frequency (IF2)		40	45	60	MHz		1
IFLO input level		–10	—	—	dBm		
Conversion gain 1		10.5	13.0	15.5	dB	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	2
Conversion gain 2		–5.5	–3.0	–0.5	dB	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	2
Noise figure 1		—	6.0	7.5	dB	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	1, 2
Noise figure 2		—	12.0	13.5	dB	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	1, 2
3rd order input intercept point 1		–15.0	–13.0	—	dBm	IF1 = 225.8MHz, IF2 = 226.6MHz, LO = 540MHz, 2ndIF = 45MHz	1, 2
3rd order input intercept point 2		–11.0	–9.0	—	dBm	IF1 = 225.8MHz, IF2 = 226.6MHz, LO = 540MHz, 2ndIF = 45MHz	1, 2
3rd order output intercept point 1		–2.0	0.0	—	dBm	IF1 = 225.8MHz, IF2 = 226.6MHz, LO = 540MHz, 2ndIF = 45MHz	1, 2
3rd order output intercept point 2		–14.0	–12.0	—	dBm	IF1 = 225.8MHz, IF2 = 226.6MHz, LO = 540MHz, 2ndIF = 45MHz	1, 2
1dB input compression point 1		–24.0	–22.0	—	dBm	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	2
1dB input compression point 2		–21.0	–19.0	—	dBm	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	2
1dB output compression point 1		–12.0	–10.0	—	dBm	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	1, 2
1dB output compression point 2		–24.0	–22.0	—	dBm	IF1 = 225MHz, IFLO = 540MHz, IF2 = 45MHz	1, 2
Isolation		50	—	—	dB	between Mixer1 output and Mixer2 input	1, 2

Note: 1. These values are not tested in mass production.
2. The loss (3.6 dB) of test circuit at Mixer2 output is calculated.

- PGA and IQ Demodulator specifications (terminated by 10 kΩ at IQ demodulator output)

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Input frequency		40	45	60	MHz		1
Gain range		—	98	—	dB		1
Gain linearity		–0.8	—	0.8	dB	(in any 20dB window)	1
Gain step		—	2	—	dB		1
Noise figure 1		—	10.9	14	dB	IF2 = 45MHz, bitNo46	1, 2
Noise figure 2		—	21.2	24	dB	IF2 = 45MHz, bitNo26	1, 2
Noise figure 3		—	53.4	60	dB	IF2 = 45MHz, bitNo6	1, 2
Gain 1		47.0	51.5	56.0	dB	IF2 = 45MHz, bitNo46	2
Gain 2		7.0	11.5	16.0	dB	IF2 = 45MHz, bitNo26	2
Gain 3		–33.0	–28.5	–24.0	dB	IF2 = 45MHz, bitNo6	2
i/p CP 1		–70.5	–66	—	dBm	IF2 = 45MHz, bitNo46	2
i/p CP 2		–37	–34	—	dBm	IF2 = 45MHz, bitNo26	2
i/p CP 3		–14	–11	—	dBm	IF2 = 45MHz, bitNo6	2
IQ phase accuracy		—	0.2	1.0	deg.	Baseband = 67.7kHz	
IQ amplitude mismatch		—	0.1	0.5	dB	Baseband = 67.7kHz	2
Output DC offset voltage		0	—	| 60 |	mV	| IOUT–IOUTB | and | QOUT–QOUTB | Load out = 10kΩ	
IQ maximum output swing (Single ended)		0.8	1.06	—	Vp-p	Baseband = 67.7kHz IOUT, IOUTB, QOUT, QOUTB Load out = 10kΩ	
I/Q common mode output voltage		1.15	1.35	1.55	V		

Note: 1. These values are not tested in mass production.
2. The loss (3.6 dB) of test circuit at PGA input is calculated.

- IQ Modulator and Offset PLL specifications (IFLO is supplied by signal generator equipment)

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Frequency (RF)	GSM	880	—	915	MHz		1
	PCN	1710	—	1785	MHz		
Frequency (LO)	GSM	1150	—	1185	MHz		1
	PCN	1530	—	1665	MHz		
Frequency (IF)	GSM	—	270	—	MHz		
	PCN	—	135	—	MHz		
RFLO input level		–8	—	—	dBm		
IFLO input level		–20	–10	—	dBm		
VCOIN1 & VCOIN2 input level		–25	–15	–10	dBm		1
Carrier suppression ratio		31	40	—	dBc	All ‘1’ GMSK (Differential encode: off) (Baseband = 67.7kHz)	
Side-band suppression ratio		35	40	—	dBc	I/Q input swing = 1.0Vp-p, I/Q common mode input voltage = 1.0Vdc	
Phase accuracy	GSM	—	1.0	2.5	RMS	200kHz BW	1
	GSM	—	3.0	7.5	peak	200kHz BW	
	PCN	—	1.0	2.4	RMS	200kHz BW	
	PCN	—	3.0	7.0	peak	200kHz BW	
Modulation spectrum	GSM	—	–34.0	—	dB	200kHz offset	1
	PCN	—	–34.5	—	dB	30kHz bandwidth	
Spectrum analyzer condition	GSM	—	–68.0	—	dB	400kHz offset	1
Detector mode: positive peak	PCN	—	–67.0	—	dB	30kHz bandwidth	
	GSM	—	–71.0	—	dB	600kHz to 1.8MHz offset	1
	PCN	—	–70.0	—	dB	30kHz bandwidth	
	GSM	—	–71.5	—	dB	1.8MHz to 3MHz offset	1
	PCN	—	–72.0	—	dB	100kHz bandwidth	
	GSM	—	–74.0	—	dB	3MHz to 6MHz offset	1
	PCN	—	–74.0	—	dB	100kHz bandwidth	
	GSM	—	–76.0	—	dB	6MHz upward offset	1
	PCN	—	–76.0	—	dB	100kHz bandwidth	
Isolation of the 1st local input to TxVCO input		—	43	—	dB		1
IQ input swing (Single ended)		0.8	1.0	1.2	Vp-p	IIN, IINB, QIN, QINB	1
I/Q common mode input voltage		0.8	1.0	1.2	V	IIN, IINB, QIN, QINB	1
PLLOUT output current ratio		—	1:0.5	—		IPLLOUT GSM : IPLLOUT PCN	1
Phase detector offset current ratio		0.30	0.35	0.45		offset current / output current IIN = 1.5V (DC), IINB = 0.5V (DC) QIN = 1.5V (DC), QINB = 0.5V (DC)	1

Note: 1. These values are not tested in mass production.

- IQ Modulator and Offset PLL specifications (IFLO is supplied by signal generator equipment) (cont)

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Tx noise in Rx band	GSM	—	–155.1	—	dBc/Hz	925MHz to 935MHz - 10MHz up from Txband	1
	GSM	—	–164.1	—	dBc/Hz	935MHz to 960MHz - 20MHz up from Txband	
	PCN	—	–156	—	dBc/Hz	1805MHz - 20MHz up from Txband	
	PCN	—	–162	—	dBc/Hz	1850MHz - 65MHz up from Txband	
Lock up time	GSM	—	35	80	µsec		1
	PCN	—	65	80	µsec		

Note: 1. These values are not tested in mass production.

- IFVCO specifications

Item	Mode	Min	Typ	Max	Unit	Test Condition
Bias current		0.9	2.0	2.5	mA	

Rx Gain Control Stage

The PGA amplifier of the HD155121F is the main Rx gain control stage. However, Mixer1 and Mixer2 gain level can switched as an optional function in order to optimize system performance.

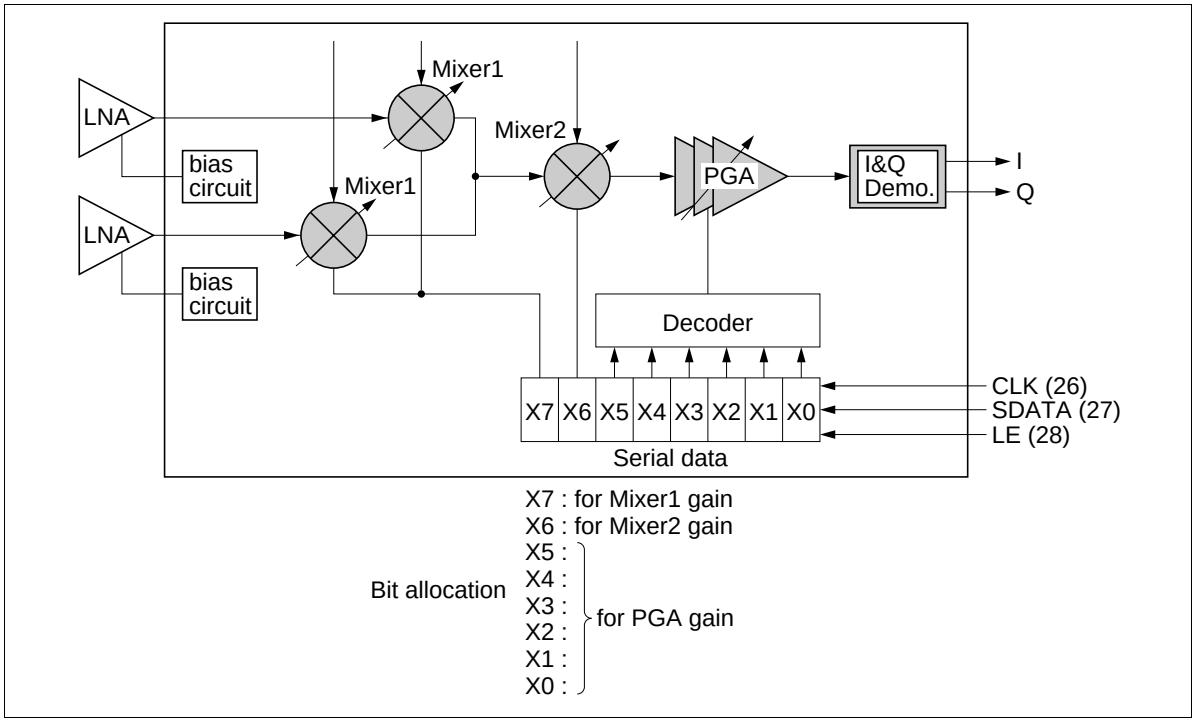


Figure 1

Table 2 First Mixer Gain Control Table (as optional function)

Item	Band	Gain (typ)	X7
Gain 1 (normal gain)	GSM	9.5 dB	0
	PCN	8.5 dB	0
Gain 2 (low gain)	GSM	–2.5 dB	1
	PCN	–3.5 dB	1

Table 3 Second Mixer Gain Control Table (as optional function)

Item	Gain (Typ)	X6
Gain 1 (normal gain)	13.0 dB	0
Gain 2 (low gain)	–3.0 dB	1

Table 4 PGA and IQ Demodulator Block Gain Control

bitNo	Gain (dB) (Typ)	Bit Allocation					
		X5	X4	X3	X2	X1	X0
49	57.5	1	1	0	0	0	1
48	55.5	1	1	0	0	0	0
47	53.5	1	0	1	1	1	1
46	51.5	1	0	1	1	1	0
45	49.5	1	0	1	1	0	1
44	47.5	1	0	1	1	0	0
43	45.5	1	0	1	0	1	1
42	43.5	1	0	1	0	1	0
41	41.5	1	0	1	0	0	1
40	39.5	1	0	1	0	0	0
39	37.5	1	0	0	1	1	1
38	35.5	1	0	0	1	1	0
37	33.5	1	0	0	1	0	1
36	31.5	1	0	0	1	0	0
35	29.5	1	0	0	0	1	1
34	27.5	1	0	0	0	1	0
33	25.5	1	0	0	0	0	1
32	23.5	1	0	0	0	0	0
31	21.5	0	1	1	1	1	1
30	19.5	0	1	1	1	1	0
29	17.5	0	1	1	1	0	1
28	15.5	0	1	1	1	0	0
27	13.5	0	1	1	0	1	1
26	11.5	0	1	1	0	1	0
25	9.5	0	1	1	0	0	1
24	7.5	0	1	1	0	0	0
23	5.5	0	1	0	1	1	1
22	3.5	0	1	0	1	1	0
21	1.5	0	1	0	1	0	1
20	–0.5	0	1	0	1	0	0
19	–2.5	0	1	0	0	1	1
18	–4.5	0	1	0	0	1	0
17	–6.5	0	1	0	0	0	1
16	–8.5	0	1	0	0	0	0
15	–10.5	0	0	1	1	1	1
14	–12.5	0	0	1	1	1	0
13	–14.5	0	0	1	1	0	1
12	–16.5	0	0	1	1	0	0
11	–18.5	0	0	1	0	1	1
10	–20.5	0	0	1	0	1	0
9	–22.5	0	0	1	0	0	1
8	–24.5	0	0	1	0	0	0
7	–26.5	0	0	0	1	1	1
6	–28.5	0	0	0	1	1	0
5	–30.5	0	0	0	1	0	1
4	–32.5	0	0	0	1	0	0
3	–34.5	0	0	0	0	1	1
2	–36.5	0	0	0	0	1	0
1	–38.5	0	0	0	0	0	1
0	–40.5	0	0	0	0	0	0

Serial Data Interface

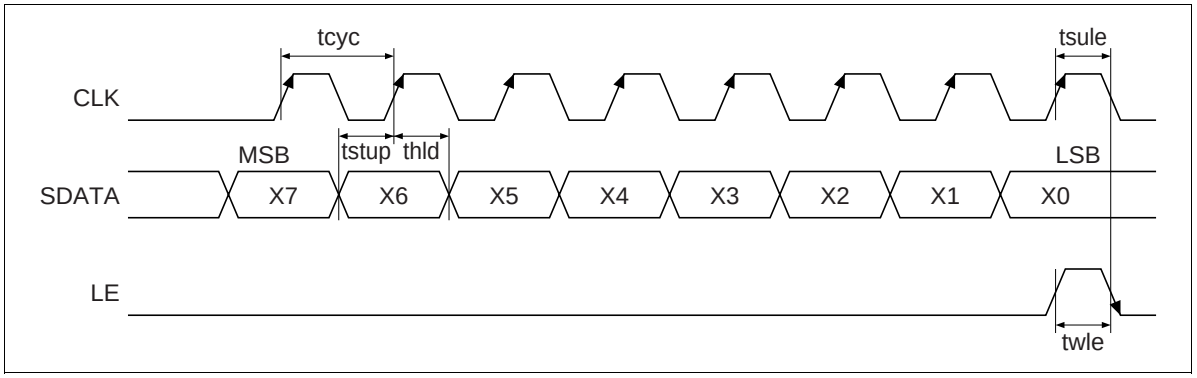


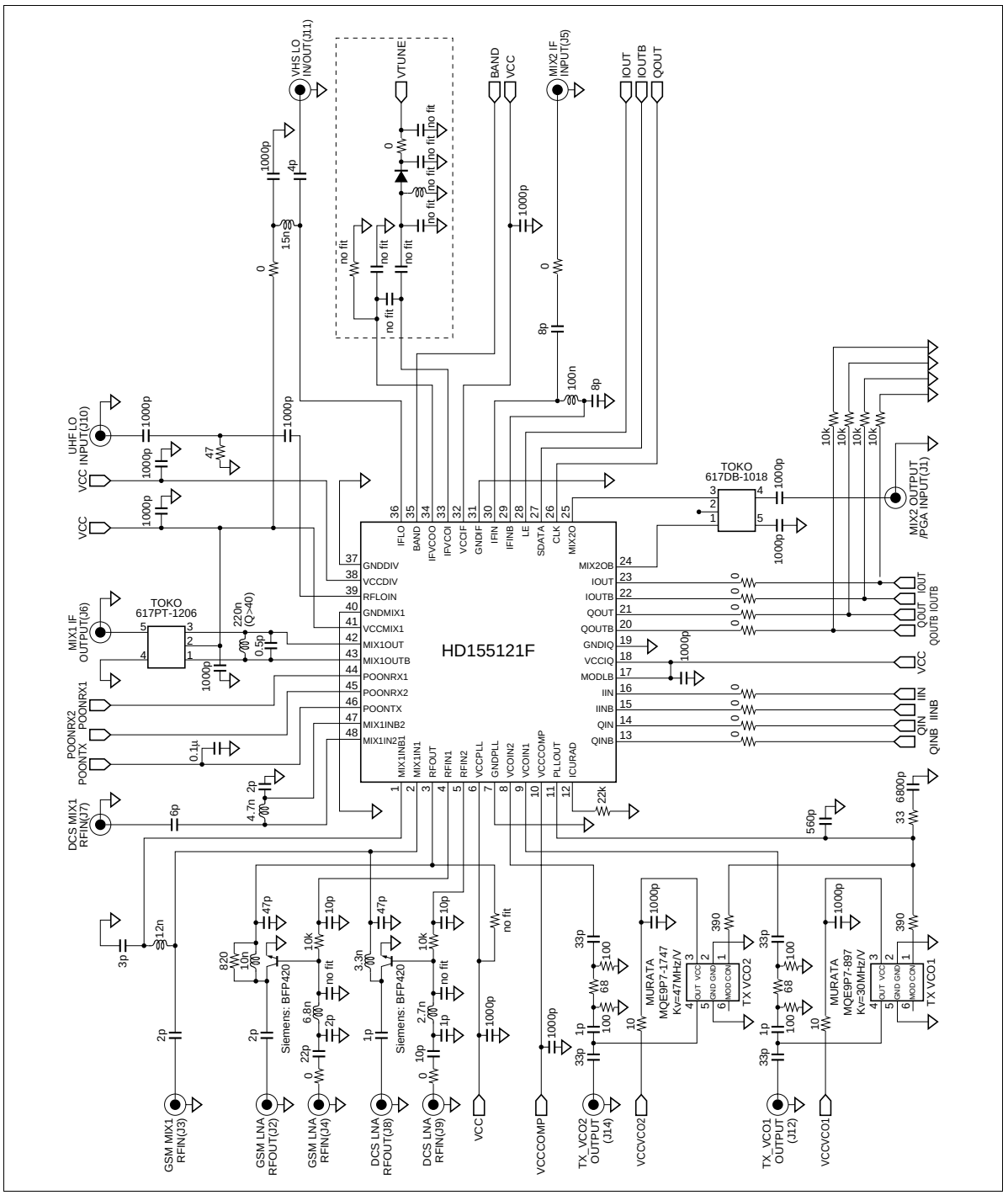
Figure 2 Three-Wire Bus Timing Diagram

Serial Data Interface Specifications (V_{CC} = 3 V, Ta = 25°C unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Cycle time	tcyc	50	—	—	nsec		1
Setup time	tstup	10	—	—	nsec		1
Hold time	thld	10	—	—	nsec		1
LE setup time	tsule	25	—	—	nsec		1
LE width	twle	25	—	—	nsec		1

Note: 1. These values are not tested in mass production.
2. User can program the data for the PGA, while in any state.

Test Circuit



Typical Performance

Power Supply Current Typical Performance

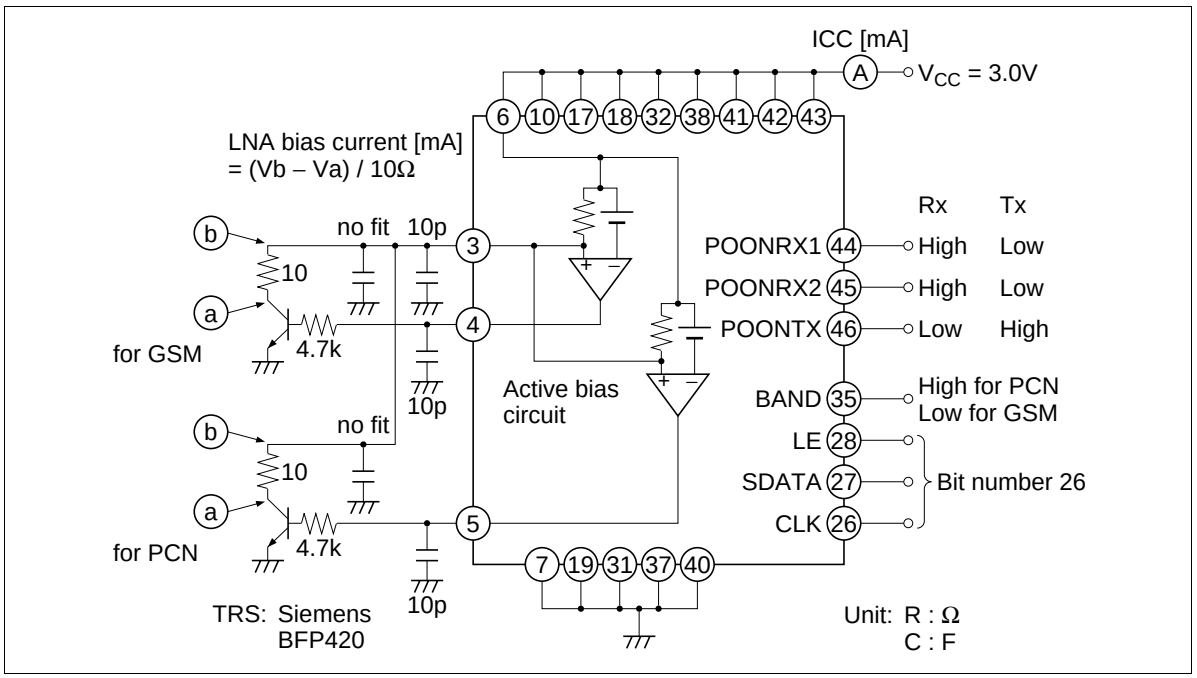


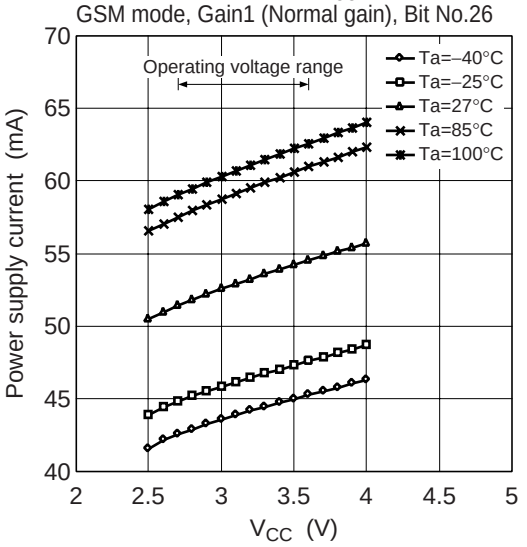
Figure 3

Power supply current does not include the LNA bias current calculated by below formula.

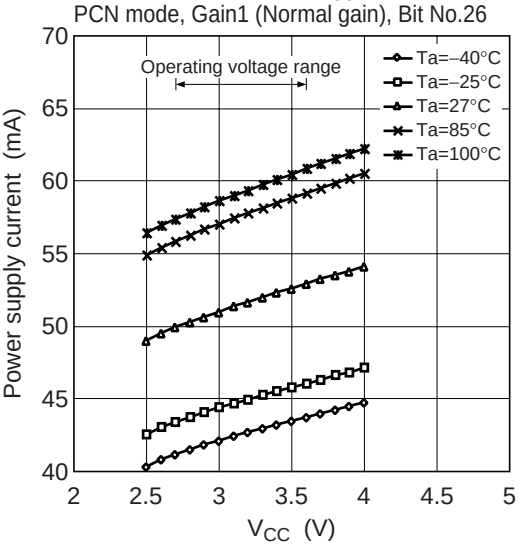
Power supply current [mA] = ICC [mA] – LNA Bias current [mA]

Power Supply Current Typical Performance (cont)

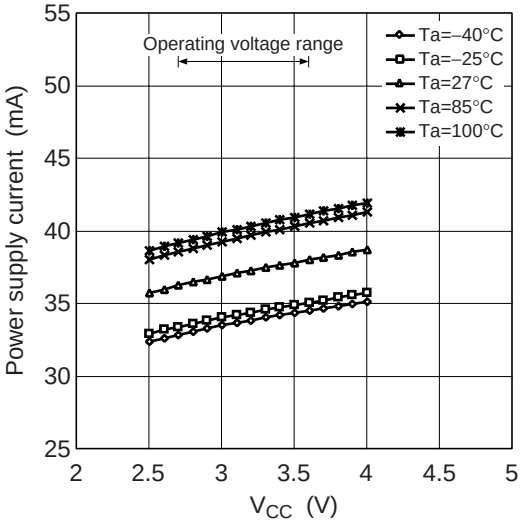
Receive mode
Power supply current vs. V_{CC} and Temperature
GSM mode, Gain1 (Normal gain), Bit No.26



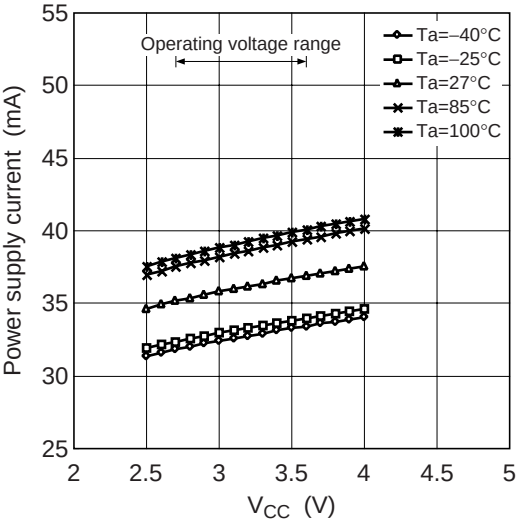
Receive mode
Power supply current vs. V_{CC} and Temperature
PCN mode, Gain1 (Normal gain), Bit No.26



Transmit mode
Power supply current vs. V_{CC} and Temperature
GSM mode



Transmit mode
Power supply current vs. V_{CC} and Temperature
PCN mode



LNA Bias Circuit Typical Performance

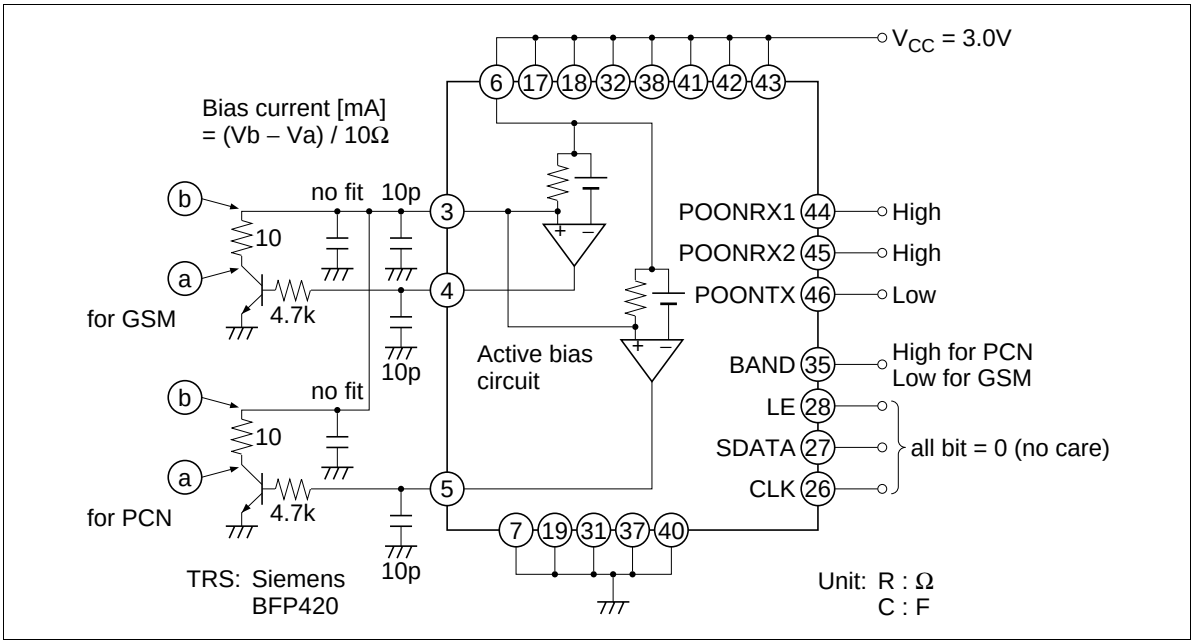
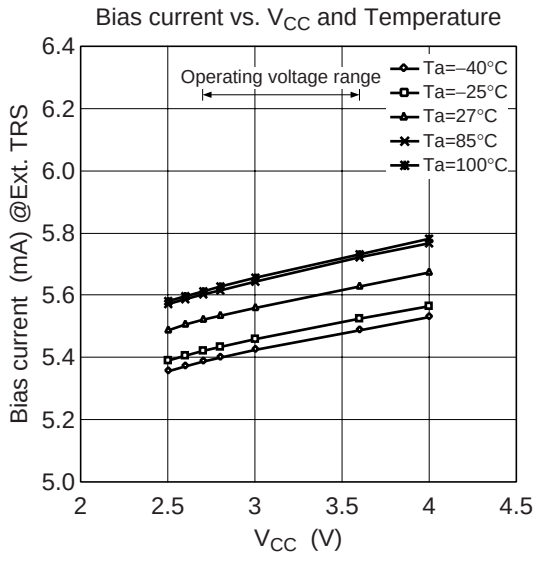
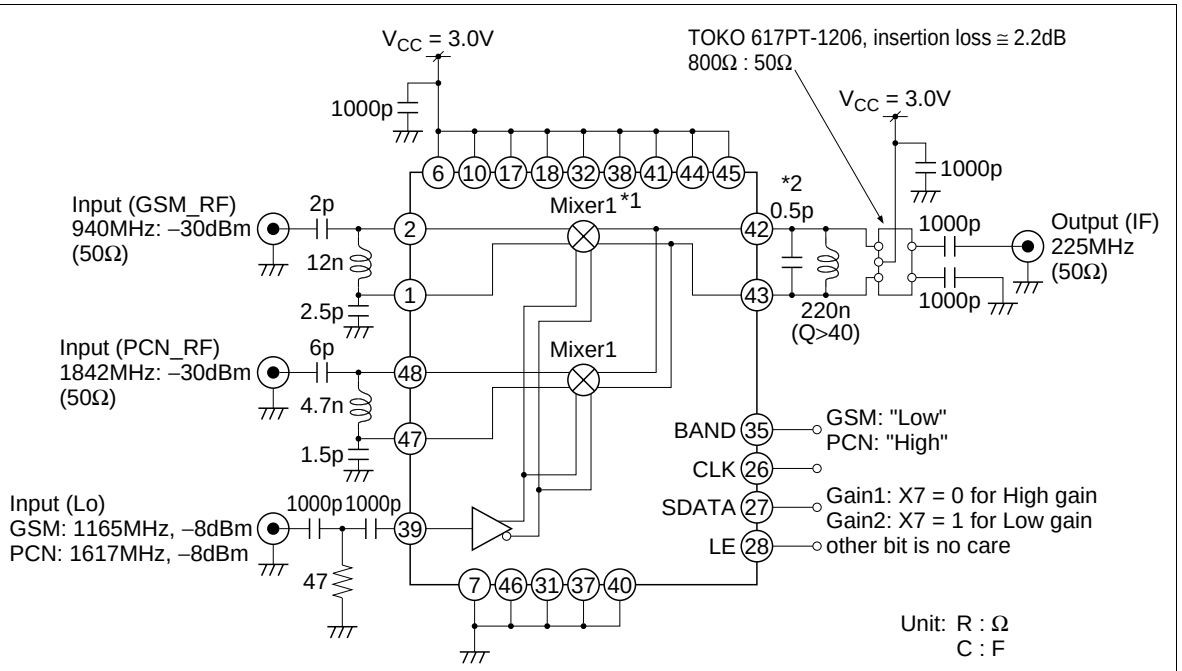


Figure 4



Mixer1 Typical Performance



Note: 1. Mixer1 is open collector type.
2. Please tune this LC resonant circuit to get the maximum conversion gain at 225MHz.

Figure 5

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Input (RF) Z	GSM	—	50	—	Ω	RF = 940MHz	1
	PCN	—	50	—	Ω	RF = 1842MHz	
Differential output load between pin42 and pin43	—	—	800	—	Ω	IF = 225MHz	1
Output (IF) Z	—	—	50	—	Ω	IF = 225MHz	1
Input (LO) Z	—	—	50	—	Ω	LO = 1165, 1617MHz	1
Input (RF) VSWR	GSM	—	—	2		RF = 940MHz	1
	PCN	—	—	2		RF = 1842MHz	
Input (LO) VSWR	GSM	—	—	2		LO = 1150 to 1185MHz	1
	PCN	—	—	4		LO = 1580 to 1655MHz	

Note: 1. These values are not tested in mass production.

Mixer1 Typical Performance (cont)

- Mixer1 S parameters Port1: pin2 (MIX1IN1) Port2: pin1 (MIX1INB1)

Frequency	S11		S21		S12		S22	
(MHz)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)
895	754.62	–82.557	109.41	91.89	107.94	90.73	739.46	–79.502
900	752.44	–82.957	111.75	91.71	110.03	90.71	737.07	–79.884
905	752.00	–83.314	114.04	91.39	112.02	90.57	735.32	–80.164
910	750.32	–83.658	116.14	90.76	113.69	90.19	733.45	–80.543
915	749.06	–84.053	117.73	90.14	115.37	89.68	732.38	–80.877
920	748.42	–84.440	119.37	89.31	116.73	89.03	731.16	–81.223
925	748.51	–84.849	120.64	88.41	118.02	88.48	730.91	–81.544
930	747.39	–85.213	121.21	87.64	118.93	87.72	729.92	–81.910
935	747.02	–85.626	121.81	86.90	119.54	87.08	729.54	–82.283
940	747.44	–86.053	121.93	85.90	119.78	86.27	729.38	–82.668
945	747.37	–86.488	121.22	85.11	119.74	85.56	730.05	–83.100
950	747.45	–87.054	119.98	84.55	119.01	85.13	730.63	–83.532
955	747.73	–87.535	118.34	84.32	117.70	84.95	730.78	–84.137
960	746.74	–88.119	116.90	84.63	116.32	85.38	730.02	–84.752
965	745.30	–88.735	116.23	85.41	116.29	86.13	728.56	–85.411
970	743.28	–89.301	116.77	86.34	116.94	87.04	724.68	–86.052
975	740.18	–89.825	118.14	87.31	119.06	87.75	721.14	–86.574
980	737.01	–90.247	120.72	87.54	121.81	87.96	717.34	–86.974
985	734.02	–90.646	123.00	87.15	124.35	87.64	713.39	–87.278
990	732.70	–90.928	124.32	86.51	125.87	86.67	711.49	–87.564

- Mixer1 S parameters Port1: pin48 (MIX1IN2) Port2: pin47 (MIX1INB2)

Frequency	S11		S21		S12		S22	
(MHz)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)
1795	522.87	–137.31	173.99	54.38	179.98	56.40	601.94	–158.40
1800	523.98	–137.67	174.59	54.42	178.85	56.36	601.55	–158.76
1805	525.39	–138.01	174.84	54.36	178.30	56.29	600.91	–159.11
1810	526.77	–138.39	175.19	54.40	177.57	56.30	600.89	–159.53
1815	527.49	–138.68	175.11	54.23	176.49	56.34	599.30	–159.93
1820	528.26	–139.03	175.97	54.08	176.09	56.40	599.71	–160.34
1825	529.92	–139.36	175.84	53.85	175.23	56.38	598.92	–160.88
1830	531.15	–139.75	175.93	53.54	174.88	56.61	598.29	–161.22
1835	532.28	–140.13	176.03	53.25	174.18	56.57	597.93	–161.63
1840	533.43	–140.54	175.87	52.85	173.91	56.55	597.23	–162.11
1845	534.27	–140.93	175.65	52.50	172.74	56.68	596.37	–162.53
1850	535.62	–141.23	175.01	52.14	172.61	56.61	596.30	–163.01
1855	536.47	–141.66	174.36	51.65	171.73	56.67	594.72	–163.49
1860	537.71	–142.01	173.43	51.37	171.48	56.79	594.24	–163.88
1865	538.84	–142.45	172.32	51.08	170.72	56.84	592.85	–164.40
1870	539.18	–142.85	170.91	50.76	170.10	56.93	592.38	–164.88
1875	540.41	–143.27	169.63	50.55	169.55	56.99	591.02	–165.30
1880	541.22	–143.76	167.87	50.28	168.56	56.99	590.16	–165.77
1885	541.78	–144.18	166.42	50.26	168.32	57.05	589.17	–166.18
1890	542.05	–144.59	164.56	50.29	167.81	57.13	588.64	–166.65

Mixer1 Typical Performance (cont)

- Mixer1 S parameters Port1: pin42 (MIX1OUT) Port2: pin43 (MIX1OUTB)

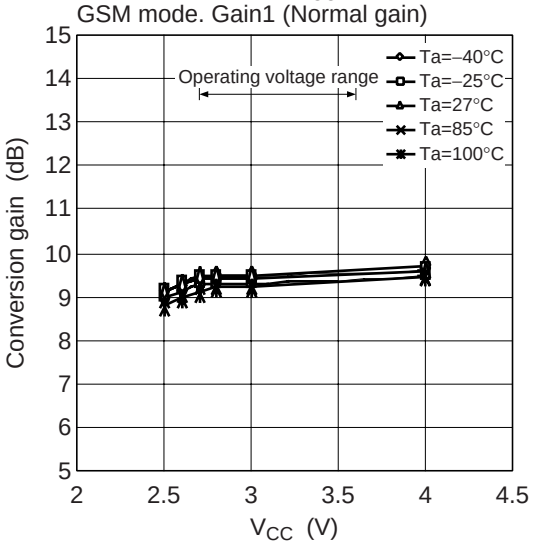
Frequency	S11		S21		S12		S22	
(MHz)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)
200	979.93	–21.27	39.05	71.100	39.14	71.494	979.20	–21.64
205	979.30	–21.81	39.96	70.994	40.15	71.345	978.83	–22.17
210	978.24	–22.34	40.89	70.756	41.05	71.132	977.99	–22.73
215	977.43	–22.87	41.69	70.563	41.89	70.953	977.11	–23.29
220	976.58	–23.40	42.67	70.378	42.91	70.816	977.38	–23.85
225	976.18	–23.92	43.57	70.299	43.78	70.541	975.97	–24.42
230	975.31	–24.52	44.53	70.052	44.63	70.304	974.84	–25.00
235	975.16	–25.09	45.42	69.956	45.54	70.236	974.52	–25.58
240	974.11	–25.63	46.28	69.759	46.48	69.980	974.24	–26.15
245	973.55	–26.17	47.20	69.519	47.37	69.706	972.84	–26.77
250	972.26	–26.73	48.11	69.336	48.19	69.524	972.50	–27.34
255	972.06	–27.26	49.00	69.190	49.14	69.408	971.62	–27.92
260	970.73	–27.84	49.94	68.994	50.02	69.103	971.00	–28.50
265	970.76	–28.39	50.80	68.729	50.89	68.995	970.58	–29.05
270	970.42	–28.96	51.86	68.590	51.76	68.833	969.11	–29.65
275	969.30	–29.53	52.79	68.259	52.69	68.558	968.29	–30.23
280	968.44	–30.07	53.69	68.041	53.58	68.427	967.22	–30.82
285	967.83	–30.62	54.68	67.840	54.51	68.220	966.67	–31.40
290	967.14	–31.22	55.62	67.524	55.43	67.966	965.98	–32.00
295	966.09	–31.81	56.58	67.183	56.32	67.699	965.50	–32.63

- Mixer1 S parameters Port1: pin39 (RFLOIN)

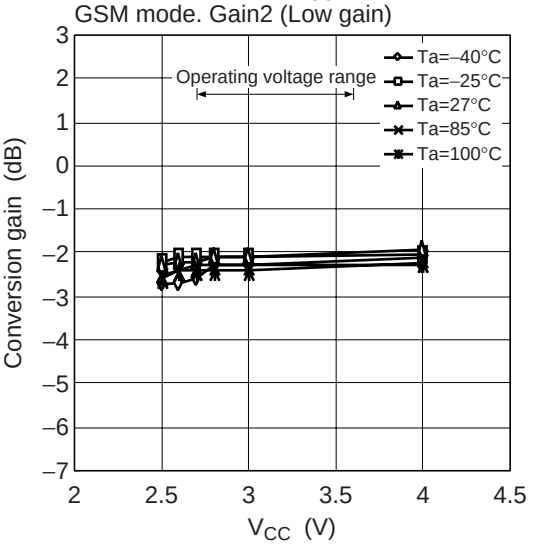
Frequency	S11		Frequency	S11	
(MHz)	Mag.(mU)	Ang.(degree)	(MHz)	Mag.(mU)	Ang.(degree)
1120	831.05	–71.478	1570	690.53	–101.924
1125	829.47	–71.805	1575	689.12	–102.299
1130	827.93	–72.134	1580	686.98	–102.703
1135	827.36	–72.485	1585	685.49	–103.040
1140	825.87	–72.816	1590	683.72	–103.392
1145	825.65	–73.101	1595	682.04	–103.758
1150	823.25	–73.414	1600	679.93	–104.098
1155	823.08	–73.701	1605	677.68	–104.415
1160	821.69	–74.035	1610	675.71	–104.781
1165	820.33	–74.371	1615	674.24	–105.128
1170	820.23	–74.659	1620	671.69	–105.454
1175	818.66	–75.064	1625	669.77	–105.790
1180	817.64	–75.335	1630	667.97	–106.114
1185	816.39	–75.674	1635	664.89	–106.415
1190	815.89	–76.100	1640	663.02	–106.713
1195	813.73	–76.425	1645	661.31	–107.018
1200	813.55	–76.784	1650	658.60	–107.243
1205	812.42	–77.127	1655	656.49	–107.590
1210	811.32	–77.471	1660	653.78	–107.769
1215	810.04	–77.885	1665	651.73	–108.016

Mixer1 Typical Performance (cont)

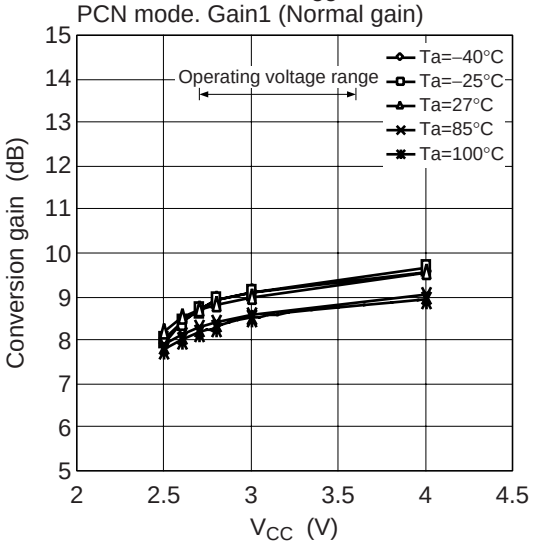
Conversion gain vs. V_{CC} and Temperature
GSM mode. Gain1 (Normal gain)



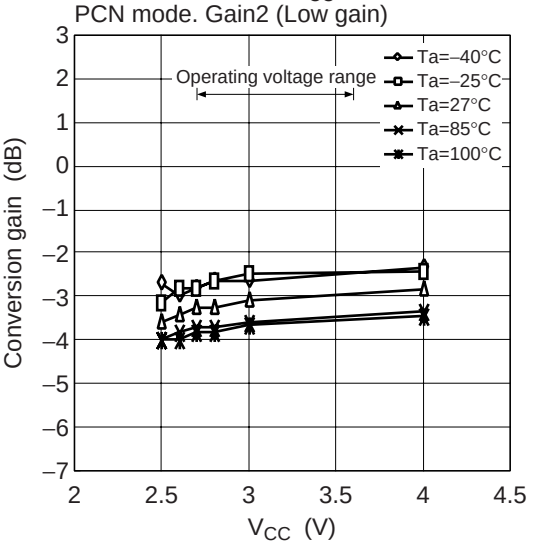
Conversion gain vs. V_{CC} and Temperature
GSM mode. Gain2 (Low gain)



Conversion gain vs. V_{CC} and Temperature
PCN mode. Gain1 (Normal gain)

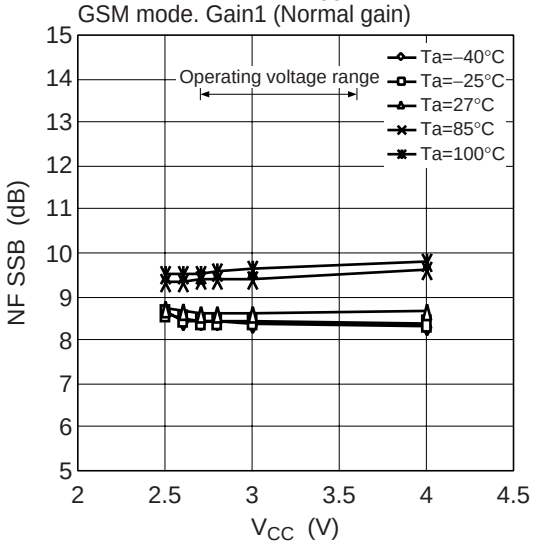


Conversion gain vs. V_{CC} and Temperature
PCN mode. Gain2 (Low gain)

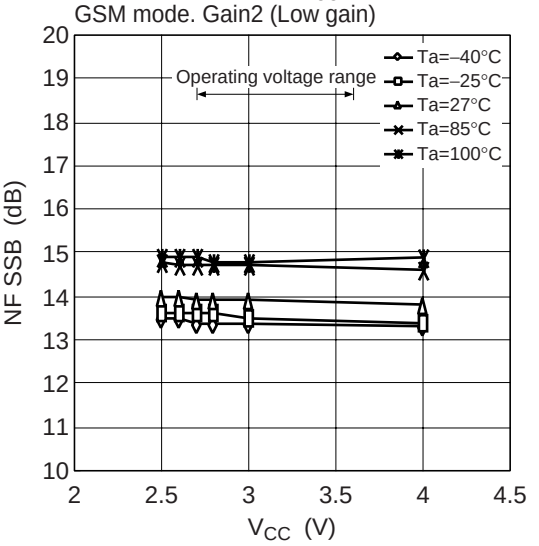


Mixer1 Typical Performance (cont)

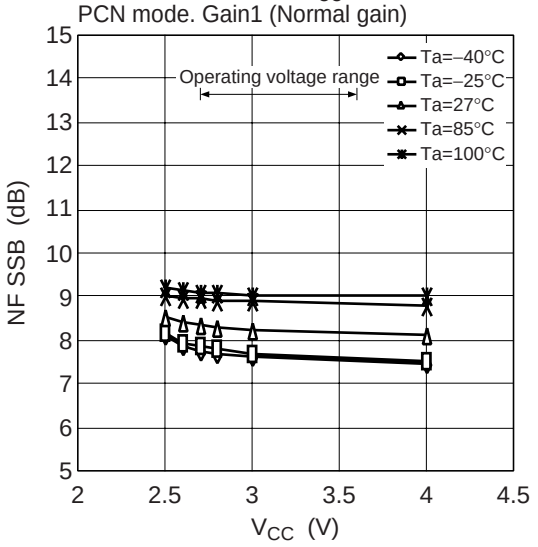
Noise figure(SSB) vs. V_{CC} and Temperature
GSM mode. Gain1 (Normal gain)



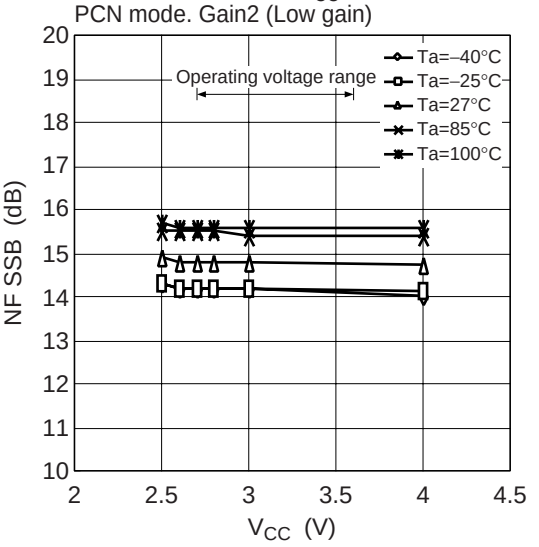
Noise figure(SSB) vs. V_{CC} and Temperature
GSM mode. Gain2 (Low gain)



Noise figure(SSB) vs. V_{CC} and Temperature
PCN mode. Gain1 (Normal gain)

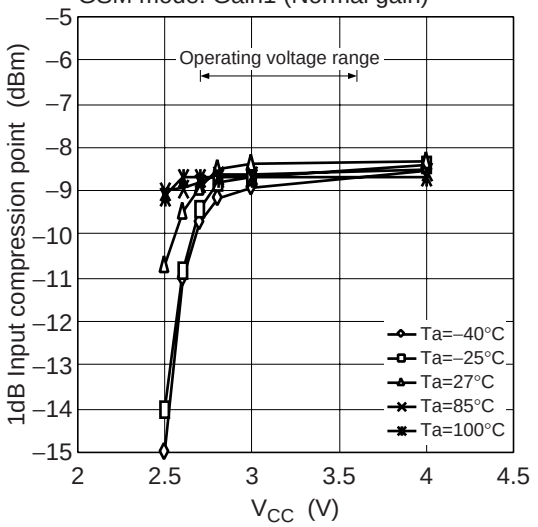


Noise figure(SSB) vs. V_{CC} and Temperature
PCN mode. Gain2 (Low gain)

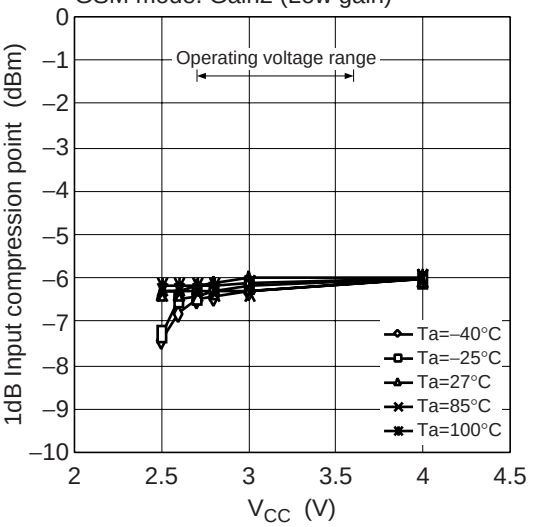


Mixer1 Typical Performance (cont)

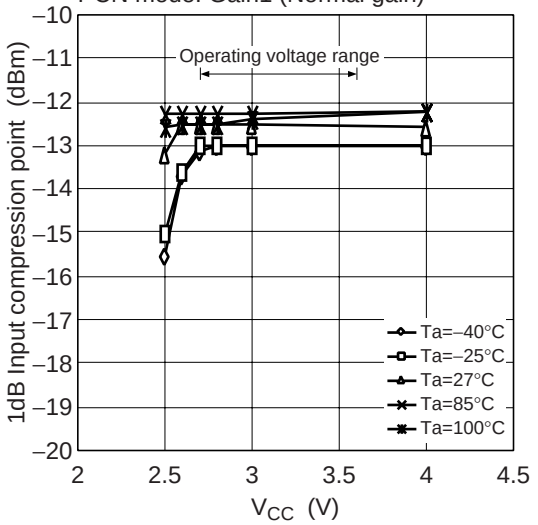
1dB Input compression point vs.
V_{CC} and Temperature
GSM mode. Gain1 (Normal gain)



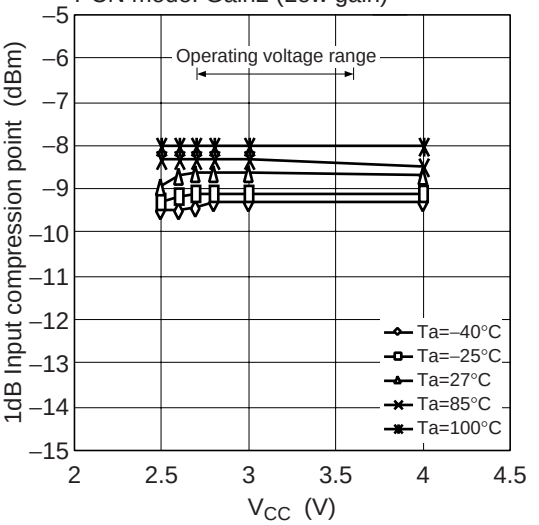
1dB Input compression point vs.
V_{CC} and Temperature
GSM mode. Gain2 (Low gain)



1dB Input compression point vs.
V_{CC} and Temperature
PCN mode. Gain1 (Normal gain)

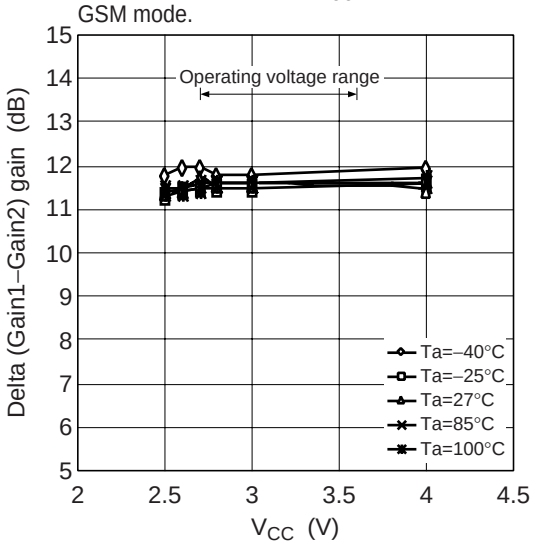


1dB Input compression point vs.
V_{CC} and Temperature
PCN mode. Gain2 (Low gain)

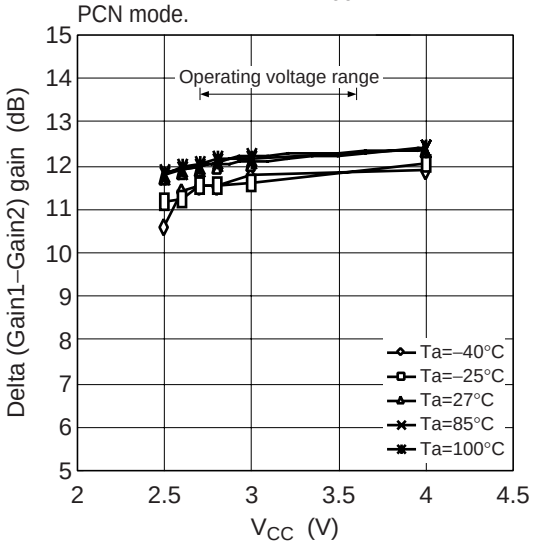


Mixer1 Typical Performance (cont)

Delta (Gain1–Gain2) vs. V_{CC} and Temperature
GSM mode.



Delta (Gain1–Gain2) vs. V_{CC} and Temperature
PCN mode.



Mixer2 Typical Performance

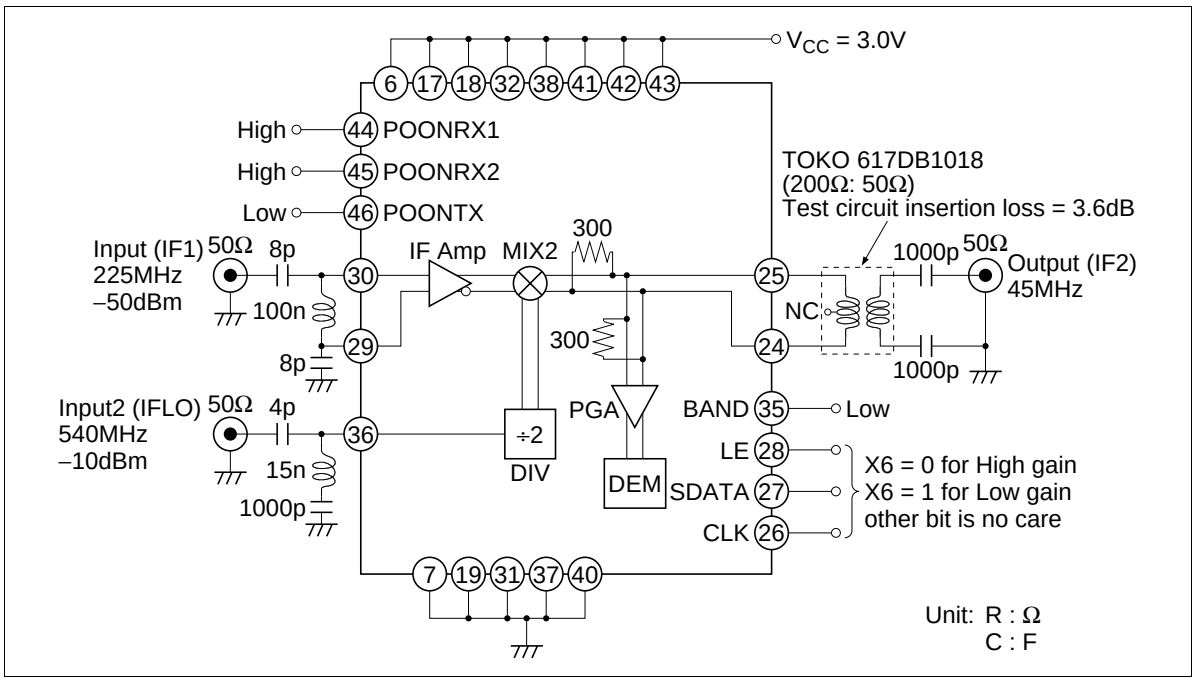


Figure 6

Item	Mode	Min	Typ	Max	Unit	Test Condition	Note
Input (IF) Z		—	50	—	Ω	IF1 = 225MHz	1
LO Z		—	50	—	Ω	IFLO = 540MHz	1
i/p VSWR		—	—	2		IF1 = 225MHz	1
LO VSWR		—	—	2		IFLO = 540MHz	1

Note: 1. These values are not tested in mass production.

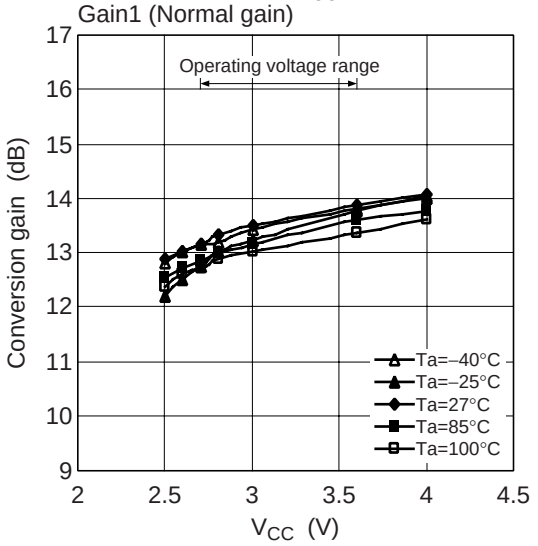
Mixer2 Typical Performance (cont)

- Mixer2 S parameters Port1: pin30 (IFIN) Port2: pin29 (IFINB)

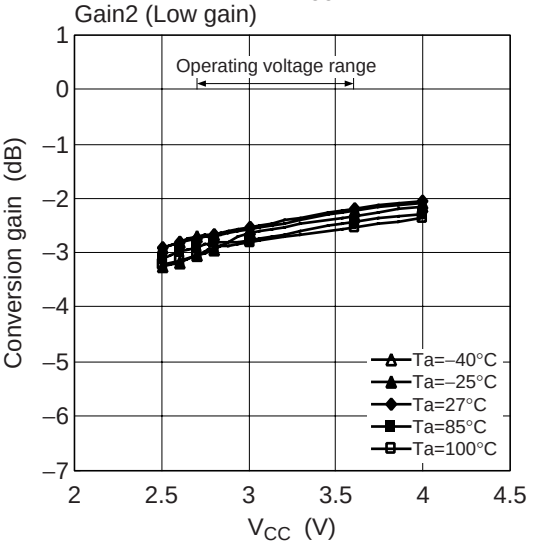
Frequency	S11		S21		S12		S22	
(MHz)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)	Mag.(mU)	Ang.(degree)
200	941.92	–20.936	47.84	12.570	47.77	12.517	941.65	–20.558
205	940.46	–21.513	47.91	12.808	47.89	12.829	941.18	–21.073
210	940.85	–22.040	47.97	13.024	47.92	13.065	939.92	–21.628
215	940.32	–22.592	47.99	13.297	47.92	13.257	939.52	–22.145
220	938.32	–23.094	48.03	13.499	47.89	13.489	938.70	–22.689
225	938.11	–23.735	48.05	13.659	47.91	13.702	937.66	–23.198
230	936.93	–24.288	48.02	14.001	48.00	13.969	937.61	–23.777
235	936.23	–24.863	48.10	14.233	47.98	14.257	936.56	–24.355
240	935.61	–25.424	48.15	14.539	48.09	14.500	936.05	–24.928
245	934.29	–26.032	48.20	14.795	48.04	14.759	934.73	–25.481
250	933.31	–26.599	48.26	15.017	48.12	15.039	934.55	–26.039
255	933.20	–27.186	48.29	15.299	48.21	15.309	933.47	–26.606
260	932.03	–27.743	48.38	15.529	48.26	15.529	933.28	–27.110
265	931.63	–28.351	48.56	15.749	48.30	15.751	931.86	–27.702
270	930.97	–28.923	48.57	15.992	48.40	16.056	931.63	–28.224
275	929.68	–29.513	48.66	16.216	48.50	16.351	930.13	–28.763
280	928.75	–30.038	48.77	16.482	48.58	16.598	929.21	–29.315
285	927.72	–30.634	48.92	16.685	48.71	16.773	928.79	–29.899
290	927.06	–31.230	49.03	16.858	48.84	17.000	927.41	–30.498
295	925.35	–31.837	49.12	17.022	48.94	17.193	926.34	–31.043

Mixer2 Typical Performance (cont)

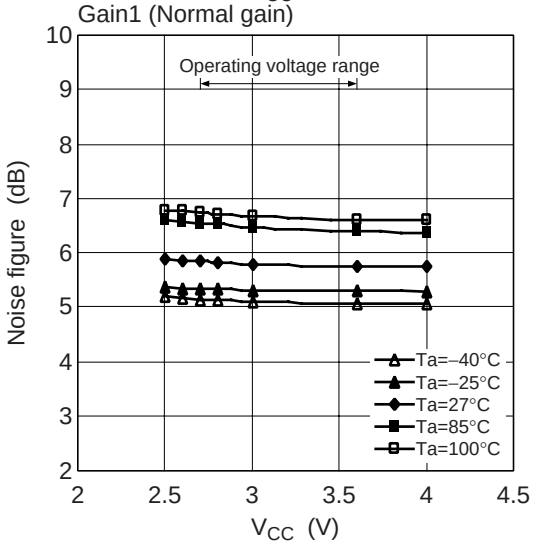
Conversion gain vs. V_{CC} and Temperature
Gain1 (Normal gain)



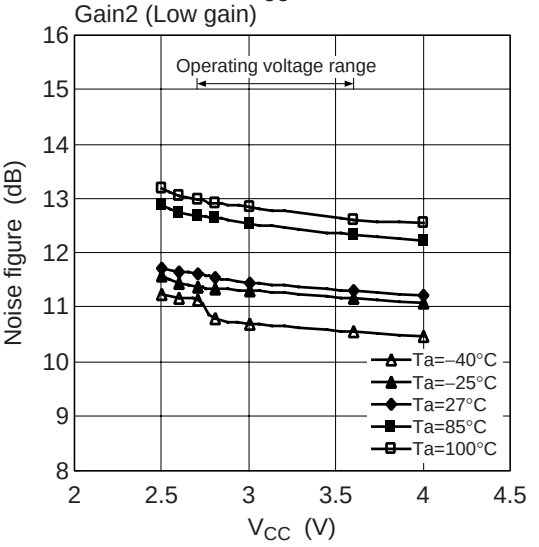
Conversion gain vs. V_{CC} and Temperature
Gain2 (Low gain)



Noise figure vs. V_{CC} and Temperature
Gain1 (Normal gain)

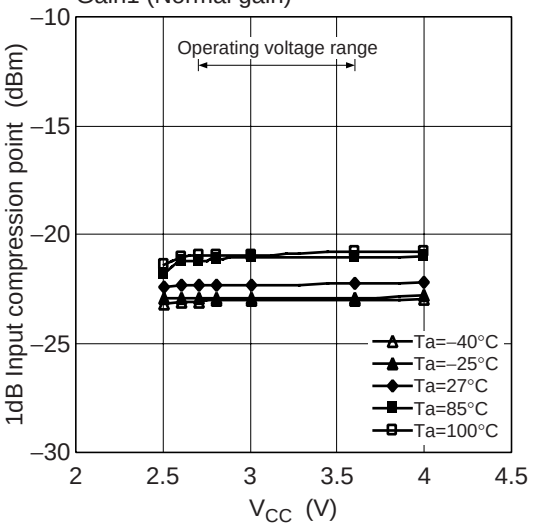


Noise figure vs. V_{CC} and Temperature
Gain2 (Low gain)

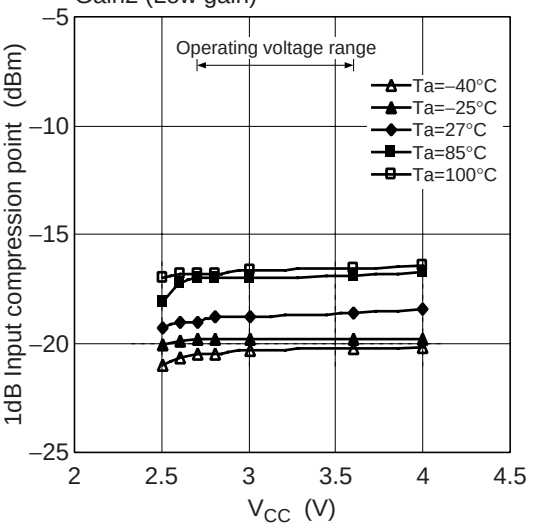


Mixer2 Typical Performance (cont)

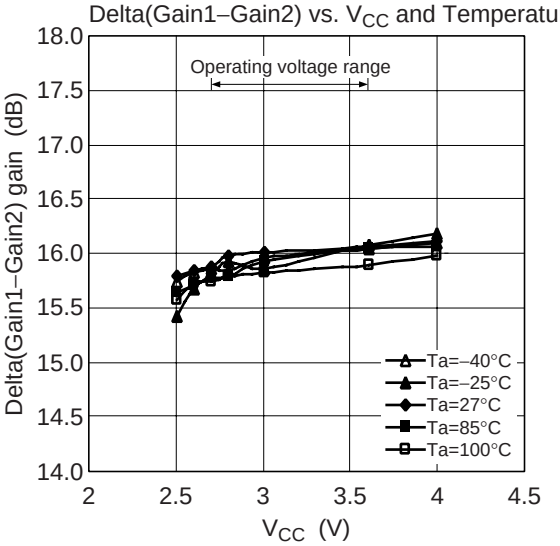
1dB Input compression point vs. V_{CC} and Temperature Gain1 (Normal gain)



1dB Input compression point vs. V_{CC} and Temperature Gain2 (Low gain)



Delta(Gain1−Gain2) vs. V_{CC} and Temperature



PGA and Demodulator Typical Performance

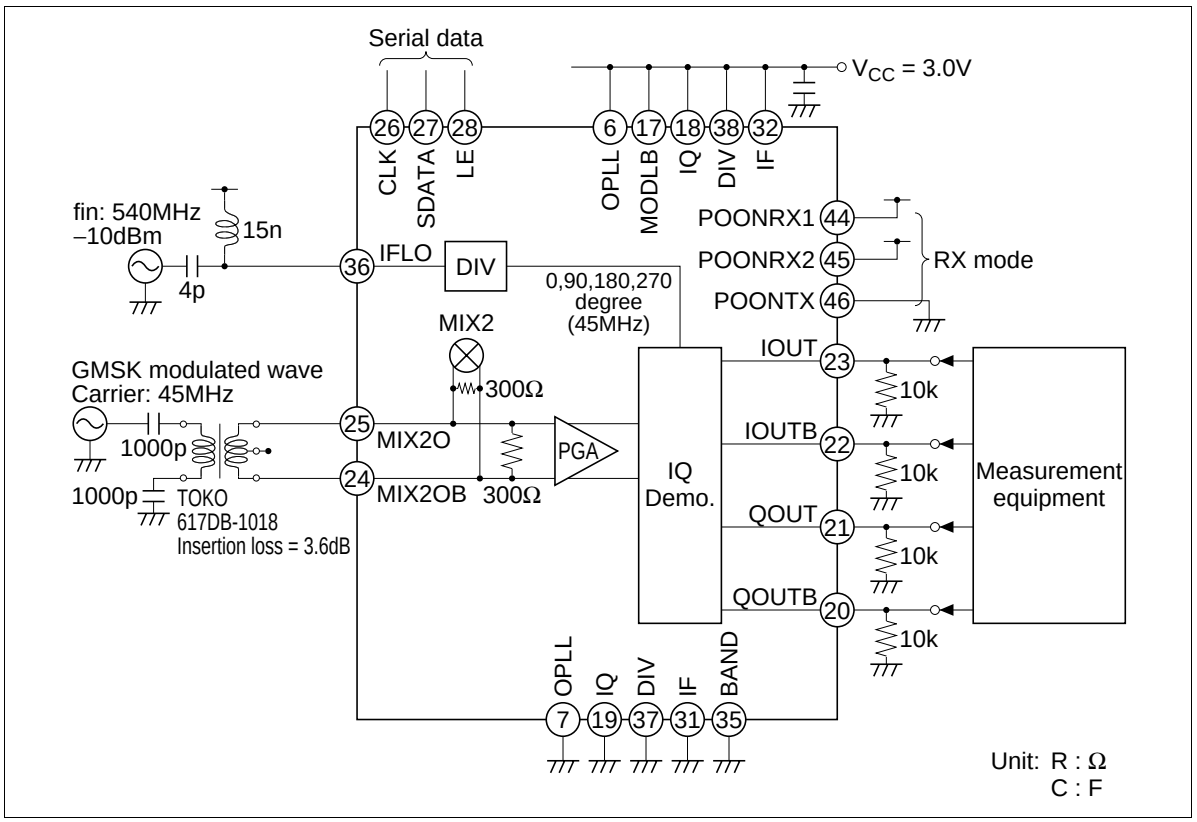
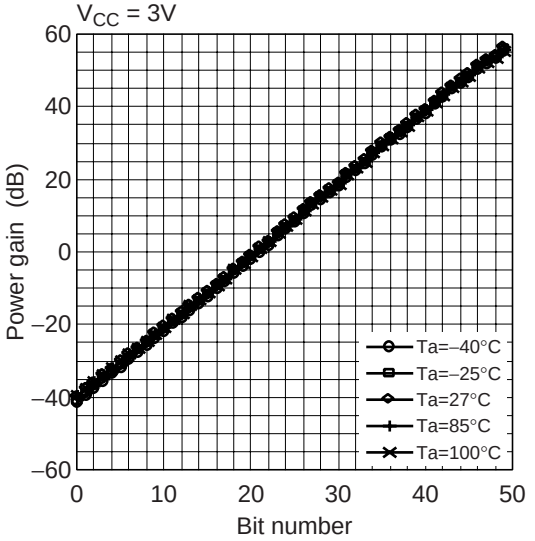


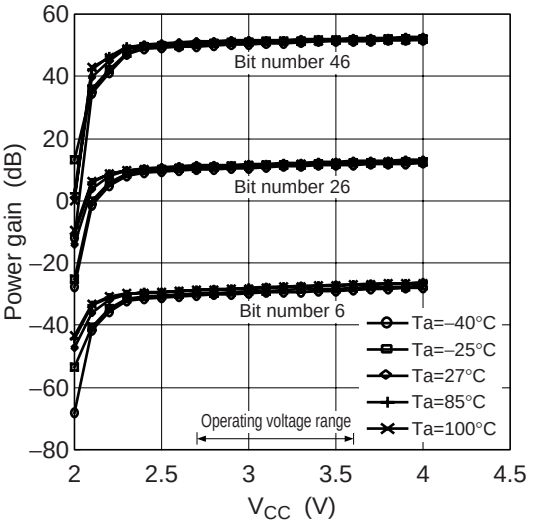
Figure 7

PGA and Demodulator Typical Performance (cont)

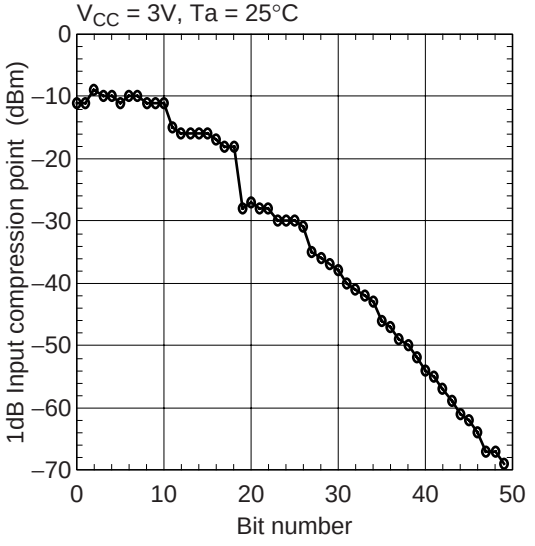
Power gain vs. Bit number with Temperature
V_{CC} = 3V



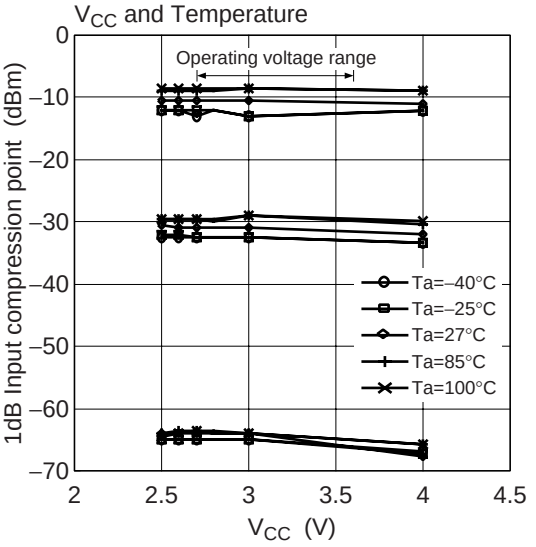
Power gain vs. V_{CC} and Temperature



1dB Input compression point vs. Bit number
V_{CC} = 3V, Ta = 25°C

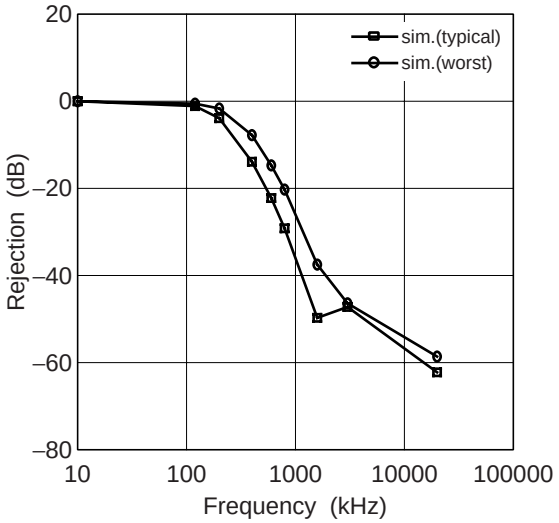


1dB Input compression point vs.
V_{CC} and Temperature



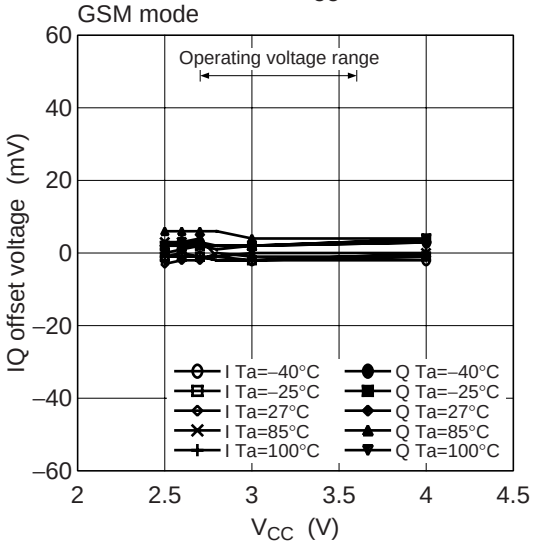
PGA and Demodulator Typical Performance (cont)

Frequency response of LPF in Demodulator

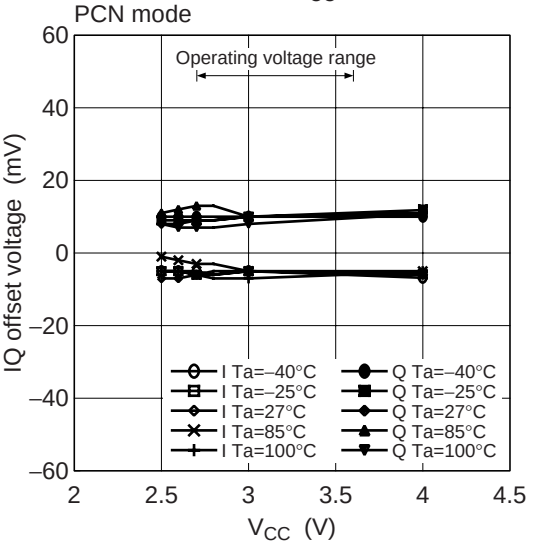


Frequency (kHz)	sim.(typ)	sim.(worst)
10	0.0	0.0
120	–1.2	–0.5
200	–4.0	–1.6
400	–14.0	–7.9
600	–22.3	–14.7
800	–29.2	–20.3
1600	–49.8	–37.6
3000	–47.3	–46.3
20000	–62.3	–58.7

IQ offset voltage vs. V_{CC} and Temperature
GSM mode



IQ offset voltage vs. V_{CC} and Temperature
PCN mode



IQ Modulator and OffsetPLL Typical Performance

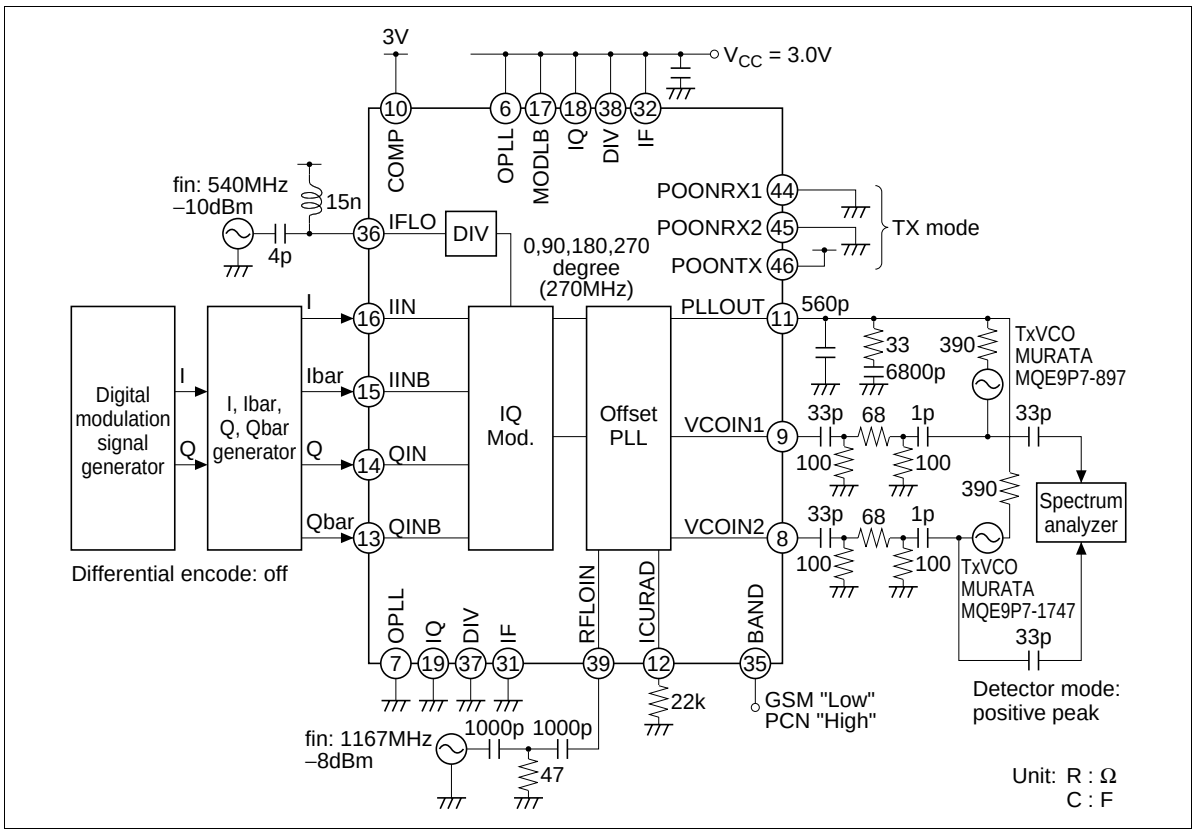


Figure 8

- Phase detector offset current ratio evaluation circuit

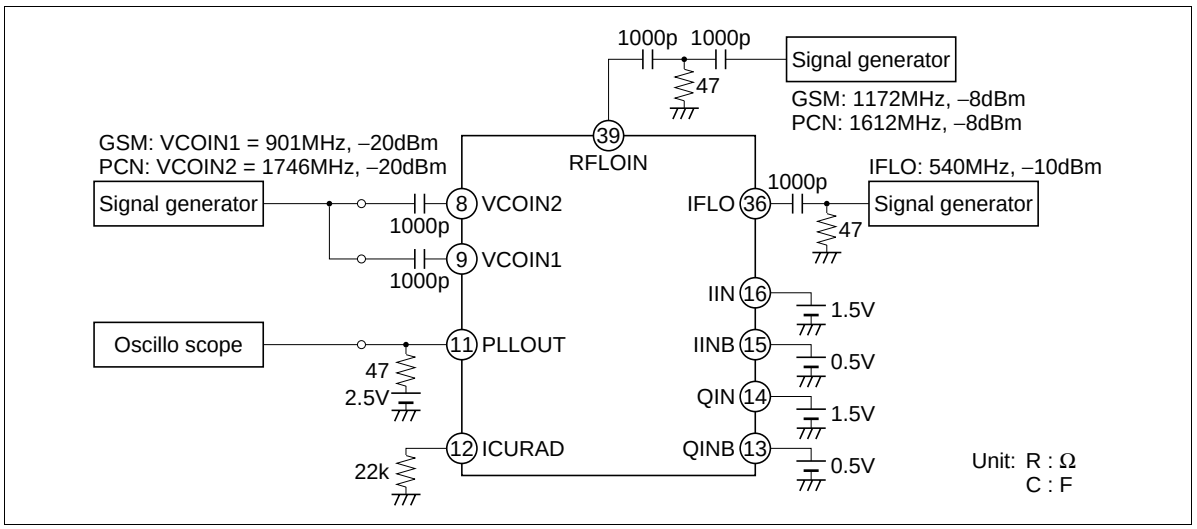
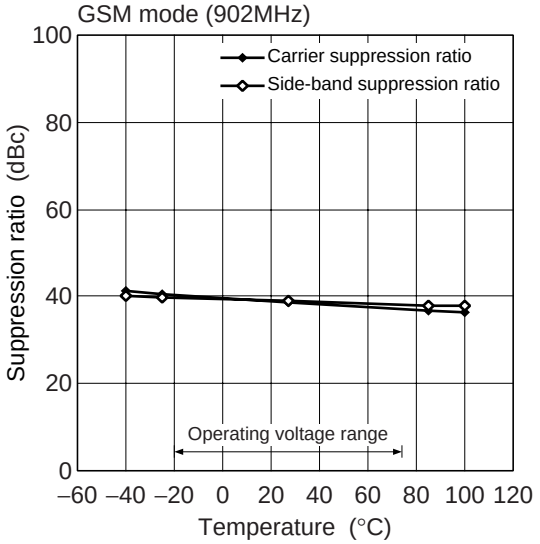


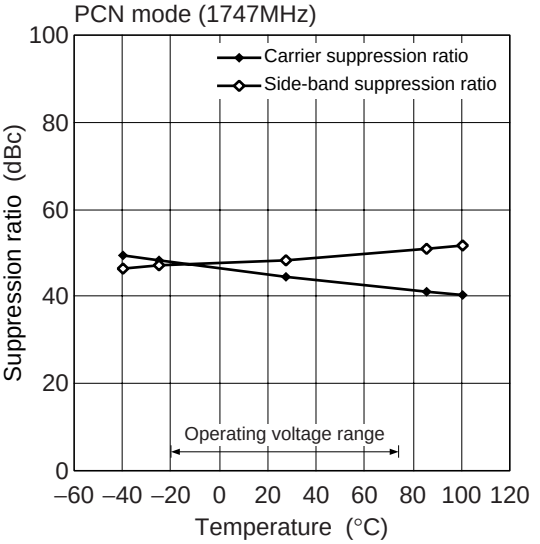
Figure 9

IQ Modulator and OffsetPLL Typical Performance (cont)

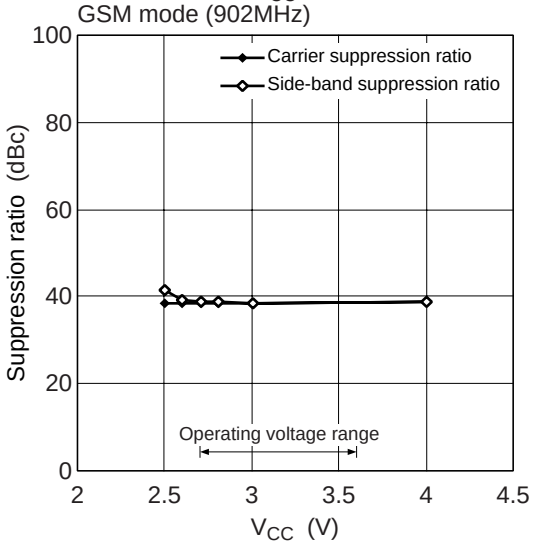
Tx spectrum vs. Temperature
GSM mode (902MHz)



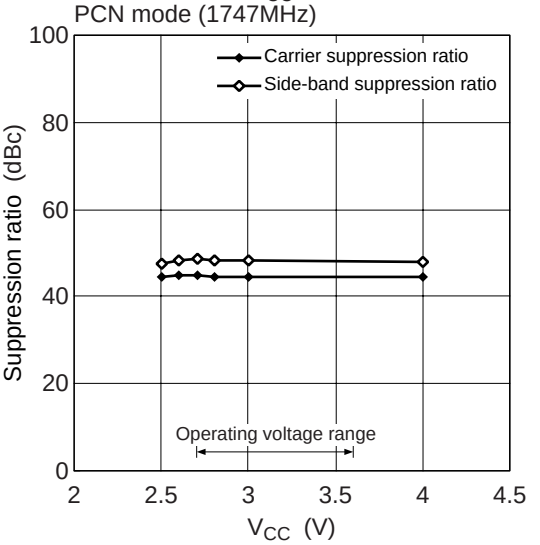
Tx spectrum vs. Temperature
PCN mode (1747MHz)



Tx spectrum vs. V_{CC}
GSM mode (902MHz)

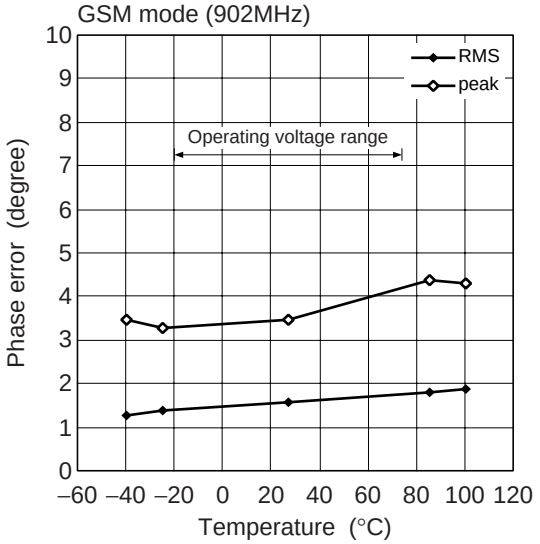


Tx spectrum vs. V_{CC}
PCN mode (1747MHz)

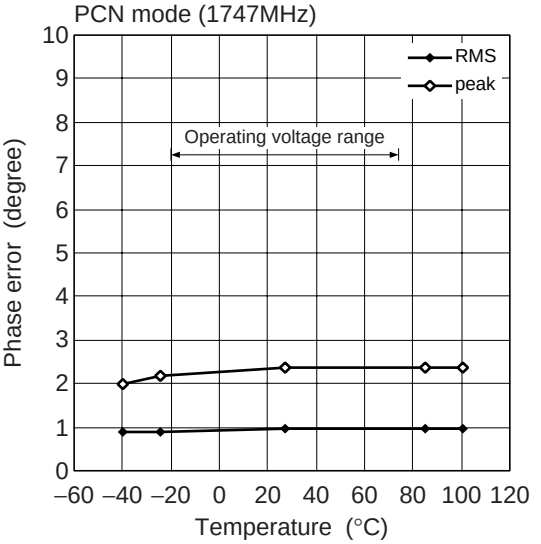


IQ Modulator and OffsetPLL Typical Performance (cont)

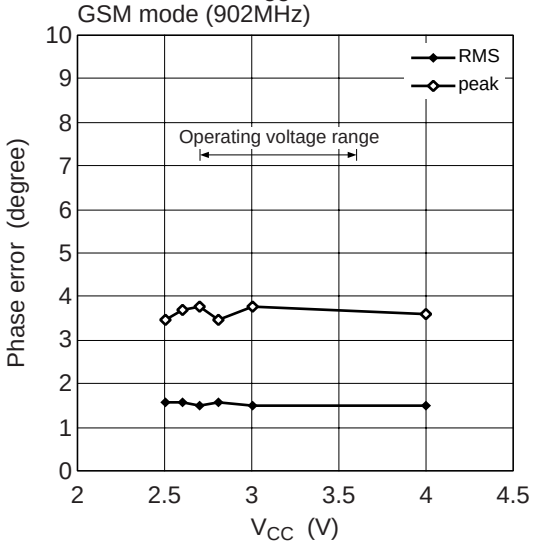
Phase error vs. Temperature
GSM mode (902MHz)



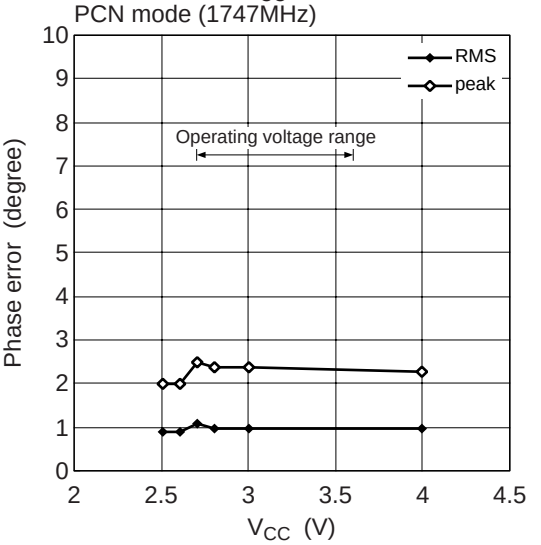
Phase error vs. Temperature
PCN mode (1747MHz)



Phase error vs. V_{CC}
GSM mode (902MHz)

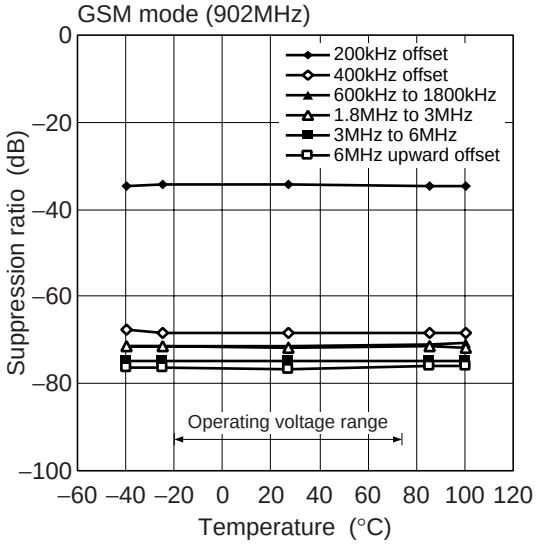


Phase error vs. V_{CC}
PCN mode (1747MHz)

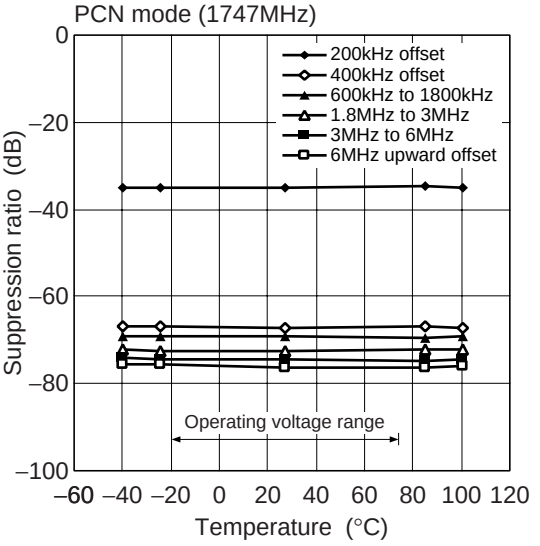


IQ Modulator and OffsetPLL Typical Performance (cont)

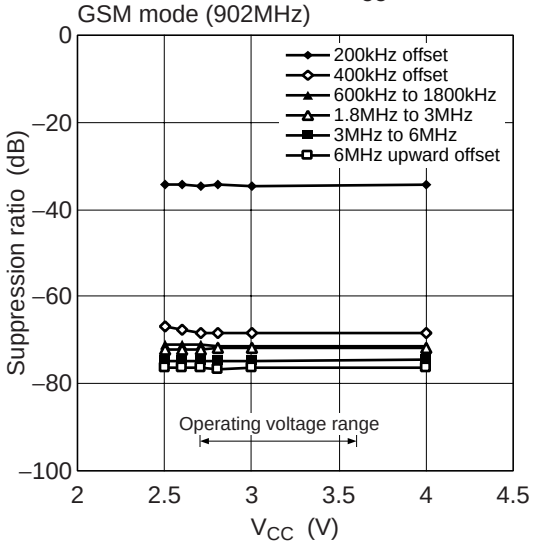
Modulation spectrum vs. Temperature
GSM mode (902MHz)



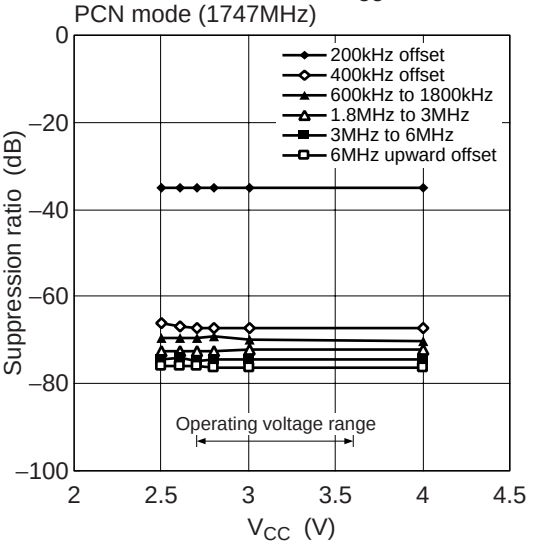
Modulation spectrum vs. Temperature
PCN mode (1747MHz)



Modulation spectrum vs. V_{CC}
GSM mode (902MHz)

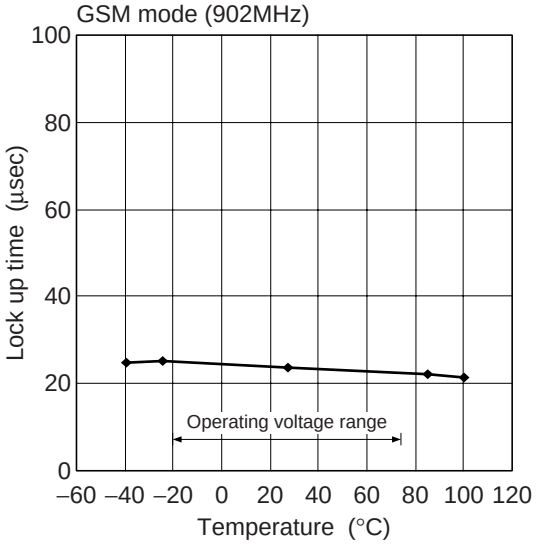


Modulation spectrum vs. V_{CC}
PCN mode (1747MHz)

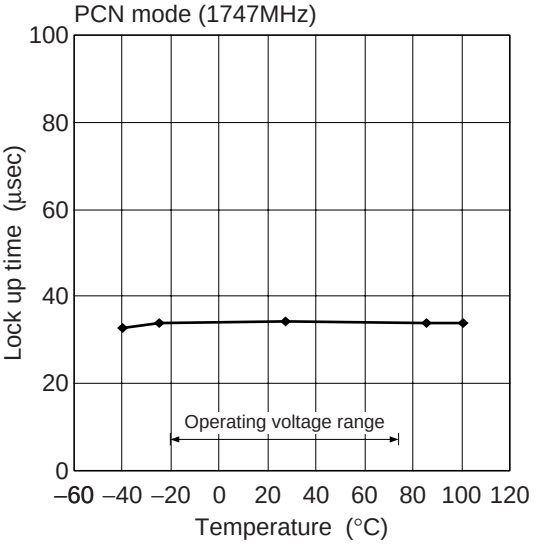


IQ Modulator and OffsetPLL Typical Performance (cont)

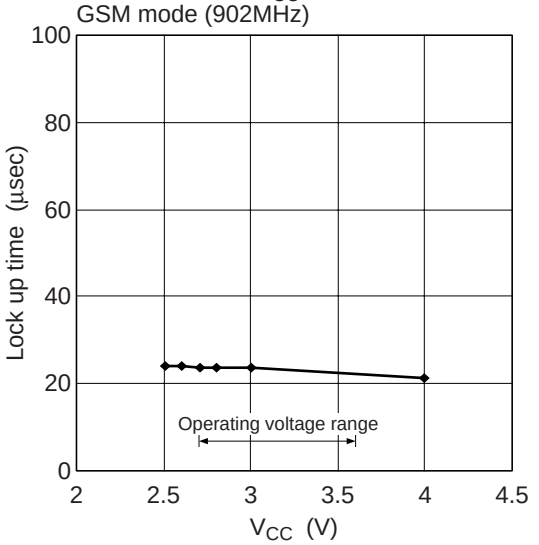
Lock up time vs. Temperature
GSM mode (902MHz)



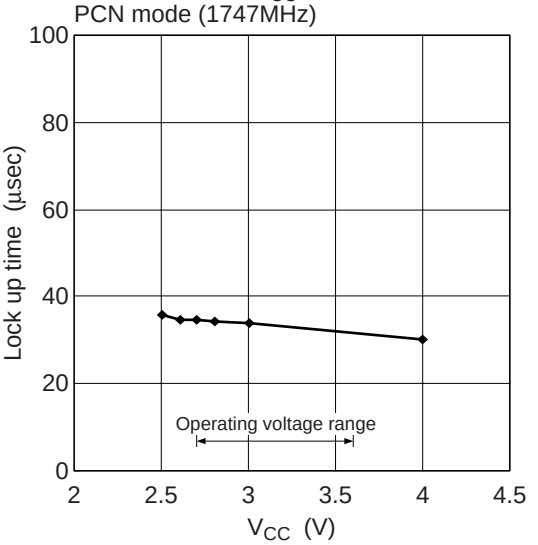
Lock up time vs. Temperature
PCN mode (1747MHz)



Lock up time vs. V_{CC}
GSM mode (902MHz)

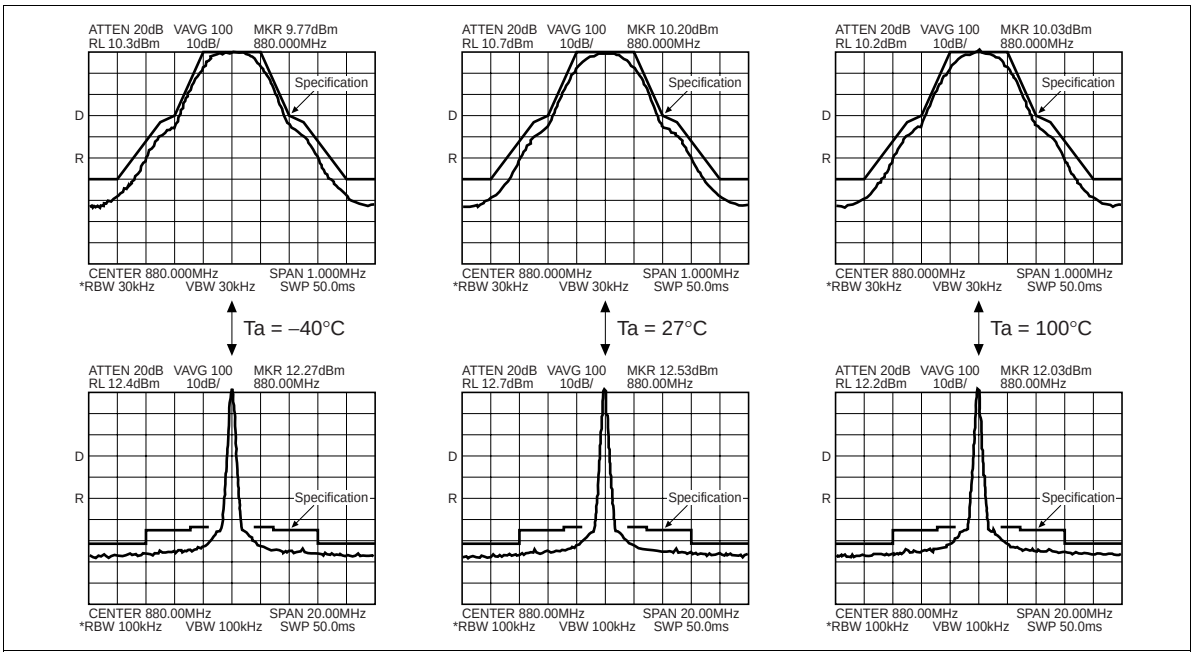


Lock up time vs. V_{CC}
PCN mode (1747MHz)

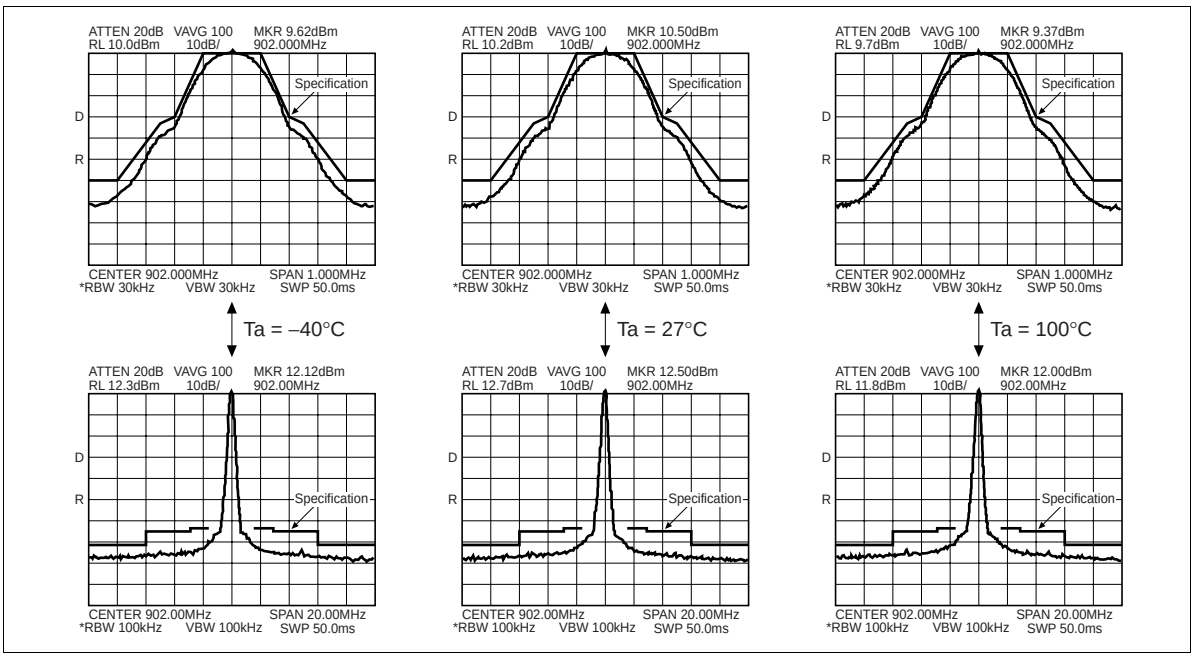


IQ Modulator and OffsetPLL Typical Performance (cont)

- Modulation spectrum wave form vs. Temperature
  GSM mode (880 MHz)

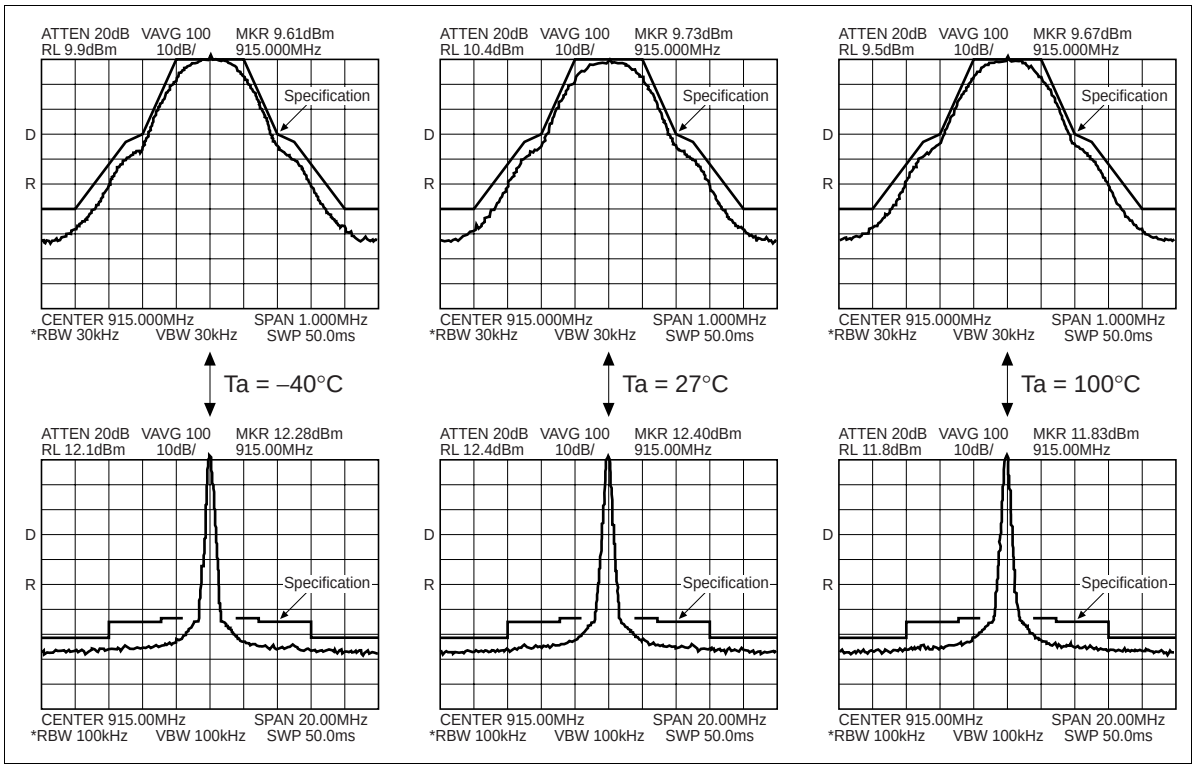


- Modulation spectrum wave form vs. Temperature
  GSM mode (902 MHz)



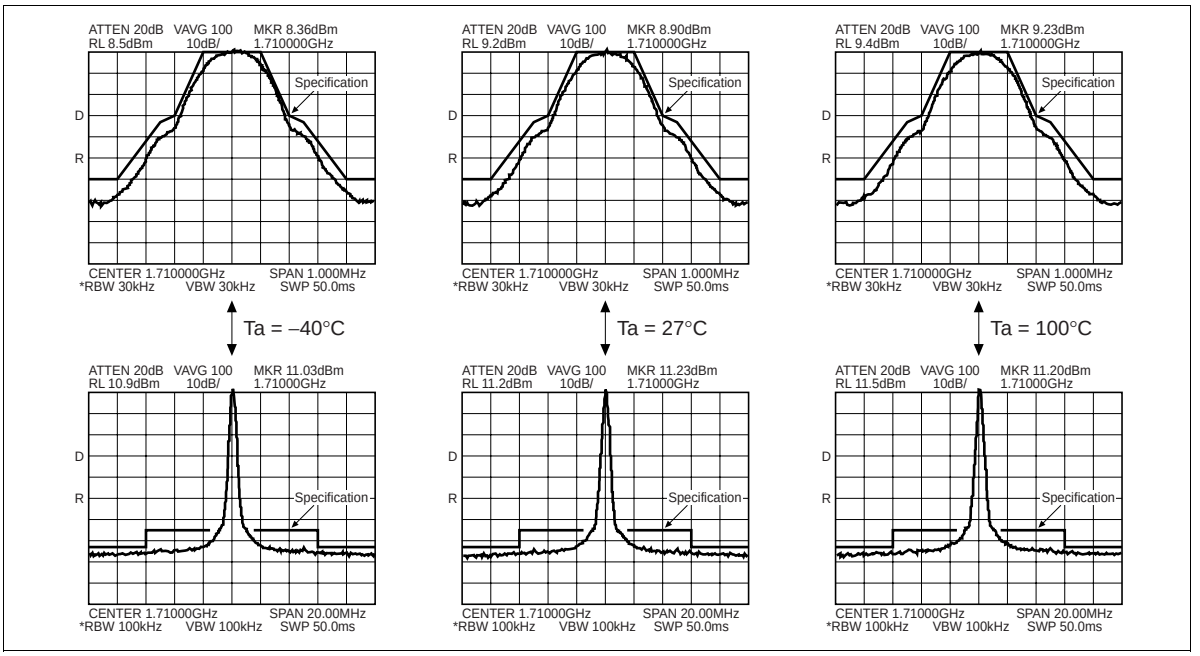
IQ Modulator and OffsetPLL Typical Performance (cont)

- Modulation spectrum wave form vs. Temperature
  GSM mode (915 MHz)

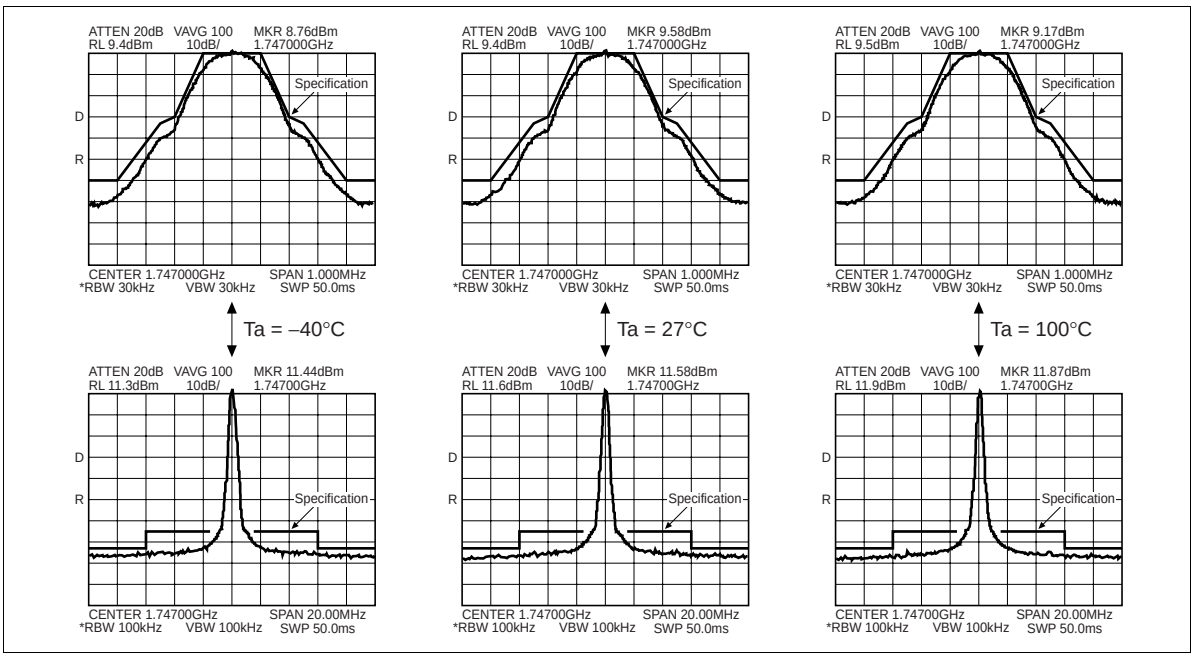


IQ Modulator and OffsetPLL Typical Performance (cont)

- Modulation spectrum wave form vs. Temperature
  PCN mode (1710 MHz)

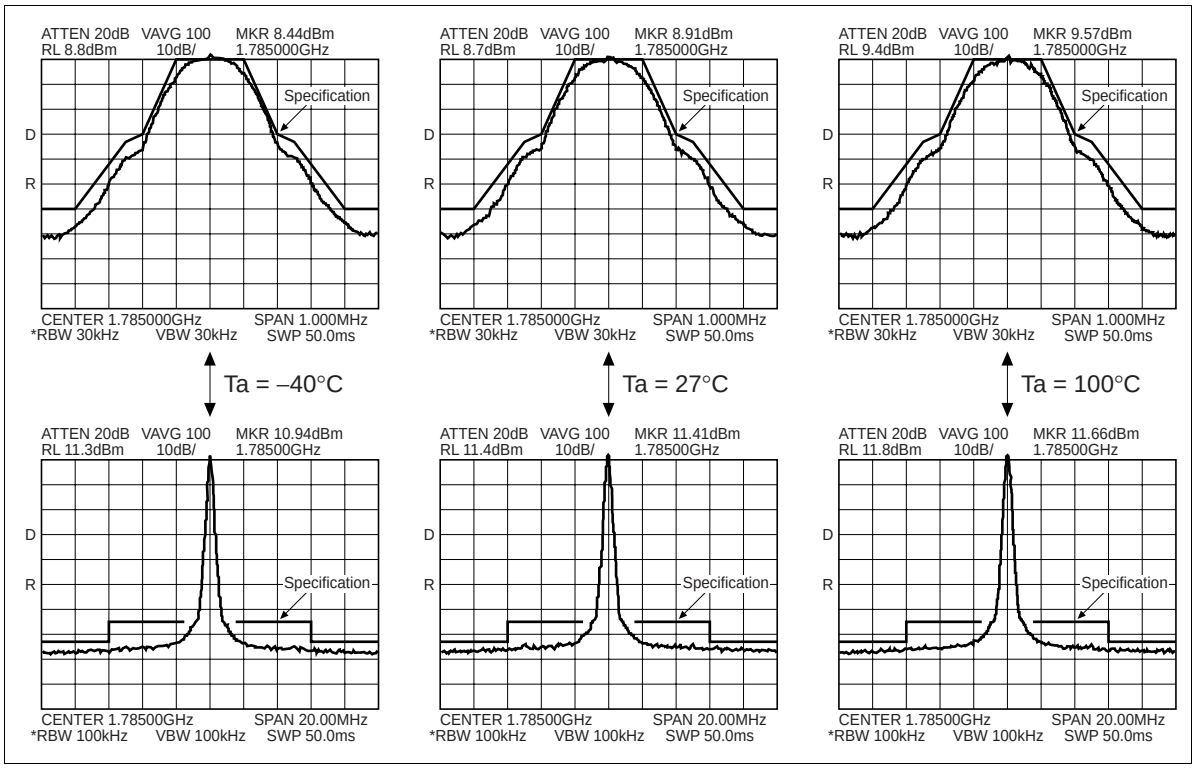


- Modulation spectrum wave form vs. Temperature
  PCN mode (1747 MHz)



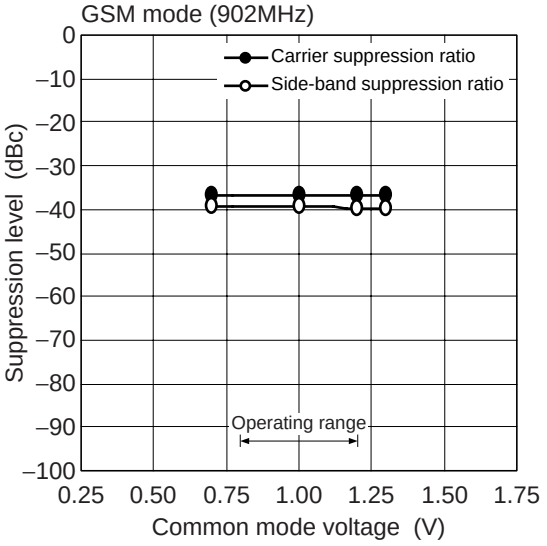
IQ Modulator and OffsetPLL Typical Performance (cont)

- Modulation spectrum wave form vs. Temperature
  PCN mode (1785 MHz)

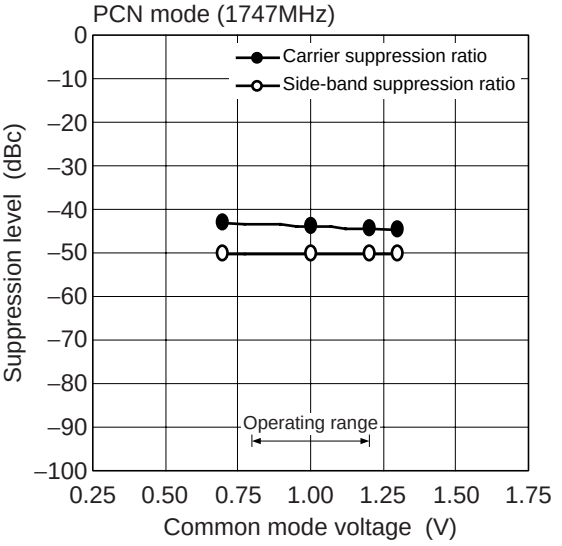


IQ Modulator and OffsetPLL Typical Performance (cont)

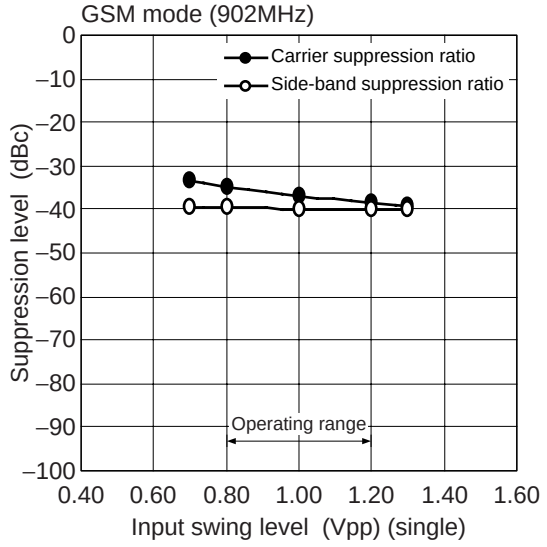
Tx spectrum vs. Common mode voltage
GSM mode (902MHz)



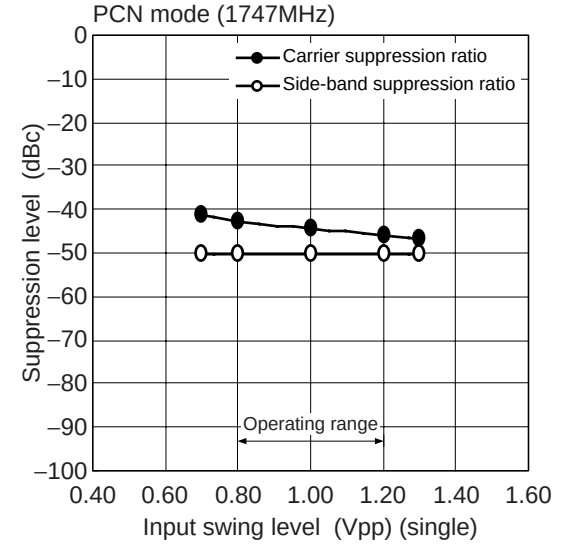
Tx spectrum vs. Common mode voltage
PCN mode (1747MHz)



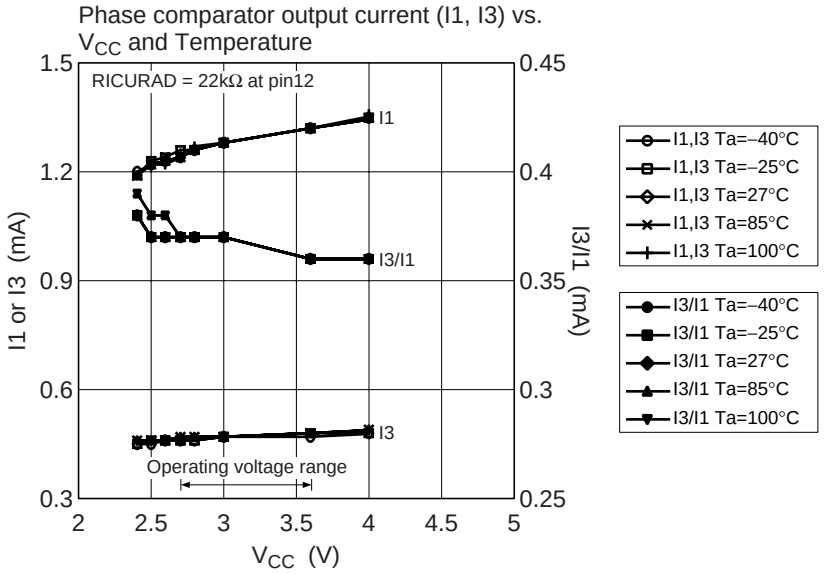
Tx spectrum vs. Input swing level
GSM mode (902MHz)



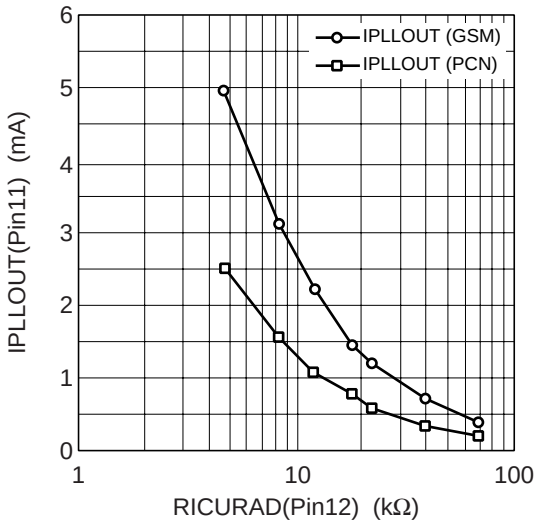
Tx spectrum vs. Input swing level
PCN mode (1747MHz)



IQ Modulator and OffsetPLL Typical Performance (cont)

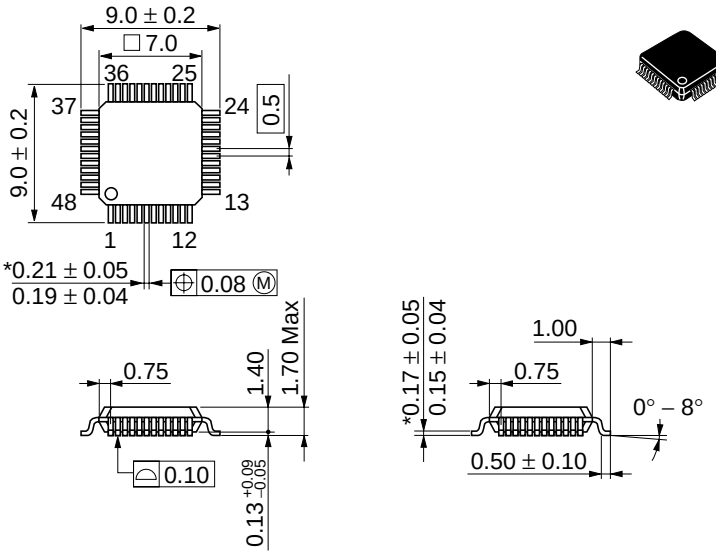


OPLL phase detector output current value is controlled by RICURAD(pin12).
Following figure is for determining phase detector output current.



Package Dimensions

Preliminary Unit: mm



Hitachi Code	FP-48C
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.2 g

*Dimension including the plating thickness
Base material dimension

Appendix A

Transmitter Architecture (offset PLL architecture)

The HD155121F generates a modulated signal at IF with a quadrature modulator and converts it to a final frequency with an Offset Phase Locked Loop (OPLL).

The Offset Phase Locked Loop is simply a PLL with a down conversion mixer in the feedback path.

Using a down converter in the feed back path acts as an up converter in the forward path, which allows the output frequency to be different from the comparison frequency without affecting the normal operation of the loop. Phase / frequency changes in the reference signal are not scaled, as they would be if a divider were used in the feed back path, and hence the modulation is faithfully reproduced at the final frequency.

The main advantage of the OPLL in this application is that it forms a tracking band pass filter around the modulated signal. This is because the loop cannot respond to phase variations at the reference that are outside its closed loop bandwidth. Thus the broad band phase noise from the quadrature modulator is shaped by the frequency response of the closed loop allowing the TX noise specifications to be met without further filtering.

A secondary advantage of the OPLL is that the output signal, coming from a VCO, is truly constant envelope. This removes the problem of spectral spreading caused by AM to AM and AM to PM conversion in the power amplifier.

The OPLL is formed from an on-chip Gilbert cell down converter, limitters and phase detector with an off-chip passive loop filter and VCO. The phase detector is implemented as a Gilbert cell with a current source output stage, which allows an integrator to be included in the passive loop filter. This is similar to the technique commonly used in PLL synthesizers.

As is well known, when out of lock, a mixer type phase detector does not provide any frequency discrimination. This means that the under normal circumstances, a loop of this type is not guaranteed to lock. However in the HD155121F, a well defined offset current is added to the phase detector output, so that when the loop is out of lock, this offset current linearly charges the capacitors in the loop filter. This has the effect of sweeping the VCO across the band. When the down converted signal from the VCO approaches the reference frequency, the Gilbert cell begins to operate as a phase detector and the loop acquires in the normal way. The presence of the offset current in lock is unimportant, as it only results in a static phase offset between the final signal and the reference signal.

At the end of the transmit burst, when the transmitter is disabled, a switch closes to discharge the loop filter capacitors. This resets the acquisition process in preparation for the start of the next burst.

The closed loop bandwidth of the OPLL should be designed to be around 1.2 to 1.5 MHz, which should be large enough to allow rapid locking and accurate tracking of the modulation. If the bandwidth is too large, the OPLL will not reject the noise from the modulator sufficiently. The ideal bandwidth will be a compromise dependant on the noise performance of the VCO and amplifier chain.

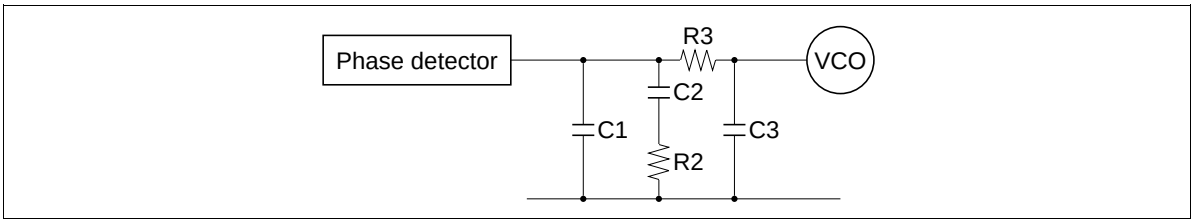


Figure A-1 Loop Filter Circuit of OPLL

The following equations provide a good starting point for the design of the OPLL.

Let:

f_0 = Closed loop unity gain frequency (Hz) (Closed loop bandwidth)
$f_n = f_0 / 2$ = Closed loop resonant frequency (Hz)
$\omega_n = 2\pi \cdot f_n$
k_v = VCO gain (Hz / V)
$k_{vr} = 2 \cdot \pi \cdot k_v$ (rad / V sec)
k_d = Peak phase dotector current = 1.2 (mA) in GSM mode (at RICURAD = 22 kΩ)
k_{dr} = Phase detector gain = $(\sqrt{2} \cdot k_d) / \pi = 1.7 / \pi$ (mA / rad) (at RICURAD = 22 kΩ)
ξ = DampingFactor ≅ 0.9

Then:

$C2 = k_{vr} \cdot k_{dr} / \omega_n{}^2$
$R2 = 2 \cdot \xi \cdot \sqrt{1/(k_v \cdot k_d \cdot C2)} = (2 \cdot \xi) / (\omega_n \cdot C2)$
$C1 = C2 / 15$
$R3 \cdot C3 \cong 1/(10 \cdot \omega_n)$

Note that many VCO modules have up to 100 pF capacitance on the control line. This can be very significant when designing high bandwidth loops.

The phase detector peak output current is centered around 1.2 mA which is set by an 22 kΩ resistor RICURAD on pin 12.

For example, the f_0 = 1.2 MHz loop filter using the VCO of k_v = 30 MHz / V (GSM) should be designed in the following method.

Let:

$f_0 = 1.2\ (\text{MHz}) = 1.2 \times 10^6$ (Hz)
$f_n = f_0 / 2 = 600\ (\text{kHz}) = 6 \times 10^5$ (Hz)
$\omega_n = 2\pi \cdot f_n = 2\pi \cdot 6 \times 10^5$ (rad / sec)
$k_v = 30\ (\text{MHz / V}) = 30 \times 10^6$ (Hz / V)
$k_{vr} = 2\pi \cdot k_v = 2\pi \times 30 \times 10^6$ (rad / V sec)
$k_d = 1.2\ (\text{mA})$ (at RICURAD = 22 kΩ)
$k_{dr} = 1.7 / \pi\ (\text{mA / rad}) = 1.7 \times 10^{-3}) / \pi\ (\text{A / rad})$ (at RICURAD = 22 kΩ)
ξ = Damping Factor ≅ 0.9

Then:

$$C2 = k_{vr} \cdot k_{dr} / \omega_n{}^2 = \frac{2 \times 30 \times 10^6 \times 1.7 \times 10^{-3}}{(2\pi \times 6 \times 10^5)^2} = 7.2 \times 10^{-9} = 7.2\ \text{nF}$$

$$R2 = (2 \cdot \xi) / (\omega_n \cdot C2) = \frac{2 \times 0.9}{2\pi \times 6 \times 10^5 \times 7.2 \times 10^{-9}} = 66\ \Omega$$

$$C1 = C2 / 15 = (7.2 \times 10^{-9}) / 15 = 480\ \text{pF}$$

$$R3 \cdot C3 \cong 1/(10 \cdot \omega_n) = \frac{1}{2\pi \times 6 \times 10^6}$$

When the VCO modules have 33 pF capacitance on the control line, C3 is 33 pF.

$C3 = 33\ \text{pF}$
$R3 = 804\ \Omega$

The result of the calculations for the PLL loop characteristic,based on the following block diagram (figure A-2), is showed in figure A-3 and figure A-4. The offset PLL will be stable if the component values shown are used.

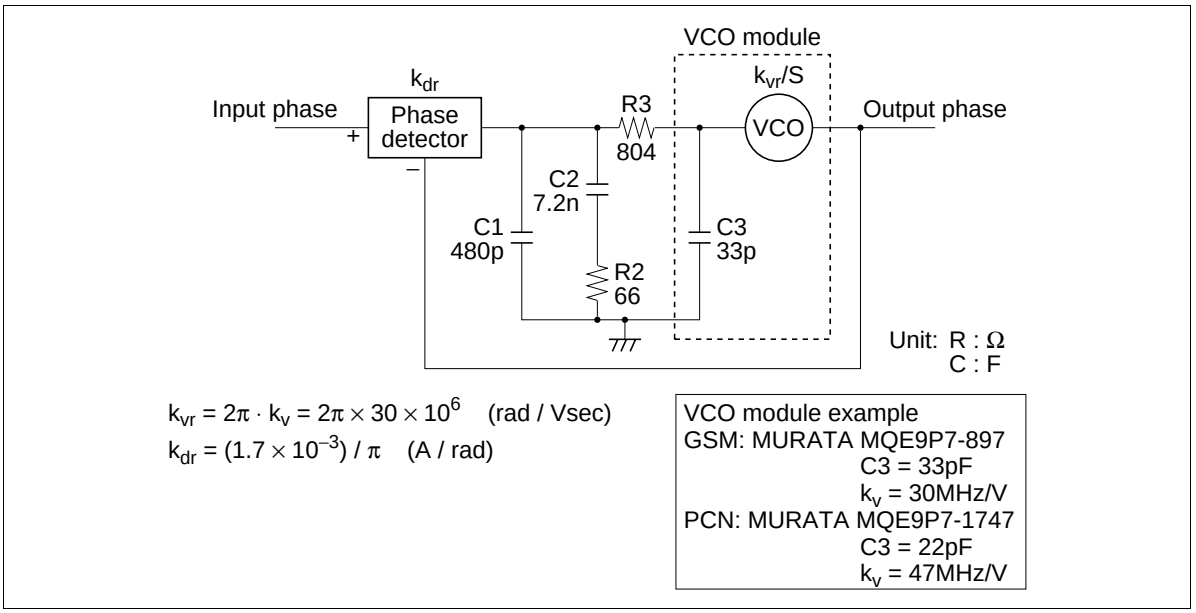


Figure A-2 Block Diagram for OPLL Simulation

The open loop transfer function, Hol(S), of OPLL as shown in figure A-2 is given below.

$$Hol(S) = \frac{k_{vr} \cdot k_{dr} \cdot (S + \omega_z)}{C1 \cdot C3 \cdot R3 \cdot S^2 \cdot (S^2 + 2S \cdot \omega_p + {\omega_p}^2)} = \frac{k_{vr} \cdot k_{dr} \cdot (S + \omega_z)}{C1 \cdot C3 \cdot R3 \cdot S^2 \cdot (S + \omega_{p1})(S + \omega_{p2})}$$

$$\omega_p = \sqrt{\frac{C1 + C2 + C3}{C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3}}$$

$$\varsigma = \frac{\omega_p \{ C2 \cdot R2 (C1 + C3) + C3 \cdot R3 (C1 + C2) \}}{2 (C1 + C2 + C3)}$$

$$\omega_z = \frac{1}{C2 \cdot R2}$$

$$\omega_{p_1} = \omega_p (\varsigma - \sqrt{\varsigma^2 - 1})$$

$$\omega_{p_2} = \omega_p (\varsigma + \sqrt{\varsigma^2 - 1})$$

Let:

C1 = 480 pF
C2 = 7.2 nF
C3 = 33 pF (VCO input capcitance on the control line)
R2 = 66 Ω
R3 = 804 Ω

Then:

$\omega_p = 35.70 \times 10^6 = 2\pi \times 5.68$ (MHz)
$\varsigma = 1.036$
$\omega_z = 2.104 \times 10^6 = 2\pi \times 335$ (kHz)
$\omega_{p1} = 27.32 \times 10^6 = 2\pi \times 4.348$ (MHz)
$\omega_{p2} = 46.65 \times 10^6 = 2\pi \times 7.425$ (MHz)
$k_{vr} = 2\pi \times 30 \times 10^6$ (rad / V sec)
$k_{dr} = (1.7 \times 10^{-3}) / \pi$ (A / rad)

The magnitude, | Hol(jω) |, and the phase, Φ(jω), of Hol(S) are as shown in the following equations. When the above constants from ω_p to k_{dr} are substituted in the equations, then | Hol(jω) | and Φ(jω) in figure A-3 can be obtained.

$$|Hol(j\omega)| = \frac{k_{vr} \cdot k_{dr} \cdot \sqrt{\omega^2 + {\omega_{p1}}^2}}{C1 \cdot C3 \cdot R3 \cdot \omega^2 \cdot \sqrt{\omega^2 + {\omega_{p1}}^2} \cdot \sqrt{\omega^2 + {\omega_{p2}}^2}}$$

$$\Phi(j\omega) = \tan^{-1}(\omega / \omega_z) - \tan^{-1}(\omega / \omega_{p1}) - \tan^{-1}(\omega / \omega_{p2}) - 180 \text{ (deg)}$$

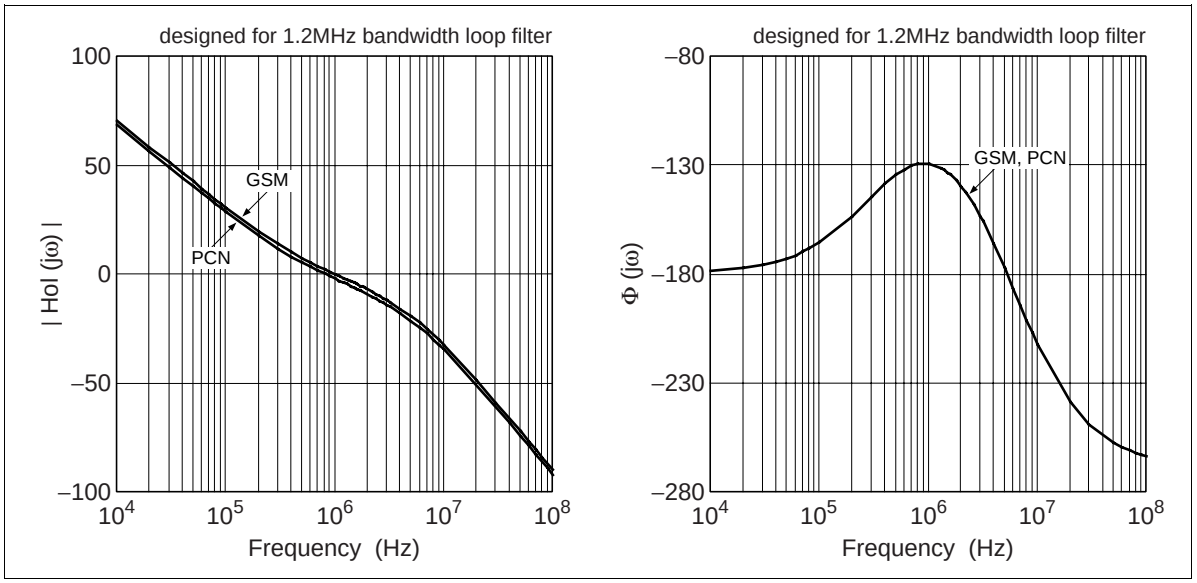


Figure A-3 The Magnitude, | Hol(jω) |, and the Phase, Φ(jω), of Open Loop Transfer Function Hol(jω)

Moreover, the closed loop transfer function, Hcl(jw) is the following equation, and the magnitude characteristic, Hcl(jω), of he closed loop is shown is figure A-4.

$$Hcl(j\omega) = \frac{Hol(j\omega)}{1 + Hol(j\omega)}$$

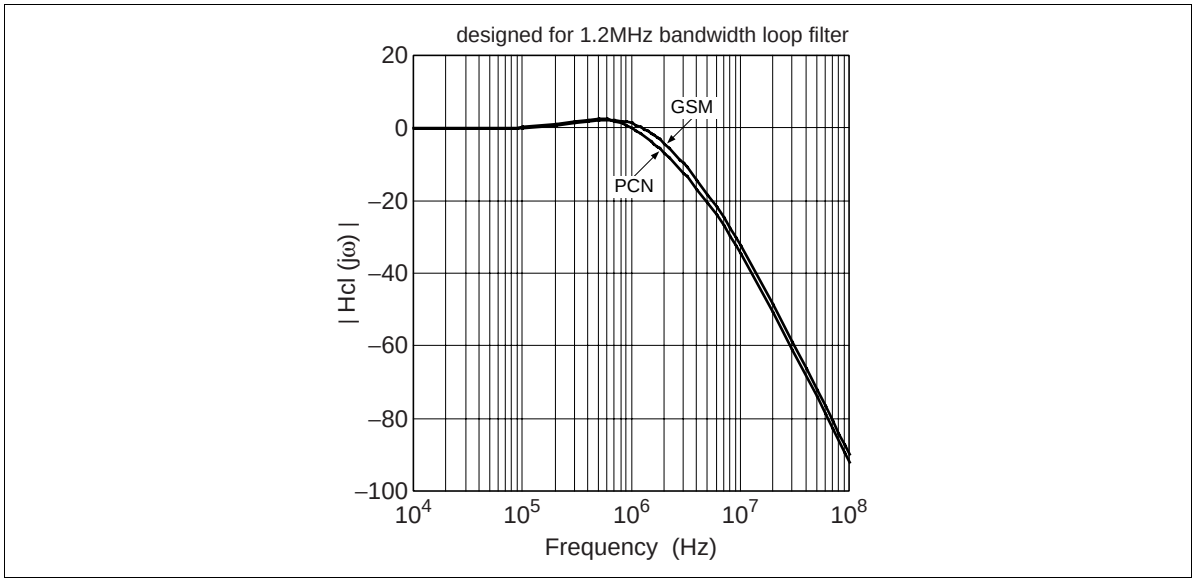


Figure A-4 The Magnitude, | Hcl(jω) | of Closed Loop Transfer Function Hcl(jω)

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