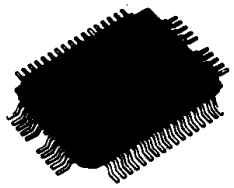
HMCS45A(HD38820,HD38825)

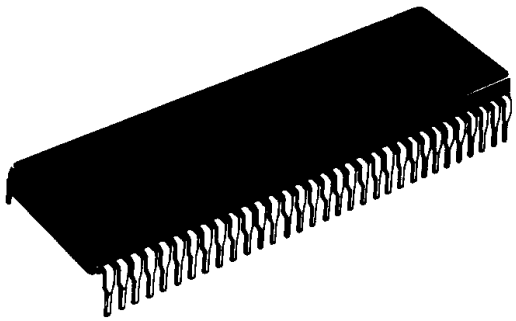
The HMCS45A is the PMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Event Counter on single chip. The HMCS45A is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The PMOS technology of the HMCS45A provides high voltage I/O capability for direct driving vacuum-fluorescent display.

HMCS45A



(FP-54)

HMCS45A

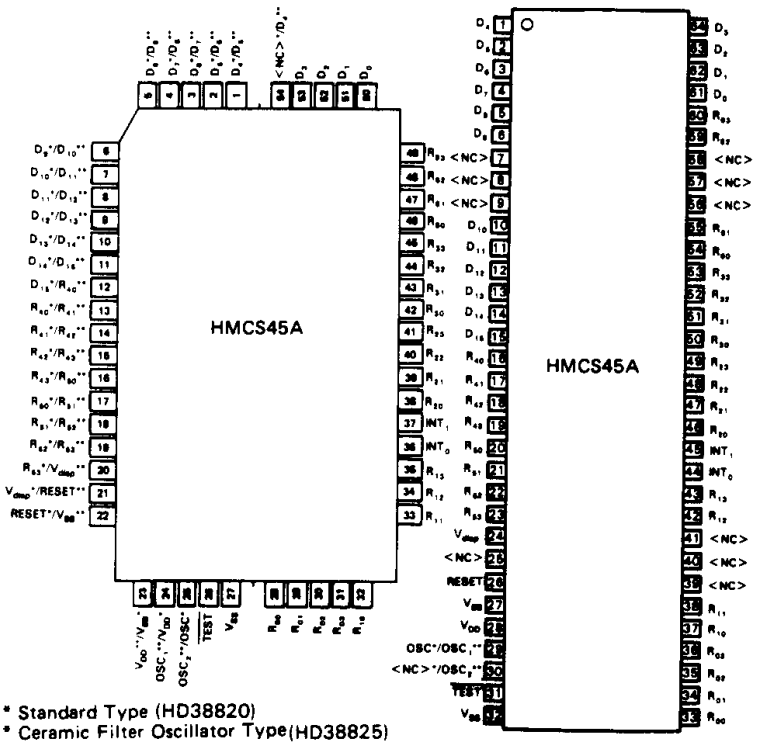


(DP-64S)

■ FEATURES

- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM (4 bits/Digit)
- 44 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- 10 μsec Instruction Cycle Time
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├─2 External Interrupt Lines
  └─Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- High Voltage I/O Capability, −49V max.
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or Open Drain
- Built-in RC Oscillator; Standard Type (HD38820)
- Built-in Ceramic Filter Oscillator; Ceramic Filter Oscillator Type(HD38825)
- Built-in Power-on Reset Circuit
- Stand-by Mode (RAM Data Hold); 8mW max.
- PMOS Technology
- Single, −10V Power Supply

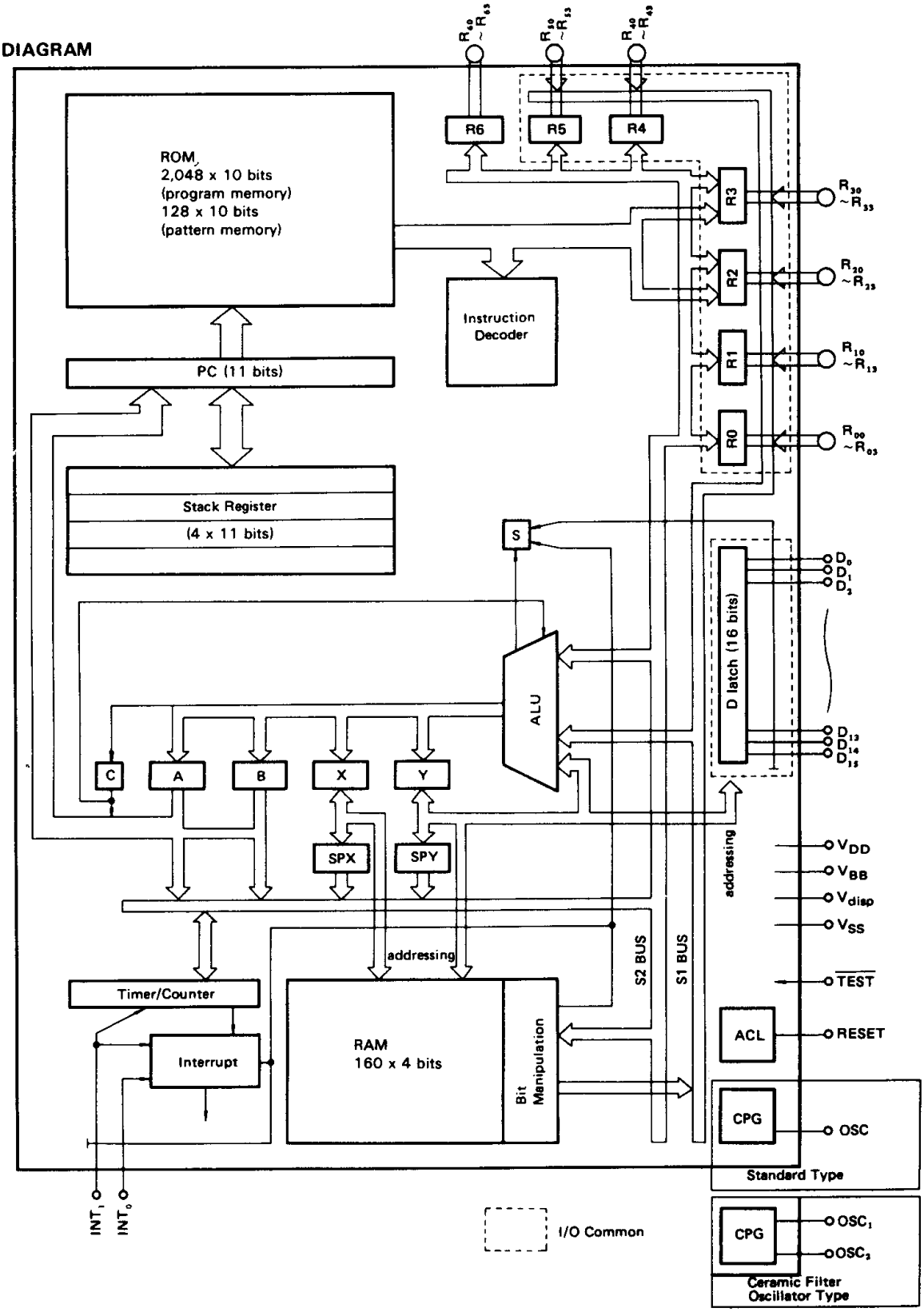
■ PIN ARRANGEMENT



* Standard Type (HD38820)
** Ceramic Filter Oscillator Type(HD38825)

(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Pin Voltage (1)	$-V_{T1}$	−0.3 to +18	V	Except for pins specified by $-V_{T2}$
Pin Voltage (2)	$-V_{T2}$	−0.3 to +50	V	Applied to high break-down voltage pins [Note 3]
Maximum Power Consumption	P_C	400	mW	
Maximum Total Output Current	$-\Sigma I_o$	45	mA	[Note 4]
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to V_{SS}.
[NOTE 3] High break-down voltage pins can be specified by user among the following pins. They are specified at ROM ordering using the "Mask Option List". (Unspecified pins are low break-down voltage pins.)
D_0 to D_{15}, R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}, R_{40} to R_{43}, R_{50} to R_{53}, R_{60} to R_{63}, INT_0, INT_1, RESET, V_{disp}.
Other pins cannot be specified as high break-down voltage pin.
[NOTE 4] Maximum Total Output Current is the total sum of output currents which can flow out simultaneously from output pins and I/O common pins.

■ ELECTRICAL CHARACTERISTICS-1 ($-V_{DD}=-V_{BB}=10V\pm10\%$, $-V_{disp}=49V$ max., Ta=−20 to +75°C)

Item	Symbol	Test Conditions	Value			Unit	Note
			min	typ	max		
Input "Low" Voltage (1)	$-V_{IL1}$	$-V_{DD}=-V_{BB}=9V$	4.0	–	49	V	3
		$-V_{DD}=-V_{BB}=11V$	4.7				
Input "Low" Voltage (2)	$-V_{IL2}$	$-V_{DD}=-V_{BB}=9V$	4.0	–	49	V	4
		$-V_{DD}=-V_{BB}=11V$	4.7				
Input "High" Voltage (1)	$-V_{IH1}$		–	–	2.55	V	3
Input "High" Voltage (2)	$-V_{IH2}$		–	–	2.0	V	4
Output "Low" Voltage (1)	$-V_{OL1}$	$-V_{disp}=49V$	45	–	–	V	5
Output "Low" Voltage (2)	$-V_{OL2}$	56kΩ to −49V	45	–	–	V	6
Output "High" Voltage (1)	$-V_{OH1}$	$-I_{OH}=3mA$	–	–	1.8	V	7
Output "High" Voltage (2)	$-V_{OH2}$	$-I_{OH}=10mA$	–	–	1.8	V	8
Interrupt Input Hold Time	t_{IINT}		$2\cdot T_{inst}$	–	–	μs	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	
Input Leakage Current	$-I_{IL}$	$-V_{in}=0$ to 49V	–	–	50	μA	9
Pull up MOS Current	I_P	$-V_{disp}=45V$	100	–	400	μA	2
Supply Current	$-I_{DD}$		–	–	30	mA	
	$-I_{BB}$		–	–	4	mA	

(to be continued)

Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
External Clock Operation [Standard Type]							
External Clock Frequency	f_{cp}		200	–	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
External Clock "Low" Level	$-V_{CPL}$	$-V_{DD}=-V_{BB}=9V$	4.0	–	17	V	
		$-V_{DD}=-V_{BB}=11V$	4.7				
External Clock "High" Level	$-V_{CPH}$		–	–	1.0	V	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{cp}$	9.1	–	20	μs	
Internal Clock Operation (R_f C_f Oscillation) [Standard Type]							
Clock Oscillation Frequency	f_{OSC}	$R_f=30k\Omega\pm2\%$, $C_f=100pF\pm5\%$	320	–	480	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{OSC}$	8.4	–	12.5	μs	
Internal Clock Operation (Ceramic Filter Oscillation) [Ceramic Filter Oscillator Type]							
Clock Oscillation Frequency	f_{OSC}	Ceramic Filter	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{OSC}$	9.8	–	10.2	μs	

Specifications of low break-down voltage pins specified by user are as follows.
($-V_{DD}=-V_{BB}=10V\pm10\%$, $-V_{disp}=17V$ max., Ta = −20 to +75°C)

Item	Symbol	Test Conditions	Value min	Value max	Unit	Note
Input "Low" Voltage (1)	$-V_{IL1}$	$-V_{DD}=-V_{BB}=9V$	4.0	17	V	3
		$-V_{DD}=-V_{BB}=11V$	4.7			
Input "Low" Voltage (2)	$-V_{IL2}$	$-V_{DD}=-V_{BB}=9V$	4.0	17	V	4
		$-V_{DD}=-V_{BB}=11V$	4.7			
Output "Low" Voltage (1)	$-V_{OL1}$	$-V_{disp}=10V$	8.5	–	V	5
Output "Low" Voltage (2)	$-V_{OL2}$	56kΩ to −10V	8.5	–	V	6
Input Leakage Current	$-I_{IL}$	$-V_{in}=0$ to 17V	–	5	μA	9
Pull up MOS Current	I_P	$-V_{disp}=10V$	80	350	μA	2

[NOTE 1] All voltages are with respect to V_{SS}.
[NOTE 2] Pull up MOS current (the current which flows in V_{disp} through pull up MOS when the pin is connected to V_{SS}) varies with the value of V_{disp}. It is shown as follows.

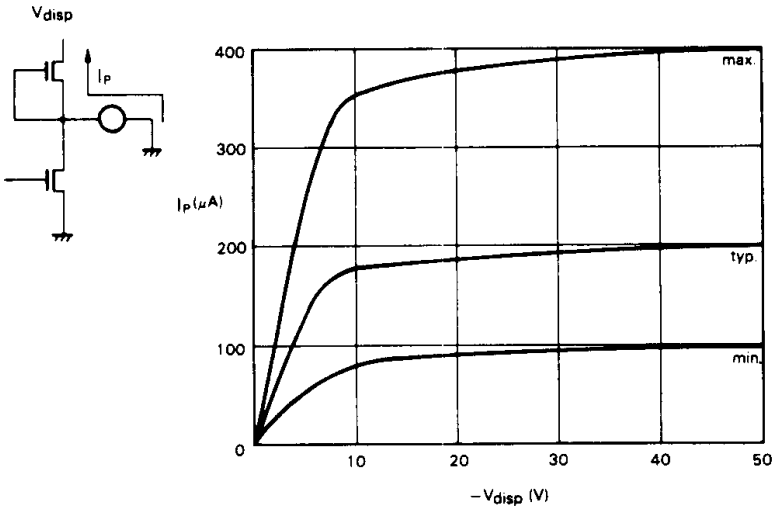


Figure 1 I_P vs. V_{disp}

[NOTE 3] This is applied to D_0 to D_{15}, R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}, R_{40} to R_{43}, R_{50} to R_{53}.
[NOTE 4] This is applied to INT_0, INT_1 and RESET. The system is in the reset state when RESET is at "1" (High) level, and in the operating state at "0" (Low) level. When Built-in Reset is used, RESET should be connected to V_{DD}.
[NOTE 5] This is applied to With Pull up MOS pins.
[NOTE 6] This is applied to No Pull up MOS pins.
[NOTE 7] This is applied to R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}, R_{40} to R_{43}, R_{50} to R_{53}, R_{60} to R_{63}.
[NOTE 8] This is applied to D_0 to D_{15}.
[NOTE 9] Pull up MOS current is excluded.

■ ELECTRICAL CHARACTERISTICS-2 (Ta = −20 to +75°C)

• Reset

Item	Symbol	Test Conditions	Value min	Value max	Unit
Power Supply Fall Time	t_{fDD}	Built-in Reset	0.1	10	ms
Power Supply OFF Time	t_{OFF}	Built-in Reset	1	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset $-V_{DD}=-V_{BB}=9$ to 11V [Standard Type] (External Clock Operation, R_f C_f Oscillation)	1	–	ms
		External Reset $-V_{DD}=-V_{BB}=9$ to 11V [Ceramic Filter Oscillator Type] (Ceramic Filter Oscillation)	4	–	
RESET Pulse Width (2)	t_{RST2}	External Reset $-V_{DD}=-V_{BB}=9$ to 11V	$2 \cdot T_{inst}$	–	μs
RESET Rise Time	t_{rRST}	$-V_{DD}=-V_{BB}=9$ to 11V	–	20	ms
RESET Fall Time	t_{fRST}	$-V_{DD}=-V_{BB}=9$ to 11V	–	20	ms

[NOTE] All voltages are with respect to V_{SS}.

• Data Hold

Item	Symbol	Test Conditions	Value min	Value max	Unit
Data Hold Voltage	$-V_{DR}$	RESET = −0.2V	2.0	–	V
Data Hold Current	$-I_{DR}$	RESET = −0.2V, $-V_{DR}$ = 2V	–	4	mA
Data Save Time	t_{DR}		100	–	μs
Operation Recovery Time	t_{RC}	[Standard Type] (External Clock Operation, R_f C_f Oscillation)	1	–	ms
		[Ceramic Filter Oscillator Type] (Ceramic Filter Oscillation)	4	–	

[NOTE] All voltages are with respect to V_{SS}.

■ SIGNAL DESCRIPTION

The input and output signals for the HMCS45A, shown in PIN ARRANGEMENT, are described in the following paragraphs.

- **V_{DD}, V_{BB} and V_{SS}**

Power is supplied to the HMCS45A using these pins. V_{DD} is power of logic parts except RAM, V_{BB} is power of RAM and V_{SS} is ground connection.

- **V_{disp}**

V_{disp} is used as power supply of Pull up MOS and has no relation to internal logic operation.

- **RESET**

This pin resets the HMCS45A independently of the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS45A. The HMCS45A can be reset by pulling RESET high.

Refer to RESET FUNCTION for additional information.

- **OSC (OSC$_1$ and OSC$_2$)**

These pins provide control input for the built-in oscillator circuit. Resistor and capacitor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

- **$\overline{TEST}$**

This pin is not for user application and must be connected to V_{SS}.

- **INT_0 and INT_1**

These pins generate interrupt request to the HMCS45A.

Refer to INTERRUPTS for additional information.

- **R_{00} to R_{03}, R_{10} to R_{13}, R_{20} to R_{23}, R_{30} to R_{33}, R_{40} to R_{43}, R_{50} to R_{53}**

These 24 lines are arranged into six 4-bit Data Input/Output Common Channels. The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

- **R_{60} to R_{63}**

These 4 lines are the 4-bit Data Output Channel. The 4-bit register (Data I/O Register) is attached to this channel. This channel is directly addressed by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

- **D_0 to D_{15}**

These lines are sixteen 1-bit Discrete Input/Output Common Pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. The D_0 to D_3 pins are also addressed directly by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

■ ROM

- **ROM Address Space**

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS45A consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

The ROM address is composed of the program area (page 0 to page 31) and the pattern area (pages 61, 62). (64 words/page).

The ROM capacity is 2,176 words (1 word = 10 bits) in all.

Only the program area can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 2.

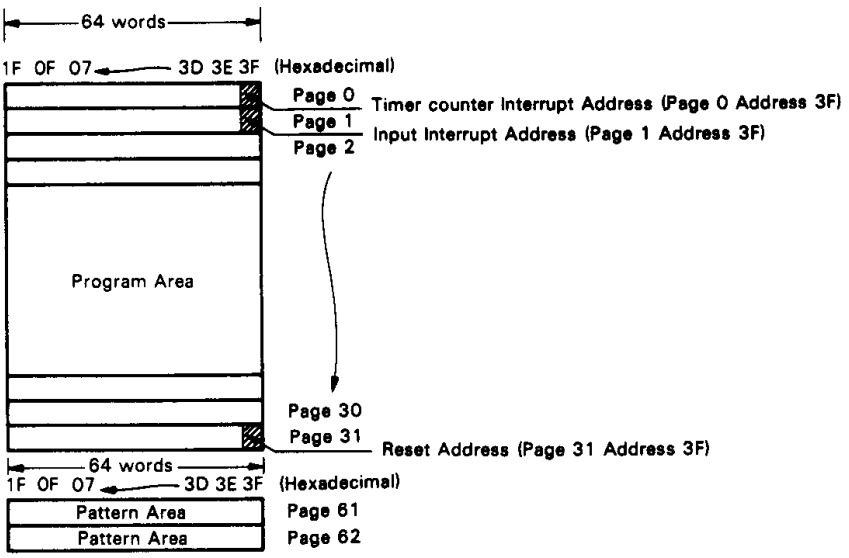


Figure 2 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing of ROM. It consists of the page part and the address part as shown in Figure 3.

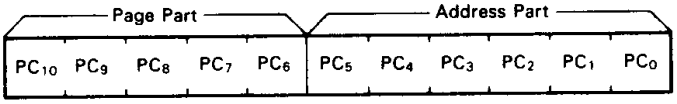


Figure 3 Configuration of Program Counter

Once a certain value is loaded into a page part, the content is unchanged until other value is loaded by the program. Any number among 0 to 31 can be set in the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexadecimal system is shown in Table 1. This sequence forms a loop and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

- **Designation of ROM Address and ROM Code**

The page part of the ROM address is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexadecimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10}) and represented by hexadecimal. The examples are shown in Figure 4.

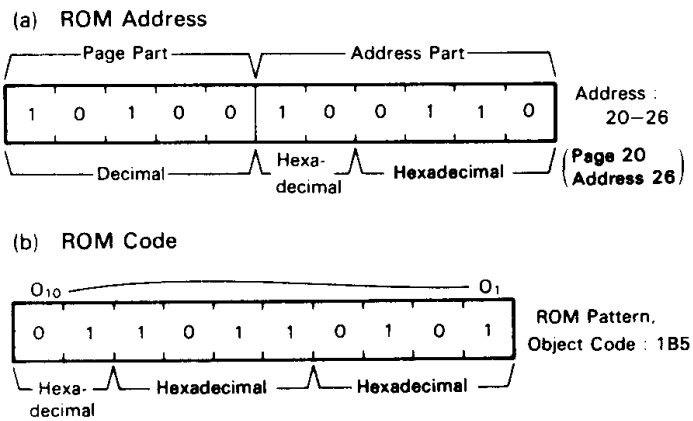


Figure 4 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

• Reference

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 5 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part is ORed with the upper 2 bits of B register, the Carry F/F and the operand p (p_0, p_1). The upper bit (p_2) of the operand is for referring to the pattern area.

The contents of the program counter is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and the next instruction is executed.

The pattern instruction is executed in 2 cycles.

Even when interrupt is enable, interrupt is disabled in the second cycle of the pattern instruction. However, the interrupt request is latched into the interrupt request F/F.

• Generation

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii)The pattern is loaded into the Data I/O registers R2 and R3.

The command bits (O_9, O_{10}) in the pattern determine which way is taken.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and mode (ii) are simultaneously performed when both O_9 and O_{10} are "1".

The correspondence of each bit of the pattern is shown in Figure 6.

Examples of how to use the pattern instruction is shown in Table 2.

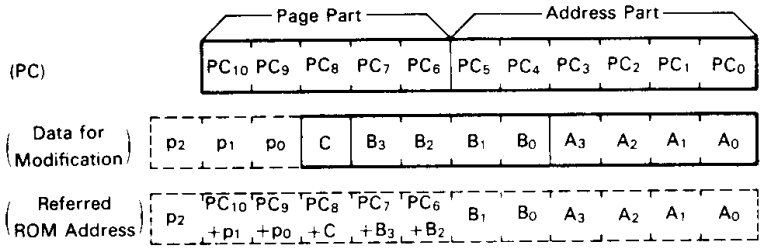


Figure 5 ROM Addressing for Pattern Generation

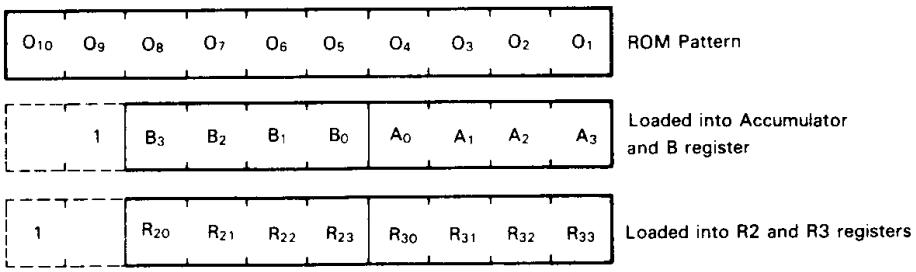


Figure 6 Correspondence of Each Bit of Pattern

Table 2 Example of how to use Pattern Instruction

Before Execution					Referred ROM Address	Pattern	After Execution			
PC Value	p	C	B	A			B	A	R2	R3
0-3F	1	0	A	0	10-20	12D	2	B	–	–
0-3F	7	1	4	0	61-00	22D	–	–	4	B
30-00	4	0/1	0	9	62-09	32D	2	B	4	B
30-00	4	0/1	F	9	63-39					

"–" means that the value is unchanged after the execution.
"0/1" means that either "0" or "1" will do.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways.

They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when

the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 7.

- **LPU**

By LPU instruction, a jump between pages is performed.

The lower 5 bits of the ROM Object Code (operand u) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is a conditional instruction and performed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped. The operation is shown in Figure 8.

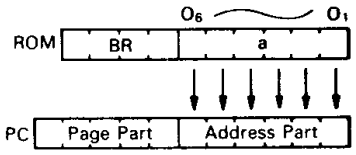


Figure 7 BR Operation

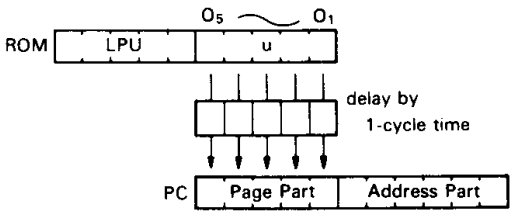


Figure 8 LPU Operation

- **BRL**

By BRL instruction, the program branches to an address in any page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two steps as follows.

```
                                BRL  a – b→LPU a
<Jump to address b on page a>       BR   b
```

BRL instruction is a conditional instruction because of its characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F becomes "1".

- **TBR (Table Branch)**

By TBR instruction, the program branches referring to the table.

The program counter is modified with the accumulator, the B register, the Carry F/F, the operand p. The method for modification is shown in Figure 9.

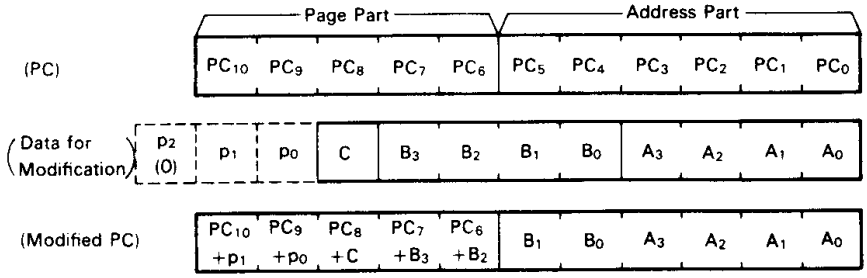


Figure 9 Modification of Program Counter by TBR Instruction

The accumulator and the lower 2 bits of B register are assigned into the address part of the program counter. The upper 2 bits of B register, Carry F/F, and the operand p_1, p_0 are ORed with the page part of the program counter.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

- **CAL**

By CAL instruction, subroutine jump to an address in the Subroutine Page is performed.

The Subroutine Page is page 0.

The address next to CAL instruction address is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 10.

The page part of the program counter is 0. The lower 6 bits (operand a, O_6 to O_1) of the ROM Object Code are transferred to the address part of the program counter.

The HMCS45A has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

- **CALL**

By CALL instruction, subroutine jump to an address in any page is performed.

This instruction is a macro instruction of LPU and CAL. The subroutine jumps to the page specified by LPU enables the subroutine jump to an optional address.

```
                                CALL  a – b→LPU a
<Subroutine jump to address b on page a>      CAL b
```

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

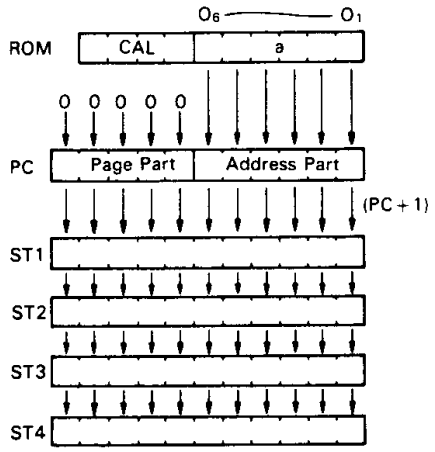


Figure 10 Subroutine Jump Stacking Order

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 160 digits (640 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits, 16 digits (MR0 to MR15), are called "Memory Register (MR)". The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 11.

If an instruction consists of a simultaneous read/write operation of RAM (exchange between the contents of RAM and those of the register), the writing data doesn't affect the reading data because read operation precedes write operation.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status F/F "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 12.

X \ Y (f \ d)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
← digit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0															
1	1															
2	2															
3	3															
4	4															
5	5															
6	6															
7	7															
8–11*	8															
12–15*	9	MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

↑ file No.

* The file 8 is selected when X register has any value among 8 to 11, and the file 9 is selected when 12 to 15.

Figure 11 RAM Address Space

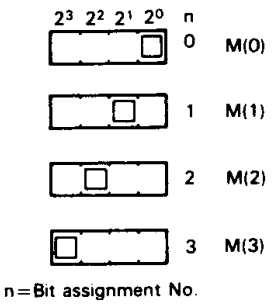


Figure 12 RAM Bit and Operand n

■ REGISTER

The HMCS45A has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

• Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1"

• Accumulator (A; A Register) and Carry F/F (C)

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F respectively. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

• B Register (B)

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

• X Register (X)

The result of ALU operation (4 bits) is loaded into this register. The X register is exchangeable with the SPX register and addresses the RAM file.

• SPX Register (SPX)

The SPX register is exchangeable with the X register.

The SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with the X register.

• Y Register (Y)

The result of ALU operation (4 bits) is loaded into this register. The Y register is exchangeable with the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digits and 1-bit Discrete I/Os.

• SPY Register (SPY)

The SPY register is exchangeable with the Y register. The SPY register is used to stack the contents of the Y register and expand the addressing system of RAM and 1-bit Discrete I/Os in combination with the Y register.

■ INPUT/OUTPUT

• 4-bit Data Input/Output Channel (R)

The HMCS45A has six 4-bit Data I/O Common Channels (R0 to R5) and one 4-bit Output Channel (R6).

The 4-bit registers (Data I/O Register) are attached to these channels.

Each channel is directly addressed by the operand p of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R6 via the bus lines. ROM bit patterns are loaded into the Data I/O Registers R2 and R3 by the pattern instruction.

The input instruction inputs the 4-bit data into the accumulator and the B register through the channels R0 to R5. Note that, since the Data I/O Register output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register output and the pin input.

Therefore, the Data I/O Register should be set to 0 (all bits of the Data I/O Register is "0") not to affect the pin input before execution of input instruction.

The block diagram is shown in Figure 13. The I/O timing is shown in Figure 14.

• 1-bit Discrete Input/Output Common Pin (D)

The HMCS45A has sixteen 1-bit Discrete I/O Common Pins.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and level ("0" or "1") of the addressed pin can be tested by an input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch output and the pin input. Therefore, the latch should be reset to "0" not to affect the pin input before execution of input instruction.

The D_0 to D_3 are also addressed directly by the operand n of input/output instruction and can be set or reset.

The block diagram is shown in Figure 15 and the I/O timing is in Figure 16.

• I/O Configuration

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 17.

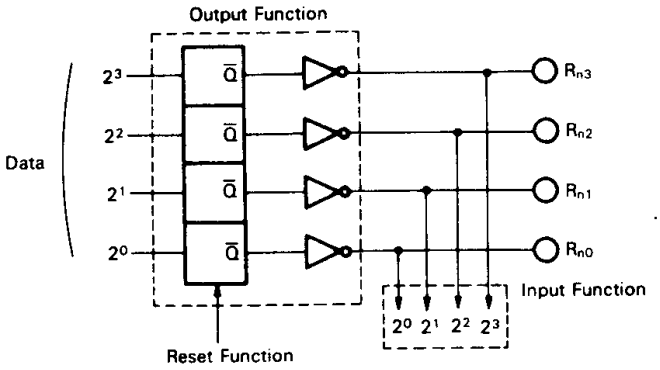


Figure 13 4-bit Data I/O Block Diagram

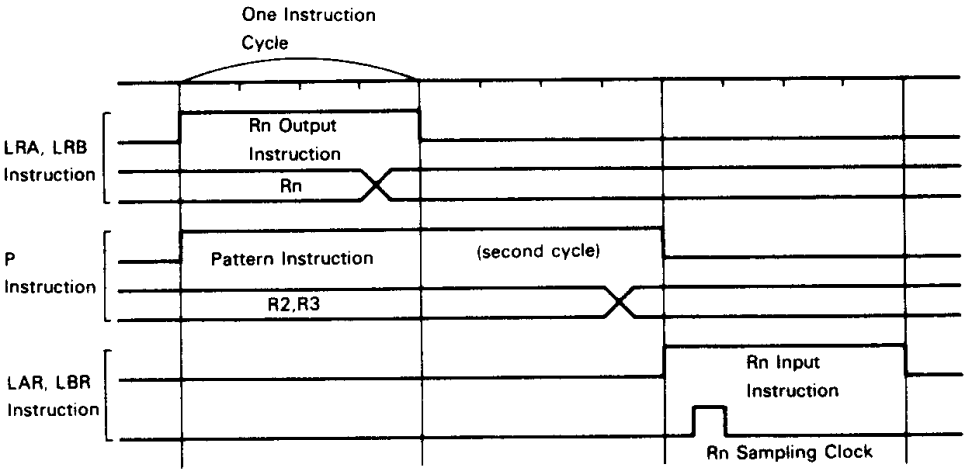


Figure 14 4-bit Data I/O Timing

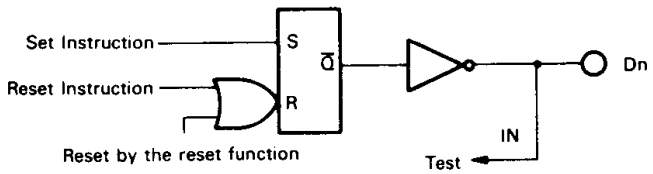


Figure 15 1-bit Discrete I/O Block Diagram

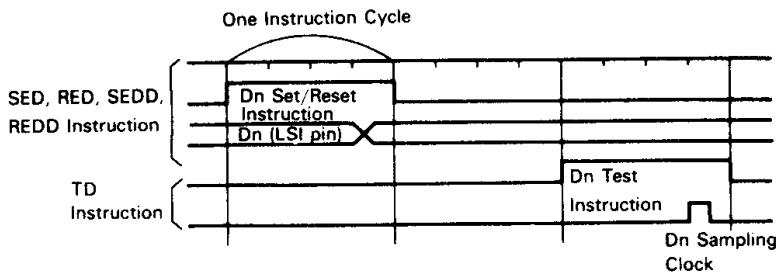
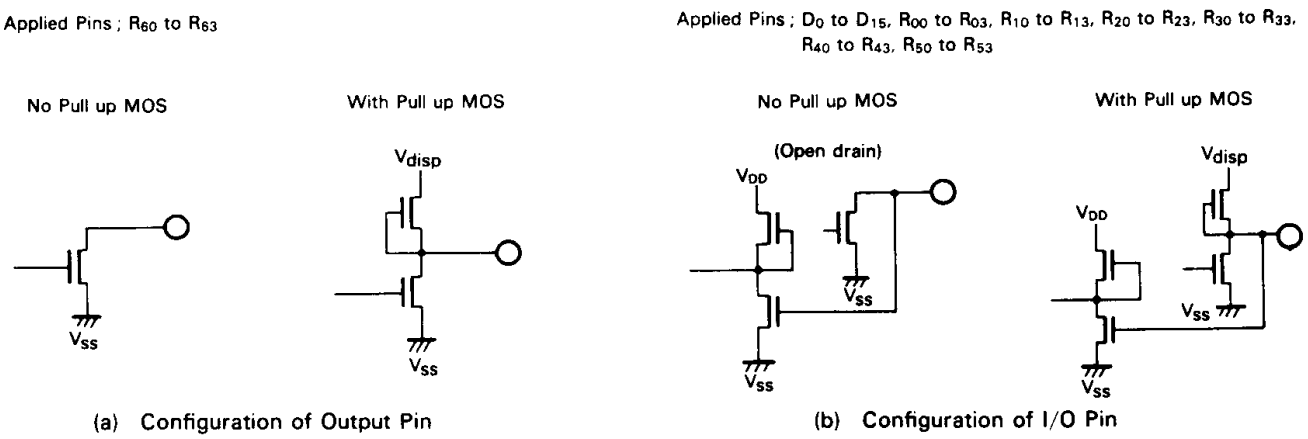


Figure 16 1-bit Discrete I/O Timing



(a) Configuration of Output Pin (b) Configuration of I/O Pin

Figure 17 I/O Configuration

■ TIMER/COUNTER

The timer/counter consists of 4-bit counter and 6-bit prescaler as shown in Figure 18.

The counter operates in the Timer Mode or Counter Mode according to the counting object. In the timer mode it counts overflow output pulse from the prescaler, and in the Counter Mode it counts INT_1 input pulse (counts leading edge), and increments to 15. Mode selection is determined according to the state of the CF. When the counter reaches zero (returns from 15), overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow \cdots$).

The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 3.

The prescaler is a 6-bit frequency divider. It generates 100/64 kHz pulses by dividing the system clock by 64. The prescaler is cleared when the data is loaded into the 4-bit counter by LTA, LTI instructions. The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output pulse is generated from the prescaler. During operation of the LSI, the prescaler operates and cannot be stopped.

The CF is the flip-flop (F/F) which controls the counter input. When the CF F/F is "1", input pulse of INT_1 is input to the counter (Counter Mode). When the CF is "0", prescaler overflow output pulse is input to the counter (Timer Mode).

The TF is the flip-flop (F/F) which masks the interrupt request from the timer/counter. It is set, reset and tested by instructions. If the overflow output pulse of the counter is generated when the TF F/F is "0", an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is "1", no interrupt request occurs. So it can be used as timer/counter interrupt mask.

The pulse width of INT_1 in the Counter Mode should be two or more cycles both at "High" and "Low" levels as shown in Figure 19.

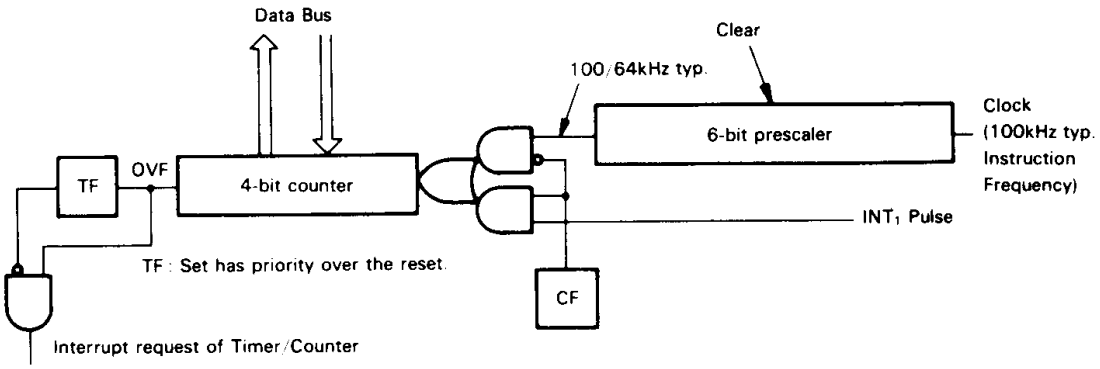


Figure 18 Timer/Counter Block Diagram

Table 3 Timer Range

Specified Value	Cycles	Time (ms)	Specified Value	Cycles	Time (ms)
0	1,024	10.24	8	512	5.12
1	960	9.60	9	448	4.48
2	896	8.96	10	384	3.84
3	832	8.32	11	320	3.20
4	768	7.68	12	256	2.56
5	704	7.04	13	192	1.92
6	640	6.40	14	128	1.28
7	576	5.76	15	64	0.64

[NOTE] Time is based on instruction frequency 100kHz. (one instruction cycle = 10μs)

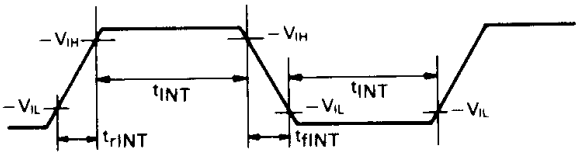


Figure 19 The Pulse Width of the INT_1 pin in the Counter Mode

■ INTERRUPT

The HMCS45A can be interrupted in two different ways: through the external interrupt input pins (INT_0, INT_1) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the contents of the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively. At that time, the Interrupt Enable F/F (I/E) is set and the address jumps to a fixed destination (Interrupt Address), and then the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI (Return Interrupt) instruction which sets the I/E F/F simultaneously with the RTN instruction.

The Interrupt Address:

Input Interrupt Address . . . . .
Page 1 Address 3F

Timer/Counter Interrupt Address . . . . .
Page 0 Address 3F

The input interrupt has priority over the timer/counter interrupt.

The INT_0 and INT_1 pins have interrupt request functions.

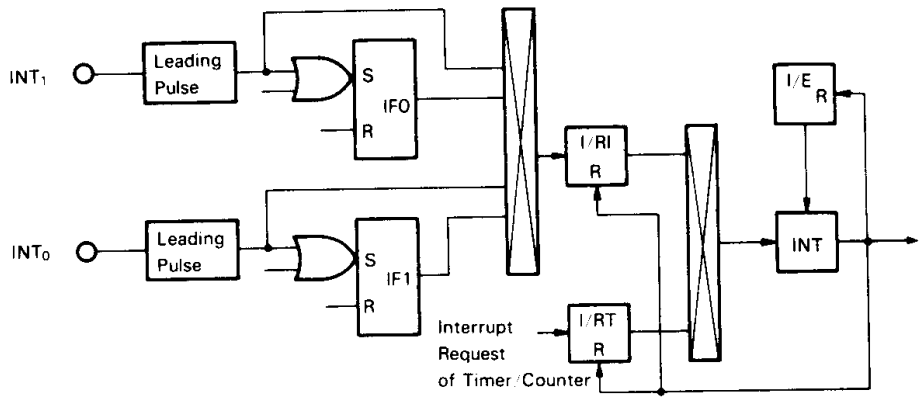
Each pin consists of a circuit which generates leading pulse and the interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the INT_0 or INT_1 pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, it is an interrupt mask for INT_0 or INT_1. (If a leading pulse is generated, no interrupt request occurs.)

An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS45A gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the INT_0 pin and the INT_1 pin can be tested by interrupt instruction. Therefore, the INT_0 and the INT_1 can be used as additional input pins with latches.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are the same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt servicing is achieved.

The interrupt circuit block diagram is shown in Figure 20.



IF0, IF1 : Set has priority over the reset.

Figure 20 Interrupt Circuit Block Diagram

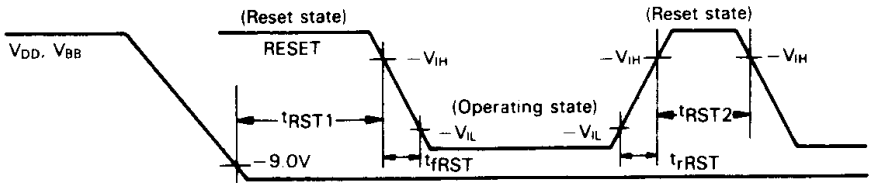
■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS45A gets into operation by setting it to "0" ("Low" level); Refer to Figure 21. Moreover, the HMCS45A has the automatic reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply; Refer to Figure 22. When the Built-in Reset Circuit is used, RESET should be connected to V_{SS}.

Internal state of the HMCS45A is specified as follows by the reset function.

- Program Counter (PC) is set to 3F address on 31 page (31-3F).
- I/RI, I/RT, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- I/O latch and registers (D_0 to D_{15}, R0 to R6) are set to "0".

Note that other blocks (Status, Register, Timer/Counter, RAM, etc.) are not cleared.



- t_{RST1} includes the time required from the power ON until the operation gets into the constant state.
- t_{RST2} is applied when the operation is in the constant state.

Figure 21 RESET Timing

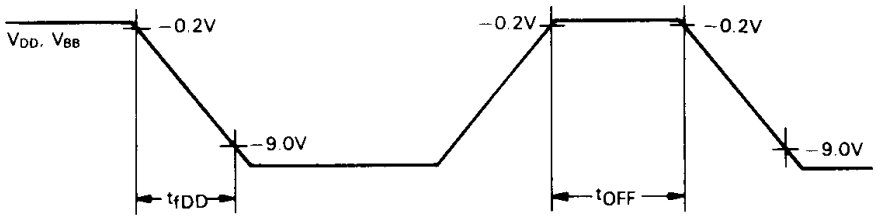


Figure 22 Power Supply Timing for Built-in Reset Circuit

■ DATA HOLD FUNCTION

The Data Hold Function is the function to hold the data of RAM at low power dissipation. In the Data Hold Mode, all the data of RAM are held.

The power supply consists of V_{DD} and V_{BB}, but these are used as one power supply (that is, $V_{DD} = V_{BB}$) in the operation. V_{disp} is only used as a power supply of Pull up MOS of I/O pin.

V_{DD} is the power supply of logic parts except RAM and V_{BB} is that of RAM. Therefore, the "Data Hold" is feasible at V_{DD} OFF and V_{BB} ON. The system should be in the reset state during the "Data Hold" in order to prevent RAM from writing at V_{DD} OFF.

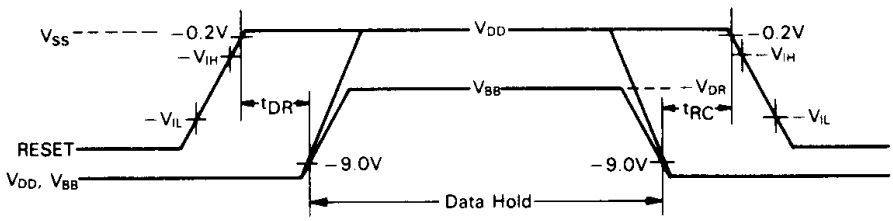


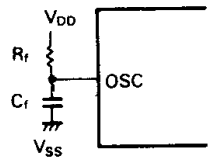
Figure 23 Data Hold Timing

■ OSCILLATOR

The HMCS45A contains its own on-board oscillator and clock circuit (Built-in CPG) requiring only an external timing control element. Also the HMCS45A can be provided an externally generated clock as a frequency source by an external oscillator (External CPG).

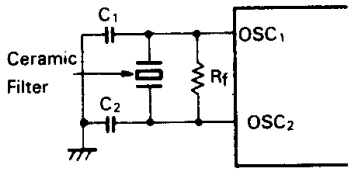
The user can select one clock operation mode using a mask option as shown in Figure 24.

(a) Internal Clock Operation Using R_f and Capacitor C_f (Built-in CPG ; R_f C_f Oscillator)



Wiring of OSC pin should be as short as possible because the oscillation frequency is modified by C_f.

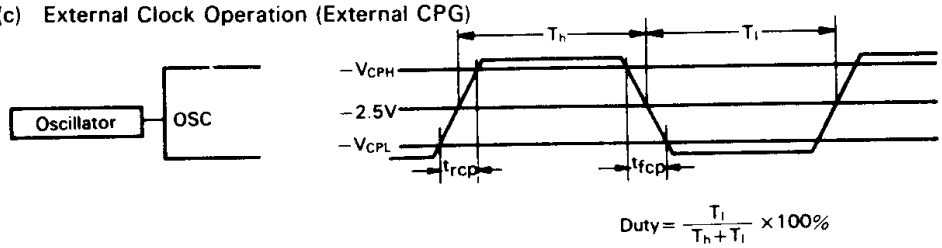
(b) Internal Clock Operation Using Ceramic Filter Circuit (Built-in CPG ; Ceramic Filter Oscillator)



Ceramic Filter ; CSB400P (MURATA)
R_f ; 1MΩ ± 10%
C_1 ; 220pF ± 10% (Ceramic Capacitor)
C_2 ; 220pF ± 10% (Ceramic Capacitor)

This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

(c) External Clock Operation (External CPG)



$$\text{Duty} = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 24 Clock Operation Mode

■ INSTRUCTION LIST

The instructions of the HMCS45A are listed according to their functions, as shown in Table 4.

Table 4 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAB	B → A	
	LBA	A → B	
	LAY	Y → A	
	LASPX	SPX → A	
	LASPY	SPY → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
	XSPY	Y ↔ SPY	
	XSPXY	X ↔ SPX, Y ↔ SPY	
RAM · Register Instruction	LAM (XY)	M → A (XY ↔ SPXY)	
	LBM (XY)	M → B (XY ↔ SPXY)	
	XMA (XY)	M ↔ A (XY ↔ SPXY)	
	XMB (XY)	M ↔ B (XY ↔ SPXY)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
	LBI i	i → B	
Arithmetic Instruction	AI i	A+i → A	C
	IB	B+1 → B	NZ
	DB	B−1 → B	NB
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−C (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	A+1 → A	
	COMB	B → B	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
	OR	A ∪ B → A	

(to be continued)

Group	Mnemonic	Function	Status
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
	BLEM	B ≦ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M (n)
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt Instruction	SEIE	"1" → I/E	
	SEIF0	"1" → IF0	
	SEIF1	"1" → IF1	
	SETF	"1" → TF	
	SECF	"1" → CF	
	REIE	"0" → I/E	
	REIF0	"0" → IF0	
	REIF1	"0" → IF1	
	RETF	"0" → TF	
	RECF	"0" → CF	
	TI0	Test INT_0	INT_0
	TI1	Test INT_1	INT_1
	TIF0	Test IF0	IF0
	TIF1	Test IF1	IF1
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
	LTA	A → Timer/Counter	
	LAT	Timer/Counter → A	
	RTNI	Return Interrupt	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R(p)	
	LRB p	B → R(p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

	Mnemonic only	Instruction execution only
	Mnemonic with X	After instruction execution, X ↔ SPX
	Mnemonic with Y	After instruction execution, Y ↔ SPY
	Mnemonic with XY	After instruction execution, X ↔ SPX, Y ↔ SPY
(Example)	LAM	M → A
	LAMX	M → A, X ↔ SPX
	LAMY	M → A, Y ↔ SPY
	LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ..... ALU Not Zero
   - C ..... ALU Overflow in Addition, that is, Carry
   - NB ..... ALU Overflow in Subtraction, that is, No Borrow
   - Except above ..... Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F.
   Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1 cycle. The pattern instruction (P) is executed in 2 cycles.

HMCS45A Mask Option List

Date	
Customer	
Dept.	
Name	
ROM CODE ID	
LSI Type Name (entered by Hitachi)	

(1) I/O Option

Pin Name	I/O	I/O Option A	I/O Option B	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	Remarks
D_0	I/O				R_{00}	I/O			
D_1	I/O				R_{01}	I/O			
D_2	I/O				R_{02}	I/O			
D_3	I/O				R_{03}	I/O			
D_4	I/O				R_{10}	I/O			
D_5	I/O				R_{11}	I/O			
D_6	I/O				R_{12}	I/O			
D_7	I/O				R_{13}	I/O			
D_8	I/O				R_{20}	I/O			
D_9	I/O				R_{21}	I/O			
D_{10}	I/O				R_{22}	I/O			
D_{11}	I/O				R_{23}	I/O			
D_{12}	I/O				R_{30}	I/O			
D_{13}	I/O				R_{31}	I/O			
D_{14}	I/O				R_{32}	I/O			
D_{15}	I/O				R_{33}	I/O			
					R_{40}	I/O			
					R_{41}	I/O			
					R_{42}	I/O			
					R_{43}	I/O			
					R_{50}	I/O			
					R_{51}	I/O			
					R_{52}	I/O			
					R_{53}	I/O			
INT_0	I				R_{60}	O			
INT_1	I				R_{61}	O			
RESET	I				R_{62}	O			
V_{disp}	Power Supply				R_{63}	O			

☆ Specify the I/O composition with a mark of "○" in the applicable composition column.
A: High Break-down Voltage B: With pull up MOS

(2) Package

Package
□ FP-54
□ DP-64S

☆ Mark "✓" in "□" for the selected package.

(3) CPG

CPG
□ External CPG
□ Built-in CPG (R_f C_f Oscillator)
□ Built-in CPG (Ceramic Filter Oscillator)

☆ Mark "✓" in "□" for the selected CPG.