

# HD44237P, HD44238P

## Single Chip CODEC with Filters (COMBO)

### Features

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package
- Power Supply Voltage  $\pm 5\text{ V} \pm 5\%$ , Low Power Dissipation (50 mW typ.)
- Follows A-Law (HD44237P)/ $\mu$ -law (HD44238P)
- Exceeds CCITT and D4 Specifications
- Synchronous/Asynchronous Operation
- Internal Clock Generator Operation for 64 kHz to 2048 kHz PCM Rate as PLL Circuit
- Anti-Aliasing Filter (2nd order CR Active Filter)
- Voltage Reference (Internal-Trimmed)
- Input Amplifier with Uncommitted Plus/Minus Terminals
- Auto-Zero Cancel Circuit without External Component

### Pin Configuration

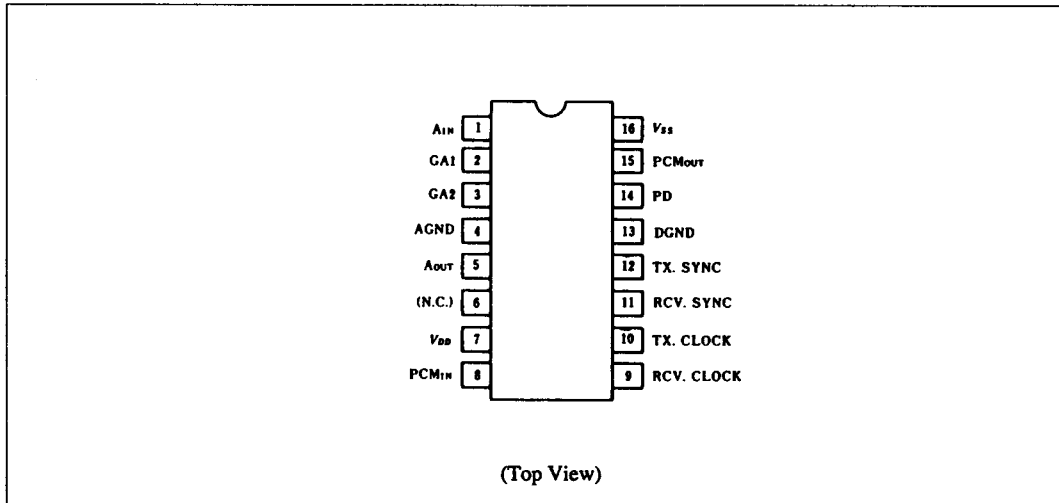


Figure 1 Pin Assignment

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Table 1. Pin Descriptions

| HD44237P<br>HD44238P |                  | Function          | Remarks   |
|----------------------|------------------|-------------------|---|
| No.                  | Symbol           |                   |   |
| 1                    | A <sub>IN</sub>  | Analog Input      |   |
| 2                    | GA <sub>1</sub>  | Gain Adjust 1     | Feed-Back Input                                   |
| 3                    | GA <sub>2</sub>  | Gain Adjust 2     | 10 kΩ ≤ R <sub>L</sub><br>C <sub>L</sub> ≤ 100 pF |
| 4                    | AGND             | Analog Ground     |   |
| 5                    | A <sub>OUT</sub> | Analog Output     | R <sub>L</sub> ≥ 600 Ω, C <sub>L</sub> ≤ 100 pF   |
| 6                    | N.C.             |                   | Open  |
| 7                    | V <sub>DD</sub>  | Positive Pow.Sup. | 5 V ± 5%  |
| 8                    | PCMIN            | PCM Data Input    | (TTL)   |
| 9                    | RCV.CLK          | PCM Bit Clock     | (TTL) 64 to 2048 kHz                              |
| 10                   | TX.CLK           |                   |   |
| 11                   | RCV.SYNC         | Synchronization   | (TTL) 8 kHz                                       |
| 12                   | TX.SYNC          |                   |   |
| 13                   | DGND             | Digital Ground    |   |
| 14                   | P <sub>d</sub>   | Power Down        | (TTL) "0" = down                                  |
| 15                   | PCMOUT           | PCM Data Output   | Open Drain  |
| 16                   | V <sub>SS</sub>  | Negative Pow.Sup. | -5 V ± 5%   |

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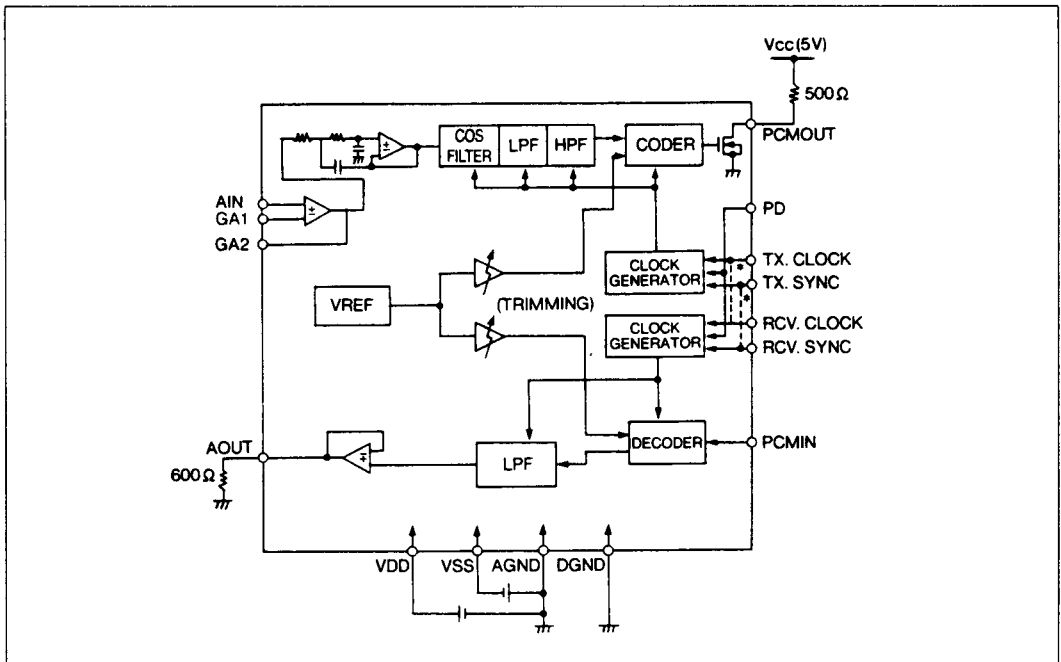


Figure 2 Block Diagram

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### General Description

The HD44237P, HD44238P are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band limiting filters and the analog/digital conversion circuits that conform to the A-Law or  $\mu$ -Law companding characteristic.

HD44237P is A-Law. HD44238P is  $\mu$ -Law.

These circuits provide the interface between the analog signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of  $\pm 5$  V.

For a sampling rate of 8 kHz, PCM input/output data rate can be selected from 64 kHz to 2048 kHz in synchronous or asynchronous operation. Internal PLL circuits generate the internal clock from the 8 kHz synchronization clock.

### Functional Description

Figure 2 shows the simplified block diagram of the HD44237P, HD44238P. The devices contain independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 Table 1 for HD44237P Table 2 for HD44238P respectively. A band-gap voltage generator supplies the reference level for the conversion process. 2nd Order CR Active Filter is implemented on chip to avoid the aliasing noise which is caused by the clock of transmit filter.

#### Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows gain trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 32 dB (typ) at 256 kHz and 40 dB (typ) at 512 kHz, the "effective" clock frequency of the following switched-capacitor Cosine Filter. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 128 kHz, followed by a 3rd Order High-Pass Filter clocked at 8 kHz. The resulting band-pass characteristics meet the CCITT, G.712 specifications. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of 64 kHz to 2048 kHz. A auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the HD44237P is a signbit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

#### Receive Section

A shift clock, from 64 kHz to 2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin  $x/x$  distortion due to the sample and hold operation. The filter output is available for driving electronic or transformer directly as long as the impedance is greater than 600  $\Omega$ .

#### Companding Law

The encoding and decoding characteristics of the Codecs comply with the requirements of CCITT G711 Table 1 or Table 2, corresponding to their comparing law. The even bits of PCM words are inverted for A-Law devices. Positive logic is used (the High level corresponds to '1').

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#### Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input will also put the chip into the stand-by mode. The SYNC input can be held high, low or disconnected. After the chip being activated by these functions, the PCMOUT is in high impedance state and the AOOUT is connected to AGND for about 1 ms to avoid the power-on noise.

#### Voltage Reference Circuit

A temperature compensated band-gap voltage generator provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply it to the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed to ensure a minimum gain error of  $\pm 0.1$  dB at the nominal power supply voltage and the room temperature.

#### Timing Requirements

The CODECs do not require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 64 kHz to 2048 kHz.

#### System Clock

The basic timing of the Codecs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128 kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range from 64 kHz to 2.048 MHz.

#### Bit Steal Control (HD44238P only)

For the bit steal period, the decoder output of  $\mu$ -law CODEC should be shifted as half-bit of steps. For the CODECs, the power down control pin provides this function. If the low state of PD pin is less than 6 frames (0.75 ms), the device is not deactivated and the decoder output corresponding to the frame of the rising and falling edge of the pin is shifted as half-bit. And, if the low state is longer than 1.0 ms, the device is deactivated.

**Pin/Function Descriptions**

| Pin       | No | Descriptions  |
|-----------|----|---|
| TX.CLOCK  | 9  | Any of 64 kHz to 2.048 MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks.   |
| RCV.CLOCK | 10 | These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the SYNC, TX.SYNC/RCV.SYNC respectively.   |
| TX.SYNC   | 11 | These TTL compatible pulse inputs (typ. 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK, TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the CLOCK, TX.CLOCK/RCV.CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.   |
| RCV.SYNC  | 12 |   |
| PCMOUT    | 15 | This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX.SYNC/RCV.SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 $\Omega$ pull-up per 8 Codexes is required.  |
| PCMIN     | 8  | This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK, RCV.CLOCK.  |
| AIN       | 1  | These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, amplifier with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10 k $\Omega$ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. $C_L$ should be less than 100 pF. |
| GA1       | 2  |   |
| GA2       | 3  |   |
| AOUT      | 5  | This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 ohms. $C_L$ should be less than 100 pF.  |
| $V_{DD}$  | 7  | These are power supply pins. $V_{DD}$ and $V_{SS}$ are positive and negative supply pins respectively (typ. +5 V, -5 V). Analog and digital ground pins are separate for minimizing crosstalk.  |
| $V_{SS}$  | 16 |   |
| AGND      | 4  |   |
| DGND      | 13 |   |
| PD        | 14 | When this TTL compatible input is held low, the chip is put into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.<br><br>This pin should be pulled-up to $V_{DD}$ to keep the device active or to control On/Off with strobes.<br><br>For the $\mu$ -law devices, this pin also provides the half-bit decoder shift for the bit-steal frame according to alternating the state of the input.   |

**Absolute Maximum Ratings**

| Item                         | Rating  |
|------------------------------|---|
| V <sub>DD</sub>              | -0.3 to +7 V  |
| V <sub>SS</sub>              | +0.3 to -7 V  |
| Storage Temperature          | -55°C to 125°C  |
| Power Dissipation            | 0.5 W   |
| Digital Input/Output Voltage | -0.3 V < V <sub>IN</sub> < V <sub>DD</sub> + 0.3                  |
| Analog Input/Output Voltage  | V <sub>SS</sub> - 0.3 V < V <sub>IN</sub> < V <sub>DD</sub> + 0.3 |

**Electrical Characteristics**

Static Characteristics (V<sub>DD</sub> = 5 ± 0.25 V, V<sub>SS</sub> = -5 ± 0.25 V, V<sub>CC</sub> = 5 ± 0.25 V, T<sub>a</sub> = 0 to 70°C)

| Sym.               | Pin No.                 | Descriptions                     | Min                  | Typ  | Max  | Unit | Note/Conditions   |
|--------------------|-------------------------|----------------------------------|----------------------|------|------|------|---|
| I <sub>DD</sub>    | 7                       | V <sub>DD</sub> Current (OPE.)   |                      | 5.5  | 10   | mA   | Note 1  |
| I <sub>SS</sub>    | 16                      | V <sub>SS</sub> Current (OPE.)   | -10                  | -4.5 |      |      | A <sub>IN</sub> = 0 V   |
| I <sub>DDST</sub>  | 7                       | V <sub>DD</sub> Current (St.By.) |                      | 0.3  | 1    |      | PCMIN = +0 CODE   |
| I <sub>SSST</sub>  | 16                      | V <sub>SS</sub> Current (St.By.) | -0.2                 |      |      |      | R <sub>L</sub> (GA2) = 10 kΩ<br>R <sub>L</sub> (AOUT) = 600 Ω |
| I <sub>L</sub>     | 1, 2, 8,<br>9, 10, 14   | Leak Current                     | -10.0                |      | 10.0 | μA   | V <sub>M</sub> = 0.8 V  |
|                    |                         |                                  | -10.0                |      | 10.0 | μA   | V <sub>M</sub> = 2.0 V  |
|                    |                         |                                  |                      |      | 10.0 | μA   | V <sub>DD</sub> = V <sub>M</sub> = 5.25 V                     |
| I <sub>PL</sub>    | 11, 12                  | Pull Up Current                  | -100                 |      | 0    | μA   |   |
| I <sub>DL</sub>    | 15                      | Leak Current                     |                      |      | 10.0 | μA   | V <sub>DD</sub> = V <sub>M</sub> = 5.25 V                     |
| C <sub>AIN2</sub>  | 1, 2                    | Analog Input Cap.                |                      |      | 10   | pF   | at 1 MHz V <sub>bias</sub> = 0                                |
| C <sub>DIN</sub>   | 8, 9, 10,<br>11, 12, 14 | Input Capacitance                |                      |      | 10   | pF   | at 1 MHz V <sub>bias</sub> = 0                                |
| R <sub>OUTA</sub>  | 5                       | AOUT Resistance                  |                      | 1    | 10   | Ω    |   |
| R <sub>OUTG</sub>  | 3                       | GA2 Resistance                   |                      |      | 30   | Ω    | Note 1  |
| V <sub>GSW</sub>   | 3                       | GA2 Output Swing                 | -3.0                 |      | 3.0  | V    | R <sub>L</sub> = 10 kΩ  |
| V <sub>OFFIN</sub> | 1                       | Analog Offset Input              | -500                 |      | 500  | mV   | Note 1  |
| V <sub>OFFG</sub>  | 3                       | GA2 Offset Output                | -50                  |      | 50   | mV   | Note 1  |
| V <sub>OFFA</sub>  | 5                       | AOUT Offset Output               | -50                  |      | 50   | mV   | PCMIN = +0 - Code   |
| C <sub>DOUT</sub>  | 15                      | PCMOUT Capacitance               |                      |      | 15.0 | pF   | at 1 MHz V <sub>bias</sub> = 0 V                              |
| V <sub>OL</sub>    | 15                      | PCMOUT Low Voltage               |                      |      | 0.4  | V    | R <sub>L</sub> = 500 Ω<br>+I <sub>OL</sub> = 0.8 mA           |
| V <sub>OH</sub>    | 15                      | PCMOUT High Voltage              | V <sub>CC</sub> -0.3 |      |      | V    | I <sub>OH</sub> = -150 μA                                     |
| V <sub>IH</sub>    | 8, 10, 11,<br>9, 12, 14 | Digital Input High Voltage       | 2.0                  |      |      | V    |   |
| V <sub>IL</sub>    | 8, 10, 11,<br>9, 12, 14 | Digital Input Low Voltage        |                      |      | 0.8  | V    |   |

Note 1) Analog Input Amplifier Gain = 0 dB (Ga1 is connected to GA2)

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Dynamic-Characteristics ( $V_{DD} = 5 \pm 0.25$  V,  $V_{SS} = -5 \pm 0.25$  V,  $V_{CC} = 5 \pm 0.25$  V,  $T_a = 0$  to  $+70^\circ\text{C}$ )

| Sym.             | Descriptions                 | Min | Typ | Max  | Unit | Note         |
|------------------|------------------------------|-----|-----|------|------|--------------|
| FS               | Synchronization Rate         |     | 8   |      | kHz  |              |
| FC               | PCM Bit Clock Rate           | 64  |     | 2048 | kHz  |              |
| t <sub>wc</sub>  | Clock Pulse Width            | 200 |     |      | ns   |              |
| t <sub>wsh</sub> | SYNC Pulse High Width        | 200 |     |      | ns   |              |
| t <sub>wsl</sub> | SYNC Pulse Low Width         | 8   |     |      | μs   |              |
| t <sub>r</sub>   | Logic Input Rise Time        | 5   |     | 50   | ns   |              |
| t <sub>f</sub>   | Logic Input Fall Time        | 5   |     | 50   | ns   |              |
| t <sub>bcs</sub> | Previous Clock To SYNC Delay | 40  |     |      | ns   | Note 1       |
| t <sub>cs</sub>  | Clock To SYNC Delay          |     |     | 100  | ns   | Note 1, 3    |
| t <sub>cd1</sub> | Clock To PCM MSB Delay       |     |     | 170  | ns   | Note 1, 2, 4 |
| t <sub>sd</sub>  | SYNC To PCM MSB Delay        |     |     | 170  | ns   | Note 1, 2, 4 |
| t <sub>cd</sub>  | Clock To PCMOUT Delay        |     |     | 180  | ns   | Note 1, 2, 5 |
| t <sub>su</sub>  | PCMIN Setup Time             | 65  |     |      | ns   | Note 1       |
| t <sub>hd</sub>  | PCMIN Hold Time              | 120 |     |      | ns   | Note 1       |
| t <sub>bs</sub>  | PD (bit-steal) Setup         | 200 |     |      | ns   | Note 1, 6    |
| t <sub>bh</sub>  | PD (bit-steal) Hold          | 200 |     |      | ns   | Note 1, 6    |

- Notes
- 1) t<sub>r</sub>, t<sub>f</sub> of digital input or clock is assumed 5ns for timing measurement.
  - 2) PCMOUT Load Condition: 500 Ω+165 pF+ two LS-TTL Equivalent (I<sub>IL</sub> = 0.8 mA, I<sub>IH</sub> = -150 μA) Threshold Level (V<sub>OH</sub> = 2.4 V, V<sub>OL</sub> = 0.4 V)
  - 3) Positive value shows SYNC delay from CLOCK.
  - 4) t<sub>cd1</sub>, t<sub>sd</sub> are specified by CLOCK or SYNC which has slower rise time.
  - 5) t<sub>cd</sub> specification is valid for the data except MSB.
  - 6) Applicable HD44238P

System Related Characteristics ( $V_{DD} = 5 \pm 0.25$  V,  $V_{SS} = -5 \pm 0.25$  V,  $V_{CC} = 5 \pm 0.25$  V,  $T_a = 0$  to  $+70^\circ\text{C}$ , Input Amplifier Gain = 0 dB, GA2 Load = 10 kΩ, Aout Load = 600 Ω, Synchronous operation. f<sub>c</sub> (PCM Bit Clock) = 2048 kHz)

For HD44237P

| Sym. | Descriptions                | Test Conditions | Min       | Typ | Max | Unit | Note  |
|------|-----------------------------|-----------------|-----------|-----|-----|------|-------|
| SDA  | Signal to Dist.<br>(A to A) | 820 Hz tone     | -45 dBm0  | 25  |     | dB   | p-wgt |
|      |                             |                 | -40       | 30  |     | dB   |       |
|      |                             |                 | -30 to +3 | 35  |     | dB   |       |
| SNA  | Signal to Dist.<br>(A to A) | Noise           | -55 dBm0  | 14  |     | dB   |       |
|      |                             |                 | -40       | 29  |     | dB   |       |
|      |                             |                 | -34       | 34  |     | dB   |       |
|      |                             |                 | -27 to -6 | 36  |     | dB   |       |
|      |                             |                 | -3        | 28  |     | dB   |       |
| SDX  | Signal to Dist.<br>(A to D) | 820 Hz tone     | -45 dBm0  | 26  |     | dB   | p-wgt |
|      |                             |                 | -40       | 31  |     | dB   |       |
|      |                             |                 | -30 to +3 | 36  |     | dB   |       |
| SNX  | Signal to Dist. (A to D)    | Noise           | -55 dBm0  | 15  |     | dB   |       |
|      |                             |                 | -40       | 30  |     | dB   |       |
|      |                             |                 | -34       | 35  |     | dB   |       |
|      |                             |                 | -27 to -6 | 37  |     | dB   |       |
|      |                             |                 | -3        | 28  |     | dB   |       |
| SDR  | Signal to Dist. (D to A)    | 820 Hz tone     | -45 dBm0  | 26  |     | dB   | p-wgt |
|      |                             |                 | -40       | 31  |     | dB   |       |
|      |                             |                 | -30 to +3 | 36  |     | dB   |       |

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| Sym. | Descriptions                     | Test Conditions                        | Min                | Typ   | Max   | Unit  | Note  |
|------|----------------------------------|--|--------------------|-------|-------|-------|-------|
| SNR  | Signal to Dist<br>(D to A)       | Noise                                  | -55 dBm0           | 15    |       |       | dB    |
|      |                                  |  | -40                | 30    |       |       |       |
|      |                                  |  | -34                | 35    |       |       |       |
|      |                                  |  | -27 to -6          | 37    |       |       |       |
| GTA  | Gain Track (A to A)              | 820 Hz tone<br>Relative to<br>-10 dBm0 | -55 to -50 dBm0    | -1.0  | 1.0   |       | dB    |
|      |                                  |  | -50 to -40         | -0.5  | 0.5   |       |       |
|      |                                  |  | -40 to +3          | -0.3  | 0.3   |       |       |
| GNA  | Gain Track (A to A)              | Noise<br>Relative to<br>-10 dBm0       | -60 to -55 dBm0    | -0.8  | 0.8   |       | dB    |
|      |                                  |  | -55 to -10         | -0.4  | 0.4   |       |       |
|      |                                  |  |                    |       |       |       |       |
| GTX  | Gain Track (A to D)              | 820 Hz tone<br>Relative to<br>-10 dBm0 | -55 to -50         | -0.8  | 0.8   |       | dB    |
|      |                                  |  | -50 to -40         | -0.4  | 0.4   |       |       |
|      |                                  |  | -40 to +3 dBm0     | -0.2  | 0.2   |       |       |
| GNX  | Gain Track (A to D)              | Noise<br>Relative to<br>-10 dBm0       | -60 to -55 dBm0    | -0.6  | 0.6   |       | dB    |
|      |                                  |  | -55 to -40         | -0.4  | 0.4   |       |       |
|      |                                  |  | -40 to -10         | -0.2  | 0.2   |       |       |
| GTR  | Gain Track (D to A)              | 820 Hz tone<br>Relative to<br>-10 dBm0 | -55 to -50         | -0.8  | 0.8   |       | dB    |
|      |                                  |  | -50 to -40         | -0.4  | 0.4   |       |       |
|      |                                  |  | -40 to +3 dBm0     | -0.2  | 0.2   |       |       |
| GNR  | Gain Track (D to A)              | Noise<br>Relative to<br>-10 dBm0       | -60 to -55 dBm0    | -0.4  | 0.4   |       | dB    |
|      |                                  |  | -55 to -10         | -0.2  | 0.2   |       |       |
|      |                                  |  |                    |       |       |       |       |
| FRX  | Freq.Response<br>(A to D) (Loss) | Relative to<br>820 Hz<br>0 dBm0        | 0.06 kHz           | 24    |       |       | dB    |
|      |                                  |  | 0.2                | 0     | 2.0   |       |       |
|      |                                  |  | 0.3 to 3           | -0.15 | 0.15  |       |       |
|      |                                  |  | 3.18               | -0.15 | 0.65  |       |       |
|      |                                  |  | 3.4                | 0     | 0.8   |       |       |
| FRR  | Freq.Response<br>(D to A) (Loss) | Relative to<br>820 Hz<br>0 dBm0        | 0 to 3 kHz         | -0.15 | 0.15  |       | dB    |
|      |                                  |  | 3.18               | -0.15 | 0.65  |       |       |
|      |                                  |  | 3.4                | 0     | 0.8   |       |       |
|      |                                  |  | 3.78               | 6.5   |       |       |       |
|      |                                  |  |                    |       |       |       |       |
| AIL  | Analog Input Level               | 820 Hz<br>0 dBm0                       | 25°C nom.P.S.      | 1.217 | 1.231 | 1.246 | Vrms  |
| AOL  | Analog Output Level              | 820 Hz<br>0 dBm0                       | 25°C nom.P.S.      | 1.217 | 1.231 | 1.246 | Vrms  |
| ICNA | Idle Ch. Noise                   | A to A                                 | AIN = AGND         |       |       | -78   | dBmOP |
| ICNX | Idle Ch. Noise                   | A to D                                 | AIN = AGND         |       |       | -80   | dBmOP |
| ICNR | Idle Ch. Noise                   | D to A                                 | PCMIN =<br>+0-CODE |       |       | -80   | dBmOP |
| XTKA | AIN to AOUT<br>Crosstalk         | 820 Hz                                 | 0 dBm0             |       |       | -65   | dB    |
| XTKD | PCMIN to PCMOUT                  | 820 Hz                                 | 0 dBm0             |       |       | -65   | dB    |

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For HD44238P

| Sym  | Pin No.                          | Descriptions      | Min                | Typ   | Max   | Unit  | Note  |
|------|----------------------------------|-------------------|--------------------|-------|-------|-------|-------|
| SDA  | Signal to Dist.<br>(A to A)      | 1020 Hz tone      | -45 dBm0           | 25    |       | dB    | c-wgt |
|      |                                  |                   | -40                | 30    |       | dB    |       |
|      |                                  |                   | -30 to +3          | 35    |       | dB    |       |
| SDX  | Signal to Dist.<br>(A to D)      | 1020Hz tone       | -45 dBm0           | 26    |       | dB    | c-wgt |
|      |                                  |                   | -40                | 31    |       | dB    |       |
|      |                                  |                   | -30 to +3          | 36    |       | dB    |       |
| SDR  | Signal to Dist.<br>(D to A)      | 1020 Hz tone      | -45 dBm0           | 26    |       | dB    | c-wgt |
|      |                                  |                   | -40                | 31    |       | dB    |       |
|      |                                  |                   | -30 to +3          | 36    |       | dB    |       |
| GTA  | Gain Tracking<br>(A to A)        | 1020 Hz tone      | -55 to -50 dBm0    | -1.0  | 1.0   | dB    |       |
|      |                                  | Relative to       | -50 to -40         | -0.5  | 0.5   | dB    |       |
|      |                                  | 10 dBm0           | -40 to +3          | -0.3  | 0.3   | dB    |       |
| GTX  | Gain Tracking<br>(A to D)        | 1020 Hz tone      | -55 to -50         | -0.8  | 0.8   | dB    |       |
|      |                                  | Relative to       | -50 to -40         | -0.4  | 0.4   | dB    |       |
|      |                                  | -10 dBm0          | -40 to +3 dBm0     | -0.2  | 0.2   | dB    |       |
| GTR  | Gain Tracking<br>(D to A)        | 1020 Hz tone      | -55 to -50         | -0.8  | 0.8   | dB    |       |
|      |                                  | Relative to       | -50 to -40         | -0.4  | 0.4   | dB    |       |
|      |                                  | -10 dBm0          | -40 to +3 dBm0     | -0.2  | 0.2   | dB    |       |
| FRX  | Freq.Response<br>(A to D) (Loss) | Relative to       | 0.06 kHz           | 24    |       | dB    |       |
|      |                                  | 1020 Hz           | 0.2                | 0     | 2.0   | dB    |       |
|      |                                  | 0 dBm0            | 0.3 to 3           | -0.15 | 0.15  | dB    |       |
|      |                                  |                   | 3.18               | -0.15 | 0.65  | dB    |       |
|      |                                  |                   | 3.4                | 0     | 0.8   | dB    |       |
| FRR  | Freq.Response<br>(D to A) (Loss) | Relative to       | 0 to 3 kHz         | -0.15 | 0.15  | dB    |       |
|      |                                  | 1020 Hz           | 3.18               | -0.15 | 0.65  | dB    |       |
|      |                                  | 0 dBm0            | 3.4                | 0     | 0.8   | dB    |       |
|      |                                  |                   | 3.78               | 6.5   |       | dB    |       |
| AIL  | Analog Input<br>Level            | 1020 Hz<br>0 dBm0 | 25°C nom. P.S.     | 1.213 | 1.227 | 1.241 | Vrms  |
| AOL  | Analog Output<br>Level           | 1020 Hz<br>0 dBm0 | 25°C nom. P.S.     | 1.213 | 1.227 | 1.241 | Vrms  |
| ICNA | Idle Ch. Noise                   | A to A            | AIN = AGND         |       |       | 16    | dBmCO |
| ICNX | Idle Ch. Noise                   | A to D            | AIN = AGND         |       |       | 16    | dBmCO |
| ICNR | Idle Ch. Noise                   | D to A            | PCMIN =<br>+0-Code |       |       | 10    | dBmCO |
| XTKA | AIN to AOUT<br>Crosstalk         | 1020Hz 0 dBm0     |                    |       |       | -65   | dB    |
| XTKD | PCMIN to<br>PCMOUT               | 1020 Hz 0 dBm0    |                    |       |       | -65   | dB    |

HITACHI

For HD44237P, HD44238P

| Sym. | Descriptions                   | Test Conditions                                     |  | Min        | Typ    | Max  | Unit               | Note    |
|------|--------------------------------|---|--|------------|--------|------|--------------------|---------|
| AT   | AIL, AOL Variation with temp.  | Relative to 25°C nominal P.S.                       |  |            | ±20    |      | ppm/°C             |         |
| AP   | AIL, AOL Variation with P.S.   | 25°C, Supplies ± 5%                                 |  |            | ± 0.01 |      | dB                 |         |
| ALS  | GAIN Variation over Temp. P.S. | A to D<br>D to A                                    | Initial  | -0.2       |        | -0.2 | dB                 | Note 1) |
| AIP  | Peak Analog Input              |   |  | 3.0        |        |      | V                  |         |
| AOP  | Peak Analog Output             |   |  | 2.5        |        |      | V                  |         |
| PDL  | Propagation Delay              | A to A  | 0 dBmO   |            | 450    | 480  | µs                 |         |
| DD   | Delay Distortion               | A to A  | 0.5 to   |            |        | 1.4  | ms                 |         |
|      |                                |   | 0 dBmO   | 0.6 kHz    |        |      |                    |         |
|      |                                |   |  | 0.6 to 1.0 |        | 0.7  | rel. to min. delay |         |
|      |                                |   |  | 1.0 to 2.6 |        | 0.2  |                    |         |
|      |                                |   | 2.6 to 2.8   |            | 1.4    |      |                    |         |
| PSRR | PSRR                           | A to A<br>AIN =<br>AGND<br>0.3 –<br>50 kHz          | V <sub>DD</sub> Mod. =<br>+5 V + 100 mVop<br>V <sub>SS</sub> Mod. =<br>-5 V + 100 mVop | 30         |        |      | dB                 |         |
| IM1  | Intermodulation                | A to A(2a-b)<br>a; 0.47 kHz, -4 dBmO<br>b; 0.32, -4 |  |            |        | -38  | dB                 |         |
| IM2  | Intermodulation                | A to A(a-b)<br>a; 1.02 kHz, -4 dBmO<br>b; 0.05, -23 |  |            |        | -52  | dB                 |         |
| ICS  | Single Freq.Noise              | A to A<br>AIN =<br>AGND                             | 8,16,24,<br>32,40 kHz  |            |        | -50  | dBmO               |         |
| DIS  | Discrimination                 | A to A  | 4.6 to<br>0 dBmO 200 kHz   | 30         |        |      | dB                 |         |

Note 1) Total variation of GAIN including the initial fluctuation temperature variation and power supply dependence (0 to +70°C, V<sub>DD</sub>/V<sub>SS</sub> = ± 5 V ± 5%)

Timing Chart

