HD44790, HD44795 (LCD-III)

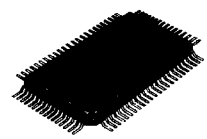
4-Bit CMOS Microcomputer

AUTOMOTIVE VERSION

The LCD-III is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-III is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-III provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.

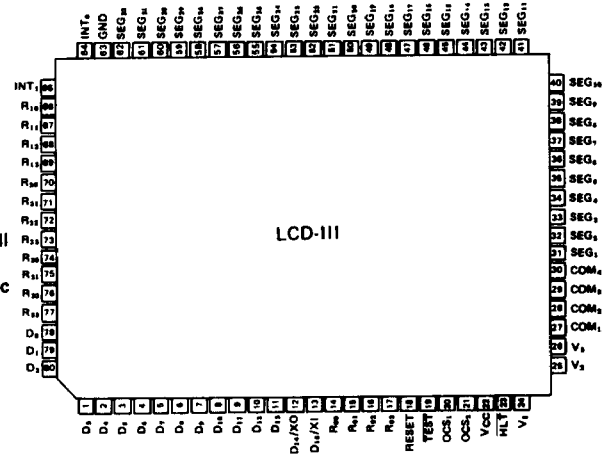
- **FEATURES**
- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
  128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
  4 Commons (Duty Radio; Static, 1/2, 1/3, 1/4)
  32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100s)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  – Table Look Up Capability –
- Powerful Interrupt Function
  3 Interrupt Sources
  ├ 2 External Interrupt Lines
  └ Timer/Event Counter
  Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Built-in Power-on Reset Circuit
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50μW max.
- 2 Versions; HD44790 V_{CC} = 5V ± 10%, 10μs Instruction Cycle Time
  HD44795 V_{CC} = 2.7V to 5.5V, 20 μs Instruction Cycle Time

LCD-III



(FP-80)

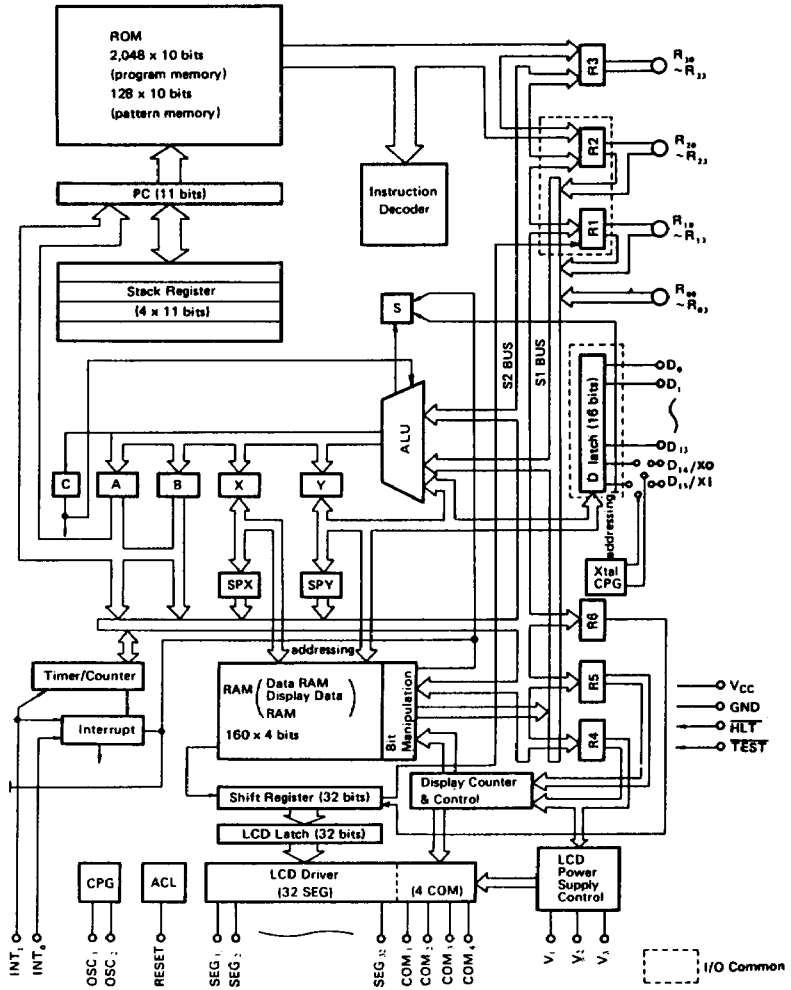
- **PIN ARRANGEMENT**



(Top View)

Data Sheets contain information for automotive operation only. Refer to **Reference Guide** (Section 9) for a listing of supplementary publications which provide complete specifications.

■ BLOCK DIAGRAM



■ HD44790 ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage (1)	V_{T1}	-0.3 to V_{CC}+0.3	V	Applied to all pins except those specified in V_{T2}.
Pin Voltage (2)	V_{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	–40 to +85	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded.
Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$ should be maintained.

• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 5V±10%, T_a = –40 to +85°C)

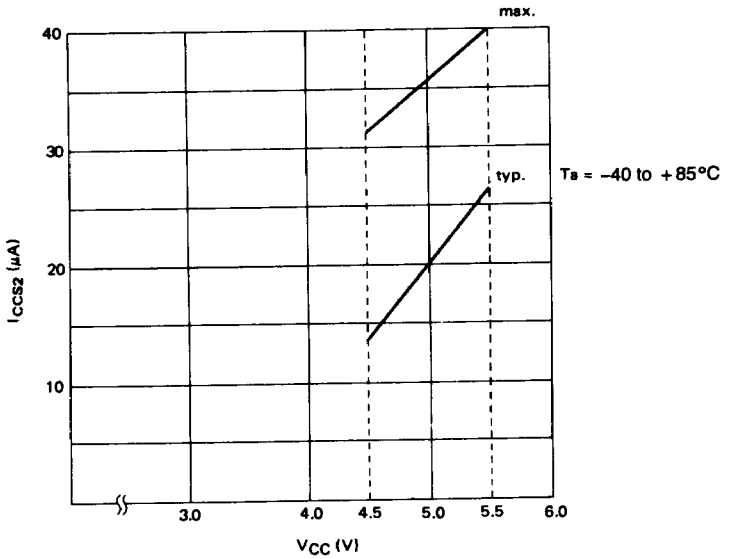
Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	1.0	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}-1.0	–	V_{CC}	V	(9)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	–	10	V	(10)
Output "Low" Voltage	V_{OL}	I_{OL} = 1.6 mA	–	–	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 1.0 mA	2.4	–	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	(2)
Driver Voltage Descending (COM)	V_{d_1}	Id = 0.05 mA	–	–	0.4	V	(13)
Driver Voltage Descending (SEG)	V_{d_2}	Id = 0.01 mA	–	–	0.4	V	(13)
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	kΩ	
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	–	μs	(15)
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	(15)
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	(15)
Output "High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	(3), (9)
		V_{in} = 0 to 10V	–	–	3		(3), (10)
Pull up MOS Current	$-I_P$	V_{CC} = 5V	45	–	250	μA	
Supply Current (1)	I_{CC1}	V_{in} = V_{CC}, V_{CC} = 5V, Ceramic Filter Oscillation (f_{osc} = 400 kHz)	–	–	1.3	mA	(5)
Supply Current (2)	I_{CC2}	V_{in} = V_{CC}, V_{CC} = 5V R_f Oscillation (f_{osc} = 400 kHz) External Clock Operation (f_{cp} = 400 kHz)	–	–	0.6	mA	(5), (12)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 1.0V, V_{in} = 0 to V_{CC}	–	–	1.0	μA	(6), (9)
		$\overline{HLT}$ = 1.0V, V_{in} = 0 to 10V	–	–	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	10	μA	(11)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.2V	–	–	40	μA	(7)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$			Hz	
LCD Display Voltage	V_{LCD}	V_{CC}–V_3	2.5	–	V_{CC}	V	(8)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		40	400	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	9.1	10	100	μs	
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	R_f = 110kΩ±2%	300	–	500	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	8.0	–	13.3	μs	
Internal Clock Operation (Ceramic Filter Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	392	–	408	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	9.8	–	10.2	μs	
Internal Clock Operation (Crystal Oscillation); Clock for Timer							
Clock Oscillation Frequency	f_{oscx}	Crystal	32.768			kHz	

- **ELECTRICAL CHARACTERISTICS – 2** (T_a = -40 to +85°C)

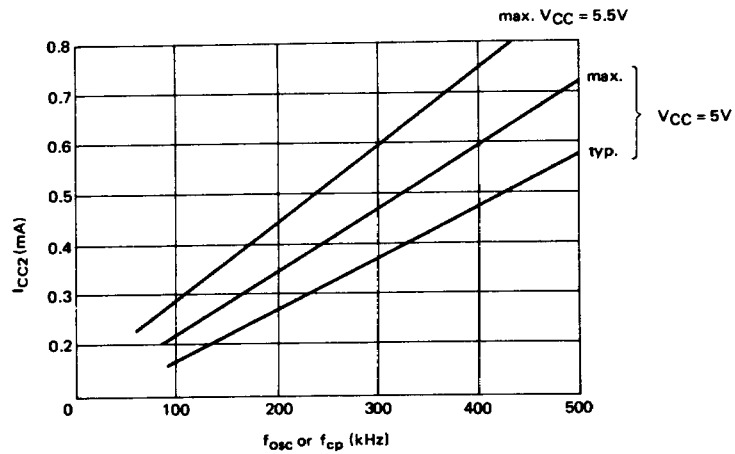
Item	Symbol	Test Conditions	Value min	Value max	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V	
Halt Current	I_{DH}	$V_{in} = V_{CC}$, $\overline{HLT}$ = 0.2V, V_{DH} = 2.3V	–	4.0	μA	(14)
Halt Delay Time	t_{HD}		100	–	μs	
Operation Recovery Time	t_{RC}		100	–	μs	
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	100	–	μs	
		Ceramic Filter Oscillation	4000	–		
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT} = V_{CC}$	0.1	10	ms	
Power Supply OFF Time	t_{OFF}	Built-in Reset, $\overline{HLT} = V_{CC}$	1	–	ms	
RESET Pulse Width (1)	t_{RST1}	External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (R_f Oscillation, External Clock Operation)	1	–	ms	
		External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (Ceramic Filter Oscillation)	4	–		
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = System Clock)	$2 \cdot T_{inst}$	–	μs	
		External Reset, V_{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = Crystal Clock)	$32 \times 10^6 / f_{oscx}$	–		
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 4.5 to 5.5V	–	100	μs	
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 4.5 to 5.5V	–	100	μs	

(NOTE)
1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
   Test Conditions: RESET, $\overline{HLT}$, $\overline{TEST} = V_{CC}$ (Reset State)
   INT_0, INT_1, R_{00} to R_{33}, D_0 to $D_{13} = V_{CC}$
   D_{14}/XO, D_{15}/XI — D_{14}/XO, $D_{15}/XI = V_{CC}$ (Crystal oscillation for timer is not selected).
   — D_{14}/XO = Open, $D_{15}/XI = V_{CC}$ (Crystal oscillation for timer is selected).
   V_1, V_2, $V_3 = V_{CC}$
   COM_1 to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC1} or I_{CC2}. When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 5V±10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).

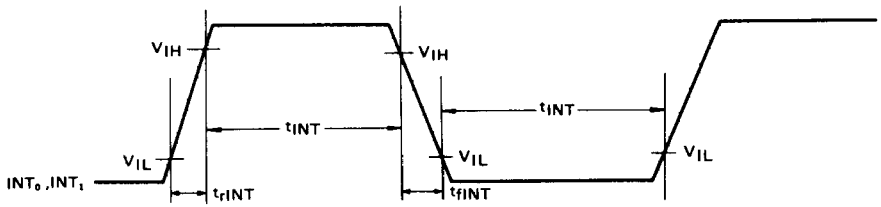


8. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
9. Applied to the following pins.
   (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R pins.
   (2) RESET, $\overline{HLT}$, OSC_1, INT_0 and INT_1
10. Applied to open-drain I/O common pins among D and R pins.
11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at V_{CC} = 5V±10% in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply pins (V_{CC}, V_1, V_2, V_3) and each common or segment output pin.
14. The supply current at V_{CC} = V_{DH} = 2.3V in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

15. Interrupt inputs must be retained for two or more cycles at both "High" and "Low" levels.



■ HD44795 ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V)

• ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage (1)	V_{T1}	-0.3 to V_{CC}+0.3	V	Applied to all pins except those specified in V_{T2}.
Pin Voltage (2)	V_{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{o1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{o2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	-40 to +85°C	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded.
Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$ should be maintained.

4

• ELECTRICAL CHARACTERISTICS – 1 (V_{CC} = 2.7 to 5.5V, T_a = -40 to +85°C)

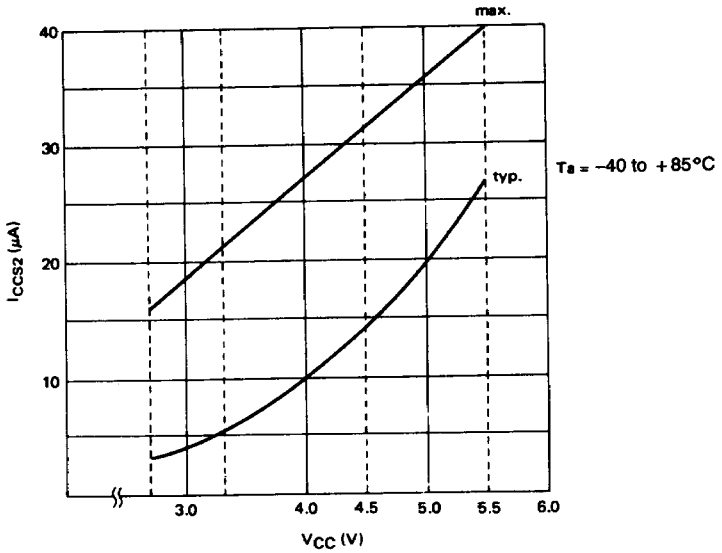
Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage	V_{IL}		–	–	0.4	V	
Input "High" Voltage (1)	V_{IH1}		V_{CC}-0.4	–	V_{CC}	V	(9)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-0.4	–	10	V	(10)
Output "Low" Voltage	V_{OL}	I_{OL} = 0.4 mA	–	–	0.4	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH}$ = 0.08 mA	V_{CC}-0.4	–	–	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH}$ = 0.01 mA	V_{CC}-0.3	–	–	V	(2)
Driver Voltage Descending (COM)	V_{d_1}	Id = 0.05 mA	–	–	0.4	V	(13)
Driver Voltage Descending (SEG)	V_{d_2}	Id = 0.01 mA	–	–	0.4	V	(13)
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	kΩ	
Interrupt Input Hold Time	t_{INT}		2•T_{inst}	–	–	μs	(15)
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	(15)
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	(15)
Output " High" Current	I_{OH}	V_{OH} = 10V	–	–	3	μA	(3)
Input Leakage Current	I_{IL}	V_{in} = 0 to V_{CC}	–	–	1.0	μA	(3), (9)
		V_{in} = 0 to 10V	–	–	3		(3), (10)
Pull up MOS Current	$-I_P$	V_{CC} = 3V	15	–	80	μA	
Supply Current	I_{CC}	V_{in} = V_{CC}, V_{CC} = 3V R_f Oscillation (f_{osc} = 200 kHz) External Clock Operation (f_{cp} = 200 kHz)	–	–	0.15	mA	(5), (12)
Standby I/O Leakage Current	I_{LS}	$\overline{HLT}$ = 0.5V, V_{in} = 0 to V_{CC}	–	–	1.0	μA	(6), (9)
		$\overline{HLT}$ = 0.5V, V_{in} = 0 to 10V	–	–	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.1V V_{CC} = 2.7 to 3.3V	–	–	6	μA	(11)
Standby Supply Current (2)	I_{CCS2}	V_{in} = V_{CC}, $\overline{HLT}$ = 0.1V V_{CC} = 2.7 to 3.3V	–	–	21	μA	(7)
Frame Frequency of LCD Drive	f_F	n = 1 (static) n = 2 (1/2 Duty) n = 3 (1/3 Duty) n = 4 (1/4 Duty)	$\frac{1}{128 \times n \times T_{inst}}$			Hz	
LCD Display Voltage	V_{LCD}	V_{CC}-V_3	2.5	–	V_{CC}	V	(8)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		40	200	240	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{cp}	16.6	20	100	μs	
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	R_f = 200kΩ±2%, V_{CC} = 2.7 to 3.3V	150	–	250	kHz	
		R_f = 200kΩ±2%, V_{CC} = 2.7 to 5.5V	150	–	350		
Instruction Cycle Time	T_{inst}	T_{inst} = 4/f_{osc}, V_{CC} = 2.7 to 3.3V	16	–	26.6	μs	
		T_{inst} = 4/f_{osc}, V_{CC} = 2.7 to 5.5V	11.4	–	26.6		
Internal Clock Operation (Crystal Oscillation); Clock for Timer							
Clock Oscillation Frequency	f_{oscx}	Crystal	32.768			kHz	

• ELECTRICAL CHARACTERISTICS – 2 (T_a = -40 to +85°C)

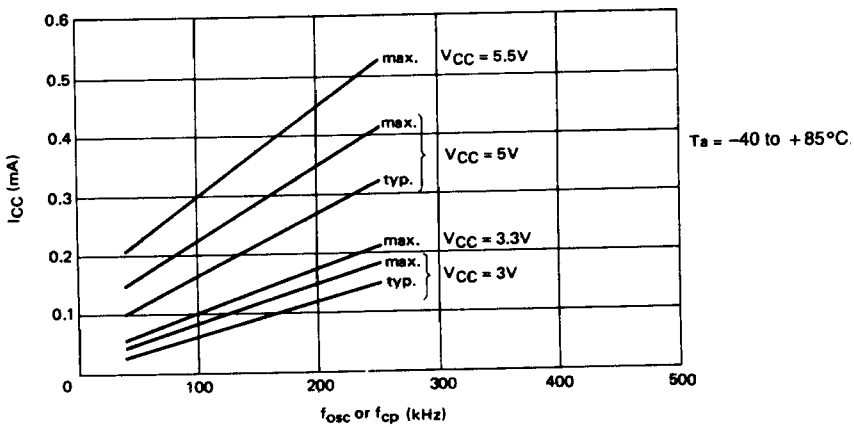
Item	Symbol	Test Conditions	Value min	Value max	Unit	Note
Halt Duration Voltage	V_{DH}	$\overline{HLT}$ = 0.2V	2.3	–	V	
Halt Current	I_{DH}	$V_{in} = V_{CC}$, $\overline{HLT}$ = 0.1V, V_{DH} = 2.3V	–	4.0	μA	(14)
Halt Delay Time	t_{HD}		100	–	μs	
Operation Recovery Time	t_{RC}		100	–	μs	
$\overline{HLT}$ Fall Time	t_{fHLT}		–	1000	μs	
$\overline{HLT}$ Rise Time	t_{rHLT}		–	1000	μs	
$\overline{HLT}$ "Low" Hold Time	t_{HLT}		400	–	μs	
$\overline{HLT}$ "High" Hold Time	t_{OPR}	R_f Oscillation, External Clock Operation	100	–	μs	
Power Supply Rise Time	t_{rCC}	Built-in Reset, $\overline{HLT} = V_{CC}$	0.1	10	ms	
Power Supply OFF Time	t_{OFF}	Built-in Reset, $\overline{HLT} = V_{CC}$	1	–	ms	
RESET Pulse Width (1)	t_{RST1}	External Reset, $\overline{HLT} = V_{CC}$	1	–	ms	
RESET Pulse Width (2)	t_{RST2}	External Reset, V_{CC} = 2.7 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = System Clock)	$2 \cdot T_{inst}$	–	μs	
		External Reset, V_{CC} = 2.7 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = Crystal Clock)	$32 \times 10^6 / f_{oscx}$	–		
RESET Rise Time	t_{rRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 2.7 to 5.5V	–	100	μs	
RESET Fall Time	t_{fRST}	External Reset, $\overline{HLT} = V_{CC}$, V_{CC} = 2.7 to 5.5V	–	100	μs	

(NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
4. Pull up MOS current is excluded.
5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).
   Test Conditions: RESET, $\overline{HLT}$, $\overline{TEST}$ = V_{CC} (Reset State)
   INT_0, INT_1, R_{00} to R_{33}, D_0 to D_{13} = V_{CC}
   D_{14}/XO, D_{15}/XI ┬ D_{14}/XO, D_{15}/XI = V_{CC} (Crystal oscillation for timer is not selected)
   D_{14}/XO, D_{15}/XI └ D_{14}/XO = Open, D_{15}/XI = V_{CC} (Crystal oscillation for timer is selected).
   V_1, V_2, V_3 = V_{CC}
   COM_1 to COM_4, SEG_1 to SEG_{32} = Open
   When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}.
   When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

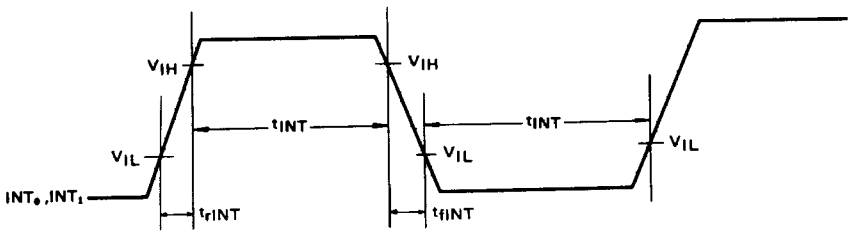
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 3V±10% in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).



8. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
9. Applied to the following pins.
   (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R pins.
   (2) RESET, $\overline{HLT}$, OSC_1, INT_0 and INT_1
10. Applied to open-drain I/O common pins among D and R pins.
11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at V_{CC} = 3V±10% in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply pins (V_{CC}, V_1, V_2, V_3) and each common or segment output pin.
14. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.
15. Interrupt inputs must be retained for two or more cycles at both "High" and "Low" levels.



■ SIGNAL DESCRIPTION

The input and output signals for the LCD-III shown in PIN ARRANGEMENT are described in the following paragraphs.

- **V_{CC} and GND**
  Power is supplied to the LCD-III using these two pins. V_{CC} is power and GND is the ground connection.

- **RESET**
  This pin resets the LCD-III independently of the automatic resetting capability (ACL; Built-in Reset Circuit) already in the LCD-III. The LCD-III can be reset by pulling RESET High.
  Refer to RESET FUNCTION for additional information.

- **OSC_1 and OSC_2**
  These pins provide control input for the on-chip clock oscillator circuit. A resistor, a ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.
  Refer to OSCILLATOR for recommendations about these pins.

- **$\overline{HLT}$**
  This pin is used to enter the LCD-III into the HALT state (Stand-by Mode). The LCD-III can be moved into the halt state by pulling $\overline{HLT}$ Low.
  In the halt state the internal clock stops and all the internal statuses (RAM, Registers, Carry, Status, Program Counter, etc.) are maintained. Consequently power consumption is greatly reduced. By pulling $\overline{HLT}$ high, the LCD-III starts operation from the status just before the halt state.
  Refer to HALT FUNCTION for details of halt mode.

- **$\overline{TEST}$**
  This pin is not for user application and must be connected to V_{CC}.

- **INT_0 and INT_1**
  These pins generate interrupt request to the LCD-III.
  Refer to INTERRUPT for additional information.

- **V_1, V_2 and V_3**

Power for liquid crystal display are supplied to the LCD-III using these pins ($V_{CC} \geqq V_1 \geqq V_2 \geqq V_3 \geqq GND$).

- **R_{00} to R_{03}**
  These four lines are a 4-bit input channel.
  Refer to INPUT/OUTPUT for additional information.

- **R_{10} to R_{13}, R_{20} to R_{23}**
  These 8 lines are arranged into two 4-bit Input/Output common channels. 4-bit registers (data I/O register) are attached to these channels. Each channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain, With Pull Up MOS, and CMOS using a mask option.
  Refer to INPUT/OUTPUT for additional information.

- **R_{30} to R_{33}**
  These four lines are a 4-bit output channel. 4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option.
  Refer to INPUT/OUTPUT for additional information.

- **D_0 to D_{13}**
  These are 14 discrete signals which can be configured as Input/Output lines.
  Refer to INPUT/OUTPUT for additional information.

- **D_{14}/XO, D_{15}/XI**
  D_{14}/XO and D_{15}/XI select in the following 3 types with a mask option.
  - Discrete I/O (common pin)
  - Crystal circuit connecting pins (with internal halt)
  - Crystal circuit connecting pins (no internal halt)

  Refer to INPUT/OUTPUT for additional information.

- **COM_1 to COM_4**
  These pins are common pins for liquid crystal display.
  Refer to LIQUID CRYSTAL DISPLAY for additional information.

- **SEG_1 to SEG_{32}**
  These are segment pins for liquid crystal display.

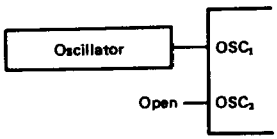
4

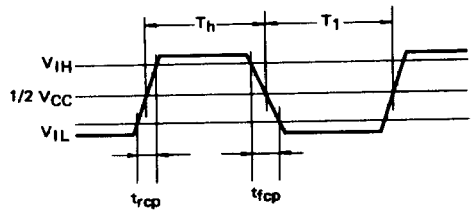
Refer to LIQUID CRYSTAL DISPLAY for additional information.

■ OSCILLATOR

A resistor, a ceramic filter circuit or an external oscillator can be connected to OSC_1 and OSC_2. However, a ceramic filter circuit cannot be used on the HD44795. The connection methods are shown in Figure 1.

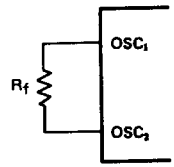
(1) External Clock



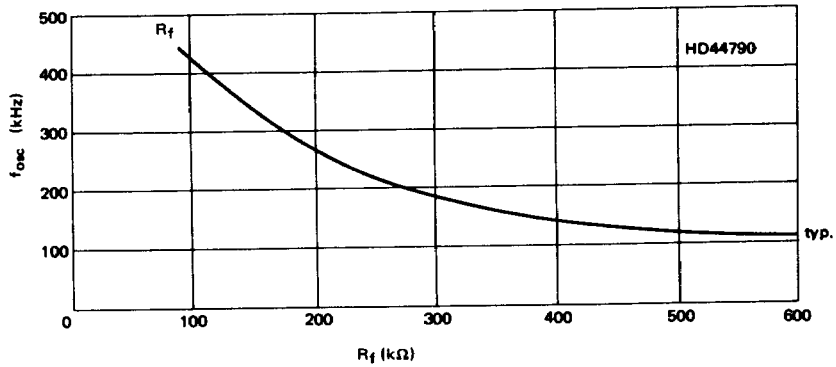


$$\text{Duty} = \frac{T_1}{T_h + T_1} \times 100\%$$

(2) Resistor



Length of the wirings for OSC_1 and OSC_2 pins should be minimized because the oscillation frequency varies depending on the capacitance of these pins.



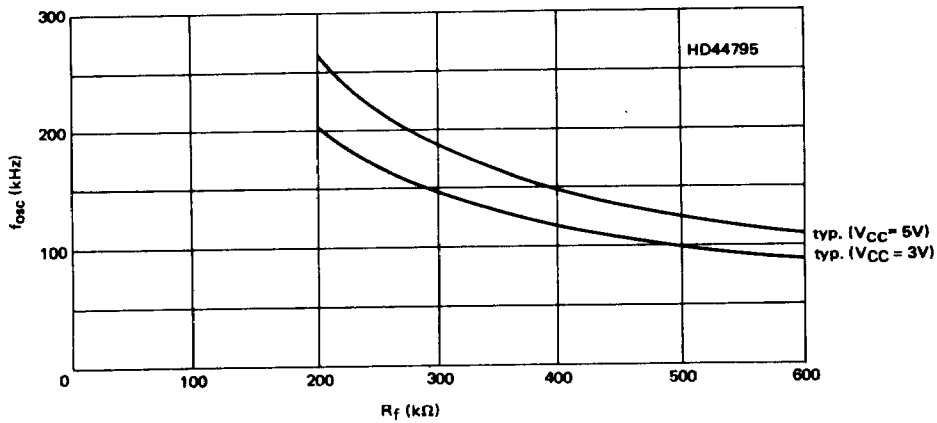


Figure 1 Connection Methods for Oscillator (to be continued)