HD61100A

(LCD Driver with 80-Channel Outputs)

HITACHI

Description

The HD61100A is a driver LSI for liquid crystal display systems. It receives serial display data from a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

It has liquid crystal driving outputs which correspond to internal 80-bit flip/flops. Both static drive and dynamic drive are possible according to the combination of transfer clock frequency and latch clock frequency.

Features

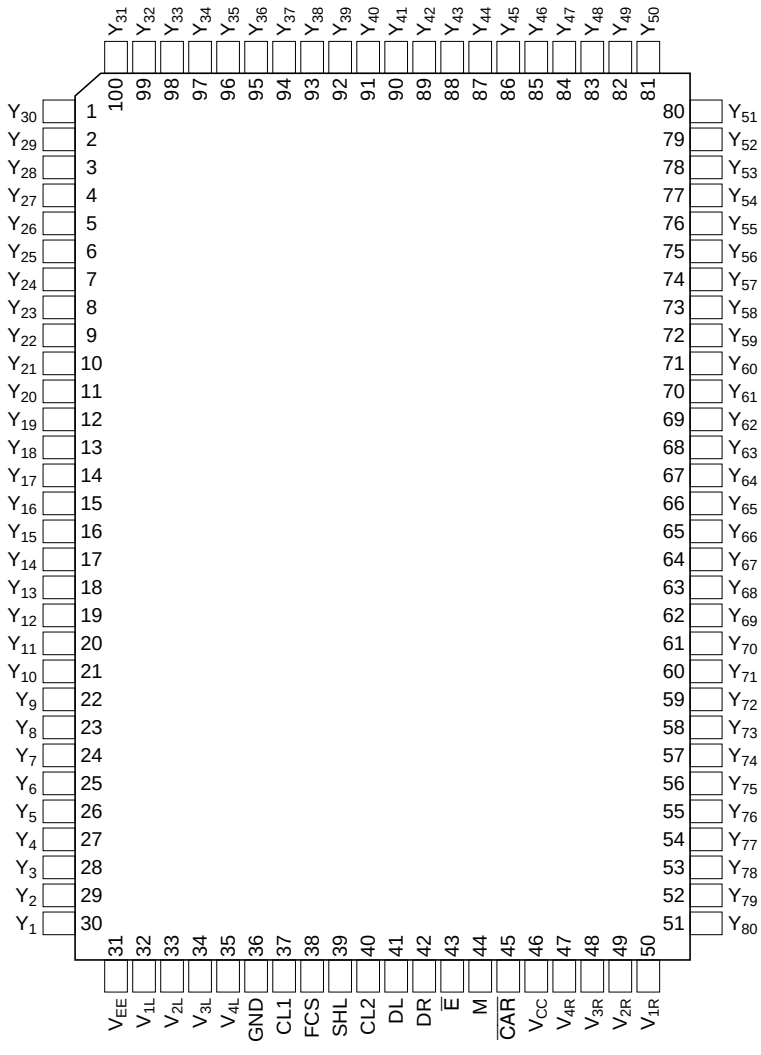
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Display duty cycle
  Any duty cycle is selectable according to combination of transfer clock and latch clock
- Data transfer rate: 2.5 MHz max.
- Power supply
  - — V_{CC}: +5.0 V ± 10% (internal logic)
  - — V_{CC}–V_{EE}: 5.5 to 17.0 V (liquid crystal display driver circuit)
- Liquid crystal driving level: 17.0 V max.
- CMOS process

Ordering Information

Type No.	Package
HD61100A	100-pin plastic QFP (FP-100)

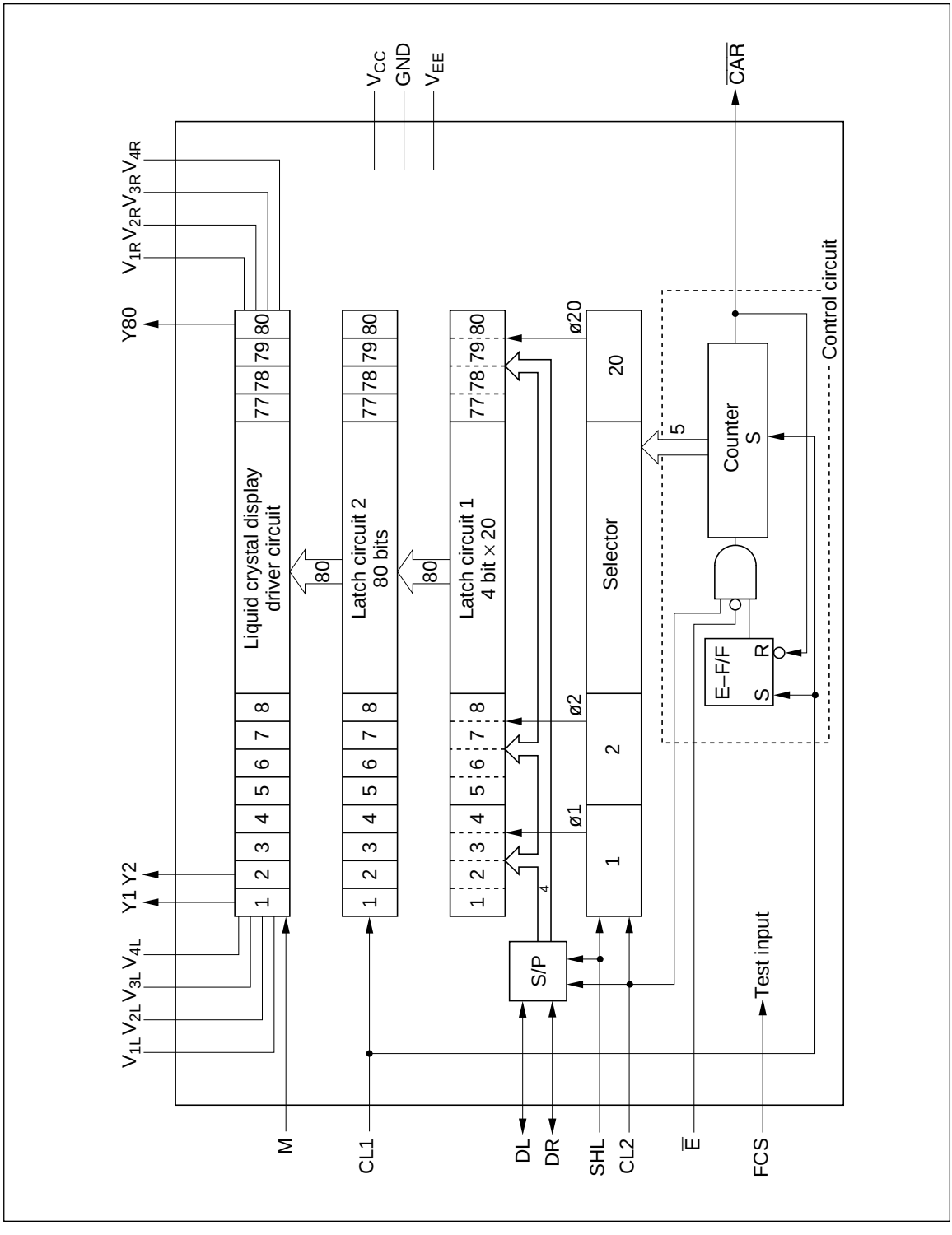
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

80-Bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is “L” level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don’t connect any lines to terminal DR which is in the output status.

When SHL is “H” level, input data from terminal DR without connecting any lines to terminal DL.

80-Bit Latch Circuit 1

The 4-bit data is latched at ø1 to ø20 and output to latch circuit 2. When SHL is “L” level, the data from DL are latched one in order of 1 → 2 → 3 → ... 80 of each latch. When SHL is “H” level, they are latched in a reverse order (80 → 79 → 78 → ... 1).

Selector

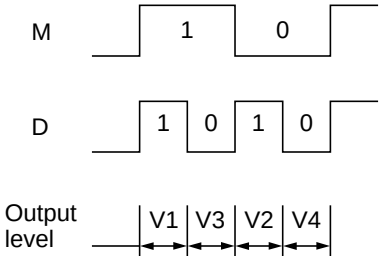
The selector decodes output signals from the counter and generates latch clock ø1 to ø20. When the LSI is not active, ø1 to ø20 are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E—F/F (enable F/F) indicates “1”, S/P conversion is started by inputting “L” level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into “L” level and E—F/F is reset to “0”, and consequently the conversion stops. E—F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at “H” level of CL1.

Counter consists of 7 bits, and the output signals of upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into “H” level at the rise of CL1 and the number of bit which can be S/P-converted increases by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61100A.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1–Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2, V3, and V4. Relation among output level, M and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Latch clock of display data (fall edge trigger). Liquid crystal driver signals corresponding to the display data are output synchronized with the fall of CL1.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge trigger.
DL, DR	2	I/O	Controller	Input of serial display data (D). **(D) / Liquid Crystal Driver Output / Liquid Crystal Display** 1 (high) / Selection level / On 0 (low) / Non-selection level / Off I/O status of DL and DR terminals depends on SHL input level. **SHL / DL / DR** High / O / I Low / I / O

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects a shift direction of serial data.

When the serial data (D) is input in order of D1 → ... → D80, the relations between the data (D) and output Y are as follows.

<table><tr><th>SHL</th><th>Y1</th><th>Y2</th><th>Y3</th><th>...</th><th>Y80</th></tr><tr><td>Low</td><td>D1</td><td>D2</td><td>D3</td><td>...</td><td>D80</td></tr><tr><td>High</td><td>D80</td><td>D79</td><td>D78</td><td>...</td><td>D1</td></tr></table>
When SHL is low, data is input from the terminal DL. No lines should be connected to the terminal DR, as it is in the output state.

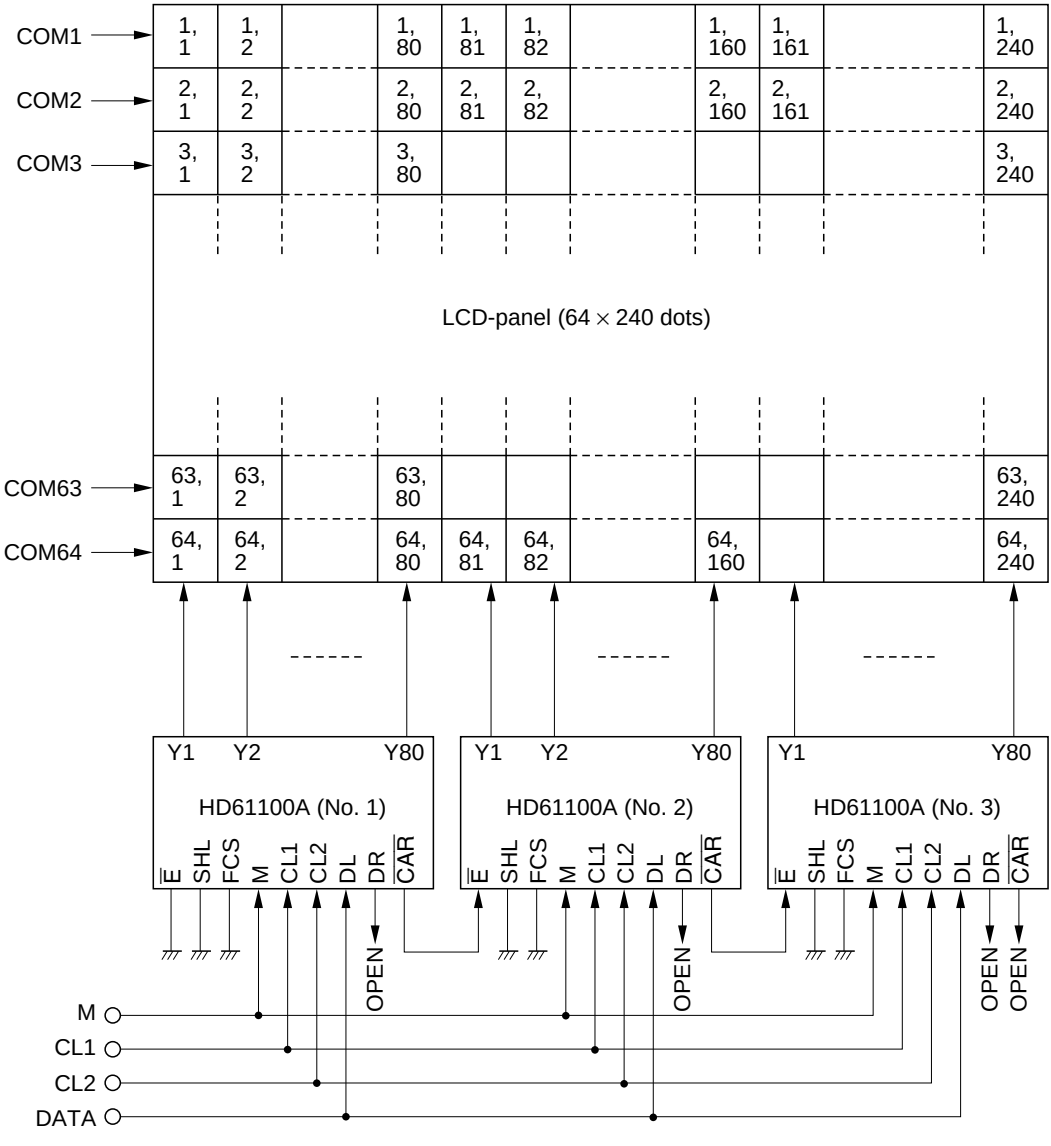
When SHL is high, the relation between DL and DR reverses.</td></tr>
<tr><td>$\overline{E}$</td><td>1</td><td>I</td><td>GND or the terminal $\overline{CAR}$ of the HD61100A</td><td>Controls the S/P conversion.

The operation stops when $\overline{E}$ is high, and the S/P conversion starts when $\overline{E}$ is low.</td></tr>
<tr><td>$\overline{CAR}$</td><td>1</td><td>O</td><td>Input terminal $\overline{E}$ of the HD61100A</td><td>Used for cascade connection with the HD61100A to increase the number of bits which can be S/P converted.</td></tr>
<tr><td>FCS</td><td>1</td><td>I</td><td>GND</td><td>Input terminal for test.

Connect to GND.</td></tr>
</table>

Operation of the HD61100A

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61100A's. Figure 2 is a time chart of HD61100A I/O signals.



Cascade three HD61100As. Input data to the terminal DL of No. 1, No. 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61103A. (m, n) in LCD panel is the address corresponding to each dot. Timing chart for the example of connection, DL input (m, n) in this figure is the data that corresponds to each address (m, n) of LCD panel.

Figure 1 LCD Driver with 64 × 240 Dots

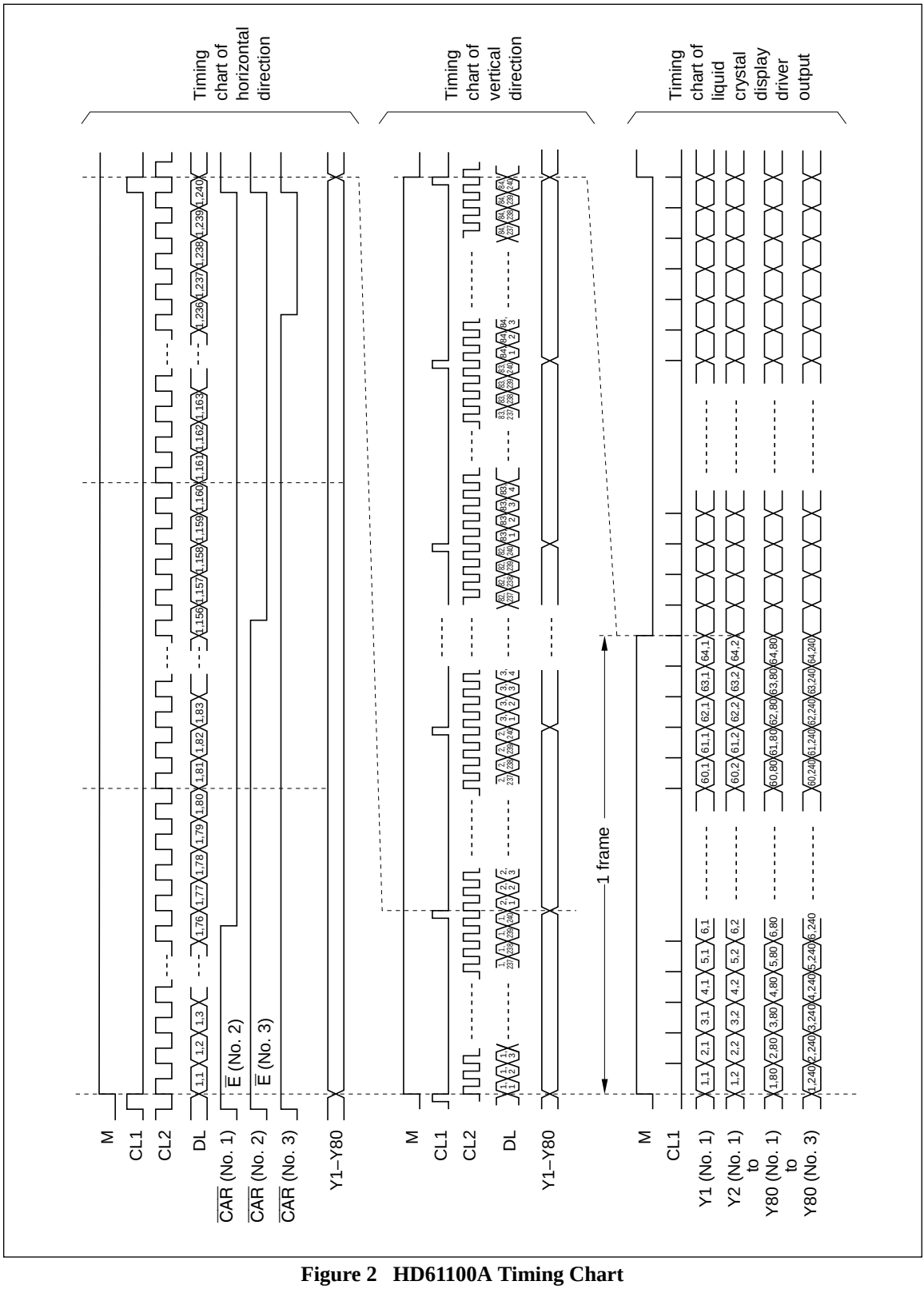


Figure 2 HD61100A Timing Chart

Application Examples

An Example of 128 × 240 Dot Liquid Crystal Display (1/64 Duty Cycle)

The liquid crystal panel (figure 3) is divided into upper and lower parts. These two parts are driven separately. HD61100As No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA(1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow ... Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61100As No. 4 to No. 6 drive the lower half. Serial data, which are input from the DATA(2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow ... Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high). As shown in this example, PC board for display divided into upper and lower half can be easily designed by using SHL terminal effectively.

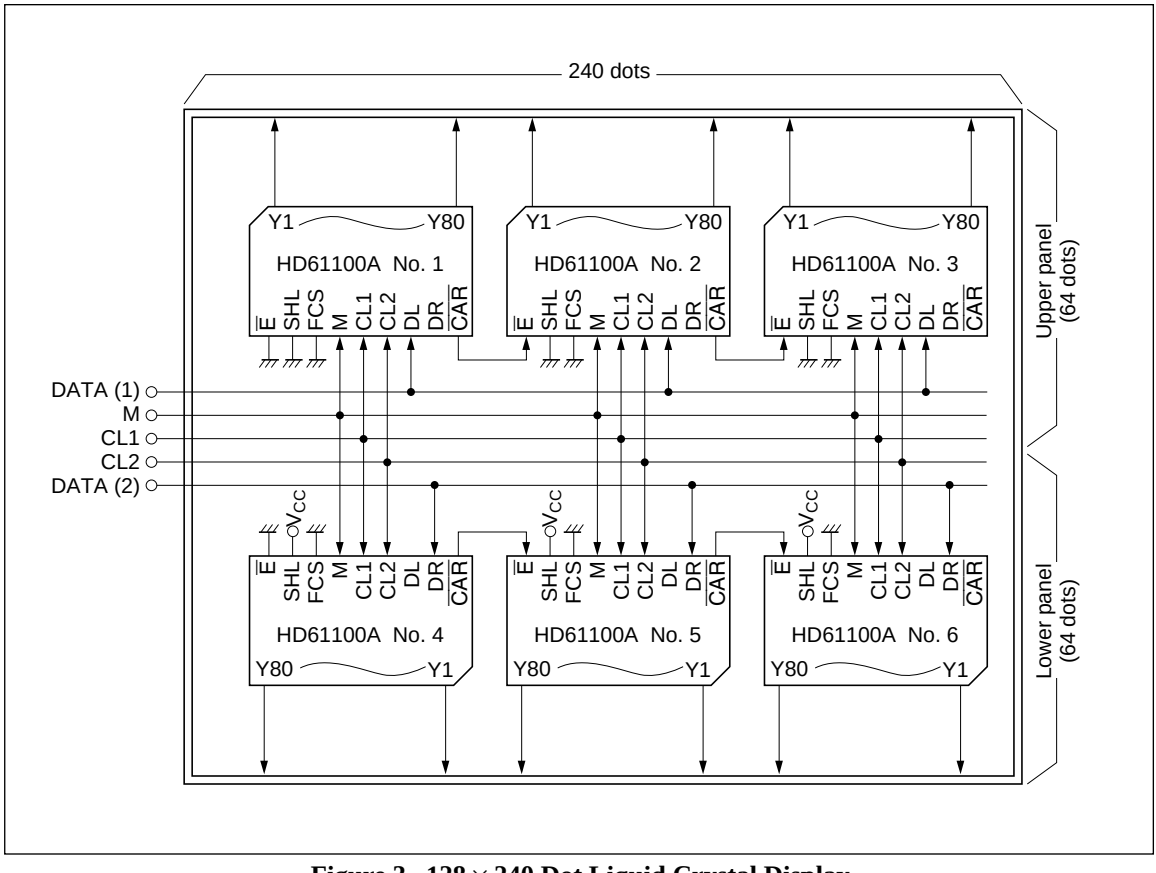


Figure 3 128 × 240 Dot Liquid Crystal Display

Example of 64 × 150 Dot Liquid Crystal Display (1/64 Duty Cycle, SHL = Low)

4-bit parallel process is used in this LSI to lessen the power dissipation.

Thus, the sum of the dots in horizontal direction should be multiple of 4.

If not, as this example (figure 4), consideration is needed for input signals (figure 5).

As the sum of dots in lateral direction is 150, 2 more dummy data bits are transferred (152 = 4 × 38).

Dummy data, which is output from Y71 and Y72 of No. 2, can be either 0 or 1 because these terminals do not connect with the liquid crystal display panel.

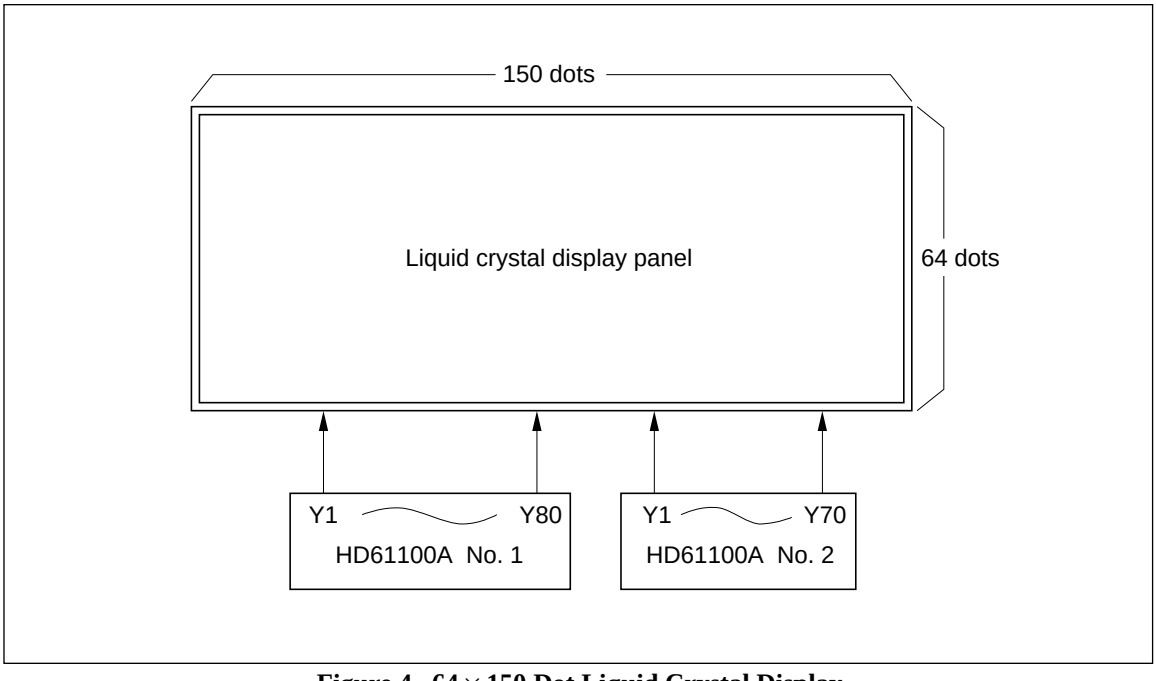


Figure 4 64 × 150 Dot Liquid Crystal Display

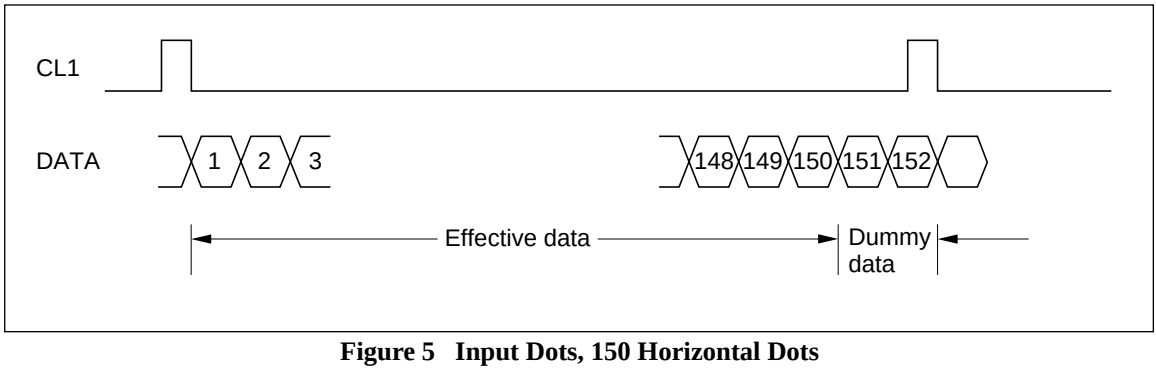


Figure 5 Input Dots, 150 Horizontal Dots

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be permanently destroyed if used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using it beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referred to GND = 0 V.

3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.

4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L} and V_{4R}. Must maintain:
   $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$.
   Connect a protection resistor of 15 Ω ± 10% to each terminals in series.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, $V_{CC} - V_{EE}$ = 5.5 to 17 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = +400 µA	2
Driver resistance	R_{ON}	—	—	7.5	kΩ	V_{EE} = –10 V, load current = 100 µA	3
Input leakage current	I_{IL1}	–1	—	+1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	+2	µA	V_{IN} = V_{EE} to V_{CC}	4
Dissipation current (1)	I_{GND}	—	—	1.0	mA		5
Dissipation current (2)	I_{EE}	—	—	0.1	mA		5

Notes: 1. Applies to CL1, CL2, FCS, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to DL, DR, and $\overline{CAR}$.
3. Applies to Y1–Y80.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
5. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified when $V_{IH} = V_{CC}$, V_{IL} = GND and no load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.

AC Characteristics (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – V_{EE} = 5.5 to 17 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
$\overline{E}$ setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuits are connected for specification: