HD61103A

(Dot Matrix Liquid Crystal Graphic Display
64-Channel Common Driver)

HITACHI

Description

The HD61103A is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals (switch signal to convert LCD waveform to AC, frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen.

As the HD61103A is produced by a CMOS process, it is fit for use in portable battery drive equipments utilizing the liquid crystal display's low power consumption. The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61103A and the column (segment) driver HD61102.

Features

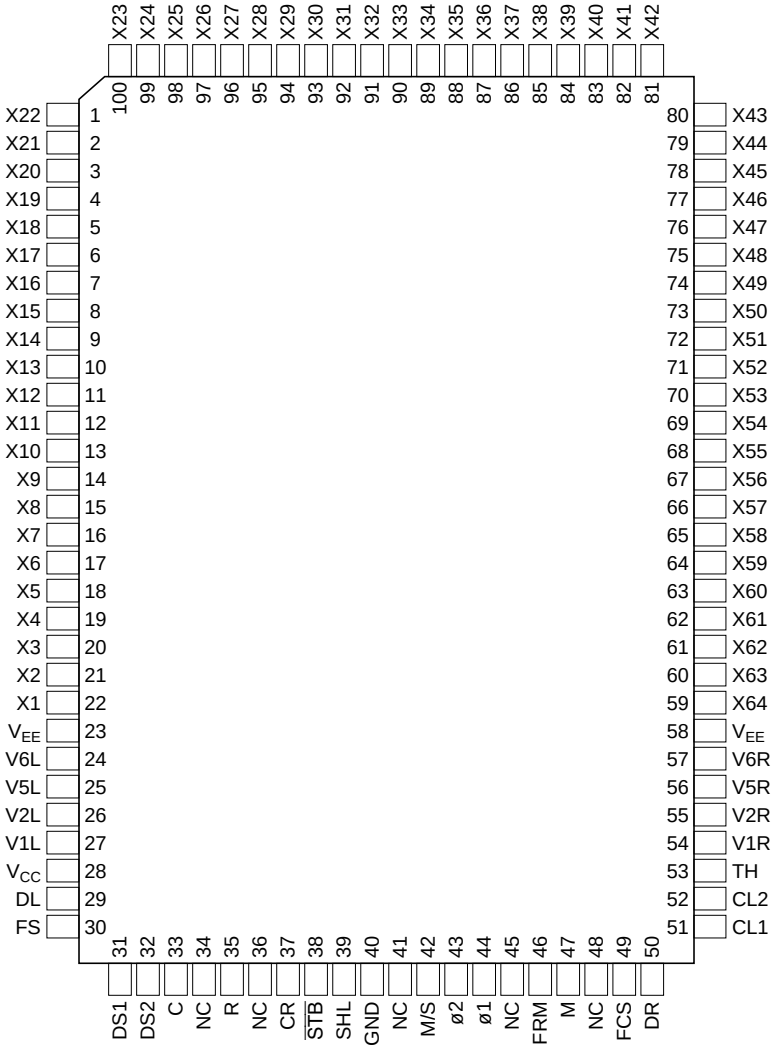
- Dot matrix liquid crystal graphic display common driver with low impedance
- Low impedance: 1.5 kΩ max
- Internal liquid crystal display driver circuit: 64 circuits
- Internal dynamic display timing generator circuit
- Selectable display duty ratio factor 1/48, 1/64, 1/96, 1/128
- Can be used as a column driver transferring data serially
- Low power dissipation: During display: 5 mW
- Power supplies:
  - V_{CC}: +5 V ± 10%
  - V_{EE}: 0 to –11.5 V
- LCD driver level: 17.0 V max
- CMOS process

Ordering Information

Type No.	Package
HD61103A	100-pin plastic QFP (FP-100)

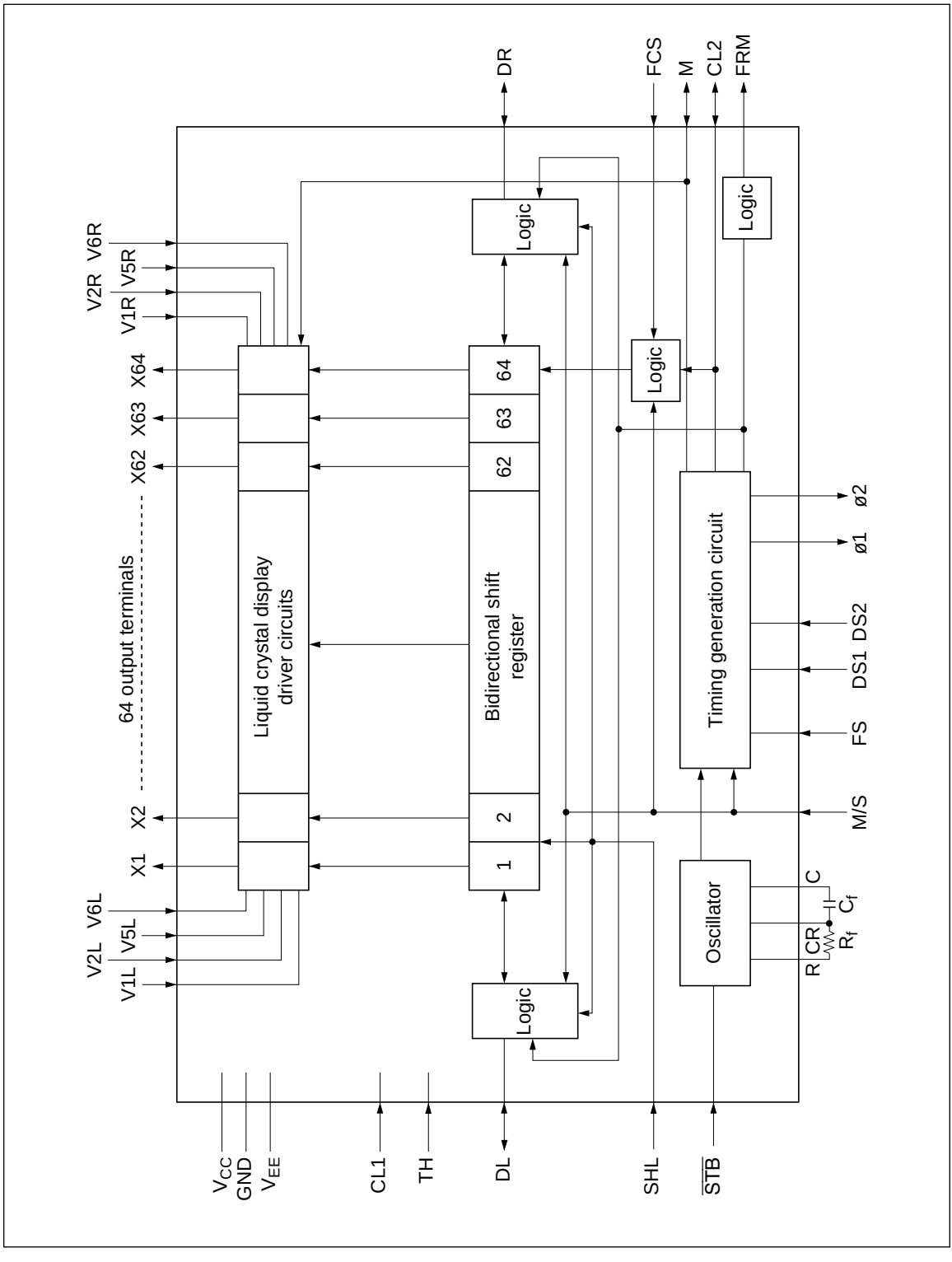
Hitachi semiconductor

Pin Arrangement



(Top view)

Block Diagram



Block Functions

Oscillator

The CR oscillator generates display timing signals and operating clocks for the HD61202. It is required when the HD61103A is used with the HD61102. An oscillation resistor Rf and an oscillation capacitor Cf are attached as shown in figure 1 and terminal $\overline{STB}$ is connected to the high level. When using an external clock, input the clock into terminal CR and don't connect any lines to terminals R and C.

The oscillator is not required when the HD61103A is used with the HD61830. Connect terminal CR to the high level and don't connect any lines to terminals R and C (figure 2).

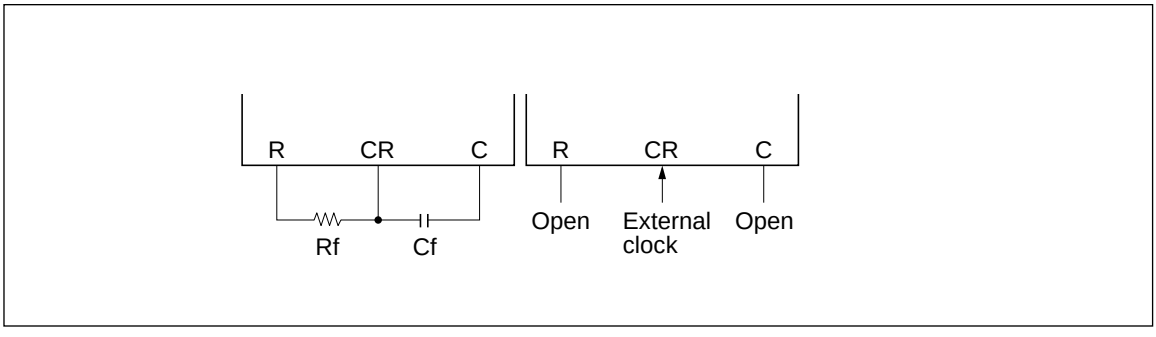


Figure 1 Oscillator Connection with HD61102

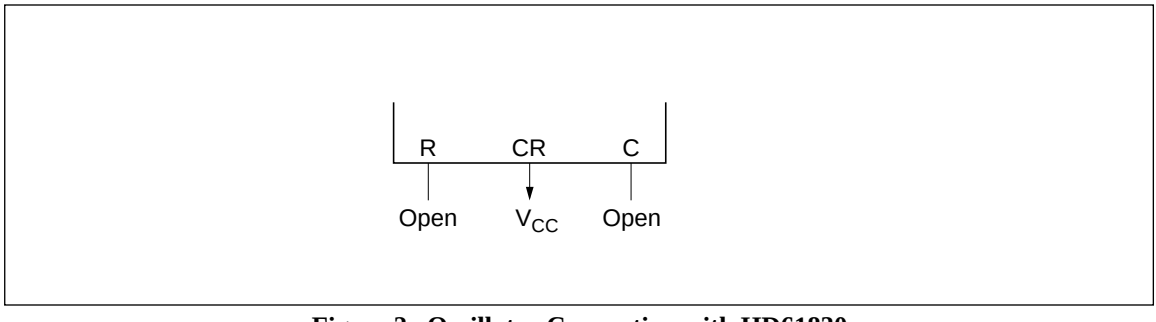


Figure 2 Oscillator Connection with HD61830

Timing Generator Circuit

The timing generator circuit generates display timing and operating clock for the HD61102. This circuit is required when the HD61103A is used with the HD61102. Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits, for example, from HD61830. In this case connect the terminals Fs, DS1, and DS2 to high level and M/S to low level (slave mode).

Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level. In this case, CL2 is used as shift clock. The lowest order bit of the bidirectional shift register, which is on the DL side, corresponds to X1 and the highest order bit on the DR side corresponds to X64.

Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals (table 1).

Table 1 Output Levels

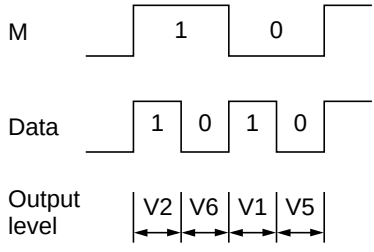
Data from the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

HD61103A Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 2		Power supply	V_{CC}–GND: Power supply for internal logic. V_{CC}–V_{EE}: Power supply for driver circuit logic.
V1L, V2L V5L, V6L V1R, V2R V5R, V6R	8		Power supply	Liquid crystal display driver level power supply. V1L (V1R), V2L (V2R): Selected level V5L (V5R), V6L (V6R): Non-selected level Voltages of the level power supplies connected to V1L and V1R should be the same. (This applies to the combination of V2L & V2R, V5L & V5R and V6L & V6R respectively)
M/S	1	I	V_{CC} or GND	Selects master/slave. • M/S = V_{CC}: Master mode When the HD61103A is used with the HD61202, timing generation circuit operates to supply display timing signals and operation clock to the HD61102. Each of I/O common terminals DL, DR, CL2, and M is in the output state. • M/S = GND: Slave mode The timing operation circuit stops operating. The HD61103A is used in this mode when combined with the HD61830. Even if combined with the HD61102, this mode is used when display timing signals (M, data, CL2, etc.) are supplied by another HD61103A in the master mode. Terminals M and CL2 are in the input state. When SHL is V_{CC}, DL is in the input state and DR is in the output state. When SHL is GND, DL is in the output state and DR is in the input state.
FCS	1	I	V_{CC} or GND	Selects shift clock phase. • FCS = V_{CC} Shift register operates at the rising edge of CL2. Select this condition when HD61103A is used with HD61102 or when MA of the HD61830 connects to CL2 in combination with the HD61830. • FCS = GND Shift register operates at the fall of CL2. Select this condition when CL1 of HD61830 connects to CL2 in combination with the HD61830.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
FS	1	I	V_{CC} or GND	Selects frequency. When the frame frequency is 70 Hz, the oscillation frequency should be: f_{OSC} = 430 kHz at FCS = V_{CC} f_{OSC} = 215 kHz at FCS = GND This terminal is active only in the master mode. Connect it to V_{CC} in the slave mode.
DS1, DS2	2	I	V_{CC} or GND	Selects display duty factor. Display Duty Factor: 1/48 / 1/64 / 1/96 / 1/128 DS1: GND / GND / V_{CC} / V_{CC} DS2: GND / V_{CC} / GND / V_{CC} These terminals are valid only in the master mode. Connect them to V_{CC} in the slave mode.
$\overline{STB}$ TH CL1	1 1 1	I	V_{CC} or GND	Input terminal for testing. Connect to $\overline{STB}$ V_{CC}. Connect TH and CL1 to GND.
CR, R, C	3			Oscillator. In the master mode, use these terminals as shown below. Usage of these terminals in the master mode: Internal oscillation: Rf, Cf; R, CR, C External clock: Open, External clock, Open; R, CR, C In the slave mode, stop the oscillator as shown below: Open, V_{CC}, Open; R, CR, C
ø1, ø2	2	O	HD61102	Operating clock output terminals for the HD61102. • Master mode Connect these terminals to terminals ø1 and ø2 of the HD61102 respectively. • Slave mode Don't connect any lines to these terminals.

<table>
<tr><th>Terminal Name</th><th>Number of Terminals</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>HD61102</td><td>Frame signal
• Master mode
Connect this terminal to terminal FRM of the HD61102.
• Slave mode
Don’t connect any lines to this terminal.</td></tr>
<tr><td>M</td><td>1</td><td>I/O</td><td>MB of HD61830 or M of HD61102</td><td>Signal to convert LCD driver signal into AC
• Master mode: Output terminal
Connect this terminal to terminal M of the HD61102.
• Slave mode: Input terminal
Connect this terminal to terminal MB of the HD61830.</td></tr>
<tr><td>CL2</td><td>1</td><td>I/O</td><td>CL1 or MA of HD61830 or CL of HD61102</td><td>Shift clock
• Master mode: Output terminal
Connect this terminal to terminal CL of the HD61102.
• Slave mode: Input terminal
Connect this terminal to terminal CL1 or MA of the HD61830.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Open or FLM of HD61830</td><td>Data I/O terminals of bidirectional shift register
DL corresponds to X1’s side and DR to X64’s side.
• Master mode
Output common scanning signal. Don’t connect any lines to these terminals normally.
• Slave mode
Connect terminal FLM of the HD61830 to DL (when SHL = V_{CC}) or DR (when SHL = GND)
<table>
<tr><td>M/S</td><td colspan="2">V_{CC}</td><td colspan="2">GND</td></tr>
<tr><td>SHL</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td></tr>
<tr><td>DL</td><td>Output</td><td>Output</td><td>Input</td><td>Output</td></tr>
<tr><td>DR</td><td>Output</td><td>Output</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>5</td><td></td><td>Open</td><td>Not used.
Don’t connect any lines to this terminal.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>V_{CC} or GND</td><td>Selects shift direction of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift Direction</td><td>Common Scanning Direction</td></tr>
<tr><td>V_{CC}</td><td>DL → DR</td><td>X1 → X64</td></tr>
<tr><td>GND</td><td>DL ← DR</td><td>X1 ← X64</td></tr>
</table></td></tr>
</table>

Terminal Name	Number of Terminals	I/O	Connected to	Functions
X1–X64	64	O	Liquid crystal display	Liquid crystal display driver output Output one of the four liquid crystal display driver levels V1, V2, V5, and V6 with the combination of the data from the shift register and M signal.  Data 1: Selected level 0: Non-selected level When SHL is V_{CC}, X1 corresponds to COM1 and X64 corresponds to COM64. When SHL is GND, X64 corresponds to COM1 and X1 corresponds to COM64.

Example of Application

HD61103A Connection List

	M/S	TH	CL1	FCS	FS	DS1	DS2	$\overline{STB}$	CR	R	C	ø1	ø2	FRM	M	CL2	SHL	DL	DR	X1–X64
A	L	L	L	L	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From CL1 of HD61830	H	From FLM of HD61830	—	COM1–COM64
																	L	—	From FLM of HD61830	COM64–COM1
B	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From FLM of HD61830	To DL/DR of HD61103A No. 2	COM1–COM64
																	L	To DL/DR of HD61103A No. 2	From FLM of HD61830	COM64–COM1
C	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From MB of HD61830	From MA of HD61830	H	From DL/DR of HD61103A No. 1	—	COM65–COM128
																	L	—	From DL/DR of HD61103A No. 1	COM128–COM65
D	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	To ø1 of HD61102	To ø2 of HD61102	To FRM of HD61102	To M of HD61102	To CL of HD61102	H	—	—	COM1–COM64
																	L	—	—	COM64–COM1
E	H	L	L	H	H	LL or LH		H	Rf Cf	Rf	Cf	To ø1 of HD61102	To ø2 of HD61102	To FRM of HD61102	To M of HD61102 HD61103A	To CL of HD61102 To CL2 of HD61103A	H	—	To DL/DR of HD61103A No. 2	COM1–COM64
																	L	To DL/DR of HD61103A No. 2	—	COM64–COM1
F	L	L	L	H	H	H	H	H	H	—	—	—	—	—	From M of HD61103A No. 1	From CL2 of HD61103A No. 1	H	From DL/DR of HD61103A No. 1	—	COM1–COM64
																	L	—	From DL/DR of HD61103A No. 1	COM64–COM1

Notes: H: V_{CC} } Fixed
L: GND }

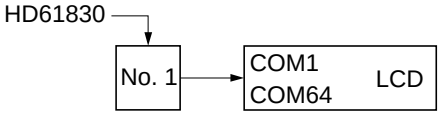
"—" means "open".

Rf: Oscillation resister
Cf: Oscillation capacitor

Outline of HD61103A System Configuration

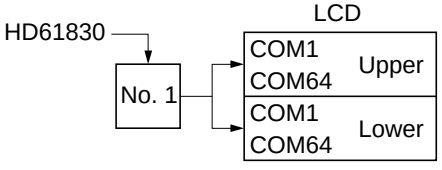
Use with HD61830

1. When display duty ratio of LCD is more than 1/64



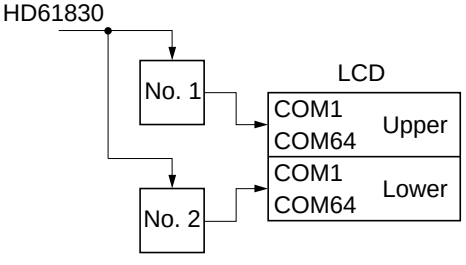
One HD61103A drives common signals.

Refer to Connection List A.



One HD61103A drives common signals for upper and lower panels.

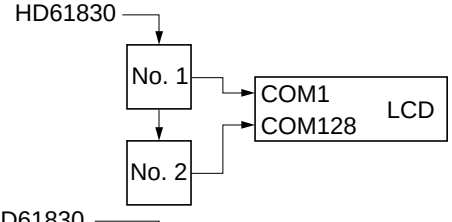
Refer to Connection List A.



Two HD61103As drive upper and lower panels separately to ensure the quality of display. No. 1 and No. 2 operate in parallel.

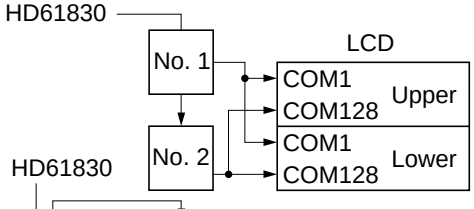
For both of No. 1 and No. 2, refer to Connection List A.

2. When display duty ratio of LCD is from 1/65 to 1/128



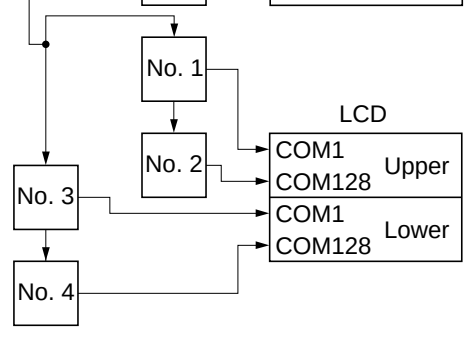
Two HD61103As connected serially drive common signals.

Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two HD61103As connected serially drive upper and lower panels in parallel.

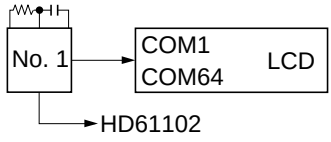
Refer to Connection List B for No. 1.
Refer to Connection List C for No. 2.



Two sets of HD61103As connected serially drive upper and lower panels in parallel to ensure the quality of display.

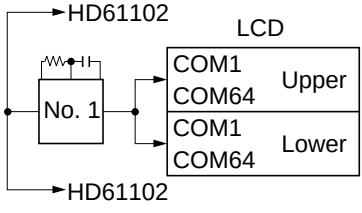
Refer to Connection List B for No. 1 and 3.
Refer to Connection List C for No. 2 and 4.

Use with HD61102 (1/64 Duty Ratio)



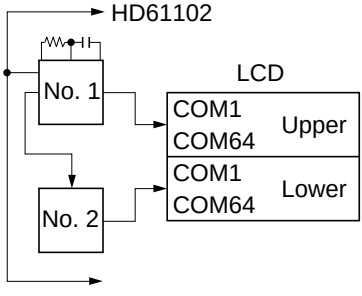
One HD61103A drives common signals and supplies timing signals to the HD61102s.

Refer to Connection List D.



One HD61103A drives upper and lower panels and supplies timing signals to the HD61102s.

Refer to Connection List D.



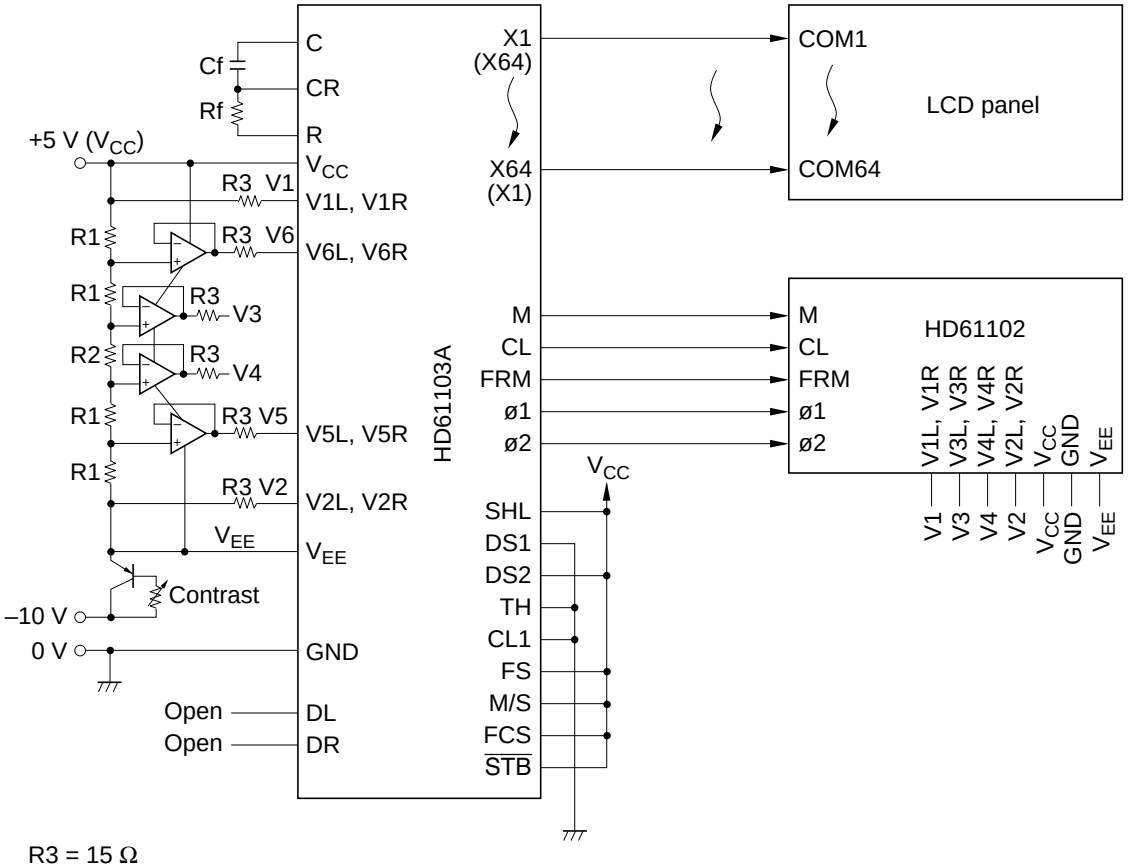
Two HD61103As drive upper and lower panels in parallel to ensure the quality of display. No. 1 supplies timing signals to No. 2 and the HD61102s.

Refer to Connection List E for No. 1.
Refer to Connection List F for No. 2.

Connection Example 1

Use with HD61102 (RAM Type Segment Driver)

1. 1/64 duty ratio (see Connection List D)



R3 = 15 Ω

( ) is at SHL = Low

Note: The values of R1 and R2 vary with the LCD panel used. When bias factor is 1/9, the values of R1 and R2 should satisfy.

$$\frac{R1}{4R1 + R2} = \frac{1}{9}$$

For example,

R1 = 3 kΩ, R2 = 15 kΩ

Figure 3 Example 1

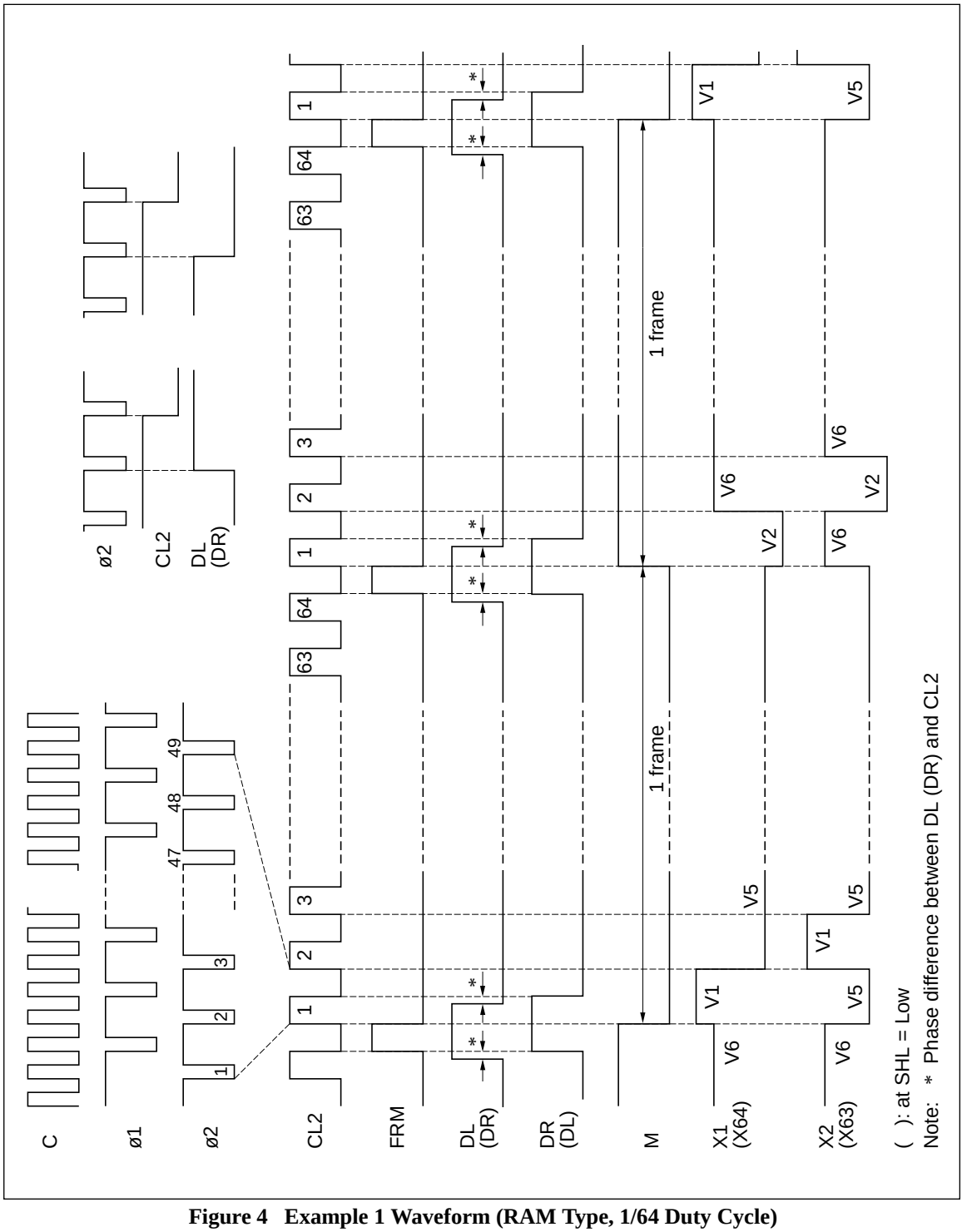


Figure 4 Example 1 Waveform (RAM Type, 1/64 Duty Cycle)

Connection Example 2

Use with HD61830 (Display Controller)

1. 1/64 duty ratio (see Connection List A)

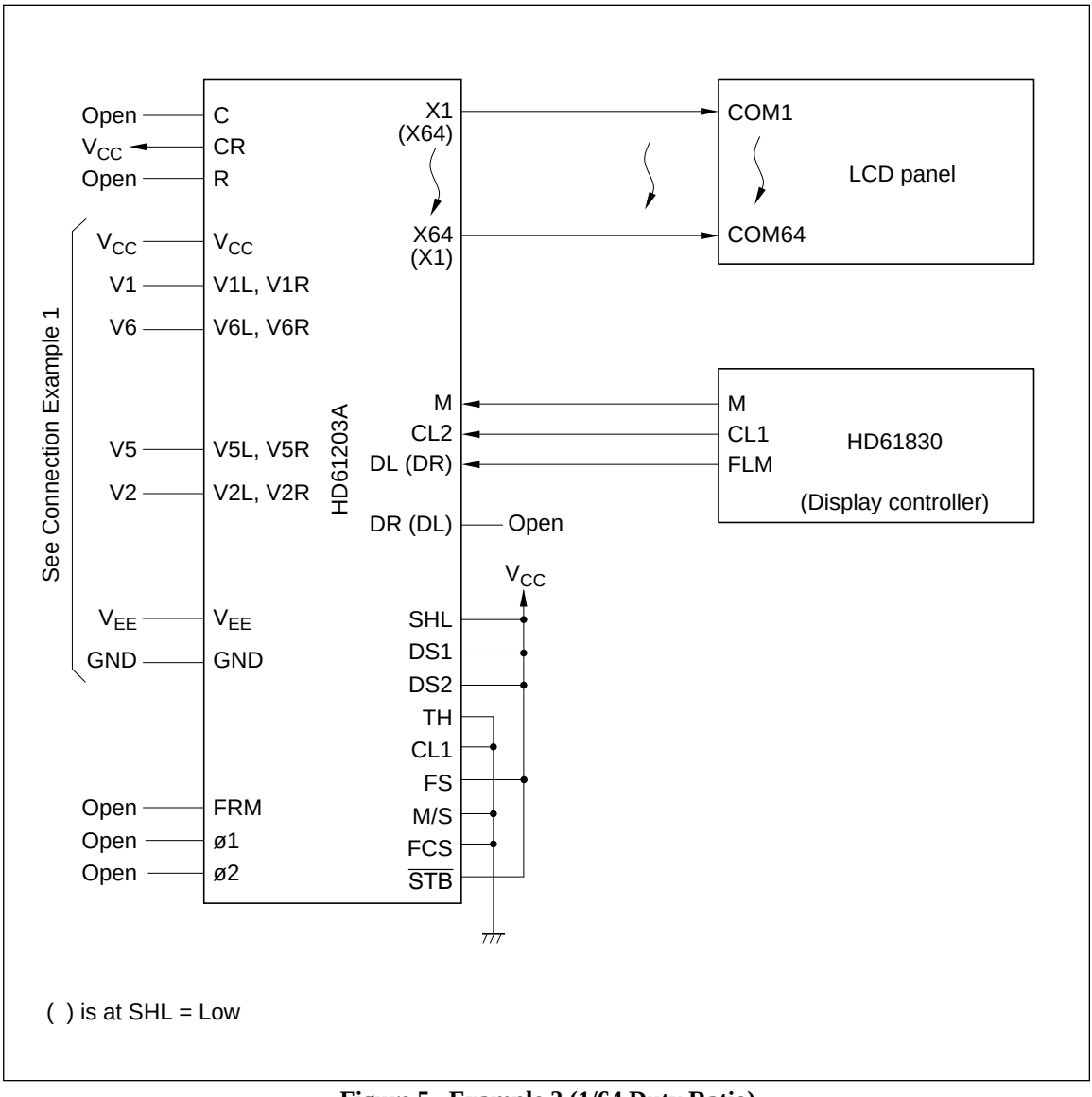


Figure 5 Example 2 (1/64 Duty Ratio)

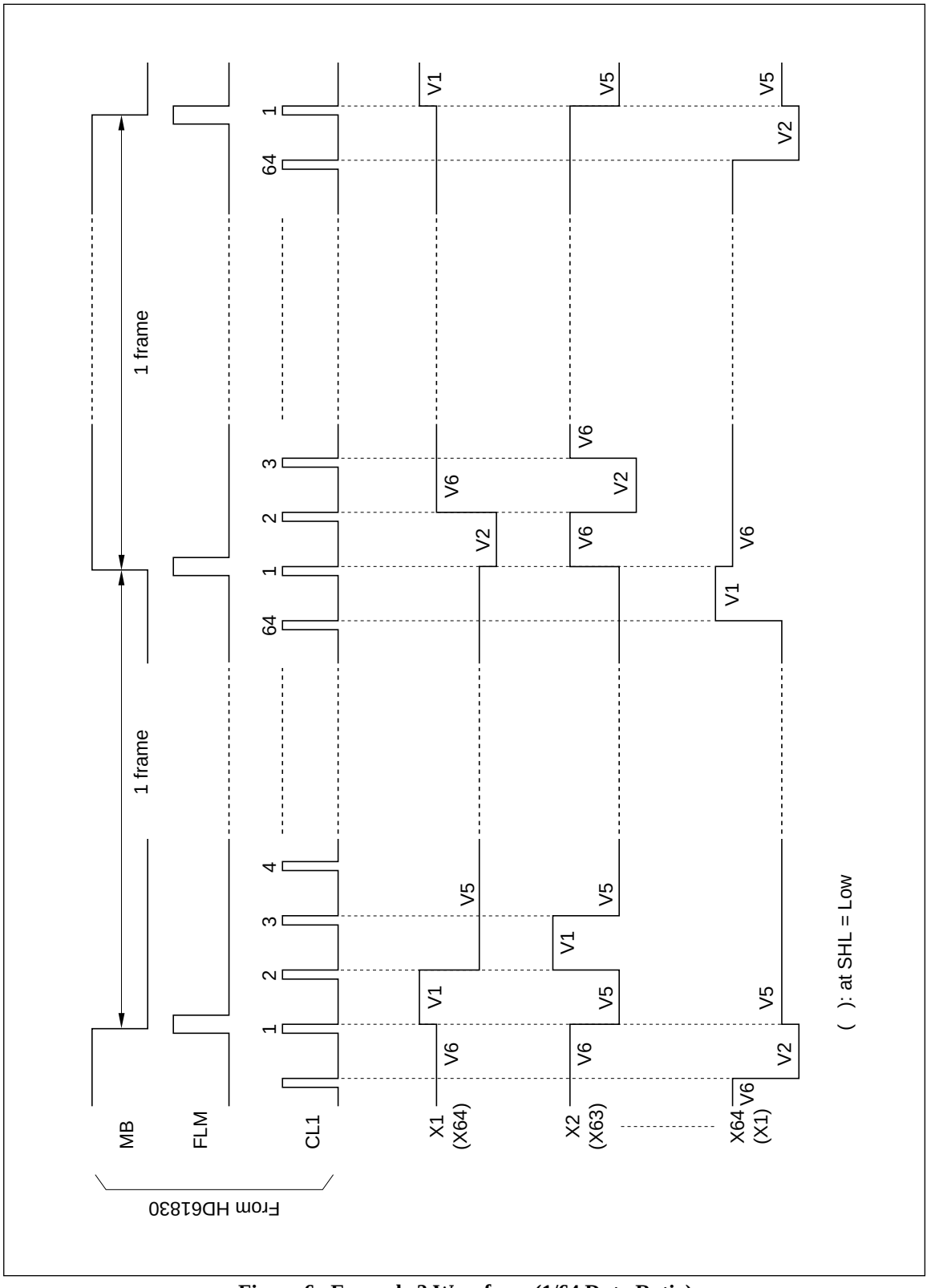


Figure 6 Example 2 Waveform (1/64 Duty Ratio)

2. 1/100 duty ratio (see Connection List B, C)

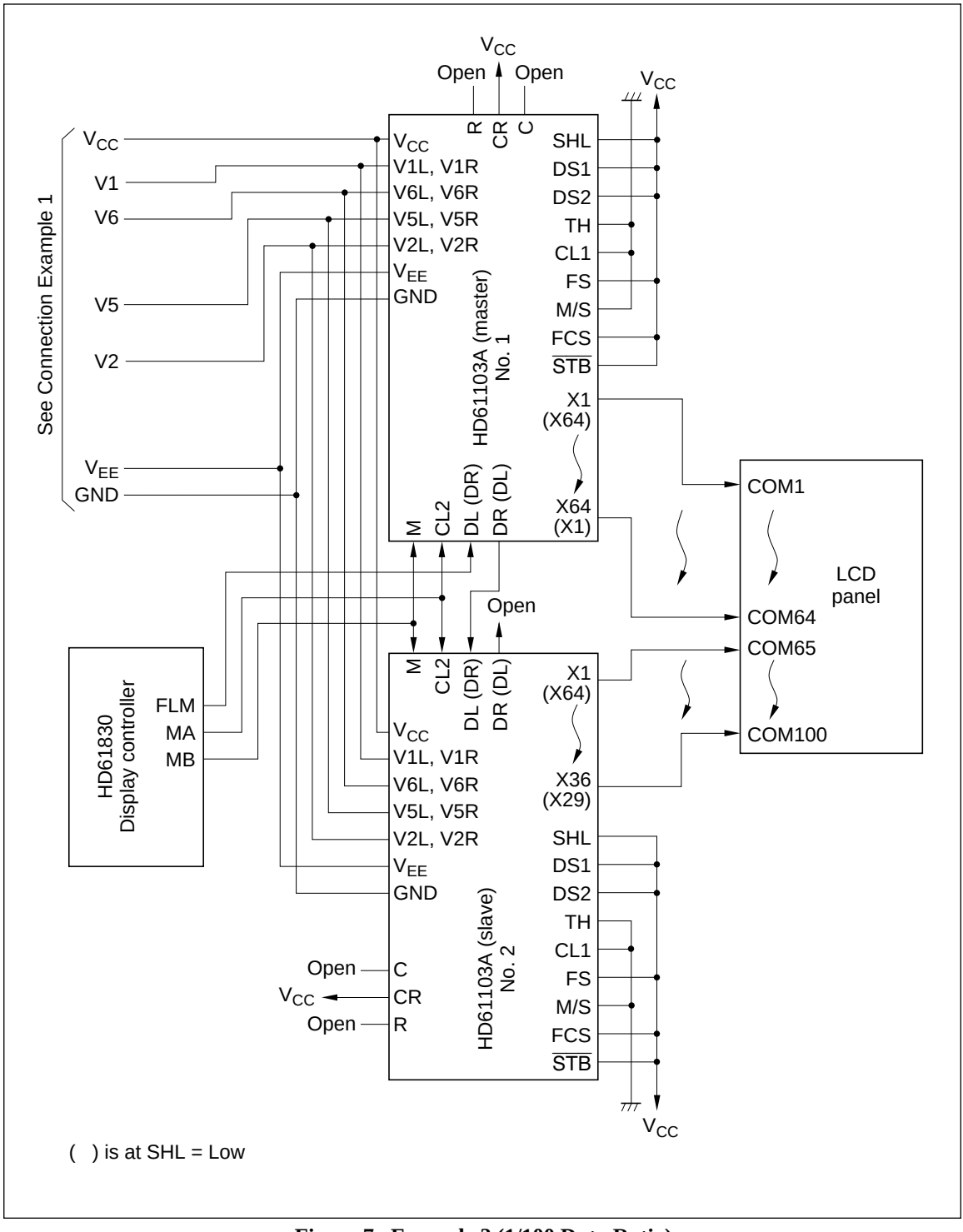


Figure 7 Example 2 (1/100 Duty Ratio)

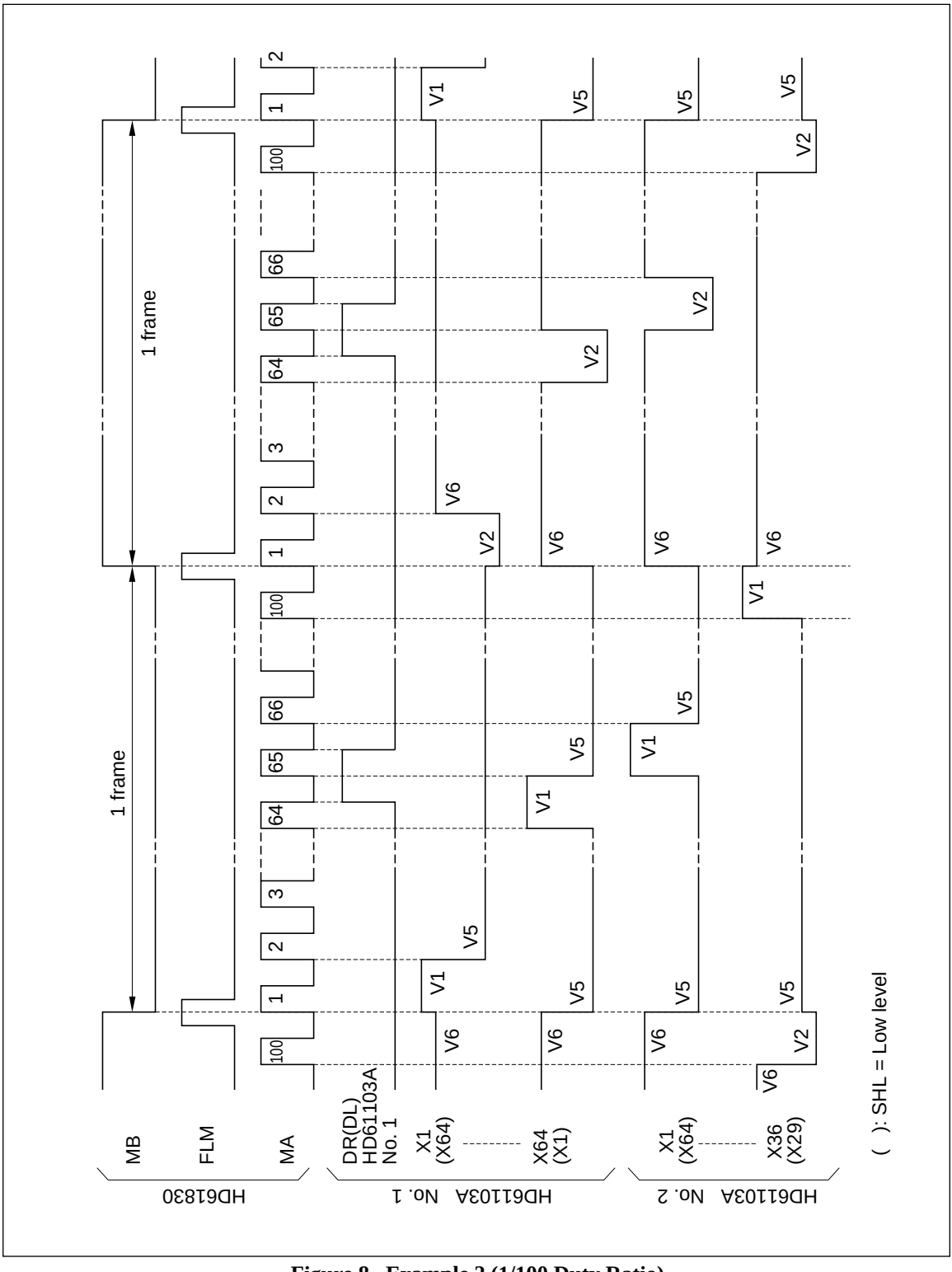


Figure 8 Example 2 (1/100 Duty Ratio)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	2
Power supply voltage (2)	V_{EE}	V_{CC} – 19.0 to V_{CC} + 0.3	V	5
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. If LSIs are used beyond absolute maximum ratings, they may be permanently destroyed. We strongly recommend you to use the LSI within electrical characteristic limits for normal operation, because use beyond these conditions will cause malfunction and poor reliability.

2. Based on GND = 0 V.
3. Applies to input terminals (except V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) and I/O common terminals at high impedance.
4. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.
5. Apply the same value of voltages to V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, V_{EE} (23 pin) and V_{EE} (58 pin) respectively.

   Maintain $V_{CC} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EE}$

Electrical Characteristics

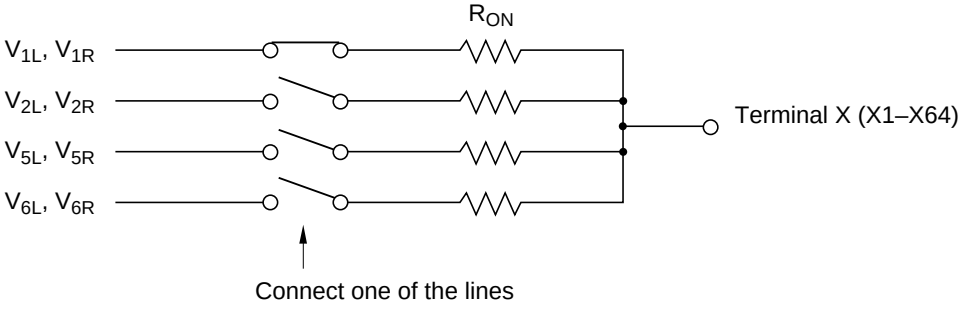
DC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

		Specifications					
Test Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	**Notes**
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	V_{CC}	V		1
Input low voltage	V_{IL}	GND	—	$0.3 \times V_{CC}$	V		1
Output high voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low voltage	V_{OL}	—	—	+0.4	V	I_{OL} = +0.4 mA	2
Vi–Xj on resistance	R_{ON}	—	—	1.5	kΩ	$V_{CC} – V_{EE}$ = 10 V Load current ±150 µA	3
Input leakage current	I_{IL1}	–1.0	—	+1.0	µA	Vin = 0 to V_{CC}	4
Input leakage current	I_{IL2}	–2.0	—	+2.0	µA	Vin = V_{EE} to V_{CC}	5
Operating frequency	f_{opr1}	50	—	600	kHz	In master mode external clock operation	6
Operating frequency	f_{opr2}	50	—	1500	kHz	In slave mode shift register	7
Oscillation frequency	f_{osc}	315	450	585	kHz	Cf = 20 pF ± 5% Rf = 47 kΩ ± 2%	8, 13
Dissipation current (1)	I_{GG1}	—	—	1.0	mA	In master mode 1/128 duty cycle Cf = 20 pF Rf = 47 kΩ	9, 10
Dissipation current (2)	I_{GG2}	—	—	200	µA	In slave mode 1/128 duty cycle	9, 11
Dissipation current	I_{EE}	—	—	100	µA	In master mode 1/128 duty cycle	9, 12

Notes: 1. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH and I/O terminals DL, M, DR and CL2 in the input state.

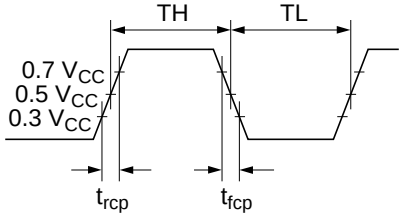
2. Applies to output terminals, ø1, ø2, and FRM and I/O common terminals DL, M, DR, and CL2 in the output status.

3. Resistance value between terminal X (one of X1 to X64) and terminal V (one of V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R) when load current is applied to each terminal X.
Equivalent circuit between terminal X and terminal V.

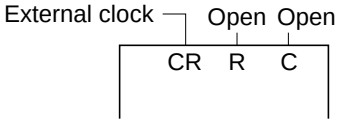


4. Applies to input terminals FS, DS1, DS2, CR, $\overline{STB}$, SHL, M/S, FCS, CL1, and TH, I/O common terminals DL, M, DR and CL2 in the input status and NC terminals.
5. Applies to V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R. Don't connect any lines to X1 to X64.
6. External clock is as follows.

External clock waveform

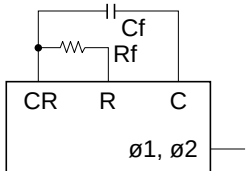


$$\text{Duty cycle} = \frac{TH}{TH + TL} \times 100\%$$



	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
t_{rcp}	—	—	50	ns
t_{fcp}	—	—	50	ns

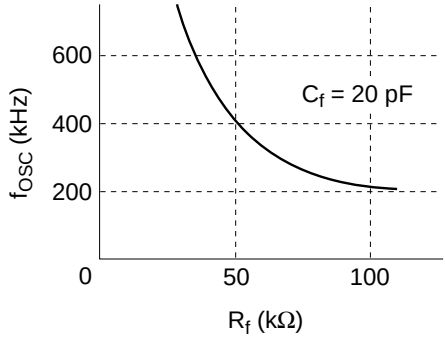
7. Applies to the shift register in the slave mode. For details, refer to AC characteristics.
8. Connect oscillation resistor (Rf) and oscillation capacitance (Cf) as shown in this figure. Oscillation frequency (f_{OSC}) is twice as much as the frequency (fø) at ø1 or ø2.



Cf = 20 pF
Rf = 47 kΩ $\quad f_{OSC} = 2 \times f\text{ø}$

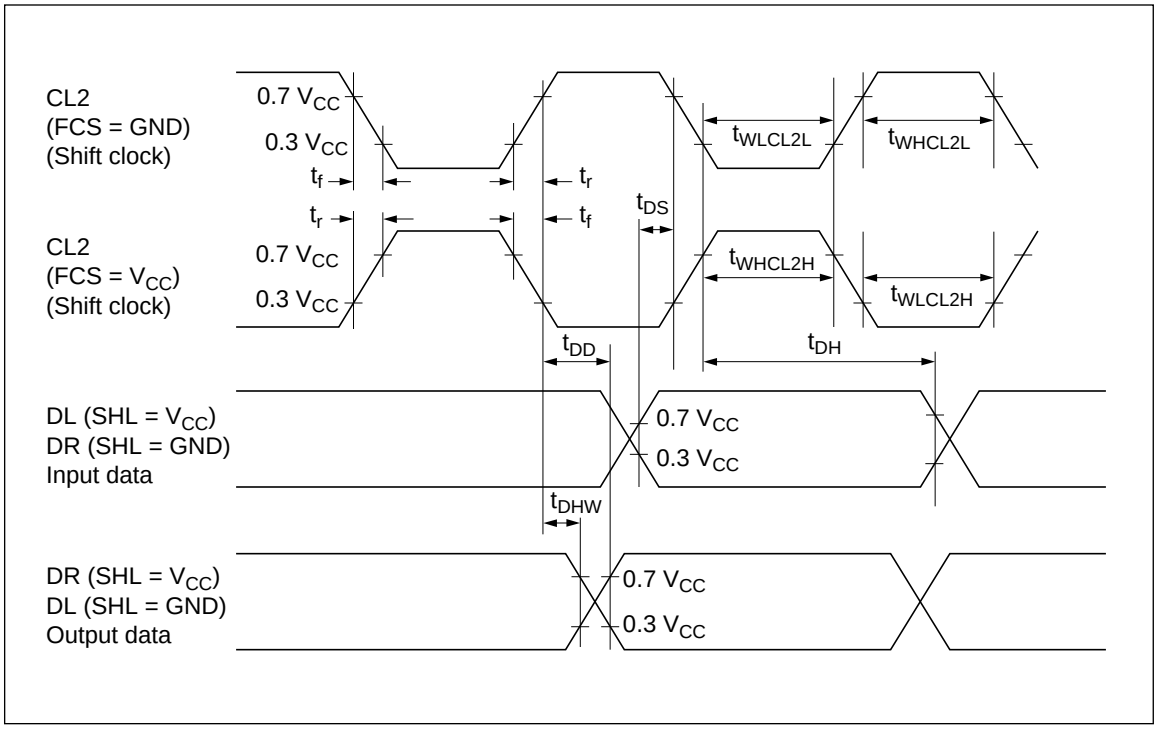
9. No lines are connected to output terminals and current flowing through the input circuit is excluded. This value is specified at $V_{IH} = V_{CC}$ and V_{IL} = GND.
10. This value is specified for current flowing through GND in the following conditions: Internal oscillation circuit is used. Each terminal of DS1, DS2, FS, SHL, M/S, $\overline{STB}$, and FCS is connected to V_{CC} and each of CL1 and TH to GND. Oscillator is set as described in note 8.
11. This value is specified for current flowing through GND under the following conditions: Each terminals of DS1, DS2, FS, SHL, $\overline{STB}$, FCS and CR is connected to V_{CC}, CL1, TH, and M/S to GND and the terminals CL2, M, and DL are respectively connected to terminals CL2, M, and DL of the HD61103A under the conditions described in note 10.
12. This value is specified for current flowing through V_{EE} under the condition described in note 10. Don't connect any lines to terminal V.

13. This figure shows a typical relation among oscillation frequency, Rf and Cf. Oscillation frequency may vary with the mounting conditions.



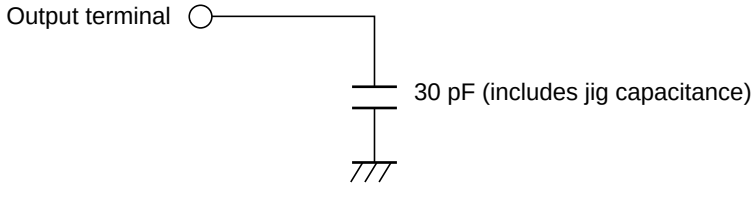
AC Characteristics (V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to –11.5 V, Ta = –20 to +75°C)

Slave Mode (M/S = GND)

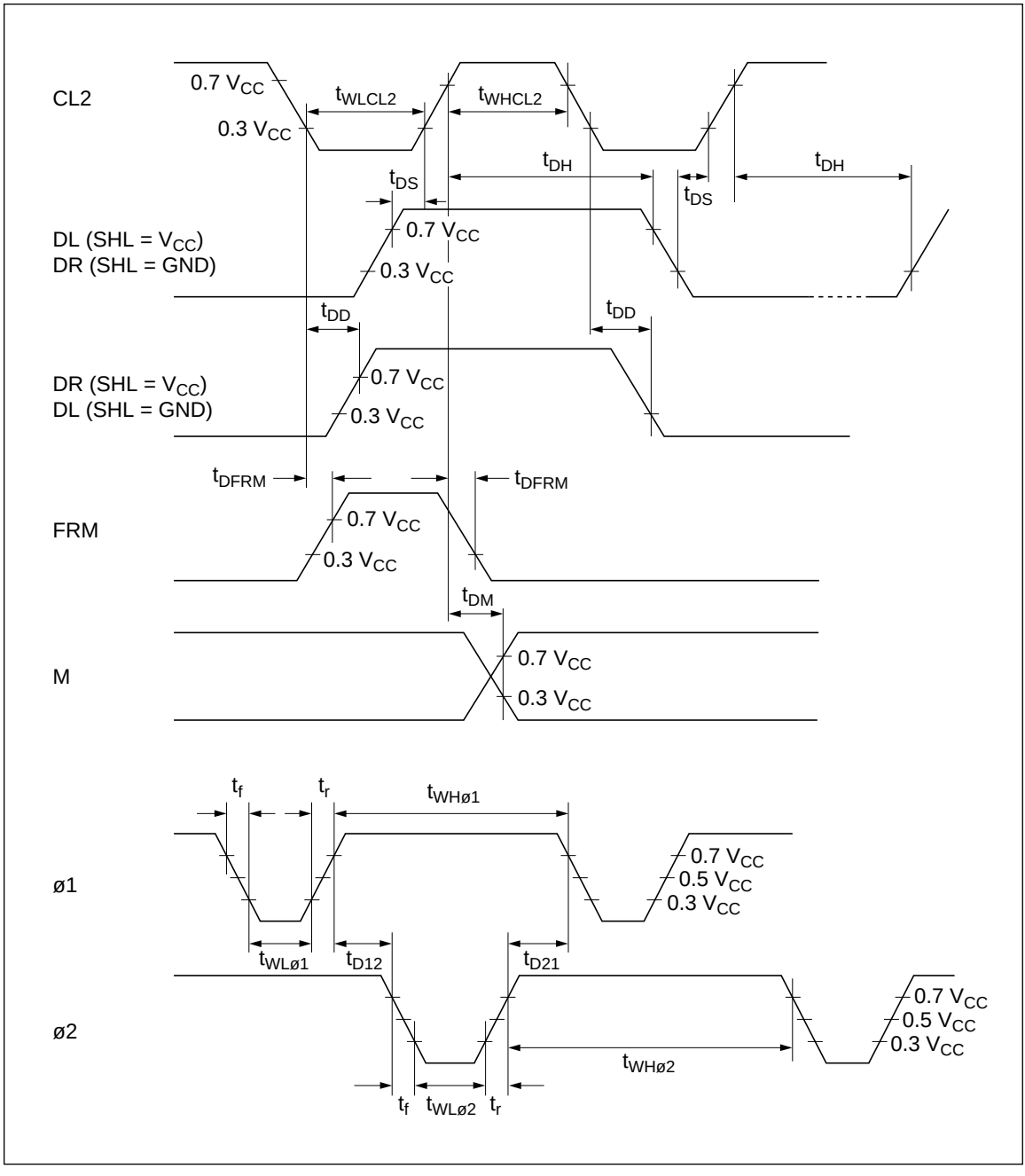


Item	Symbol	Min	Typ	Max	Unit	Note
CL2 low level width (FCS = GND)	t_{WLCL2L}	450	—	—	ns	
CL2 high level width (FCS = GND)	t_{WHCL2L}	150	—	—	ns	
CL2 low level width (FCS = V_{CC})	t_{WLCL2H}	150	—	—	ns	
CL2 high level width (FCS = V_{CC})	t_{WHCL2H}	450	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	100	—	—	ns	
Data delay time	t_{DD}	—	—	200	ns	1
Data hold time	t_{DHW}	10	—	—	ns	
CL2 rise time	t_r	—	—	30	ns	
CL2 fall time	t_f	—	—	30	ns	

Note: 1. The following load circuit is connected for specification.



Master Mode (M/S = V_{CC}, FCS = V_{CC}, Cf = 20 pF, Rf = 47 kΩ)



Item	Symbol	Min	Typ	Max	Unit
Data setup time	t_{DS}	20	—	—	µs
Data hold time	t_{DH}	40	—	—	µs
Data delay time	t_{DD}	5	—	—	µs
FRM delay time	t_{DFRM}	–2	—	+2	µs
M delay time	t_{DM}	–2	—	+2	µs
CL_2 low level width	t_{WLCL2}	35	—	—	µs
CL_2 high level width	t_{WHCL2}	35	—	—	µs
ø1 low level width	$t_{WLø1}$	700	—	—	ns
ø2 low level width	$t_{WLø2}$	700	—	—	ns
ø1 high level width	$t_{WHø1}$	2100	—	—	ns
ø2 high level width	$t_{WHø2}$	2100	—	—	ns
ø1–ø2 phase difference	t_{D12}	700	—	—	ns
ø2–ø1 phase difference	t_{D21}	700	—	—	ns
ø1, ø2 rise time	t_r	—	—	150	ns
ø1, ø2 fall time	t_f	—	—	150	ns