HMCS412C/HMCS412CL/ HMCS412AC

T-49-19-04

(HD614120/HD614125/HD614128)

Description

The HMCS412C/CL/AC are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins to drive a fluorescent display directly.

Features

- 4-bit architecture
- 2048 words of 10-bit ROM
- 160 digits of 4-bit RAM
- 36 I/O pins, including 24 high-voltage I/O pins (40 V max)
- Timer/counter
  - —11-bit prescaler
  - —8-bit auto-reload timer/event counter (timer B)
- Three interrupt sources
  - —External: 2
  - —Timer/counter: 1
- Subroutine stack
  - —Up to 16 levels including interrupts
- Minimum instruction execution time
  - —0.89 μs: HMCS412AC
  - —1.78 μs: HMCS412C
  - —3.55 μs: HMCS412CL
- Low power dissipation modes
  - —Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
  - —Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
  - —Crystal or ceramic filter
  - —External clock input
- Package
  - —Standard 42-pin dual in-line plastic package
  - —42-pin shrink dual in-line plastic package
  - —44-pin flat plastic package
- Instruction set compatible with HMCS404; 98 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD614P180 with the following fixed options:
  - —I/O pin: open drain
  - —Oscillator: crystal or ceramic filter oscillator (externally drivable)
  - —Divider: Divide by 8
  - —Package: standard 42-pin dual in-line ceramic package

Ordering Information

Item	HMCS412C	HMCS412CL	HMCS412AC
Product Name	HD614120	HD614125	HD614128
Power Supply (V)	3.5 to 6	2.5 to 6	4.5 to 6
Typical Instruction Cycle Time (μs)	2	4	1

HMCS412C/HMCS412CL/HMCS412AC

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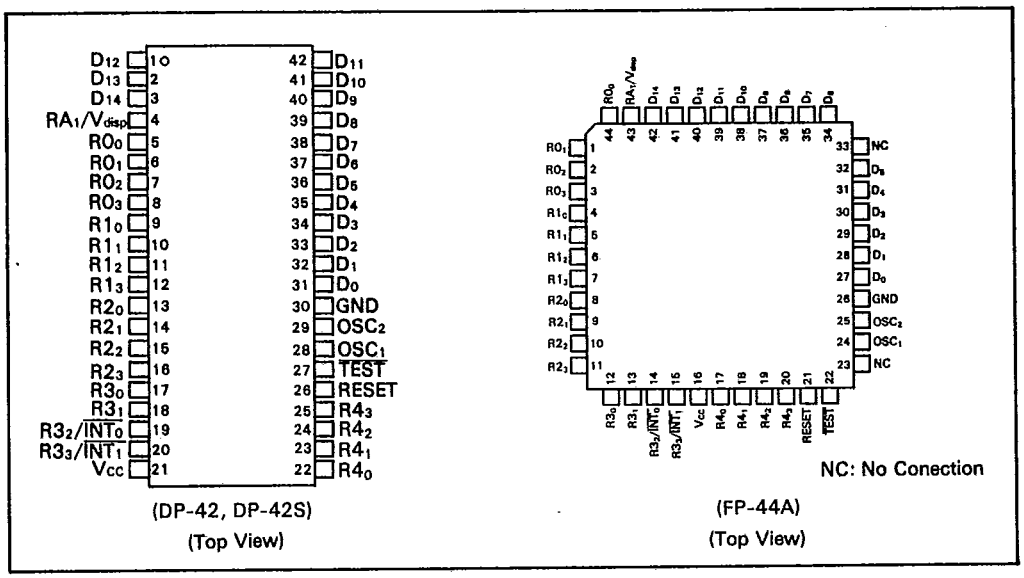
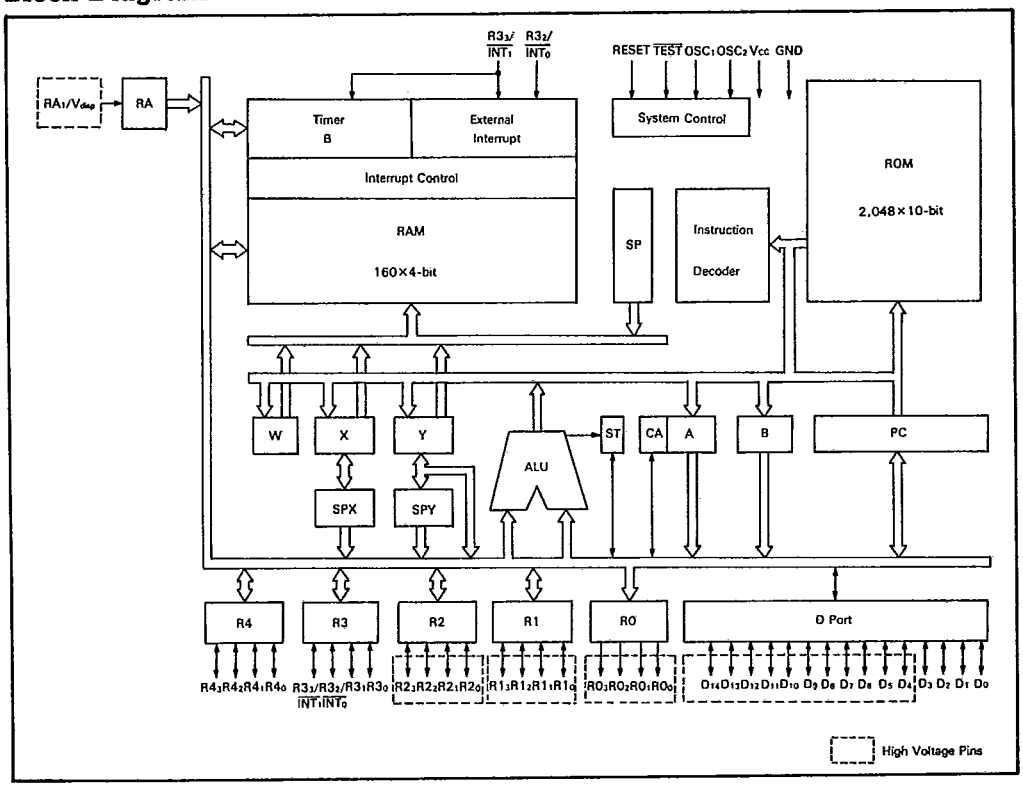
Pin Arrangement



Block Diagram



Pin Description

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GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA_1) is a power supply for high-voltage I/O pins with maximum voltage of 40 V ($V_{CC}-40$ V). For details, see Input/Output section.

$\overline{TEST}$ (Test)

$\overline{TEST}$ is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC_1, OSC_2 (Oscillator Connections)

OSC_1 and OSC_2 are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D_0-D_{14} (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D_0 to D_3 are standard and D_4 to D_{14} are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

$R0_0-R0_3$, $R1_0-R1_3$, $R2_0-R2_3$, $R3_0-R3_3$, $R4_0-R4_3$, RA_1 (R Ports)

R0 to R4 are 4-bit ports. RA is a 1-bit port. R0 is an output port, RA is an input port, and R1 to R4 are I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 and R4 are standard ports. Each pin has a mask option which selects its circuit type. The pins $R3_2$, and $R3_3$ are multiplexed with $\overline{INT_0}$ and $\overline{INT_1}$ respectively. For details, see Input/Output section.

$\overline{INT_0}$, $\overline{INT_1}$ (Interrupts)

$\overline{INT_0}$ and $\overline{INT_1}$ are external interrupts for the MCU. $\overline{INT_1}$ can be used as an external event input pin for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 2,048 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area ($0000 to $000F): Locations $0000 through $000F can be used for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area ($0000 to $003F): Locations $0000 through $003F can be used for subroutines. CAL instructions branch to subroutines.

Pattern Area ($0000 to $07FF): Locations $0000 through $07FF can be used for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area ($0000 to $07FF): Locations from $0000 to $07FF can be used for program code.

RAM Memory Map

The MCU includes 160 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area ($000 to $003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessable only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area ($004 to $00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers

cannot be accessed by RAM bit manipulation instructions.

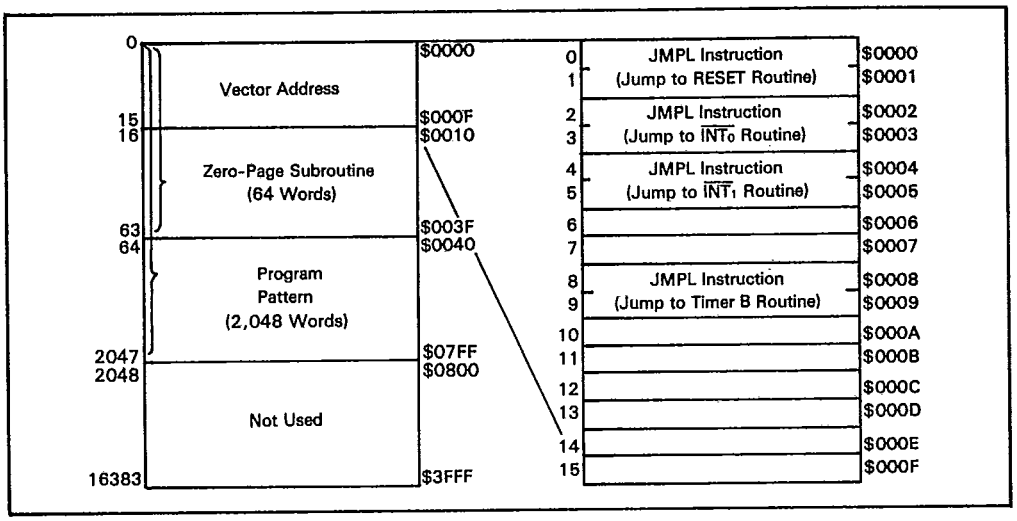

Figure 1. ROM Memory Map

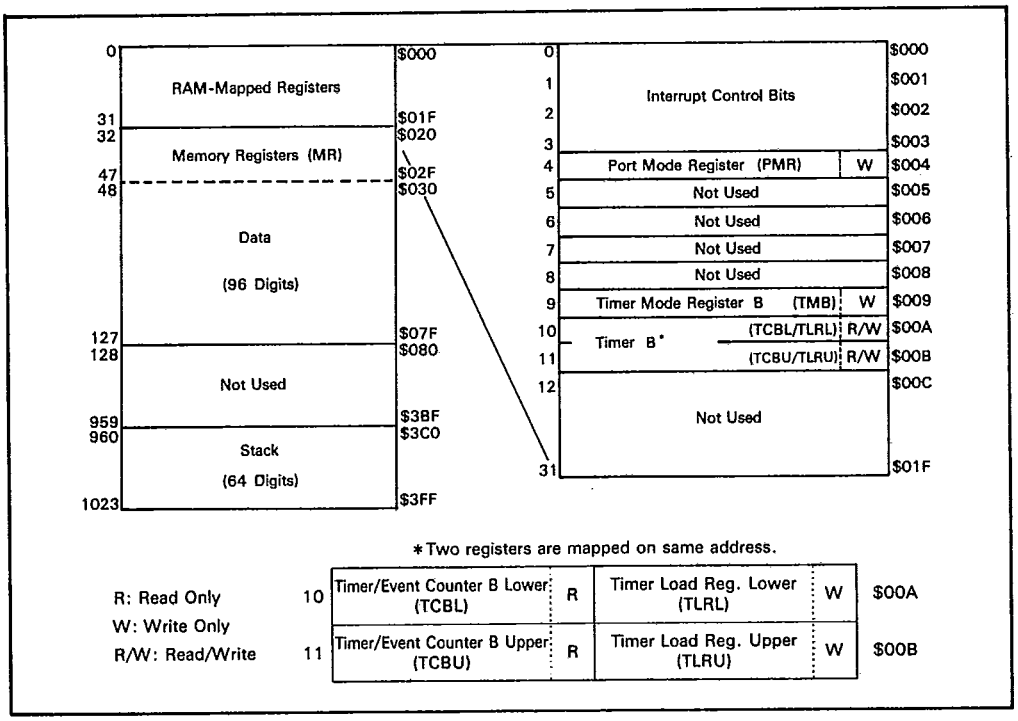

Figure 2. RAM Memory Map

Data Area ($020 to $07F): 16 digits of $020 through $02F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area ($3C0 to $3FF): Locations $3C0 through $3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	$000
1	Not Used	Not Used	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	Not Used	Not Used	IMTB (IM of Timer B)	IFTB (IF of Timer B)	$002
3	Not Used	Not Used	Not Used	Not Used	$003

IF: Interrupt Request Flag
IM: Interrupt Mask
I/E: Interrupt Enable Flag
SP: Stack Pointer
Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
The content of status becomes invalid when "Not Used" bit and RSP bit are tested by a TM or TMD instruction.

Figure 3. Configuration of Interrupt Control Bit Area

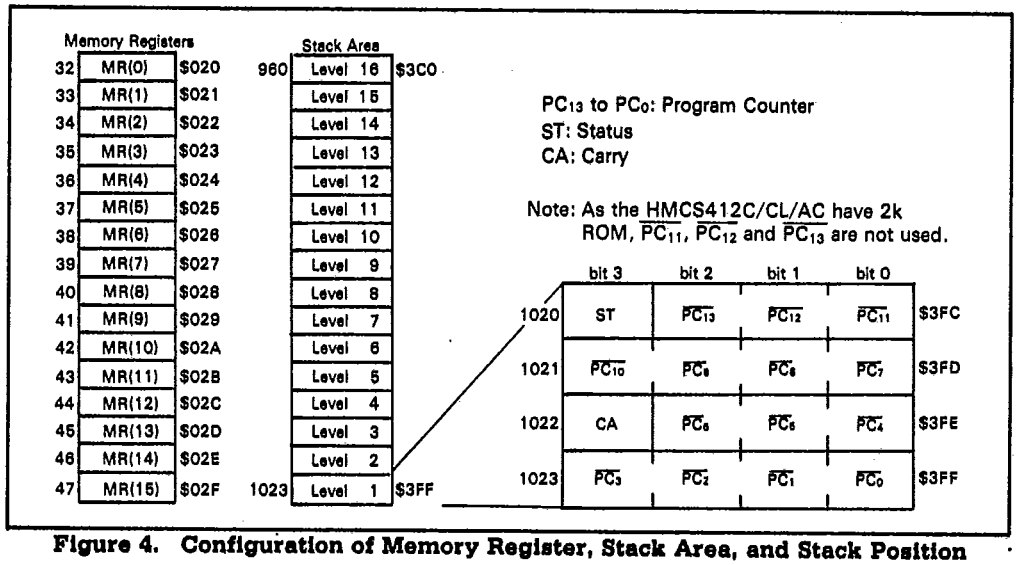

Figure 4. Configuration of Memory Register, Stack Area, and Stack Position

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W register is write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address $3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

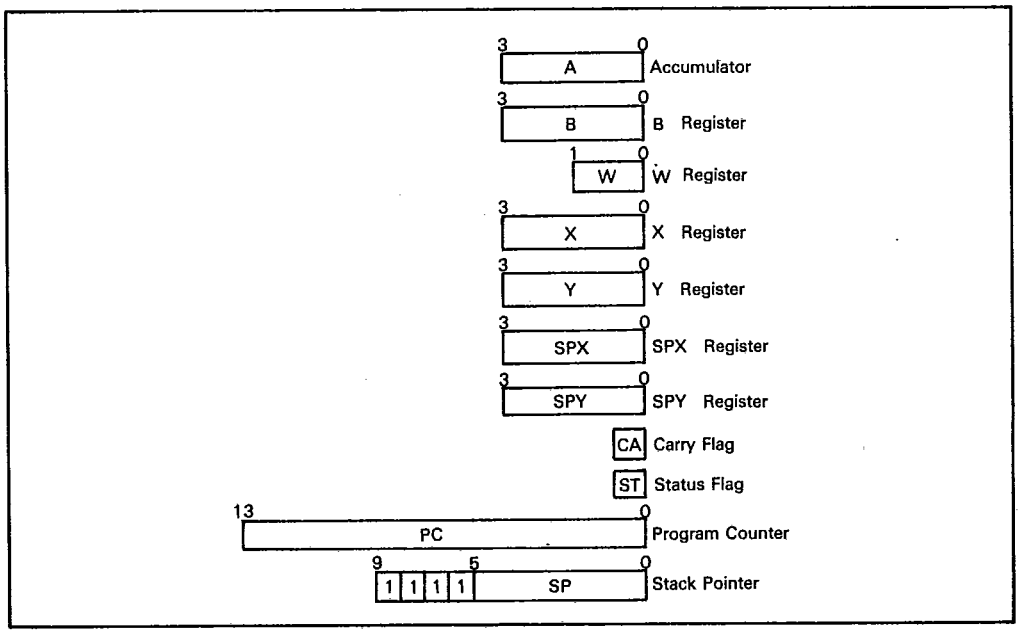

Figure 5. Registers and Flags

The stack pointer is initialized to $3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Three interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on $000 through $003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	$0000
$\overline{INT_0}$	1	$0002
$\overline{INT_1}$	2	$0004
Timer B	3	$0008

Table 2. Interrupt Service Conditions

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer B
I/E	1	1	1
IF0·$\overline{IM0}$	1	0	0
IF1·$\overline{IM1}$	*	1	0
IFTB·$\overline{IMTB}$	*	*	1

* Don't care

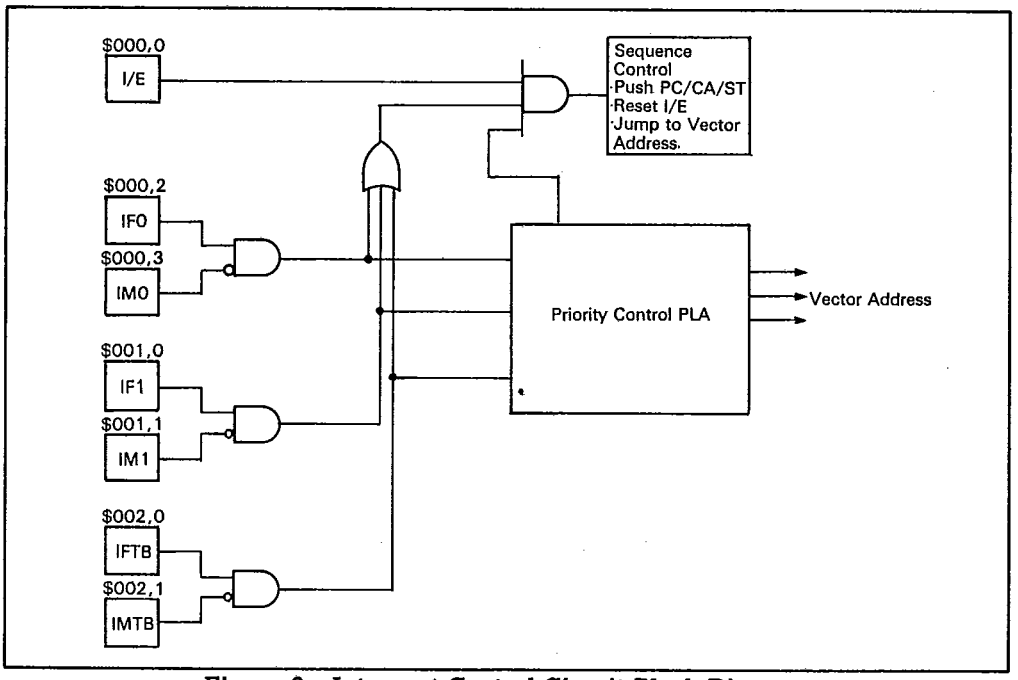

Figure 6. Interrupt Control Circuit Block Diagram

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: $000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$) can be selected by the port mode register (PMR: $004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT_1}$ pin and $R3_2/\overline{INT_0}$ pin to be used as $\overline{INT_1}$ pin and $\overline{INT_0}$ pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs (table 4).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as timer B external event input, the external interrupt mask (IM1) has to be set so that the $\overline{INT_1}$ interrupt request will not be accepted (table 5).

External Interrupt Request Flags (IF0: $000 bit 2, IF1: $001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$, and $\overline{INT_1}$ inputs respectively.

External Interrupt Masks (IM0: $000 bit 3, IM1: $001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: $004): The 4-bit write-only port mode register controls the $R3_2/\overline{INT_0}$ pin, and $R3_3/\overline{INT_1}$ pin as shown in table 6. The port mode register will be initialized to $0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin

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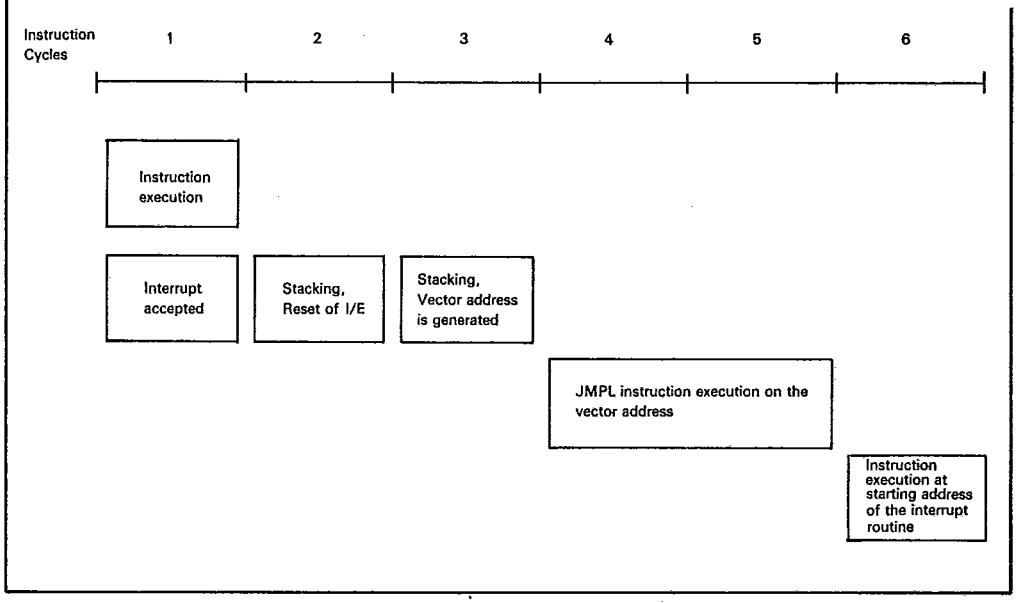


Figure 7. Interrupt Servicing Sequence

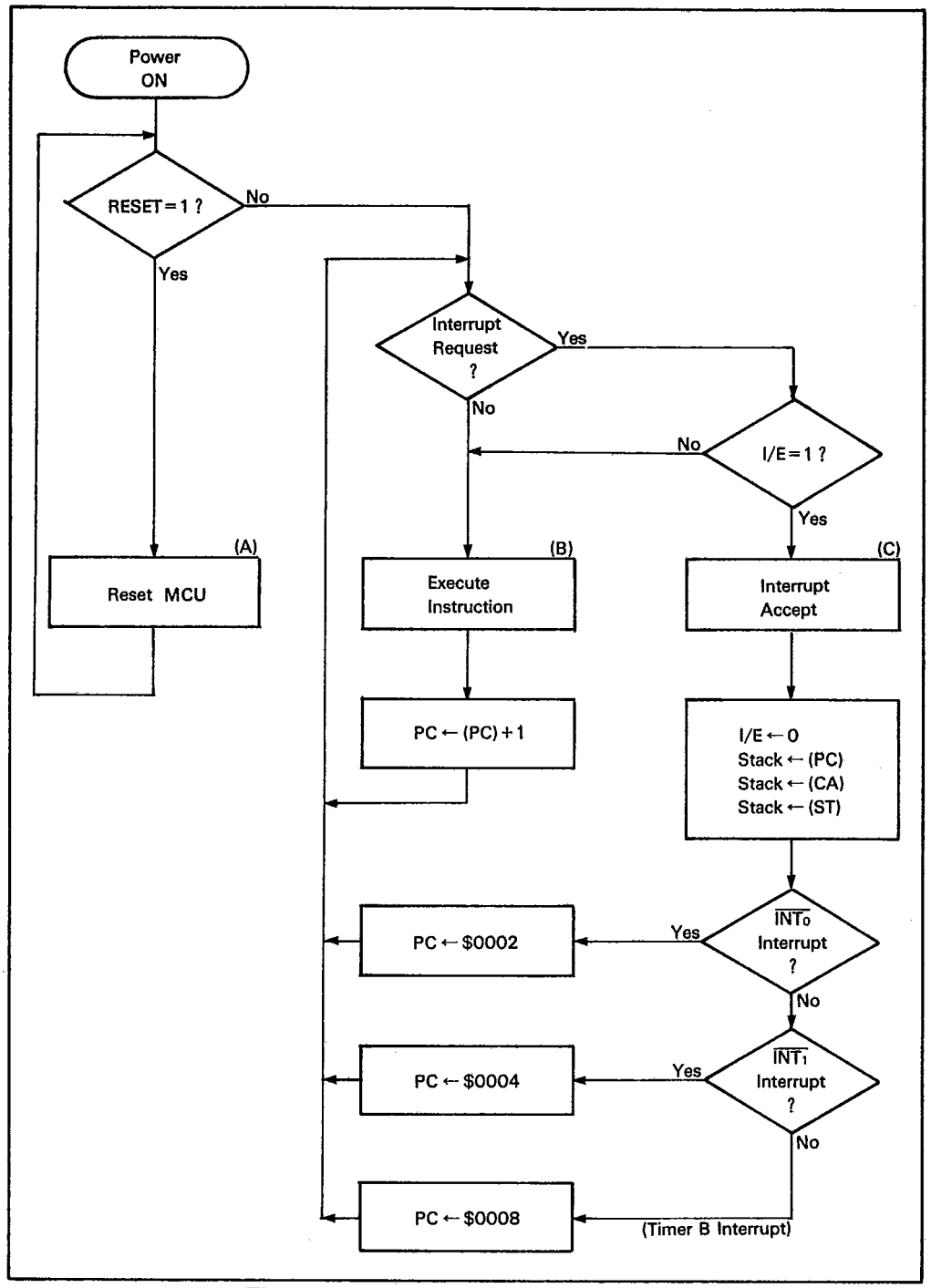


Figure 8. Interrupt Servicing Flowchart

Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to $000 by MCU reset, and it starts to count up the system clock signal as soon as the RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $R3_3/\overline{INT_1}$ as $\overline{INT_1}$ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to $FF, it will generate an overflow output. Then case, if the auto-reload function is selected, timer B is initialized to the value of the timer load register. If it is not selected, timer B goes to $00. The timer B interrupt request flag (IFTB: $002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: $009): The 4-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B) (figure 2).

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then

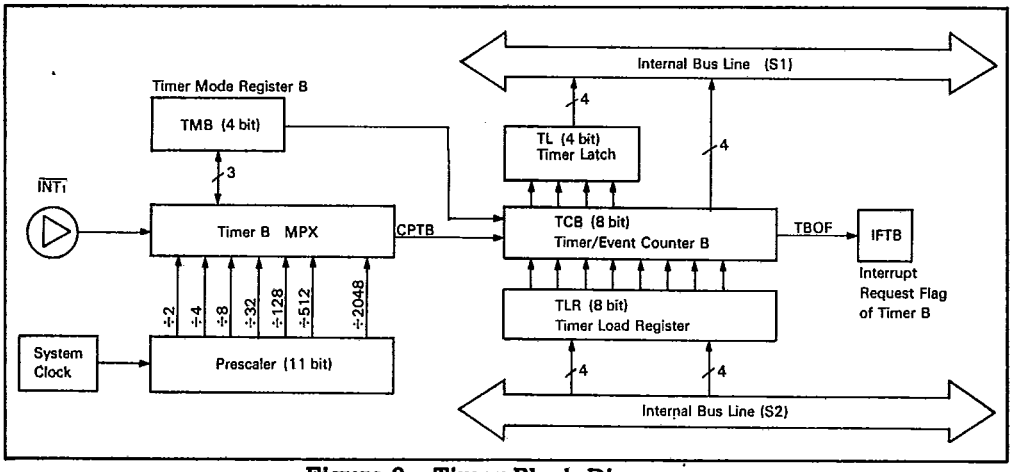


Figure 9. Timer Block Diagram

the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer B Interrupt Request Flag (IFTB: $002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: $002 bit 1): The timer B Interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT_1}$ (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

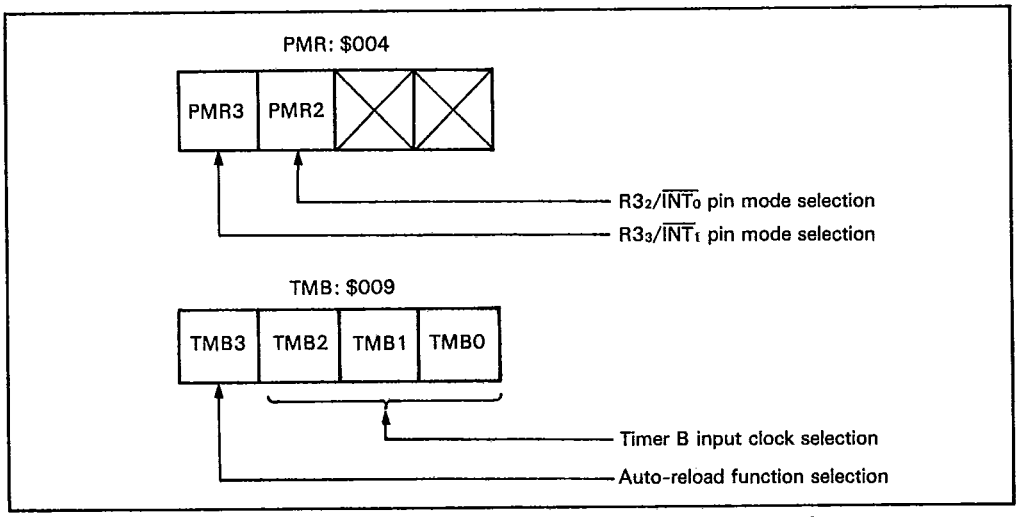


Figure 10. Mode Register Configuration and Function

Input/Output

The MCU has 36 I/O pins, 12 standard and 24 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain). One of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_1/V_{disp} pin via mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 10 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 11.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in Figure 11 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0 , a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D port I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 as for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The six R ports in the HMCS414 are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read from the output-only and/or non-existing ports.

The $R3_2$ and $R3_3$ pins are multiplexed with the $\overline{INT_0}$ and $\overline{INT_1}$ pins respectively. See table 10 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-up MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 12 shows the parts initialized by MCU reset, and the status of each. Table 13 shows how registers recover from stop mode.

Table 10. I/O Pin Circuit Types

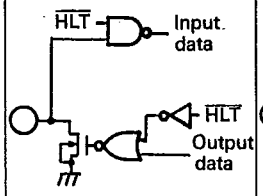
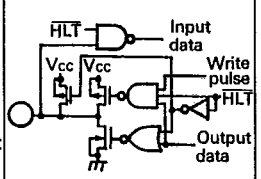
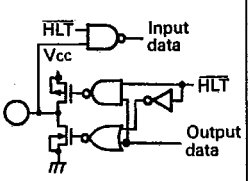
		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable pins
Standard Pins	I/O Common Pins				$D_0 - D_3$ $R3_0 - R3_3$ $R4_0 - R4_3$

Table 10. I/O Pin Circuit Types (Cont)

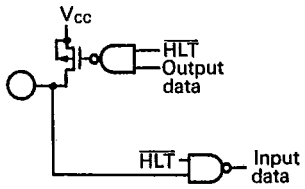
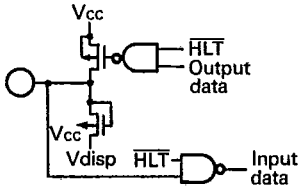
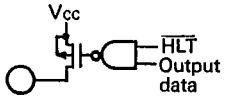
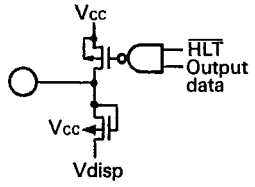
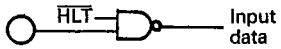
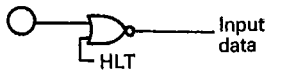
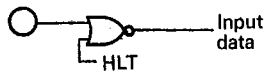
		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applicable pins
High Voltage Pins	I/O Common Pins			$D_4 - D_{14}$ $R1_0 - R1_3$ $R2_0 - R2_3$
	Output Pins			$RO_0 - RO_3$
	Input Pins			RA_1

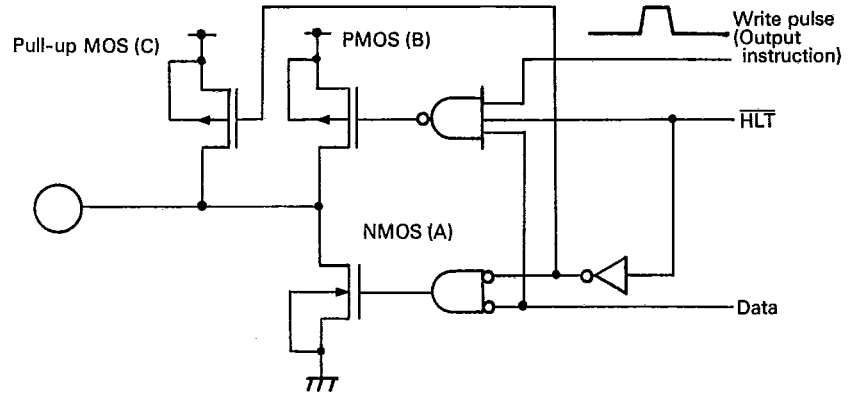
Table 10. I/O Pin Circuit Types (Cont)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applicable pins
Standard Pins	Input Pins			$\overline{INT_0}$ $\overline{INT_1}$

Note: In the stop mode, $\overline{HLT}$ signal is 0, HLT signal is 1 and I/O pins are in high impedance state.

Table 11. Data Input from Input/Output Common Pins T-49-19-04

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0



MOS Buffer	On Resistance Value	
	HMCS412C, HMCS412AC	HMCS412CL
A	approx. 250 Ω	approx. 1 kΩ
B	approx. 1 kΩ	approx. 1.7 kΩ
C	approx. 30 kΩ to 160 kΩ (V_{cc} = 5 V)	approx. 60 kΩ to 1 MΩ (V_{cc} = 3 V) approx. 30 kΩ to 160 kΩ (V_{cc} = 5 V)

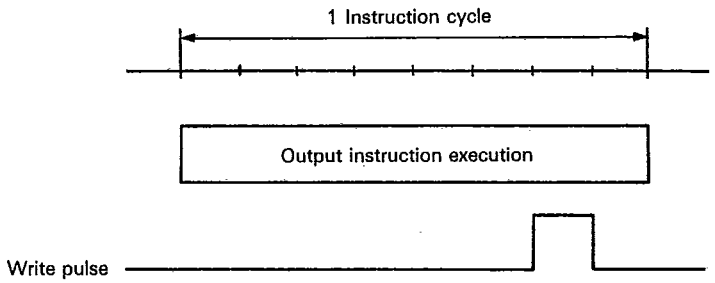


Figure 11. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Table 12. Initial Value After MCU Reset

Items			Initial Value by MCU Reset	Contents
Program Counter (PC)			$0000	Execute program from the top of ROM address
Status (ST)			1	Enable to branch with conditional branch instructions
Stack Pointer (SP)			$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin	(A) Without Pull-Up MOS	1	Enable input
		(B) With Pull-Up MOS	1	Enable input
		(C) CMOS	1	—
	High Voltage Pin	(D) Without Pull-Down MOS	0	Enable input
		(E) With Pull-Down MOS	0	Enable input
Interrupt Flag	Interrupt Enable Flag (I/E)		0	Inhibit all interrupts
	Interrupt Request Flag (IF)		0	No interrupt request
	Interrupt Mask (IM)		1	Mask interrupt request
Mode Register	Port Mode Register (PMR)		0000	See port mode register
	Timer Mode Register B (TMB)		0000	See timer mode register B
Timer/Counter	Prescaler		$000	—
	Timer/Event Counter B (TCB)		$00	—
	Timer Load Register (TLR)		$00	—

Table 13. Initial Value after Stop Reset

Item		After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop Mode)
Carry	(CA)	The contents of the items before MCU reset are not retained.	
Accumulator	(A)	It is necessary to initialize them by software.	
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. Through mask option, either crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table 15 for selection of the type. In addition, see figure 13 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available. Three divide ratios, 1/16, 1/8, and 1/4, are selectable via mask option (table 14).

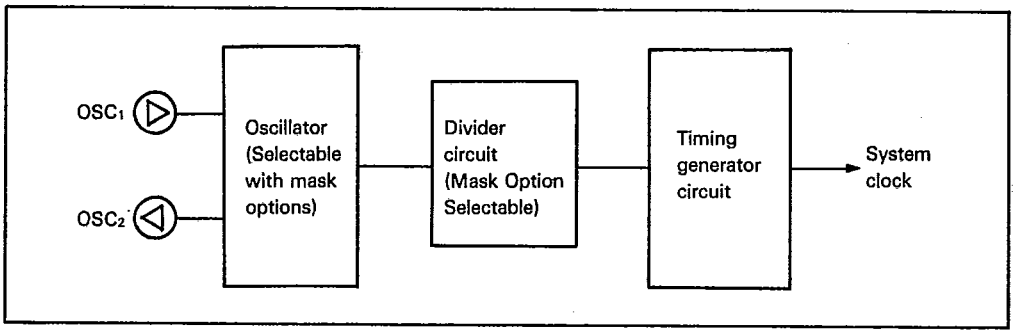


Figure 12. Internal Oscillator Circuit

Table 14. Internal Oscillation Circuit Mask Option

		HMCS 412C	HMCS 412CL	HMCS 412AC
Divider	1/16	—	○	—
	1/8	○	○	—
	1/4	○	—	○
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○

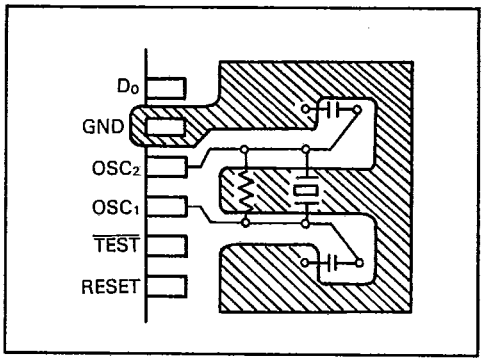
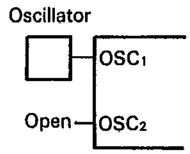
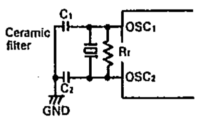
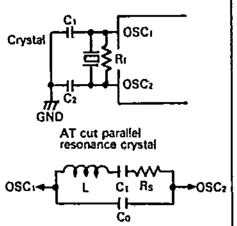
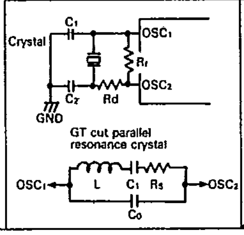


Figure 13. Layout of Crystal and Ceramic Filter

Table 15. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants		
		HMCS412C	HMCS412CL	HMCS412AC
External Clock Operation				
Ceramic Filter Oscillator		Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%	Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%	Ceramic filter CSA4.00MG (Murata) R_f: 1 MΩ ± 20% C_1: 30 pF ± 20% C_2: 30 pF ± 20%
Crystal Oscillator		R_f: 1 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: equivalent to circuit shown C_0: 7 pF max. R_s: 100 Ω max. f : 1.0–4.5 MHz	R_f: 1 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: equivalent to circuit shown C_0: 7 pF max. R_s: 100 Ω max. f : 1.0–4.5 MHz	R_f: 1 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: equivalent to circuit shown C_0: 7 pF max. R_s: 100 Ω max. f : 1.0–4.5 MHz
			R_f: 2 MΩ ± 20% C_1: 10-22 pF ± 20% C_2: 10-22 pF ± 20% Crystal: equivalent to circuit shown C_0: 7 pF max. R_s: 100 Ω max. f : 1.0–2.25 MHz	

Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.

2. Wiring between OSC_1, OSC_2, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 13).

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Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 16). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 16. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Input/ Output Pin	Timer/ Counter	Recovery Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained (Note 3)	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET (Note 1)	Stop	Retained	High impedance (Note 2)	Stop	RESET input

Notes:
1. The MCU recovers from STOP mode by RESET input. Refer to table 13 for the contents of the flags and registers.
2. A high-voltage pin with a pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is in addition to the current dissipation in stop mode (I_{stop}).
3. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is in addition to the current dissipation in standby mode.

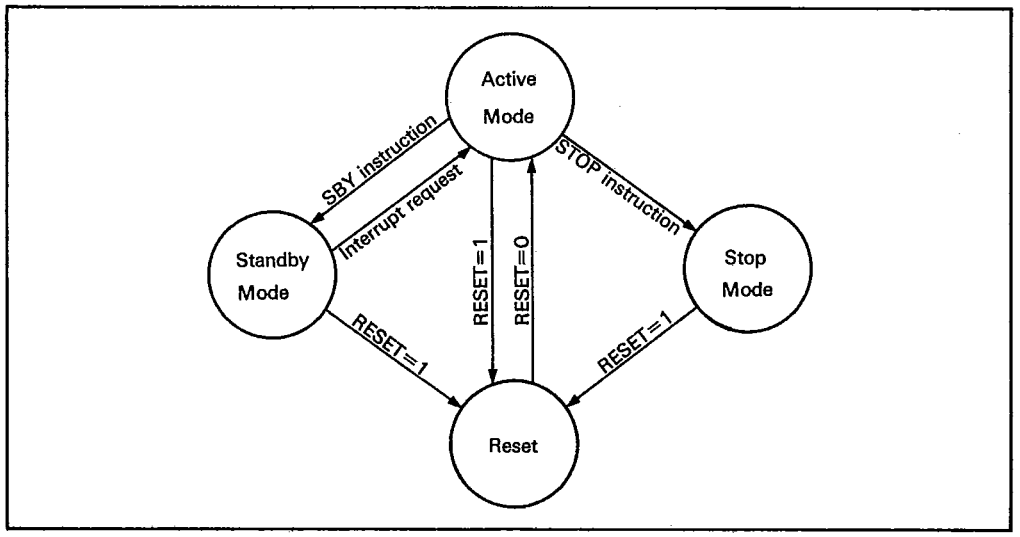

Figure 14. MCU Operation Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 15 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

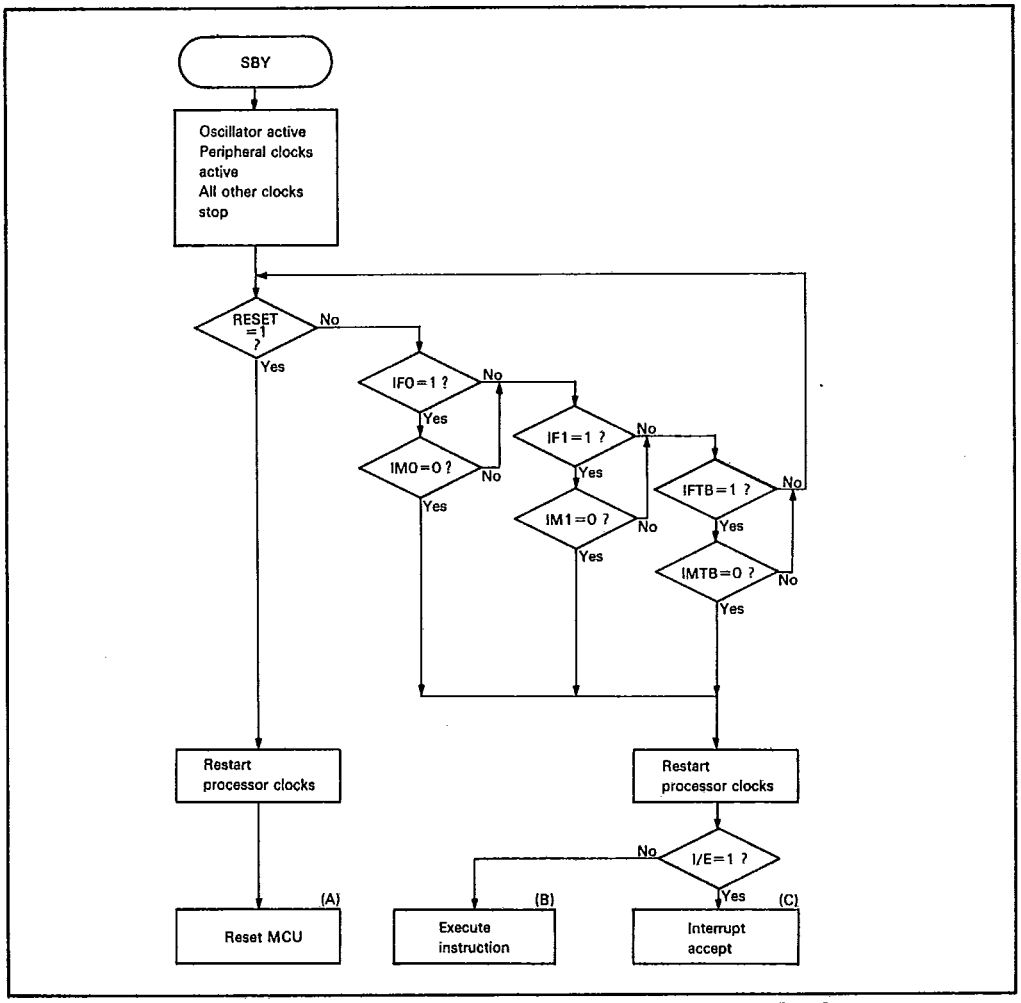

Figure 15. MCU Operating Flowchart in Standby Mode

RAM Addressing Mode

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from $020 to $02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 18.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address $0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 19), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at $0000-$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low- order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 20). When bit 8 in the ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

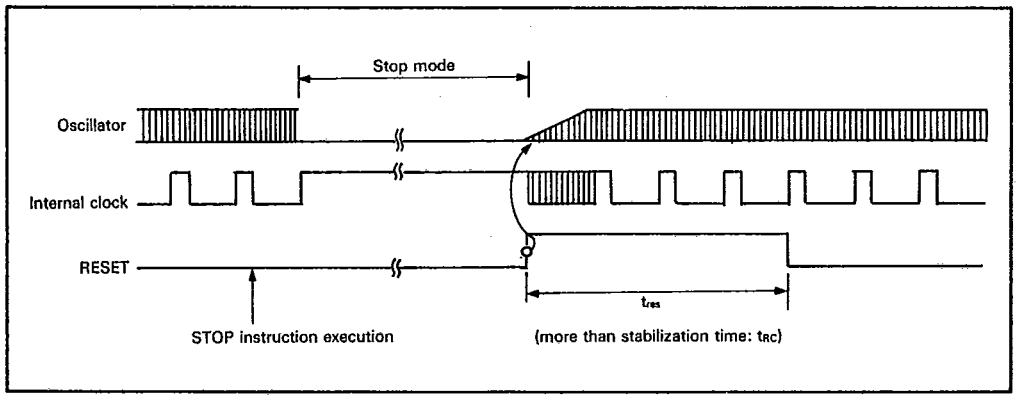

Figure 16. Timing Chart of Recovering from Stop Mode

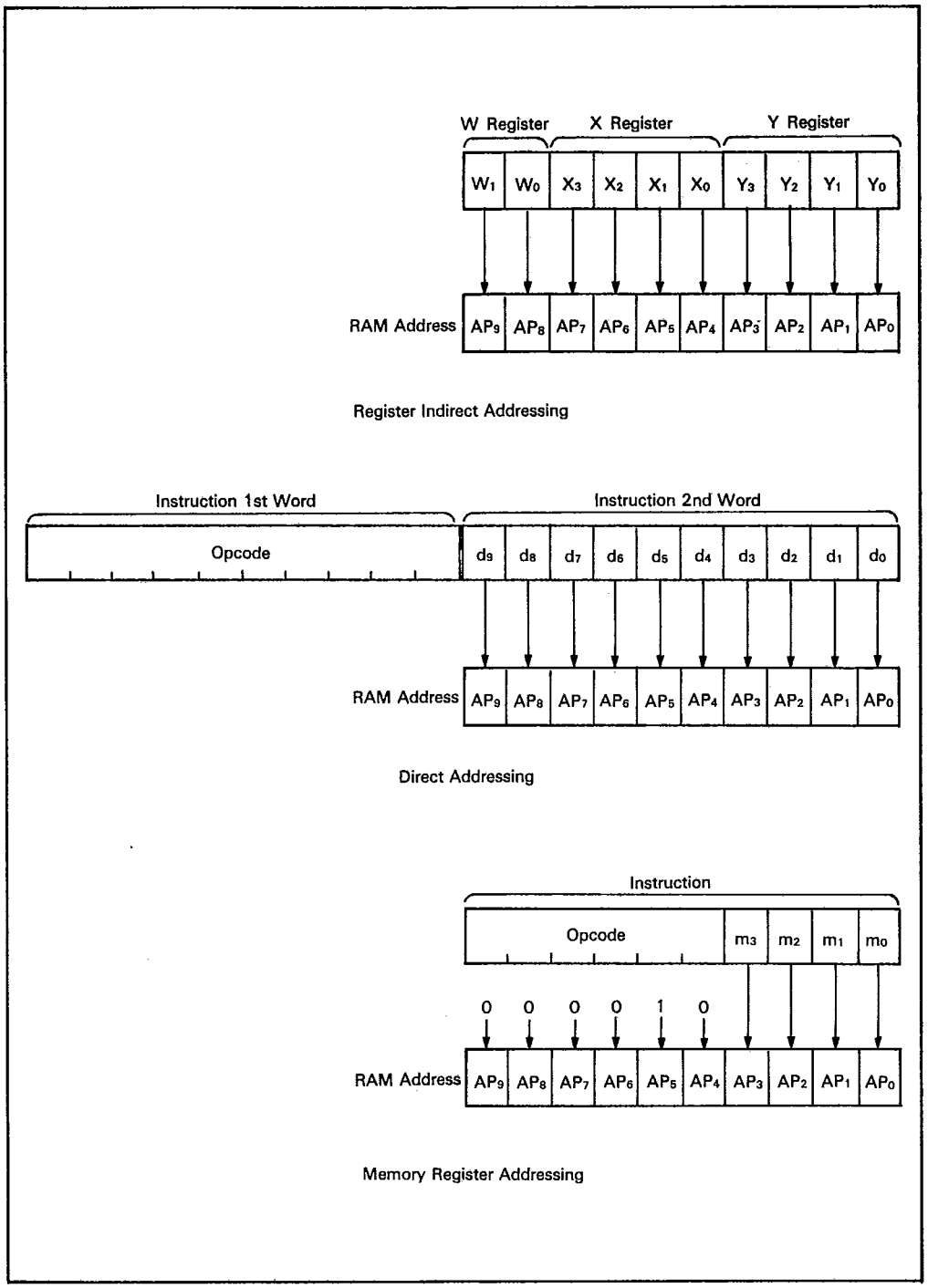

Figure 17. RAM Addressing Mode

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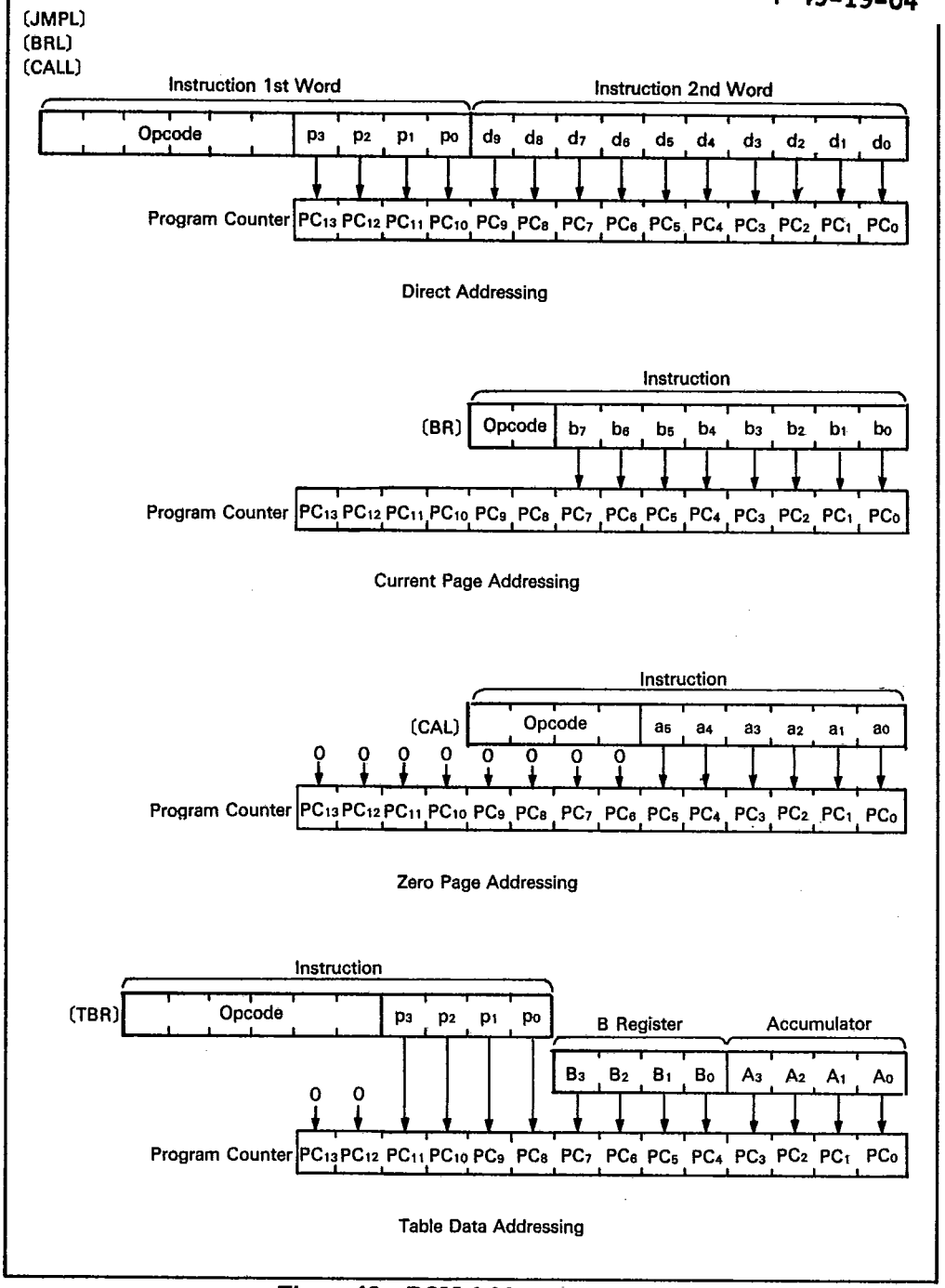

Figure 18. ROM Addressing Mode

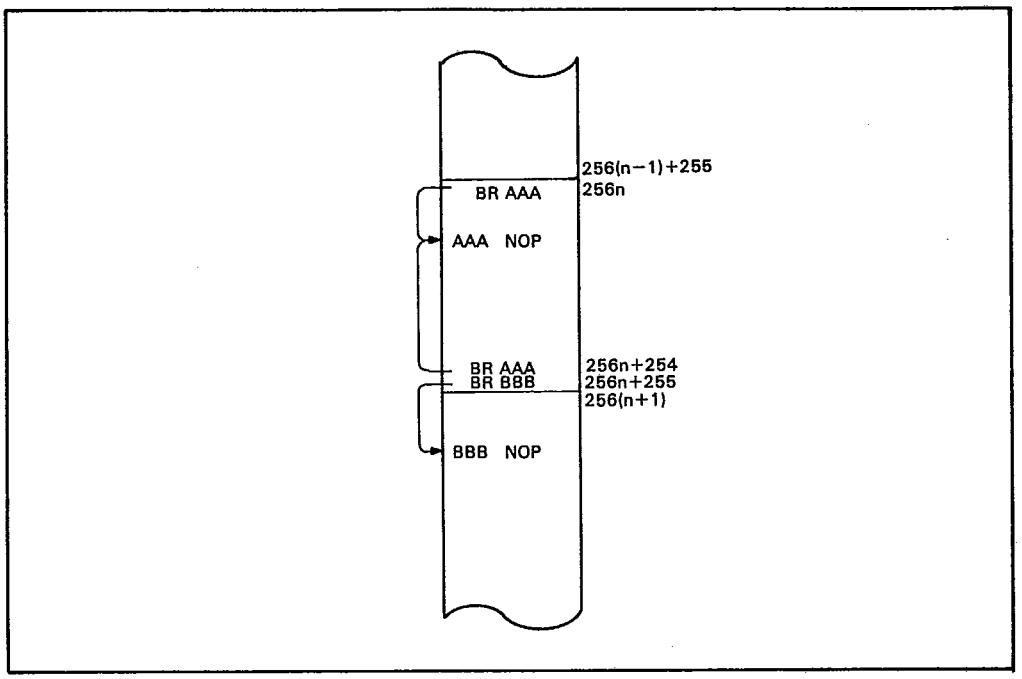

Figure 19. BR Instruction Branch Destination on Pages Boundary

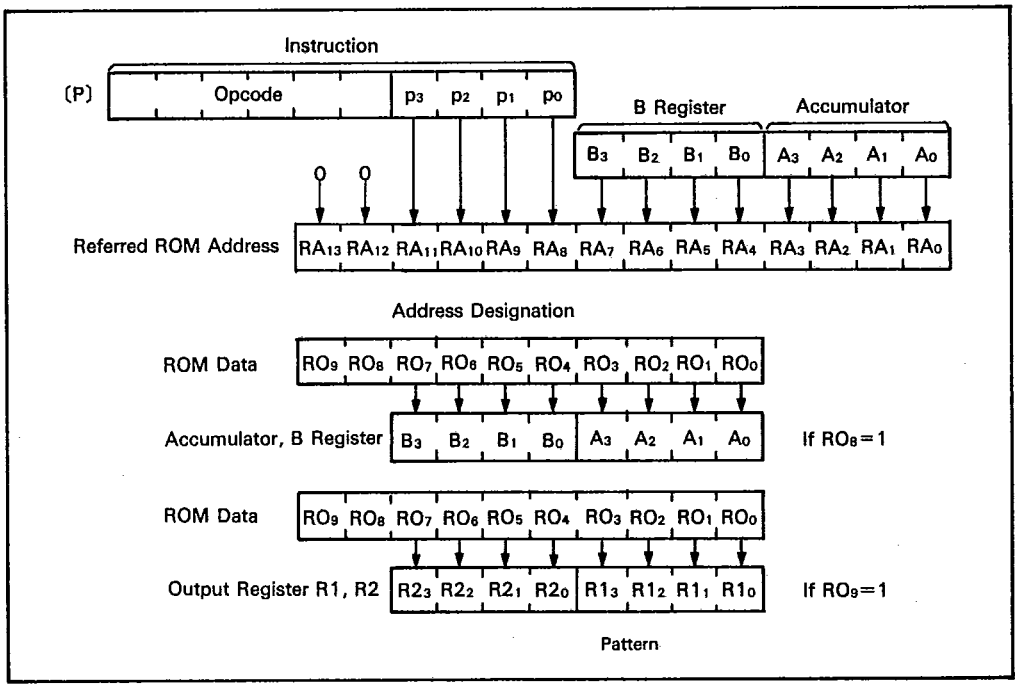

Figure 20. P Instruction

Instruction Set

T-49-19-04

The HMCS412C/CL/AC provide 98 instructions which are classified into 10 groups as follows:

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 17-26 list their functions, and table 27 is an opcode map.

Table 17. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	i→M, Y+1→Y	NZ	1/1

Table 18. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B · A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A · B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y · A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX · A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY · A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	MR(m) · A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	MR(m) ↔ A		1/1

Table 19. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	i → Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y−1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y−A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX, Y↔SPY		1/1

Table 20. RAM Register Instructions T-49-19-04

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X↔SPX, Y↔SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X↔SPX, Y↔SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X↔SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y−1→Y (X↔SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X↔SPX, Y↔SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X↔SPX, Y↔SPY)		1/1

Note: (XY)and (X) have the following meaning:

(1)The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X↔SPX, Y↔SPY

(2)The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 21. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i_3 i_2 i_1 i_0	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B−1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}$+1 →A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B}$ → B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M−A−$\overline{CA}$→A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	M−A−$\overline{CA}$→A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B→A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M→A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∩ M→A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M→A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ∪ M→A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M→A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ⊕ M→A	NZ	2/2

Note: ∩ : Logical AND
∪ : Logical OR
⊕ : Exclusive OR

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Table 22. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	A ≦ i	NB	1/1

Table 23. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	0 →M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 24. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a_5 a_4 a_3 a_2 a_1 a_0		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p_3 p_2 p_1 p_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p_3 p_2 p_1 p_0			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 →I/E CA Restore	ST	1/3

Table 25. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m_3 m_2 m_1 m_0	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m_3 m_2 m_1 m_0	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m_3 m_2 m_1 m_0		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m_3 m_2 m_1 m_0	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m_3 m_2 m_1 m_0	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m_3 m_2 m_1 m_0	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m_3 m_2 m_1 m_0	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p_3 p_2 p_1 p_0			1/2

Table 26. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: HMCS412 has no serial interface, so STS (start serial) operates the same as NOP.

Table 27. Opcode Map

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R9 \ R8		0																1													
H \ L		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSPX	XSPX	XSPY	XSP XY	AN EM			AM				ORM								AMEMD				AMD				ORMD			
	1	RTN	RTNI			ALEM				AMC				EORM								ALEMD				AMCD				EORMD			
	2	INEM i(4)																INEMD i(4)															
	3	ILEM i(4)																ILEMD i(4)															
	4	LBM(XY)				BNEM				LAB				IB				COMB				OR								SBY	STOP		
	5	LMAIY(X)				AYY				LASPY				IY				JMPL p(4)															
	6	NEGA				RED				LASPX							TC	CALL p(4)															
	7	YNEI i(4)																BRL p(4)															
	8	XMA(XY)				SEM n(2)				REM n(2)				TM n(2)				XMWD				SEMD n(2)				REMD n(2)				TMD n(2)			
	9	LAM(XY)				LMA(XY)				SMC				ANM				LAMD				LMAD				SMCD				ANMD			
	A	ROTR	ROTL					DAA				DAS					LAY	LMID i(4)															
	B	TBR p(4)																P p(4)															
	C	XMB(XY)				BLEM				LBA							DB	CAL a(6)															
	D	LMADY(X)				SYY				LYA							DY																
	E	TD				SED				LXA				REC			SEC																
	F	LWI i(2)																															
1	0	LBI i(4)																BR b(8)															
	1	LYI i(4)																															
	2	LXI i(4)																															
	3	LAI i(4)																															
	4	LBR m(4)																															
	5	LAR m(4)																															
	6	REDD m(4)																															
	7	LAMR m(4)																															
	8	AI i(4)																															
	9	LMIIY i(4)																															
	A	TDD m(4)																															
	B	ALEI i(4)																															
	C	LRB m(4)																															
	D	LRA m(4)																															
	E	SEDD m(4)																															
	F	XMRA m(4)																															

1-word/2-cycle Instruction

1-word/3-cycle Instruction

RAM Direct Address Instruction (2-word/2-cycle)

2-word/2-cycle Instruction

Absolute Maximum Ratings

Item	Symbol	Value		Unit	Note
Supply Voltage	V_{CC}	− 0.3 to + 7.0		V	
Terminal Voltage	V_T	− 0.3 to V_{CC} + 0.3		V	3
		V_{CC} − 45 to V_{CC} + 0.3		V	4
Total Allowance of Input Current	ΣI_O	25		mA	5
Maximum Input Current	I_O	15		mA	7, 8
Maximum Output Current	$-I_O$	4	(2)	mA	9, 10, 13
		6	(3)	mA	9, 11, 13
		30	(15)	mA	9, 12, 13
Total Allowance of Output Current	$-\Sigma I_O$	85	(100)	mA	6, 13
Operating Temperature	T_{opr}	− 20 to + 75		°C	
Storage Temperature	T_{stg}	− 55 to + 125		°C	

Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
3. Standard pins.
4. High-voltage pins.
5. Total allowance of input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total allowance of output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. D_0−D_3, R3 and R4.
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. D_0−D_3, R3 and R4.
11. R0−R2.
12. D_4−D_{15}.
13. $-\Sigma I_O$ = 100 mA if $-I_O$ is equal to or less than 2 mA, 3 mA, or 15 mA.

Electrical Characteristics

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DC Characteristics

**(GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to + 75°C,
HMCS412C: V_{CC} = 3.5 V to 6 V,
HMCS412CL: V_{CC} = 2.5 V to 6 V,
HMCS412AC: V_{CC} = 4.5 V to 6 V)**

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	0.8 V_{CC}	V_{CC} + 0.3	V		
		OSC_1	V_{CC} − 0.5	V_{CC} + 0.3	V	HMCS412C/AC	
			V_{CC} − 0.3	V_{CC} + 0.3	V	HMCS412CL	
Input Low Voltage	V_{IL}	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$	−0.3	0.2 V_{CC}	V		
		OSC_1	−0.3	0.5	V	HMCS412C/AC	
			−0.3	0.3	V	HMCS412CL	
Input/Output Leakage Current	$\|I_{IL}\|$	RESET, $R3_2/\overline{INT_0}$, $R3_3/\overline{INT_1}$, OSC_1		1	μA	V_{in} = 0 V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		1.8	mA	HMCS412C; V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 8, or f_{osc} = 2 MHz, ÷ 4	2,5
				0.8	mA	HMCS412CL; V_{CC} = 3 V; f_{osc} = 4 MHz, ÷ 16, or f_{osc} = 2 MHz, ÷ 8	2,5
				3.0	mA	HMCS412AC; V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 4	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		1.0	mA	HMCS412C; V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 8, or f_{osc} = 2 MHz, ÷ 4	3,5
				0.5	mA	HMCS412CL; V_{CC} = 3 V; f_{osc} = 4 MHz, ÷ 16, or f_{osc} = 2 MHz, ÷ 8	3,5
				1.4	mA	HMCS412AC; V_{CC} = 5 V; f_{osc} = 4 MHz, ÷ 4	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		10	μA	$V_{in}(\overline{TEST})$ = V_{CC} − 0.3 V to V_{CC}; V_{CC}, V_{in}(RESET) = 0 V to 3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

Notes: 1. Excluding pull-up MOS current and output buffer current.

Notes: 2. The MCU is in the reset state. Input/output current does not flow.
- MCU in reset state, operation mode
- RESET, $\overline{TEST}$: V_{CC}
- D_0-D_3, R3, R4: V_{CC}
- D_4-D_{14}, R0-R2, RA_1: V_{disp}

3. The timer/counter operates with the fastest clock. Input/output current does not flow.
- MCU in standby mode
- Input/output in reset state
- RESET: GND
- $\overline{TEST}$: V_{CC}
- D_0-D_3, R3, R4: V_{CC}
- D_4-D_{14}, R0-R2, RA_1: V_{disp}

4. Excluding pull-down MOS current.
5. When f_{osc} = x MHz, estimate the current dissipation as follows:
HMCS412C/AC; Max value @ x MHz = x/4 × (max value @ 4 MHz)
HMCS412CL; Max value @ x MHz = x/2 × (max value @ 2 MHz)

Input/Output Characteristics for Standard Pins

($GND = 0$ V, $V_{disp} = V_{CC} - 40$ V to V_{CC}, $T_a = -20°C$ to $+75°C$,
HMCS412C: $V_{CC} = 3.5$ V to 6 V,
HMCS412CL: $V_{CC} = 2.5$ V to 6 V,
HMCS412AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_0-D_3, $R3_0$, $R3_1$, R4	0.7 V_{CC}		V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_0-D_3, $R3_0$, $R3_1$, R4	−0.3		0.3V_{CC}	V		
Output High Voltage	V_{OH}	D_0-D_3, $R3_0$, $R3_1$, R4	V_{CC} − 1.0			V	HMCS412C/AC; $-I_{OH}$ = 1.0 mA	1
		D_0-D_3, $R3_0$, $R3_1$, R4	V_{CC} − 0.5			V	HMCS412C/AC; $-I_{OH}$ = 0.5 mA HMCS412CL; $-I_{OH}$ = 0.3 mA	1
Output Low Voltage	V_{OL}	D_0-D_3, $R3_0$, $R3_1$, R4			0.4	V	HMCS412C/AC; I_{OL} = 1.6 mA HMCS412CL; I_{OH} = 0.4 mA	
Input/Output Leakage Current	$\|I_{IL}\|$	D_0-D_3, $R3_0$, $R3_1$, R4			1	μA	V_{in} = 0 V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D_0-D_3, $R3_0$, $R3_1$, R4	30	60	150	μA	V_{CC} = 5 V, V_{in} = 0 V	3
		D_0-D_3, $R3_0$, $R3_1$, R4	3	15	50	μA	HMCS412CL only; V_{CC} = 3 V, V_{in} = 0 V	3

Notes: 1. I/O pins with CMOS output selected by mask option.
2. Pull-up MOS current and output buffer current are excluded.
3. I/O pins with pull-up MOS selected by mask option.

Input/Output Characteristics for High-Voltage Pins

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**(GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to +75°C,
HMCS412C: V_{CC} = 3.5 V to 6 V,
HMCS412CL: V_{CC} = 2.5 V to 6 V,
HMCS412AC: V_{CC} = 4.5 V to 6 V)**

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D_4-D_{14}, R1, R2, RA_1	0.7 V_{CC}		V_{CC} + 0.3	V		
Input Low Voltage	V_{IL}	D_4-D_{14}, R1, R2, RA_1	V_{CC} − 40		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D_4-D_{14}	V_{CC} − 3.0			V	− I_{OH}=15 mA, HMCS412C/CL; V_{CC} = 5 V ± 20% HMCS412AC; V_{CC} = 4.5 V to 6 V	
			V_{CC} − 2.0			V	− I_{OH}=10 mA, HMCS412C/CL; V_{CC} = 5 V ± 20% HMCS412AC; V_{CC} = 4.5 V to 6 V	
			V_{CC} − 1.0			V	HMCS412C/AC; − I_{OH}= 4 mA HMCS412CL; − I_{OH} = 2.5 mA	
		R0-R2	V_{CC} − 3.0			V	− I_{OH} = 3 mA, HMCS412C/CL; V_{CC} = 5 V ± 20% HMCS412AC; V_{CC} = 4.5 V to 6 V	
			V_{CC} − 2.0			V	− I_{OH} = 2 mA, HMCS412C/CL; V_{CC} = 5 V ± 20% HMCS412AC; V_{CC} = 4.5 V to 6 V	
			V_{CC} − 1.0			V	HMCS412C/AC; − I_{OH} = 0.8 mA HMCS412CL; − I_{OH} = 0.5 mA	
Output Low Voltage	V_{OL}	D_4-D_{14}, R0-R2			V_{CC} − 37	V	V_{disp} = V_{CC} − 40 V	1
		D_4-D_{14}, R0-R2			V_{CC} − 37	V	150kΩ to V_{CC} − 40V	2
Input/Output Leakage Current	$\|I_{IL}\|$	D_4-D_{14}, R0-R2, RA_1			20	μA	V_{in} = V_{CC} − 40 V to V_{CC}	3
Pull-Down MOS Current	I_d	D_4-D_{14}, R0-R2, RA_1	125	250	600	μA	V_{disp} = V_{CC} − 35 V, V_{in} = V_{CC}	4

Notes:
1. I/O pins with pull-down MOS selected by mask option.
2. I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
3. Pull-down MOS current and output buffer current are excluded.
4. I/O pins with pull-down MOS selected by mask option.

AC Characteristics

**(GND = 0 V, V_{disp} = V_{CC} − 40 V to V_{CC}, T_a = −20°C to +75°C,
HMCS412C: V_{CC} = 3.5 V to 6 V,
HMCS412CL: V_{CC} = 2.5 V to 6 V,
HMCS412AC: V_{CC} = 4.5 V to 6 V)**

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC_1, OSC_2	0.4	4	4.5	MHz	HMCS412C; divide by 8	
			0.2	2	2.25	MHz	HMCS412C; divide by 4	
			0.8	4	4.5	MHz	HMCS412CL; divide by 16	
			0.4	2	2.25	MHz	HMCS412CL; divide by 8	
			0.2	4	4.5	MHz	HMCS412AC; divide by 4	
Instruction Cycle Time	t_{cyc}		1.78	2	20	µs	HMCS412C	
			3.55	4	20	µs	HMCS412CL	
			0.89	1	20	µs	HMCS412AC	
Oscillator Stabilization Time	t_{RC}	OSC_1, OSC_2			20	ms	HMCS412C/AC	1
					60	ms	HMCS412CL	1
External Clock High, Low Level Width	t_{CPH}, t_{CPL}	OSC_1	92			ns	HMCS412C; divide by 8 HMCS412CL; divide by 16 HMCS412AC; divide by 4	2
			203			ns	HMCS412C; divide by 4 HMCS412CL; divide by 8	2

(continued)

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AC Characteristics (Cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External Clock Rise Time	t_{CPr}	OSC_1			20	ns		2
External Clock Fall Time	t_{CPf}	OSC_1			20	ns		2
$\overline{INT_0}$ High Level Width	t_{I0H}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_0}$ Low Level Width	t_{I0L}	$\overline{INT_0}$	2			t_{cyc}		3
$\overline{INT_1}$ High Level Width	t_{I1H}	$\overline{INT_1}$	2			t_{cyc}		3
$\overline{INT_1}$ Low Level Width	t_{I1L}	$\overline{INT_1}$	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	f = 1 MHz, V_{in} = 0 V	
RESET Fall Time	t_{RSTf}				20	ms	HMCS412C/AC	4
					15	ms	HMCS412CL	4

Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (HMCS412C; 3.5 V, HMCS412CL; 2.5 V, HMCS412AC; 4.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 21.)
2. See figure 22.
3. See figure 23.
4. See figure 24.

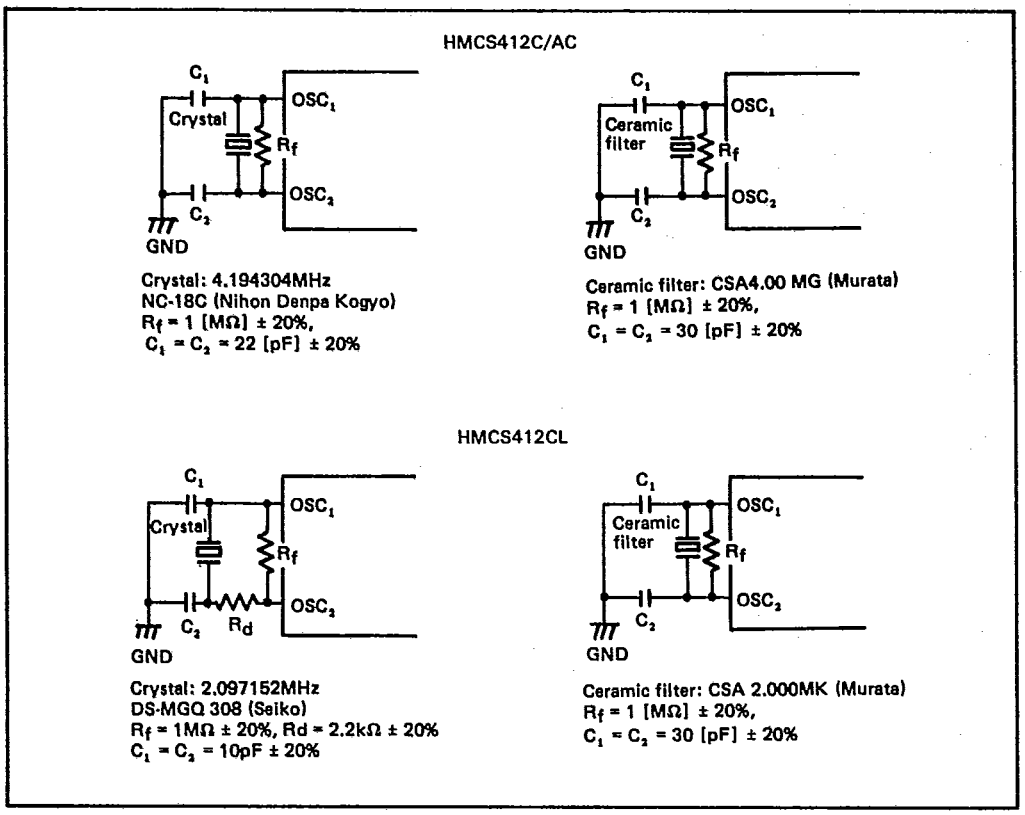

Figure 21. Oscillation Circuit

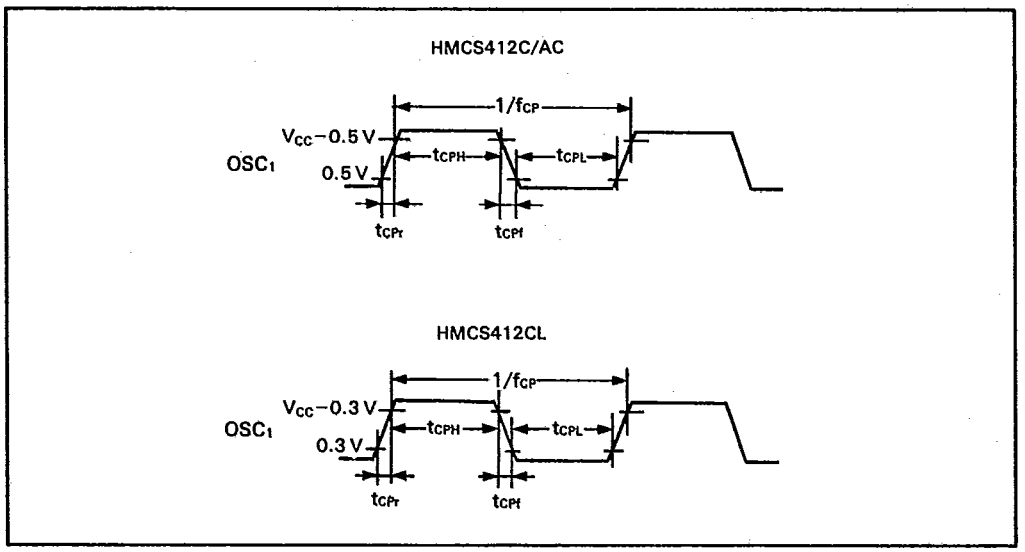

Figure 22. Oscillator Timing

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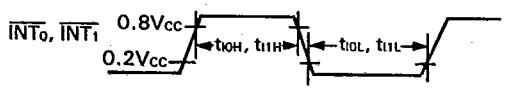

Figure 23. Interrupt Timing

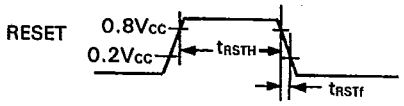

Figure 24. Reset Timing

HMCS412C/HMCS412CL/HMCS412AC

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HMCS412C/CL/AC Mask Option List

• Please enter check marks in ☐ (■, x, ✓).

5V Operation:	☐ HMCS412C
3V Operation:	☐ HMCS412CL
High Speed Operation:	☐ HMCS412AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

(1) I/O Option

Please enter 0 in applicable item to select I/O option.
A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
C: CMOS (cannot be used as input)
D: Without Pull-down MOS (PMOS Open Drain) E: With Pull-down MOS

Note: I/O options masked by ▨ are not available.

Pin		Input/Output	I/O Option A	B	C	D	E
D_0	Standard Pins	Input/Output				▨	▨
D_1		Input/Output				▨	▨
D_2		Input/Output				▨	▨
D_3		Input/Output				▨	▨
D_4	High Voltage Pins	Input/Output	▨	▨	▨		
D_5		Input/Output	▨	▨	▨		
D_6		Input/Output	▨	▨	▨		
D_7		Input/Output	▨	▨	▨		
D_8		Input/Output	▨	▨	▨		
D_9		Input/Output	▨	▨	▨		
D_{10}		Input/Output	▨	▨	▨		
D_{11}		Input/Output	▨	▨	▨		
D_{12}		Input/Output	▨	▨	▨		
D_{13}		Input/Output	▨	▨	▨		
D_{14}		Input/Output	▨	▨	▨		

Pin		Input/Output	I/O Option A	B	C	D	E
R0	$R0_0$	Output	▨	▨	▨		
	$R0_1$	Output	▨	▨	▨		
	$R0_2$	Output	▨	▨	▨		
	$R0_3$	Output	▨	▨	▨		
R1	$R1_0$	Input/Output	▨	▨	▨		
	$R1_1$	Input/Output	▨	▨	▨		
	$R1_2$	Input/Output	▨	▨	▨		
	$R1_3$	Input/Output	▨	▨	▨		
R2	$R2_0$	Input/Output	▨	▨	▨		
	$R2_1$	Input/Output	▨	▨	▨		
	$R2_2$	Input/Output	▨	▨	▨		
	$R2_3$	Input/Output	▨	▨	▨		
R3	$R3_0$	Input/Output				▨	▨
	$R3_1$	Input/Output				▨	▨
	$R3_2$	Input/Output				▨	▨
	$R3_3$	Input/Output				▨	▨
R4	$R4_0$	Input/Output				▨	▨
	$R4_1$	Input/Output				▨	▨
	$R4_2$	Input/Output				▨	▨
	$R4_3$	Input/Output				▨	▨
RA	RA_1	Input	Please Mark as RA_1/V_{disp}				

High Voltage Pins: R0, R1, R2
Standard Pins: R3, R4
High Voltage Pin: RA_1

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(2) RA_1/V_{disp}

Please check (■, X, ✓) applicable item.

RA_1/V_{disp}
☐ RA_1: Without Pull-down MOS (D)
☐ V_{disp}

Note: RA_1/V_{disp} has to be selected as V_{disp} pin exept the case that all high pins are option D.

(3) Divider (Div)

Please check (■, X, ✓) applicable item.

Divider	HMCS412C	HMCS412CL	HMCS412AC
16		☐	
8	☐	☐	
4	☐		☐

(4) ROM Code Media

Please check (■, X, ✓) applicable item.

ROM Code Media
☐ EPROM: Emulator Type
☐ EPROM: EPROM On-Package Microcomputer Type

(5) Oscillator (CPG option)

Please check (■, X, ✓) applicable item.

CPG option	☐ HMCS 412C (5V Operation)	☐ HMCS412CL (3V Operation)	☐ HMCS412AC (High Speed Operation)
	☐ Ceramic Filter	☐ Ceramic Filter	☐ Ceramic Filter
	☐ Crystal	☐ Crystal	☐ Crystal
	☐ External Clock	☐ External Clock	☐ External Clock