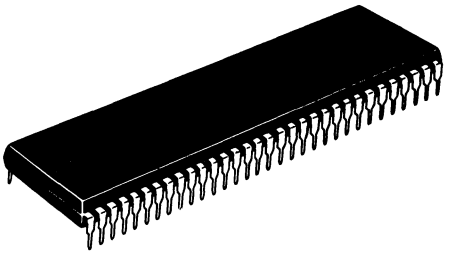
HD63084

DIPP (Document Image Pre-Processor)

—PRELIMINARY—

The HD63084 (DIPP) is an document image processor used as a peripheral of a microcomputer. It reads analog image signals that have been photoelectrically converted by CCD line sensors or other optical devices, corrects the shading distortion of the signals, then converts the signals to digital form.

HD63084P

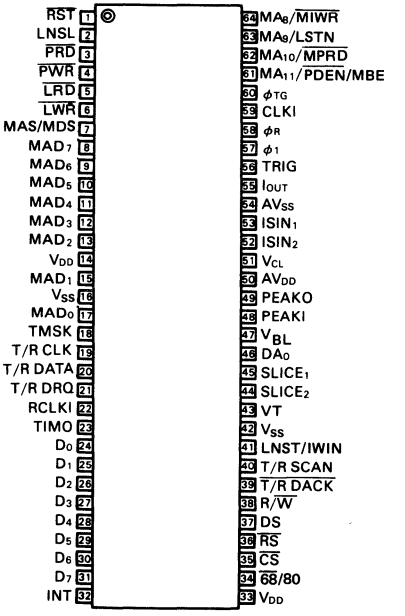


(DP-64S)

■ FEATURES

- High speed reading of image signals
  - 5M pixel/sec (at input clock frequency of 10 MHz)
- Highly accurate processing of image signals
  - Peak level of image signals, 0.1V ~ 2.0V
  - Built-in 8-bit peak value detection circuit
  - Built-in 7-bit successive approximation pixel A/D and D/A converter
  - Built-in 4-bit flash-type A/D converter
- Various output modes
  - Binary data output mode
  - Dithered data output mode (Programmable dithered pattern of 16 pixel x 16 pixel)
  - 4-bit coded data mode (16 gradations)
- Automatic judgement of horizontal and vertical resolutions
- Interfaceable with either Motorola type or Intel type MPU
- Programmable magnification and reduction rates
  - Reduction of read image signal
    : 0.125 ~ 1 times (about 1000 gradations)
  - Magnification of image signal to be recorded
    : 1 ~ 8 times (about 1000 gradations)
- Implements the following functions on a single chip
  - (Built-in) sample and hold circuit
  - (Built-in) shading distortion correction RAM
  - (Built-in) sensor interface
  - Parallel to serial conversion of the image signal to be recorded.
- 2.5 μm CMOS process technology
- Single 5V supply

■ PIN ARRANGEMENT



(Top View)

1.1 Absolute Maximum Rating

1.1.1 Internal Digital Circuits

(Voltages referenced to V_{SS} = 0V. Ta = 25°C)

No.	Item	Symbol	Value	Unit
1	Supply Voltage	V_{DD}	-0.3 to +7.0	V
2	Input Voltage (Digital Input Pins)	V_I	-0.3 to V_{DD}+0.3	V
3	Input Voltage (Digital I/O Pins)	V_{IT}	-0.3 to V_{DD}+0.3	V

1.1.2 Internal Analog Circuits

(Voltages referenced to AVss = 0V. Ta = 25°C)

No.	Item	Symbol	Value	Unit
1	Supply Voltage	AV_{DD}	-0.3 to +7.0	V
2	Reference Voltage	$V_{2.5}$ V_{CL} V_{BL}	-0.3 to V_{DD}+0.3	V
3	Input Voltage (Analog Input Pins)	V_{IA}	-0.3 to V_{DD}+0.3	V

1.1.3 Common Characteristics between Digital and Analog Circuits

No.	Item	Symbol	Value	Unit
1	Operating Temperature	Topr	0 to +70	°C
2	Storage temperature	Tstg	-55 to +125	°C
3	Power Consumption *1	Pc	500	mW

*1) Ta = 25°C

Precaution in Using the DIPP

- Applying overvoltage more than the maximum rating to the input terminals due to overshooting or under shooting may cause latch-up, electro-static breakdown, etc.
- Precaution is needed in noise protection and shield for the analog terminals.

1.2 Electrical Characteristics

1.2.1 Internal Digital Circuits

1.2.1.1 DC Characteristics

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

No.	Item	Symbol	Test Condition	min	typ	max	Unit
1	Input High Voltage	V_{IH}	V_{DD}=5.25V	2.0	-	V_{DD}	V
2	Input Low Voltage	V_{IL}	V_{DD}=4.75V	-0.3	-	0.8	V
3	Output High Voltage	V_{OH}	V_{DD}=4.75V I_{OH}=-400µA V_{IH}=2.0V V_{IL}=0.8V	3.0	-	-	V
4	Output Low Voltage	V_{OL}	V_{DD}=4.75V V_{IH}2.0V V_{IL}=0.8V Other output pins : Low I_{OL}=1.6mA	-	-	0.4	V
5	Input Leakage Voltage	I_{IN}	V_{DD}=5.25V V_I =0 to V_{DD}	-10 *1	-	10	µA
6	Three-State (Off State) Leakage Current	I_{OZH}	V_{DD}=5.25V V_O =V_{DD}	-10	-	10	µA
		I_{OZL}	V_{DD}=5.25V V_O =V_{SS}	-10	-	10	µA

*1) The minimum leakage current at pin 34 ($\overline{68}$/80) is -100µA because it has an internal pull-up resistor.

1.2.1.2 AC Characteristics

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

(1) Motorola MPU Interface Timing (68000, etc.)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
DS Pulse Width	t_{WDS6}	I	Fig. 1-1	DS	450	—	—	ns
DS to R/$\overline{W}$ Setup Time	t_{SRW6}	I	Fig. 1-1	R/$\overline{W}$	140	—	—	ns
DS to R/$\overline{W}$ Hold Time	t_{HRW6}	I	Fig. 1-1	R/$\overline{W}$	10	—	—	ns
DS to $\overline{CS}$ Setup Time	t_{SCS6}	I	Fig. 1-1	$\overline{CS}$	140	—	—	ns
DS to $\overline{CS}$ Hold Time	t_{HCS6}	I	Fig. 1-1	$\overline{CS}$	10	—	—	ns
DS to $\overline{RS}$ Setup Time	t_{SRS6}	I	Fig. 1-1	$\overline{RS}$	140	—	—	ns
DS to $\overline{RS}$ Hold Time	t_{HRS6}	I	Fig. 1-1	$\overline{RS}$	50	—	—	ns
Read Data Access Time	t_{RAC6}	O	Fig. 1-1	D0 to D7	—	—	320	ns
Read Data Hold Time	t_{RH6}	O	Fig. 1-1	D0 to D7	10	—	—	ns
Write Data Setup Time	t_{WS6}	I	Fig. 1-1	D0 to D7	200	—	—	ns
Write Data Hold Time	t_{WH6}	I	Fig. 1-1	D0 to D7	40	—	—	ns
DS to $\overline{T/RDACK}$ Setup Time	t_{SDK6}	I	Fig. 1-2	$\overline{T/RDACK}$	(140)	—	—	ns
DS to $\overline{T/RDACK}$ Hold Time	t_{HDK6}	I	Fig. 1-2	$\overline{T/RDACK}$	(10)	—	—	ns

(2) Intel MPU Interface Timing (8080, 8086, etc.)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
DS ($\overline{RD}$) Pulse Width	t_{WDS8}	I	Fig. 1-3	DS	300	—	—	ns
R/$\overline{W}$ ($\overline{WR}$) Pulse Width	t_{WRW8}	I	Fig. 1-3	R/$\overline{W}$	250	—	—	ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{SRC8}	I	Fig. 1-3	$\overline{CS}$	125	—	—	ns
$\overline{RD}$ to $\overline{CS}$ Hold Time	t_{HRC8}	I	Fig. 1-3	$\overline{CS}$	0	—	—	ns
$\overline{WR}$ to $\overline{CS}$ Setup Time	t_{SWC8}	I	Fig. 1-3	$\overline{CS}$	125	—	—	ns
$\overline{WR}$ to $\overline{CS}$ Hold Time	t_{HWC8}	I	Fig. 1-3	$\overline{CS}$	20	—	—	ns
$\overline{RD}$ to $\overline{RS}$ Setup Time	t_{SRR8}	I	Fig. 1-3	$\overline{RS}$	125	—	—	ns
$\overline{RD}$ to $\overline{RS}$ Hold Time	t_{HRR8}	I	Fig. 1-3	$\overline{RS}$	50	—	—	ns
$\overline{WR}$ to $\overline{RS}$ Setup Time	t_{SWR8}	I	Fig. 1-3	$\overline{RS}$	125	—	—	ns
$\overline{WR}$ to $\overline{RS}$ Hold Time	t_{HWR8}	I	Fig. 1-3	$\overline{RS}$	70	—	—	ns
Read Data Access Time	t_{RAC8}	O	Fig. 1-3	D0 to D7	—	—	300	ns
Read Data Hold Time	t_{RH8}	O	Fig. 1-3	D0 to D7	10	—	—	ns
Write Data Setup Time	t_{WS8}	I	Fig. 1-3	D0 to D7	180	—	—	ns
Write Data Hold Time	t_{WH8}	I	Fig. 1-3	D0 to D7	50	—	—	ns
$\overline{RD}$ to $\overline{T/RDACK}$ Setup Time	t_{SDK8}	I	Fig. 1-4	$\overline{T/RDACK}$	(125)	—	—	ns
$\overline{RD}$ to $\overline{T/RDACK}$ Hold Time	t_{HDK6}	I	Fig. 1-4	$\overline{T/RDACK}$	(0)	—	—	ns
$\overline{WR}$ to $\overline{T/RDACK}$ Setup Time	t_{SRK8}	I	Fig. 1-4	$\overline{T/RDACK}$	(125)	—	—	ns
$\overline{WR}$ to $\overline{T/RDACK}$ Hold Time	t_{HRK8}	I	Fig. 1-4	$\overline{T/RDACK}$	(25)	—	—	ns

(3) MPU Interface Timing (common to Motorola MPU and Intel MPU)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
T/RDRQ Positive Edge Delay	t_{DRQH}	O	Fig. 1-5	T/RDRQ	—	—	200	ns
T/RDRQ Negative Edge Delay	t_{DRQL}	O	Fig. 1-5	T/RDRQ	—	—	200	ns
INT Positive Edge Delay	t_{INTH}	O	Fig. 1-6	INT	—	—	300	ns
T/RSCAN input to INT Negative Edge Delay	t_{INTL}	O	Fig. 1-6	INT	—	—	100	ns
DS input to INT Negative Edge Delay	t_{DSIL}	O	Fig. 1-1 Fig. 1-3	INT	—	—	(300)	ns

(4) Clock and Control Input Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
CLKI Cycle Time	t_{CYC}	I	Fig. 1-7	CLKI *2	100	—	1000	ns
RCLK Cycle Time	t_{RCYC}	I	Fig. 1-7	RCLKI *2	200	—	10^6	ns
TSCAN Pulse Width	t_{TSW}	I	Fig. 1-7	T/RSCAN	$(^{2\ \times}_{tCYC})$	—	—	ns
RSCAN Pulse Width	t_{RSW}	I	Fig. 1-7	T/RSCAN	$(^{2\ \times}_{tCYC})$	—	—	ns
$\overline{RST}$ Pulse Width	t_{RSTW}	I	Fig. 1-7	$\overline{RST}$	$(^{2\ \times}_{tCYC})$	—	—	ns
TRIG Pulse Width	t_{TRIG}	I	Fig. 1-7	TRIG	(8)	—	—	µs

*2) Both CLKI and RCLKI input frequencies provide duty cycle of 50%.

(5) Serial Output Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
CLKI Input to TMSK Output Delay	t_{TMDT}	O	Fig. 1-8	TMSK	—	—	200	ns
CLKI Input to TMSK Output Hold	t_{TMHT}	O	Fig. 1-8	TMSK	—	—	200	ns
TDATA Output Delay	t_{TDD}	O	Fig. 1-8	T/RDATA	—	—	200	ns
TDATA Output Hold	t_{TDH}	O	Fig. 1-8	T/RDATA	—	—	250	ns
TCLK Positive Edge Delay	t_{TCH}	O	Fig. 1-8	T/RCLK	—	—	200	ns
TCLK Negative Edge Delay	t_{TCL}	O	Fig. 1-8	T/RCLK	—	—	200	ns
RCLK Output to TMSK Output Delay	t_{TMDR}	O	Fig. 1-9	TMSK	—	—	(200) *3	ns
RCLK Output to TMSK Output Delay	t_{TMHR}	O	Fig. 1-9	TMSK	—	—	(200) *3	ns
RDATA Output Delay	t_{RDD}	O	Fig. 1-9	T/RDATA	—	—	(200) *3	ns
RDATA Output Hold	t_{RDH}	O	Fig. 1-9	T/RDATA	—	—	(200) *3	ns
RCLK Positive Edge Delay	t_{RCH}	O	Fig. 1-9	T/RCLK	—	—	(200) *3	ns
RCLK Negative Edge Delay	t_{RCL}	O	Fig. 1-9	T/RCLK	—	—	(200) *3	ns

*3) Values for reference.

(6) Application Output and Sensor Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
TIMO Output Delay	t_{TO}	O	Fig. 1-10	TIMO	—	—	200	ns
LNST/IWIN Output Delay	t_{LN}	O	Fig. 1-10 (IWIN)	LNST/IWIN	—	—	250	ns
ϕTG Output Positive Edge Delay	$t_{\phi TD}$	O	Fig. 1-11	ϕTG	—	—	150	ns
ϕTG Output Negative Edge Delay	$t_{\phi TH}$	O	Fig. 1-11	ϕTG	—	—	160	ns
ϕ1 Output Delay	$t_{\phi 1D}$	O	Fig. 1-11	ϕ1	—	—	100	ns
ϕ1 Output Hold	$t_{\phi 1H}$	O	Fig. 1-11	ϕ1	—	—	130	ns
ϕR Positive Edge Delay	$t_{\phi RD}$	O	Fig. 1-13	ϕR	—	—	100	ns
ϕR Positive Edge Hold	$t_{\phi RH}$	O	Fig. 1-13	ϕR	—	—	100	ns

(7) Memory Bus Interface Timing

Item	Symbol	I/O	Test Condition	Applicable Pin	min	type	max	Unit
MAS/MDS Positive Edge Delay	t_{MASD}	O	Fig. 1-14, -16, -18, -19, -20,	MAS/MDS	—	—	200	ns
MAS/MDS Negative Edge Delay	t_{MASH}	O	Fig. 1-14, -16, -18, -19, -20,	MAS/MDS	—	—	200	ns
LNSL Output Delay	t_{LSD}	O	Fig. 1-14, -8, -19,	LNSL	—	—	200	ns
MA8 to 11 Output Delay *4	t_{MAUD}	O	Fig. 1-14, -8, -19,	MA8/$\overline{\text{MIWR}}$ to MA11/ $\overline{\text{PDEN}}$/MBE	—	—	200	ns
$\overline{\text{LRD}}$ Negative Edge Delay	t_{LRD}	O	Fig. 1-14, -8, -19,	$\overline{\text{LRD}}$	—	—	200	ns
$\overline{\text{LRD}}$ Positive Edge Hold	t_{LRH}	O	Fig. 1-14, -8, -19,	$\overline{\text{LRD}}$	—	—	200	ns
$\overline{\text{LWR}}$ Negative Edge Delay	t_{LWD}	O	Fig. 1-14, -8, -19,	$\overline{\text{LWR}}$	—	—	200	ns

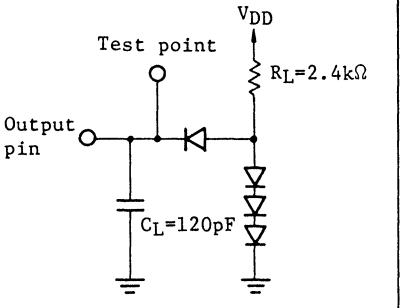
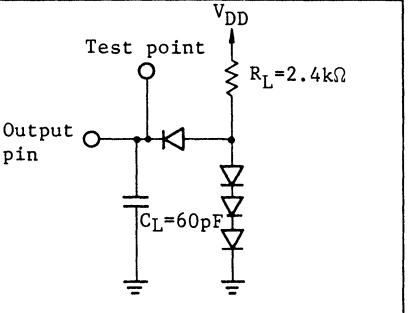
(To be continued)

*4) Values for reference.

(Continued)

Item	Symbol	I/O	Test Condition	Applicable Pin	min	typ	max	Unit
$\overline{\text{LWR}}$ Positive Edge Hold	t_{LWH}	O	Fig. 1-14 Fig. 1-19	$\overline{\text{LWR}}$	—	—	200	ns
MAD0 to 7 Delay	t_{MADD}	O	Fig. 1-14 etc.	MAD0-7	—	—	200	ns
MAD0 to 7 Hold	t_{MADH}	O	Fig. 1-14 etc.	MAD0-7	—	—	200	ns
MAD0 to 7 Setup Time	t_{RDS}	I	Fig. 1-14	MAD0-8	50	—	—	ns
MAD0 to 7 Hold Time	t_{RDH}	I	Fig. 1-14	MAD0-7	50	—	—	ns
MBE Negative Edge Delay	t_{MBEL}	O	Fig. 1-15	MBE	—	—	200	ns
$\overline{\text{T/RDACK}}$ Input to MAS Negative Edge Delay	t_{BASL}	O	Fig. 1-17	MAS/MDS	—	—	200	ns
$\overline{\text{T/RDACK}}$ Input to MAS Positive Edge Delay	t_{BASH}	O	Fig. 1-17	MAS/MDS	—	—	200	ns
$\overline{\text{T/RDACK}}$ Input to T/RDRQ Negative Edge Delay	t_{BTDR}	O	Fig. 1-17	T/RDRQ	—	—	400	ns
MLNST Positive Edge Delay	t_{MLNH}	O	Fig. 1-16 Fig. 1-17 Fig. 1-18	MA9/LNSTN	—	—	250	ns
MLNST Negative Edge Delay	t_{MLNL}	O	Fig. 1-16 Fig. 1-17 Fig. 1-18	MA9/LNSTN	—	—	300	ns
$\overline{\text{PRD}}$ Negative Edge Delay	t_{PRD}	O	Fig. 1-16 Fig. 1-19	$\overline{\text{PRD}}$	—	—	200	ns
$\overline{\text{PRD}}$ Positive Edge Hold	t_{PRH}	O	Fig. 1-16 Fig. 1-19	$\overline{\text{PRD}}$	—	—	200	ns
$\overline{\text{PWR}}$ Negative Edge Delay	t_{PWD}	O	Fig. 1-18 Fig. 1-20	$\overline{\text{PWR}}$	—	—	200	ns
$\overline{\text{PWR}}$ Positive Edge Hold	t_{PWH}	O	Fig. 1-18 Fig. 1-20	$\overline{\text{PWR}}$	—	—	200	ns
$\overline{\text{MIWR}}$ Negative Edge Delay	t_{MIWL}	O	Fig. 1-16	MA8/$\overline{\text{MIWR}}$	—	—	400	ns
$\overline{\text{MIWR}}$ Positive Edge Delay	t_{MIWH}	O	Fig. 1-16	MA8/$\overline{\text{MIWR}}$	—	—	200	ns
$\overline{\text{MPRD}}$ Negative Edge Delay	t_{MPRL}	O	Fig. 1-18	MA10/$\overline{\text{MPRD}}$	—	—	250	ns
$\overline{\text{MPRD}}$ Positive Edge Delay	t_{MPRH}	O	Fig. 1-18	MA10/$\overline{\text{MPRD}}$	—	—	250	ns
$\overline{\text{PDEN}}$ Negative Edge Delay	t_{PDEL}	O	Fig. 1-18	MA11/$\overline{\text{PDEN}}$ /MBE	—	—	200	ns

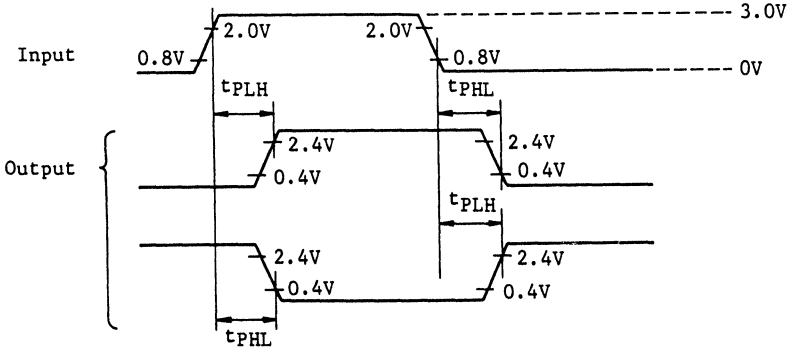
(Note 1) Bus Timing Test Loads

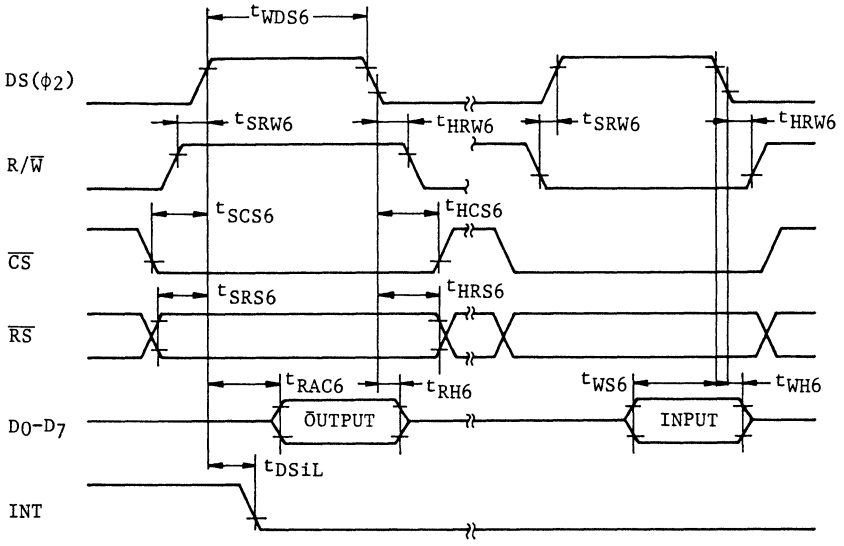
D0 to D7 pins	Other output and I/O pins (excluding analog pins)
	

[Notes] 1. C_L includes stray capacitance caused by the probe and load capacitance.

2. Diodes are 1S2074 Ⓗ or equivalents.

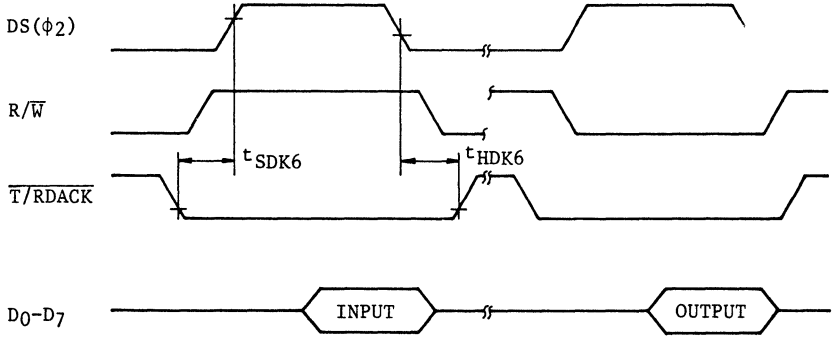
(Note 2) I/O Signal Test Points





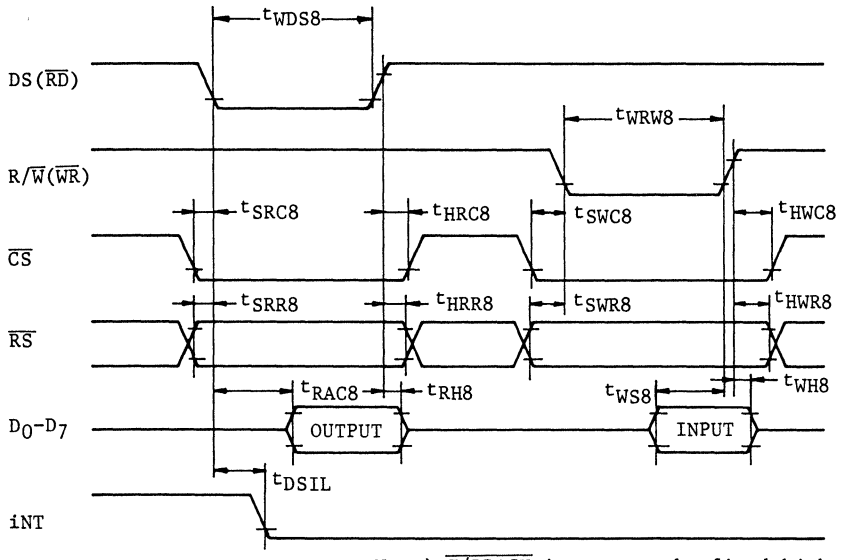
Note) $\overline{T/RDACK}$ input must be fixed high.

Fig. 1-1 Motorola MPU Access Timing



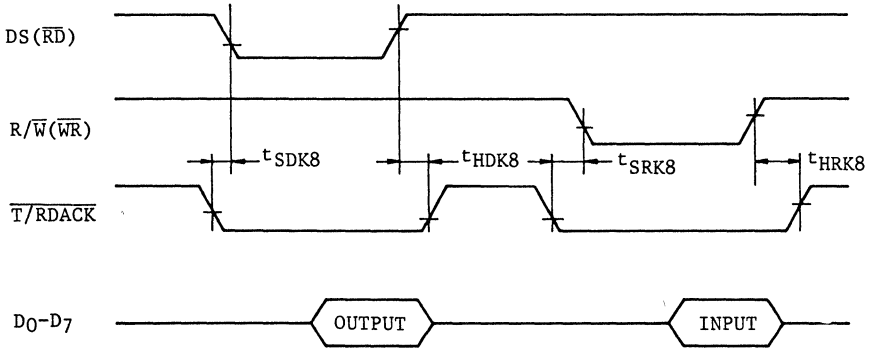
Note) $\overline{CS}$ input must be fixed high.

Fig. 1-2 DMA Operation Timing (Using Motorola MPU)



Note) $\overline{T/RDACK}$ input must be fixed high.

Fig. 1-3 Intel MPU Access Timing



Note) $\overline{CS}$ input must be fixed high.

Fig. 1-4 DMA Operation Timing (Using Intel MPU)

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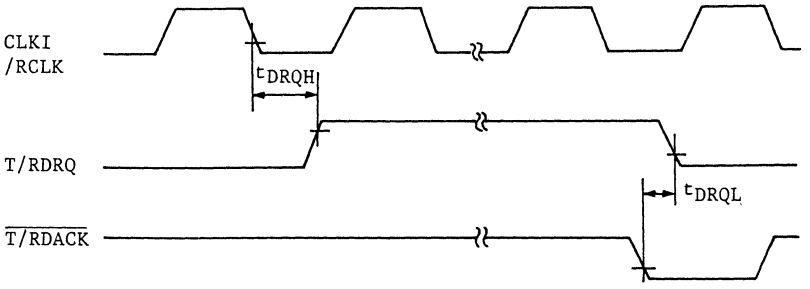


Fig. 1-5 T/RDRQ Output Timing

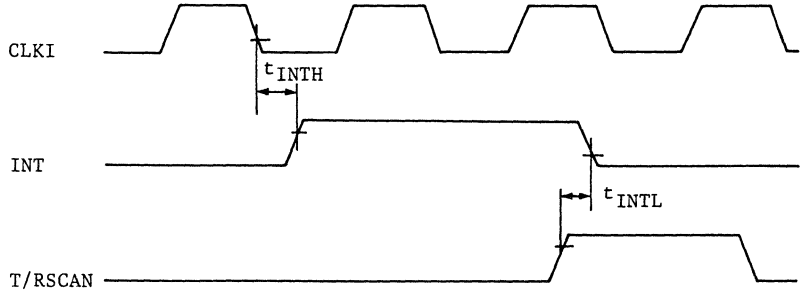


Fig. 1-6 INT Output Timing

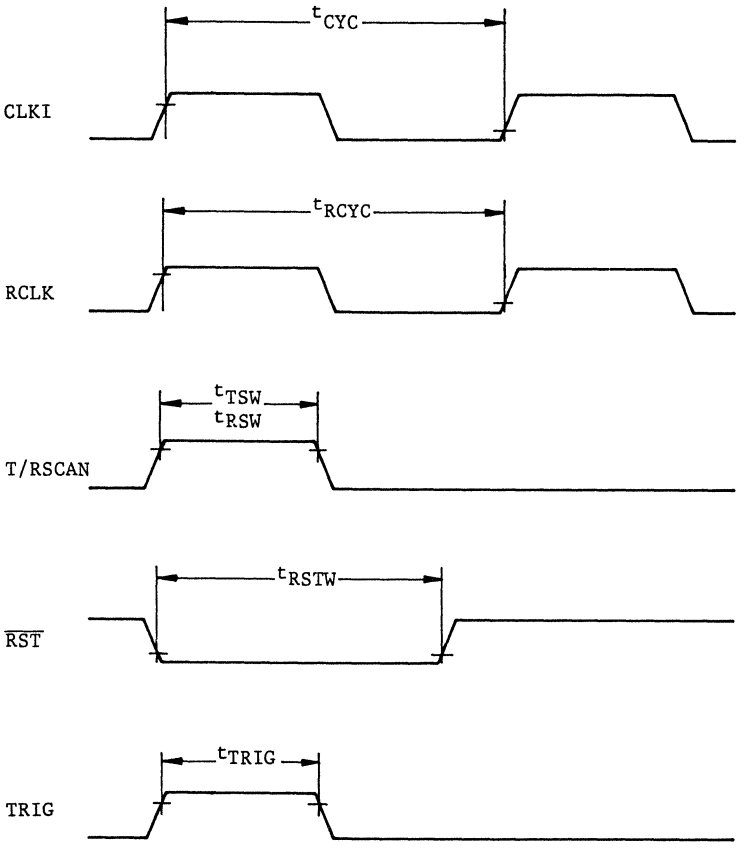


Fig. 1-7 CLKI, RCLK, T/RSCAN, $\overline{RST}$ and TRIG Input Timing

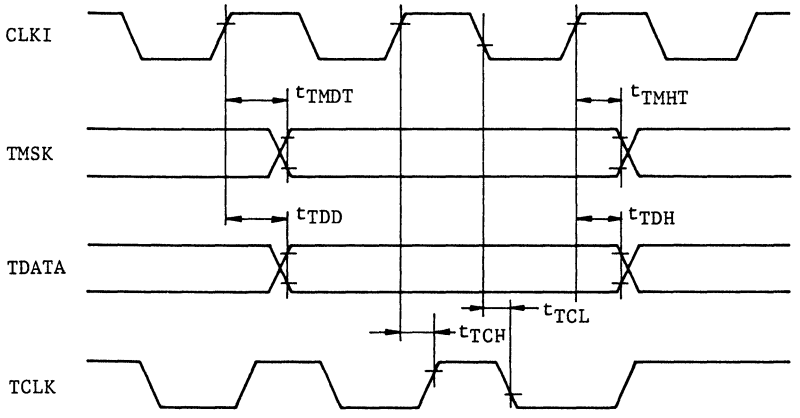


Fig. 1-8 Serial Output Timing (in Read (T) Mode)

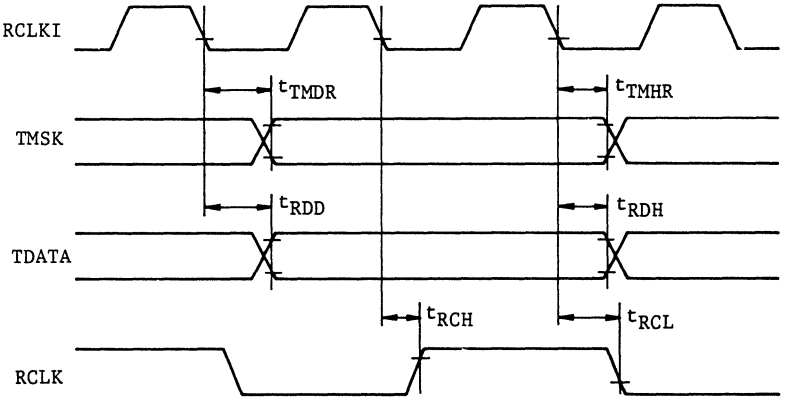


Fig. 1-9 Serial Output Timing (in Receive (R) Mode)

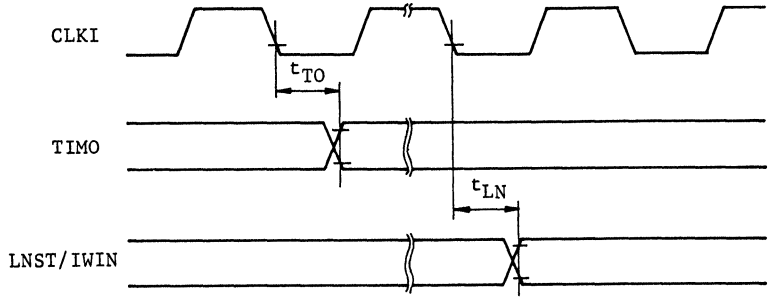
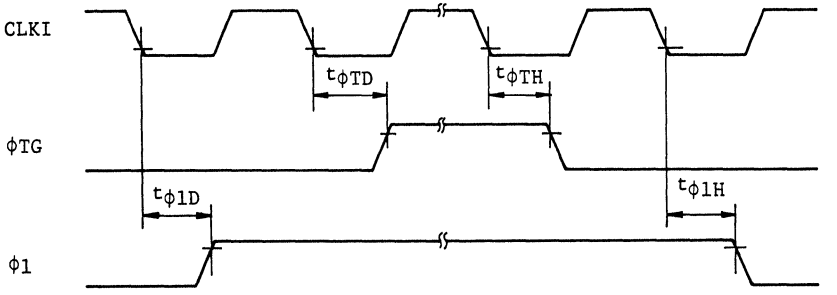
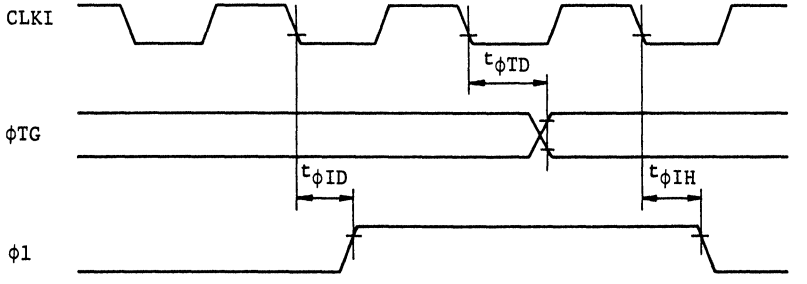


Fig. 1-10 Application Output Timing



Note) The SMD0, SMD1 and SMD2 bits in the R09 register must be 0,0 and 0 or 0,0 and 1 respectively.

Fig. 1-11 ϕTG and ϕ1 Output Timing (1)



Note) The SMD0, SMD1 and SMD2 bits must be 0,1 and 0 or 0,1 and 1 respectively.

Fig. 1-12 ϕTG and ϕ1 Output Timing (2)

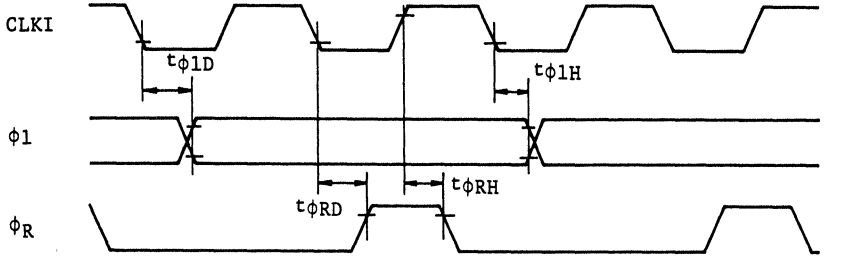


Fig. 1-13 ϕ1 and ϕR Output Timing

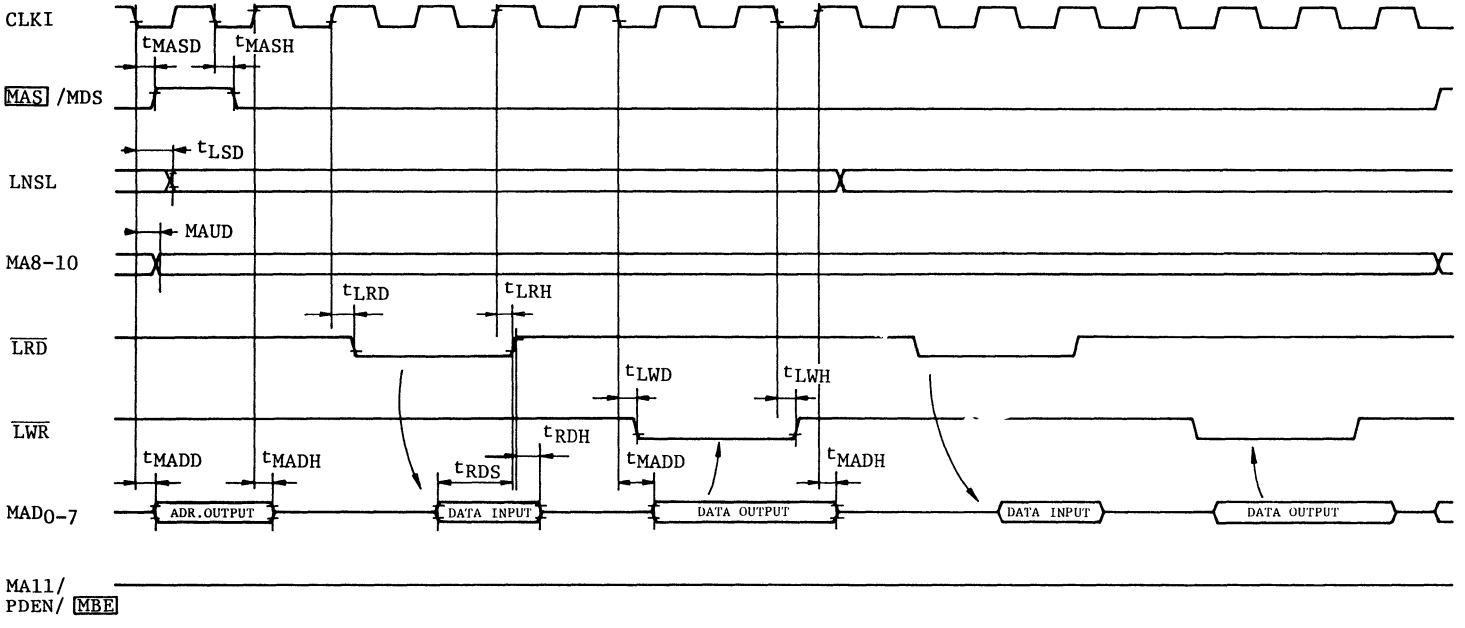


Fig. 1-14 Memory Bus Interface Timing in A Mode (1) During Image Data Processing

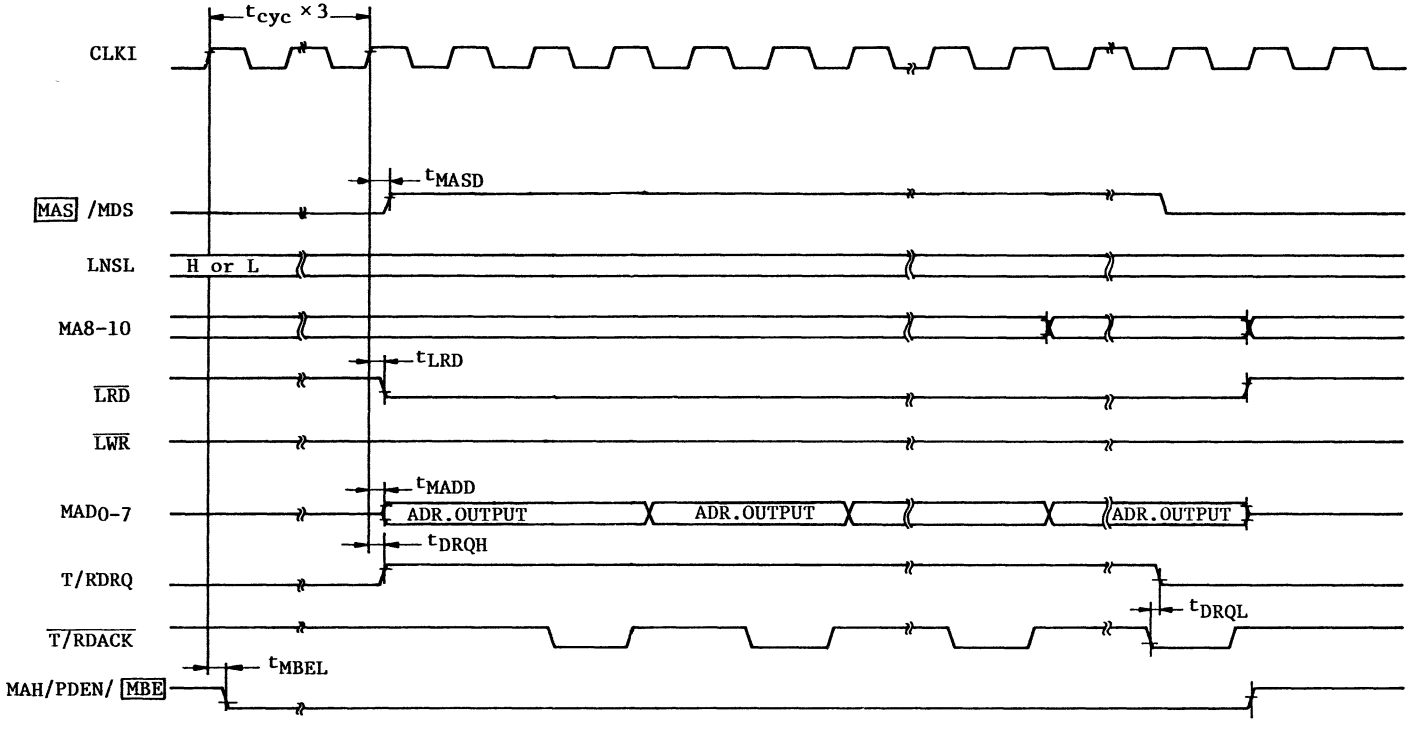


Fig. 1-15 Memory Bus Interface Timing in A Mode (2)
During Burst DMA Transfer

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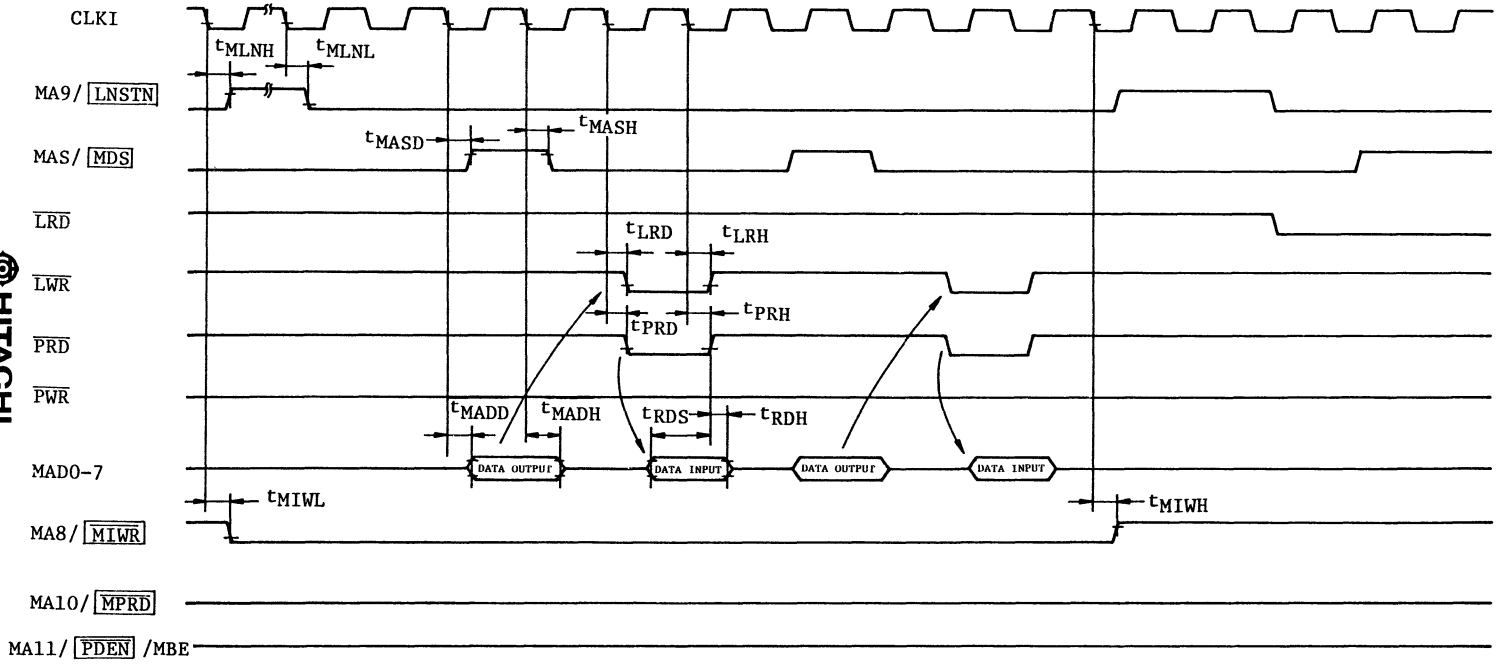

Fig. 1-16 Memory Bus Interface Timing in B Mode (1)
During 4-bit Coded Data Output

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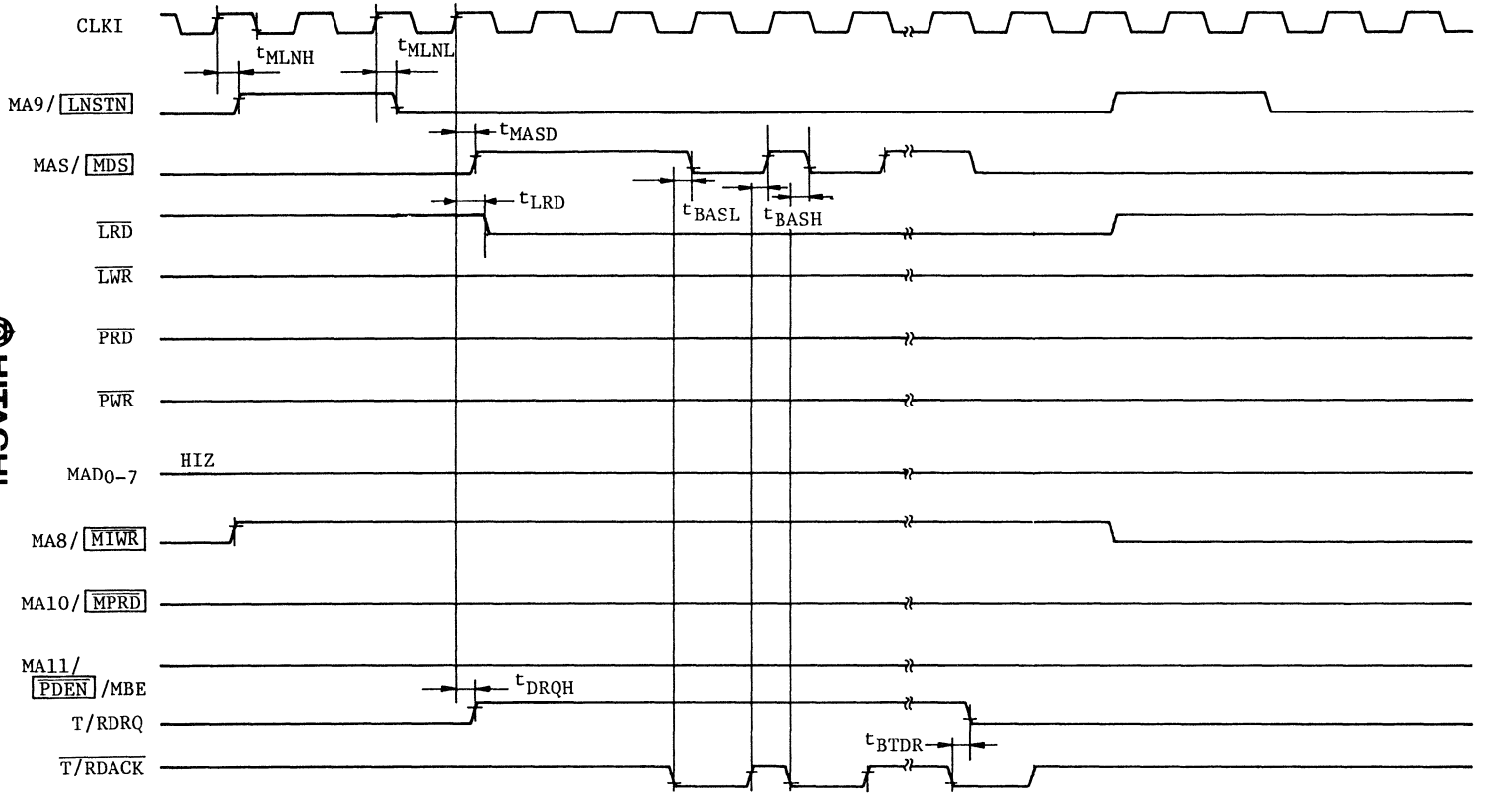

Fig. 1-17 Memory Bus Interface Timing in B Mode (2) During Burst DMA Transfer

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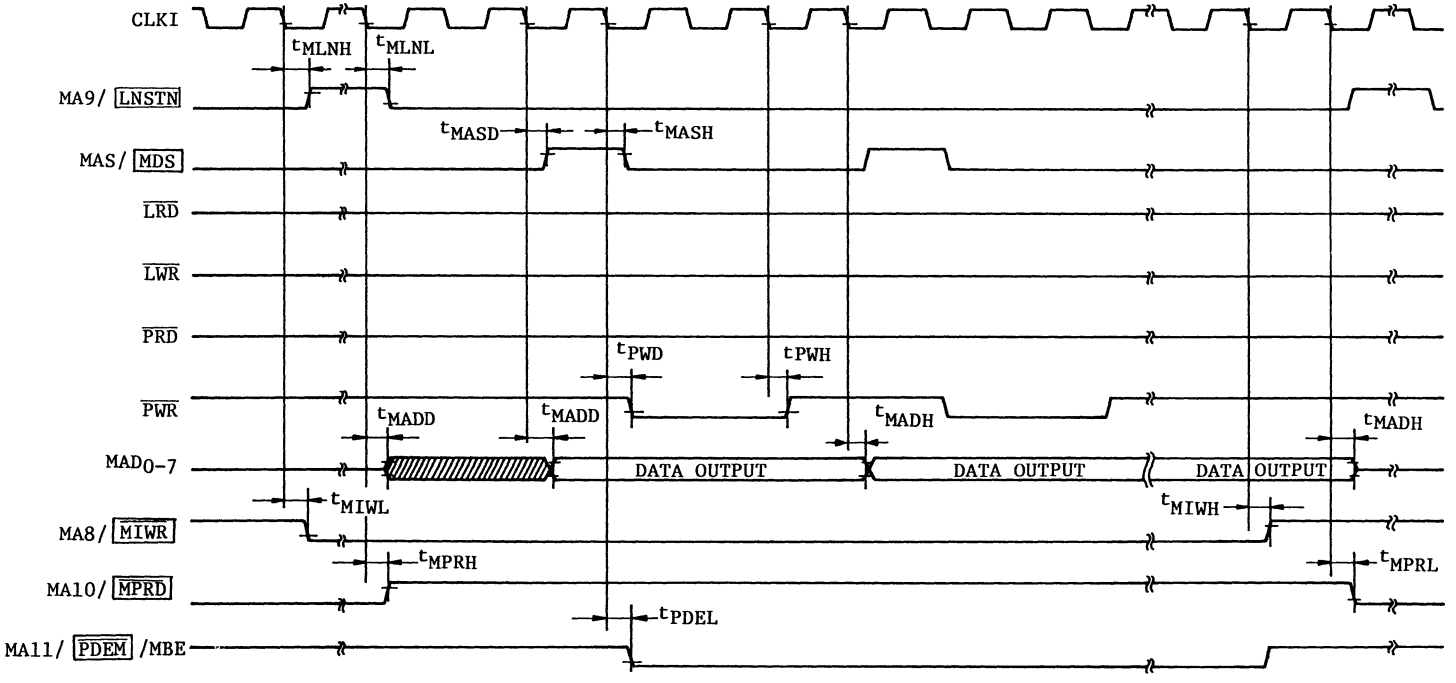

Fig. 1-18 Memory Bus Interface Timing in B Mode (3)
During Pel Correction Data Detection

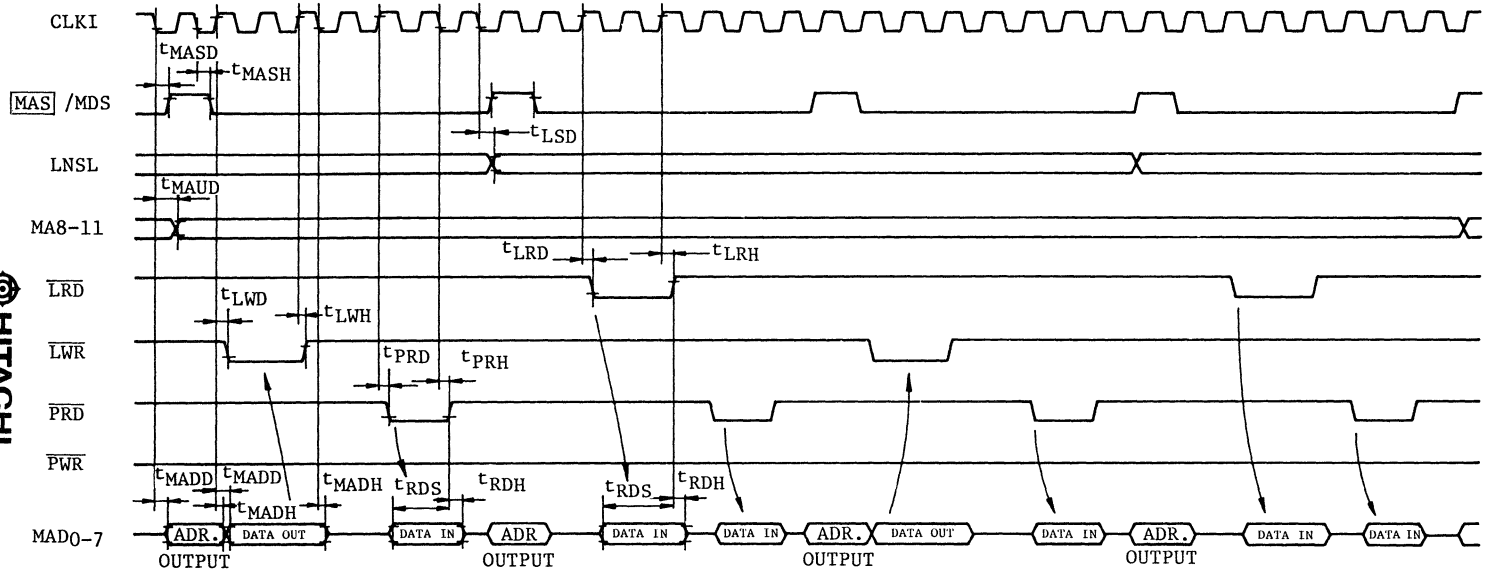

Fig. 1-19 Memory Bus Interface Timing in C or D Mode (1)
During Image Data Processing

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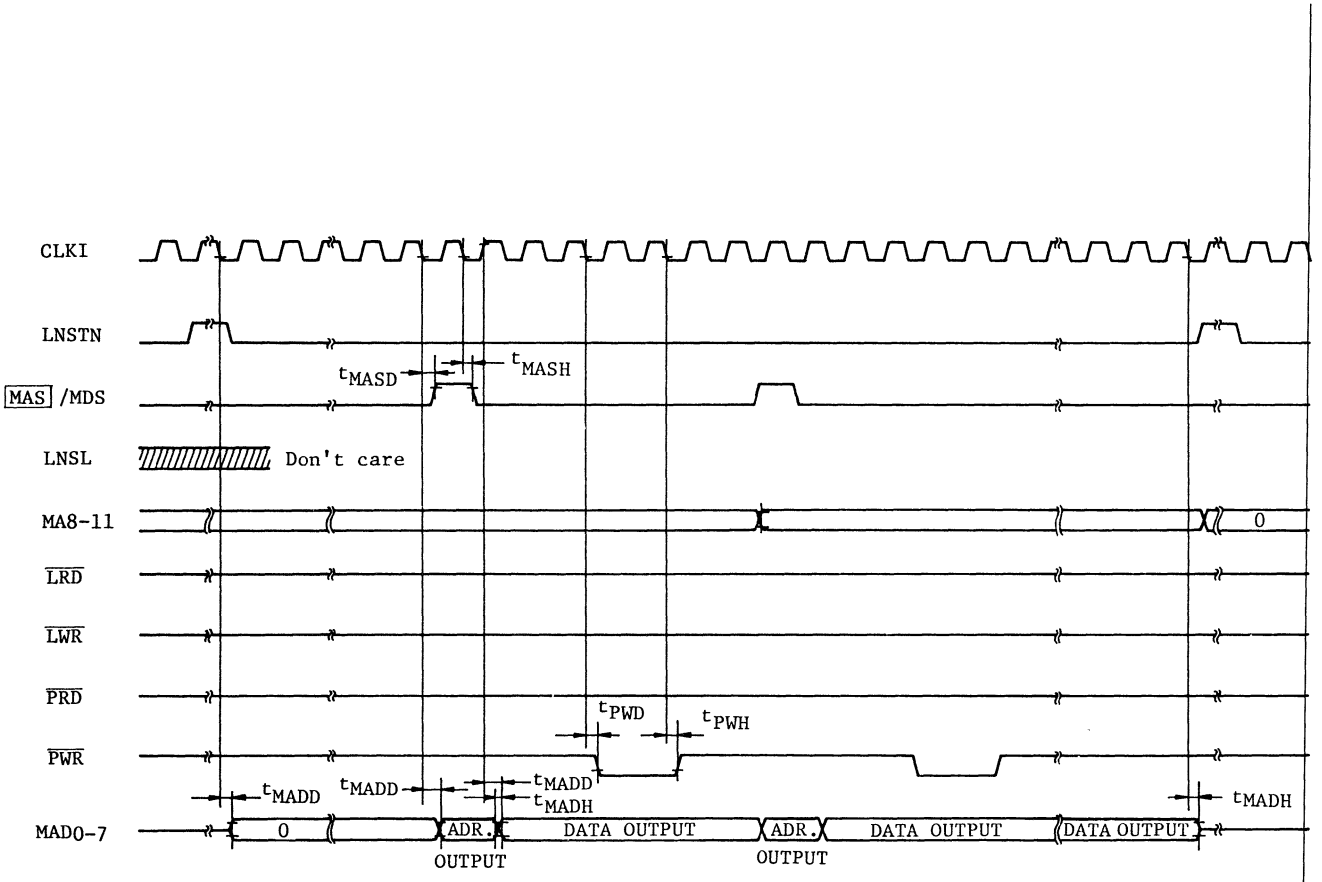

Fig. 1-20 Memory Bus Interface Timing in C or D Mode (2)
During Pel Correction Data Detection

1.2.1.3 Capacitance

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{IN}	f = 100kHz	—	—	12.5	pF
Output Capacitance	C_{OUT}		—	—	12.5	pF
Input/Output Capacitance	Cin/out		—	—	12.5	pF

* These parameters are sample values.

1.2.2 Internal Analog Circuits

1.2.2.1 DC Characteristics

Item	Detailed Item	Symbol	Test Condition	min	typ	max	Unit
Input Current	VBL	L_{BL}	V_{BL}=3.5V	—	—	1.0	mA
Input Voltage Range	ISIN1,2	$V_{ISI1,2}$		1.5	—	3.5	V
	PEAKI	V_{INP}		1.5	—	3.0	
	SLICE1	V_{INS1}		1.5	—	3.5	
	SLICE2	V_{INS2}		1.5	—	3.5	
	VBL	V_{IBL}		0.3 × VDD	—	0.7 × VDD	
	VCL	V_{ICL}		0.3 × V_{DD}	—	0.7 × V_{DD}	
Output Current	IOUT	I_{OIO}		-16.0	—	-4.0	mA
	PEAKO	I_{OPK}		-5.0	—	-0.7	
	DAO	I_{ODO}		-6.0	—	-0.7	
Supply Current	Standby	I_{DS}		—	—	1	
	Operating	I_{DD}	CLKI=10MHz	—	—	60	

(to be continued)

(continued)

Item	Detailed Item		Symbol	Test Condition	min	typ	max	Unit
Output Voltage	PEAK0	Resistance Chain Step 0	V_{P0}	$V_{CL}=V_{BL}$ =3.4V PEAKI = 1.5V	3.20	—	3.40	V
		Resistance Chain Step 255	V_{P255}		1.25	—	1.65	
	DA0	Resistance Chain Step 0	V_{D0}		1.40	—	1.60	
		Resistance Chain Step 127	V_{D127}		2.60	—	3.00	
	IOUT		V_{IOUT}	V_{ISIN1} = 2.5V	2.40	—	2.65	
Input Leakage Current	ISIN1		I_{LIS1}	V_{IN} = 0 to V_{DD}	-10	—	10	μA
	ISIN2		I_{LIS2}					
	PEAKI		I_{LPI}					
	SLICE1		I_{LSL1}					
	SLICE2		I_{LSL2}					
	VCL		I_{LVCL}					

1.2.2.2 AC Characteristics

Item	Detailed Item	Symbol	Test Condition	min	typ	max	Unit
Input Voltage Range	Peak to Peak Voltage	V_{IP}	f_{CLK}=10MHz	0.1	—	2.0	V
Operating Frequency	Image Signal Reading Frequency	V_{IF}	V_{BL}=3.4V V_{SLICE} = 1.8V	0.5	—	5.0	MHz

9.2 Function of Analog Signal Processing Block

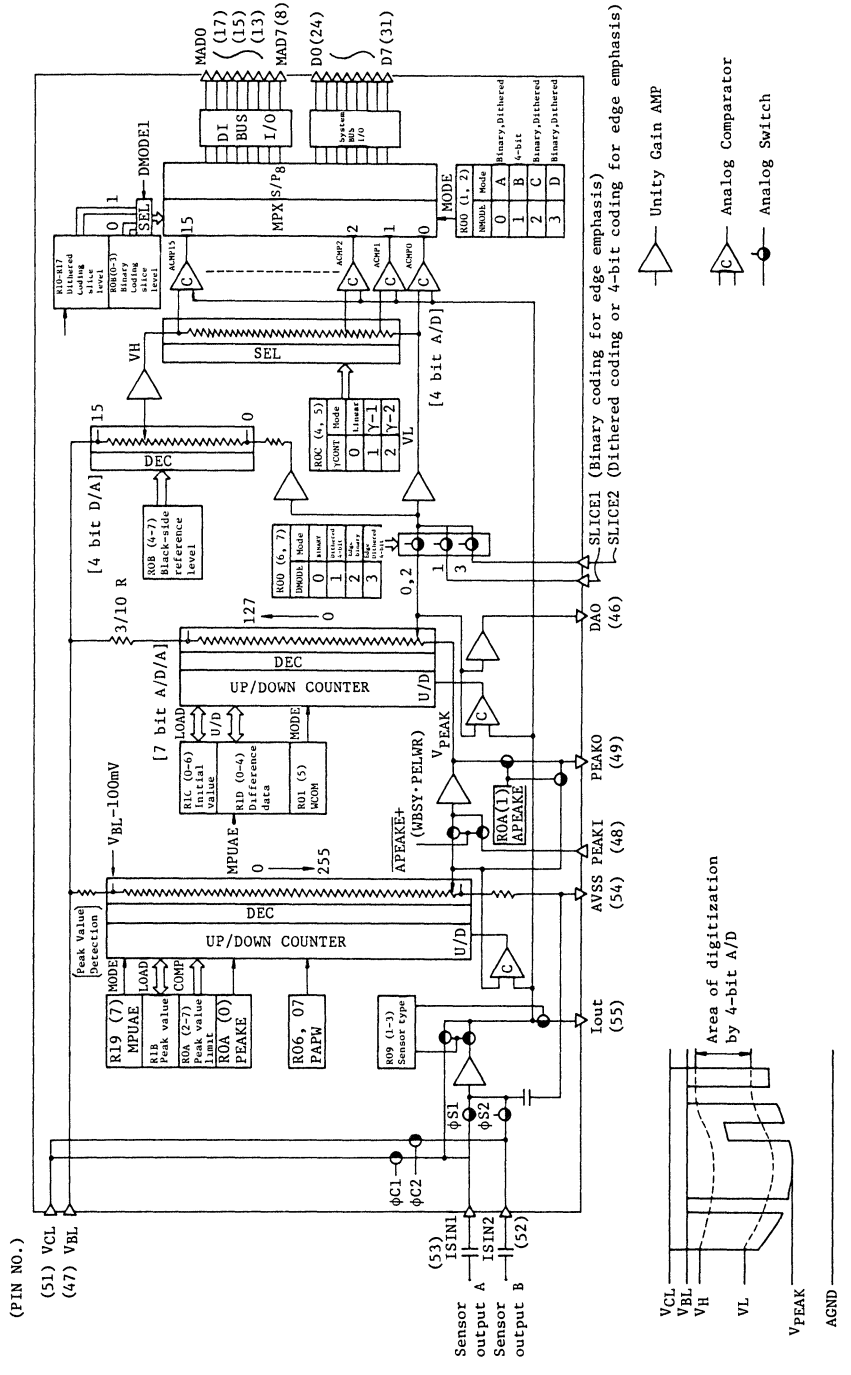

Fig. 2-1 Functional Configuration of Analog Signal Processing Block

1.2 Relation between Horizontal Resolution Conversion Ratio (β) and Parameters

Table 1-1 Relation between Horizontal Resolution Conversion Ratio (β) and Parameters (1)

β	m	k	ℓ '1'	ℓ '0'	HRCM		β	m	k	ℓ '1'	ℓ '0'	HRCM	
.125	7	1	1	0	1		1.1	8	11	3	8	0	
.15	6	3	2	1	1		1.12	8	7	1	6	0	
.16	6	4	1	3	1		1.15	7	3	2	1	0	
.18	5	9	5	4	1		1.1548	7	13	6	7	0	B5→A4, B4→A3
.2	4	1	1	0	1		1.16	7	4	1	3	0	
.22	4	11	6	5	1		1.18	6	9	5	4	8	
.25	3	1	1	0	1		1.2	5	1	1	0	0	
.28	3	7	4	3	1		1.2264	5	12	5	7	0	A4→B4
.3	3	3	1	2	1		1.2273	5	5	2	3	0	A4→B4
.32	3	8	1	7	1		1.24	5	6	1	5	0	
.35	2	7	6	1	1		1.26	4	14	11	3	0	
.375	2	3	2	1	1		1.28	4	7	4	3	0	
.4	2	2	1	1	1		1.3	4	3	1	2	0	
.44	2	11	3	8	1		1.32	4	8	1	7	0	
.45	2	9	2	7	1		1.35	3	7	6	1	0	
.5	2	1	0	1	0		1.375	3	3	2	1	0	
.52	2	12	1	11	0		1.4	3	2	1	1	0	
.55	2	9	2	7	0		1.4138	3	12	5	7	0	A4→A3, B5→B4
.56	2	11	3	8	0		1.4167	3	5	2	3	0	A4→A3, B5→B4
.6	2	2	1	1	0		1.44	3	11	3	8	0	
.6129	2	12	7	5	0	A3→B5	1.45	3	9	2	7	0	
.625	2	3	2	1	0		1.48	3	12	1	11	0	
.65	2	7	6	1	0		1.5	2	1	1	0	0	
.68	3	8	1	7	0		1.52	2	13	12	1	0	
.7	3	3	1	2	0		1.55	2	11	9	2	0	
.7073	3	12	5	7	0	A3→A4, B4→B5	1.56	2	14	11	3	0	
.72	3	7	4	3	0		1.6	2	3	2	1	0	
.75	3	1	1	0	0		1.6316	2	12	7	5	0	B5→A3
.76	4	6	1	5	0		1.6363	2	7	4	3	0	B5→A3
.78	4	11	6	5	0		1.65	2	13	7	6	0	
.8	4	1	1	0	0		1.6667	2	2	1	1	0	
.8163	5	9	4	5	0	B4→A4	1.6875	2	11	5	6	0	
.8167	5	11	5	6	0	B4→A4	1.7	2	7	3	4	0	
.825	5	7	5	2	0		1.7222	2	13	5	8	0	
.84	6	4	1	3	0		1.75	2	3	1	2	0	
.86	7	11	2	9	0		1.7692	2	10	3	7	0	
.866	7	13	6	7	0	A3→B4, A4→B5	1.8	2	4	1	3	0	
.8661	7	15	7	8	0	A3→B4, A4→B5	1.8235	2	14	3	11	0	
.875	7	1	1	0	0		1.8421	2	16	3	13	0	
.9	8	5	1	4	0		1.8667	2	13	2	11	0	
.925	8	5	2	3	0		1.8824	2	15	2	13	0	
.95	8	5	3	2	0		1.9	2	9	1	8	0	
.975	8	5	4	1	0		1.9231	2	12	1	11	0	
1.0	8	1	1	0	0		1.9412	2	16	1	15	0	
1.024	8	16	13	3	0		2.0	2	1	0	1	0	
1.03	8	13	9	4	0		2.0625	2	16	1	15	1	
1.062	8	15	8	7	0		2.0833	2	12	1	11	1	
1.081	8	5	2	3	0		2.1	2	10	1	9	1	

Table 1-1 Relation between Horizontal Resolution Conversion Ratio (β) and Parameters (2)

β	m	k	ℓ '1'	ℓ '0'	HRCM		β	m	k	ℓ '1'	ℓ '0'	HRCM	
2.125	2	8	1	7	1		3.3846	3	13	5	8	1	
2.1429	2	7	1	6	1		3.4167	3	12	5	7	1	
2.1667	2	6	1	5	1		3.4375	3	16	7	9	1	
2.1875	2	16	3	13	1		3.4545	3	11	5	6	1	
2.2143	2	14	3	11	1		3.5	3	2	1	1	1	
2.25	2	4	1	3	1		3.5333	3	15	8	7	1	
2.2727	2	11	3	8	1		3.5556	3	9	5	4	1	
2.3	2	10	3	7	1		3.5714	3	7	4	3	1	
2.3333	2	3	1	2	1		3.6	3	5	3	2	1	
2.3637	2	11	4	7	1		3.625	3	8	5	3	1	
2.3846	2	13	5	8	1		3.6667	3	3	2	1	1	
2.4167	2	12	5	7	1		3.6923	3	13	9	4	1	
2.4449	2	9	4	5	1		3.7	3	10	7	3	1	
2.4667	2	15	7	8	1		3.7277	3	11	8	3	1	
2.5	2	2	1	1	1		3.75	3	4	3	1	1	
2.5385	2	13	7	6	1		3.7778	3	9	7	2	1	
2.5625	2	16	9	7	1		3.8	3	5	4	1	1	
2.6154	2	13	8	5	1		3.8572	3	7	6	1	1	
2.6364	2	11	7	4	1		3.8889	3	9	8	1	1	
2.6667	2	3	2	1	1		3.9091	3	11	10	1	1	
2.6923	2	13	9	4	1		3.9231	3	13	12	1	1	
2.7143	2	7	5	2	1		3.9375	3	16	15	1	1	
2.7333	2	15	11	4	1		4.0	3	1	1	0	1	
2.7692	2	13	10	3	1		4.0625	4	16	1	15	1	
2.7857	2	14	11	3	1		4.0833	4	12	1	11	1	
2.8125	2	16	13	3	1		4.1	4	10	1	9	1	
2.8333	2	6	5	1	1		4.125	4	8	1	7	1	
2.8571	2	7	6	1	1		4.1429	4	7	1	6	1	
2.875	2	8	7	1	1		4.1667	4	6	1	5	1	
2.9	2	10	9	1	1		4.1818	4	11	2	9	1	
2.9167	2	12	11	1	1		4.2	4	5	1	4	1	
2.9333	2	15	14	1	1		4.2222	4	9	2	7	1	
3.0	2	1	1	0	1		4.25	4	4	1	3	1	
3.0625	3	16	1	15	1		4.2667	4	15	4	11	1	
3.0833	3	12	1	11	1		4.2857	4	7	2	5	1	
3.1111	3	9	1	8	1		4.3077	4	13	4	9	1	
3.125	3	8	1	7	1		4.3334	4	3	1	2	1	
3.1429	3	7	1	6	1		4.3572	4	14	5	9	1	
3.1667	3	6	1	5	1		4.3946	4	13	5	8	1	
3.1875	3	16	3	13	1		4.4167	4	12	5	7	1	
3.2143	3	14	3	11	1		4.4375	4	16	7	9	1	
3.2308	3	13	3	10	1		4.4545	4	11	5	6	1	
3.2667	3	15	4	11	1		4.5	4	2	1	1	1	
3.2857	3	7	2	5	1		4.5333	4	15	8	7	1	
3.3077	3	13	4	9	1		4.5556	4	9	5	4	1	
3.33	3	3	1	2	1		4.5833	4	12	7	5	1	
3.3636	3	11	4	7	1		4.625	4	8	5	3	1	

Table 1-1 Relation between Horizontal Resolution Conversion Ratio (β) and Parameters (3)

β	m	k	ℓ '1'	ℓ '0'	HRCM		β	m	k	ℓ '1'	ℓ '0'	HRCM	
4.6429	4	14	9	5	1		5.867	5	15	13	2	1	
4.6666	4	3	2	1	1		5.8889	5	9	8	1	1	
4.6875	4	16	11	5	1		5.9091	5	11	10	1	1	
4.7143	4	7	5	2	1		5.9231	5	13	12	1	1	
4.7333	4	15	11	4	1		5.9375	5	16	15	1	1	
4.75	4	4	3	1	1		6.0	5	1	1	0	1	
4.7779	4	9	7	2	1		6.0625	6	16	1	15	1	
4.8	4	5	4	1	1		6.0667	6	15	1	14	1	
4.8333	4	6	5	1	1		6.0833	6	12	1	11	1	
4.8572	4	7	6	1	1		6.1	6	10	1	9	1	
4.875	4	8	7	1	1		6.125	6	8	1	7	1	
4.9	4	10	9	1	1		6.1428	6	7	1	6	1	
4.9167	4	12	11	1	1		6.1667	6	6	1	5	1	
4.9333	4	15	14	1	1		6.1818	6	11	2	9	1	
5.0	4	1	1	0	1		6.2	6	5	1	4	1	
5.0625	5	16	1	15	1		6.2222	6	9	2	7	1	
5.0833	5	12	1	11	1		6.25	6	4	1	3	1	
5.1	5	10	1	9	1		6.2727	6	13	3	10	1	
5.125	5	8	1	7	1		6.3	6	10	3	7	1	
5.1429	5	7	1	6	1		6.3333	6	3	1	2	1	
5.1667	5	6	1	5	1		6.3636	6	11	4	7	1	
5.1875	5	16	3	13	1		6.3846	6	13	5	8	1	
5.2143	5	14	3	11	1		6.4167	6	12	5	7	1	
5.2308	5	13	3	10	1		6.4375	6	16	7	9	1	
5.2667	5	15	4	11	1		6.4615	6	13	6	7	1	
5.2857	5	7	2	5	1		6.5	6	2	1	1	1	
5.3077	5	13	4	9	1		6.5334	6	15	8	7	1	
5.333	5	3	1	2	1		6.5556	6	9	5	4	1	
5.3636	5	11	4	7	1		6.5833	6	12	7	5	1	
5.3846	5	13	5	8	1		6.6154	6	13	8	5	1	
5.4167	5	12	5	7	1		6.6364	6	11	7	4	1	
5.4375	5	16	7	9	1		6.6667	6	3	2	1	1	
5.4546	5	11	5	6	1		6.6923	6	13	9	4	1	
5.5	5	2	1	1	1		6.7143	6	7	5	2	1	
5.5385	5	13	7	6	1		6.75	6	4	3	1	1	
5.5556	5	9	5	4	1		6.7778	6	9	7	2	1	
5.5714	5	7	4	3	1		6.8	6	5	4	1	1	
5.6	5	5	3	2	1		6.8334	6	6	5	1	1	
5.625	5	8	5	3	1		6.8572	6	7	6	1	1	
5.6429	5	14	9	5	1		6.8889	6	9	8	1	1	
5.6667	5	3	2	1	1		6.909	6	11	10	1	1	
5.6923	5	13	9	4	1		6.9286	6	14	13	1	1	
5.7143	5	7	5	2	1		6.9375	6	16	15	1	1	
5.7333	5	15	11	4	1		7.0	6	1	1	0	1	
5.7692	5	13	10	3	1		7.0625	7	16	1	15	1	
5.7857	5	14	11	3	1		7.0833	7	12	1	11	1	
5.8182	5	11	9	2	1		7.1	7	10	1	9	1	
5.8461	5	13	11	2	1		7.125	7	8	1	7	1	

Table 1-1 Relation between Horizontal Resolution Conversion Ratio (β) and Parameters (4)

β	m	k	ℓ '1'	ℓ '0'	HRCM		β	m	k	ℓ '1'	ℓ '0'	HRCM	
7.1429	7	7	1	6	1								
7.1667	7	6	1	5	1								
7.1875	7	16	3	13	1								
7.2143	7	14	3	11	1								
7.25	7	4	1	3	1								
7.2727	7	11	3	8	1								
7.3	7	10	3	7	1								
7.3333	7	3	1	2	1								
7.375	7	8	3	5	1								
7.4	7	5	2	3	1								
7.4286	7	7	3	4	1								
7.4445	7	9	4	5	1								
7.4615	7	13	6	7	1								
7.5	7	2	1	1	1								
7.5385	7	13	7	6	1								
7.5625	7	16	9	7	1								
7.5833	7	12	7	5	1								
7.6154	7	13	8	5	1								
7.6364	7	11	7	4	1								
7.6666	7	3	2	1	1								
7.6923	7	13	9	4	1								
7.7143	7	7	5	2	1								
7.7334	7	15	11	4	1								
7.7692	7	13	10	3	1								
7.8	7	5	4	1	1								
7.8333	7	6	5	1	1								
7.8571	7	7	6	1	1								
7.875	7	8	7	1	1								
7.9	7	10	9	1	1								
7.9231	7	13	12	1	1								
7.9336	7	15	14	1	1								
8.0	7	1	1	0	1								