HD63085

DICEP (Document Image Compression and Expansion Processor)

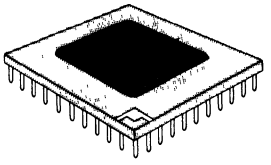
– PRELIMINARY –

The HD63085 (DICEP) is a LSI that compresses (or encodes) and expands (or decodes) the digital data representing a document image. The DICEP uses Modified Huffman (MH) coding scheme, Modified Relative Element Address Designate (MR) coding scheme and Modified MR (M^2R) coding scheme which are compatible with the CCITT (Comité Consultatif International Télégraphique et Téléphonique) recommendations for Group 3 and Group 4 facsimile apparatus.

As the DICEP stores coding and decoding algorithms in the microprogram ROM as firmare, a single MPU command allows this LSI to encode or decode a scan line of digital data.

This LSI is suitable for Group 3 and Group 4 facsimile apparatus, file serves, intelligent copies, terminals, word processors, laser beam printers and other office automation systems.

HD63085Y-8

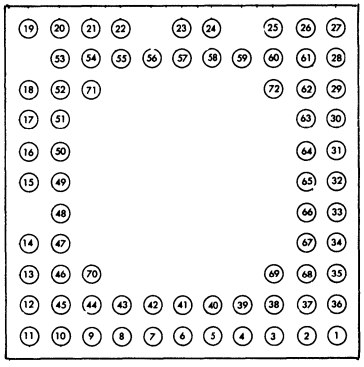


(PC-72)

■ FEATURES

- Various coding schemes ..... MH, MR, M^2R and Run Length coding
- Compatible with the CCITT recommendation for Group 3 and Group 4 facsimile apparatus
- Interfaceable with either Motorola type MPU or Intel type MPU
- DMA capability through the document image bus
  4M Byte/sec (at input clock frequency of 32 MHz)
- A variety of programmable parameters
  - The length of a scan line : 0 ~ 65535 bits
  - The number of RTC or EOL code words: 0 ~ 65535
  - Programmable starting address
  - Coding and decoding of a desired part of a document
- Selectable document image bus size
  Document image bus : 8 bits or 16 bits
  System bus : 8 bits
- 64K Bytes of document image memory is available independently of the MPU
- 2 μm CMOS process technology
- Single 5V supply

● PIN ARRANGEMENT



Pin No	Function	Pin No	Function	Pin No	Function
1	MA/MD_0	25	68/80	49	$\overline{DMA}$
2	MA/MD_1	26	NC	50	V_{SS}
3	MA/MD_4	27	$\overline{RESET}$	51	$\overline{low}$
4	MA/MD_4	28	V_{DD}	52	$\overline{DACK0}$
5	MA/MD_8	29	D_0	53	$\overline{DRQT1}$
6	MA/MD_{10}	30	D_3	54	NC
7	MA/MD_{12}	31	D_4	55	$\overline{CS}$
8	MA/MD_{14}	32	D_5	56	DRQT0
9	V_{SS}	33	V_{DD}	57	BRQT
10	TESTO	34	READY	58	A2
11	4CLK	35	MAS	59	A0
12	TDATA	36	MA/MD1	60	IRQT
13	VDS	37	MA/MD3	61	V_{DD}
14	$\overline{MW}$	38	MA/MD5	62	D_1
15	SET	39	MA/MD7	63	D_2
16	V_{SS}	40	MA/MD9	64	D_6
17	$\overline{IOR}$	41	MA/MD11	65	D_7
18	DTC	42	MA/MD13	66	V_{DD}
19	R/$\overline{W}$	43	MA/MD15	67	NC
20	AGE	44	V_{SS}	68	$\overline{MAEN}$
21	$\overline{DS}$	45	TEST1	69	NC
22	$\overline{DACK1}$	46	$\overline{LDS}$	70	NC
23	$\overline{BACK}$	47	$\overline{MDEN}$	71	NC
24	A1	48	$\overline{MR}$	72	NC

1.1 Absolute Maximum Rating

No	Item	Symbol	Value	Unit
1	Supply Voltage	VDD *	-0.3 to +7.0	V
2	Input Voltage	Vin *	-0.3 to +7.0	V
3	Operating Temperature	Topr	0 to +70	°C
4	Storage Temperature	Tstg	-55 to +150	°C

* Voltages referenced to Vss=0V.

<Recommended Operating Conditions>

No	Item	Symbol	min	typ	max	Unit
1	Supply Voltage	VDD *	4.75	5	5.25	V
2	Input Voltage	ViL *	-0.3	-	0.8	V
3		ViH *	2.2	-	VDD	V
4	Operating Temperature	Topr	0	25	70	°C

* Voltages referenced to Vss=0V.

1.2 DC Characteristics

(VDD=5.0V±5%, Vss=0V, Ta=0 to +70°C)

No	Item	Symbol	Test Condition	min	typ	max	Unit
1	Input High Voltage	VIH		2.2	-	VDD	V
2	Input Low Voltage	VIL		-0.3	-	0.8	V
3	Input Leakage Voltage	IIN	Vin=0 to 5.25V	-10	-	10	μA
4	Three-State (Off State) Leakage Current	Itsi	Vin=0 to 5.25V	-10	-	10	μA
5	Output High Voltage	VOH	IOH=-400μA	2.4	-	-	V
6	Output Low Voltage	VOL	IOL= 2mA	-	-	0.4	V
7	Standby Current	IDDS		-	-	1	mA
8	Power Dissipation	PD			150	-	mW

<Capacitance>

No	Item	Symbol	Test Codition	min	typ	max	Unit
1	Input Capacitance	CIN	f = 1MHz			8	pF
2	Output Capacitance	COUT				10	pF
3	Input/Output Capacitance	CI/O				12	pF

* These paremeters are sample values.

1.3 AC Characteristics

1.3.1 Clock Timing

(VDD=5.0V±5%, Vss=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
4CLK Cycle Time	ϕ4CLK	Fig. 1-1				ns	4CLK
4CLK Pulse Width	PWH PWL	Fig. 1-1				ns	4CLK
4CLK Rise Time	tr	Fig. 1-1				ns	4CLK
4CLK Fall Time	tf	Fig. 1-1				ns	4CLK

1.3.2 System Bus Timing

1.3.2.1 Using a Motorola MPU (68000, 6800, etc.)

(VDD=5.0V±5%, Vss=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
DS Cycle Time	tCYCE	Fig. 1-2 Fig. 1-5	500			ns	DS
DS Pulse Width	PWEH PWEL	Fig. 1-2 Fig. 1-5	220			ns	DS
DS Rise or Fall Time	tr tf	Fig. 1-2 Fig. 1-5			25	ns	DS
Address Setup Time	tAS	Fig. 1-2	70			ns	$\overline{CS}_1$, A0-A2, R/W
Address Hold Time	tAH	Fig. 1-2	30			ns	$\overline{CS}_1$, A0-A2, R/W
Output Data Delay Time	tDDR	Fig. 1-2 Fig. 1-5			180	ns	D0-D7
Output Data Hold Time	tDHR	Fig. 1-2 Fig. 1-5	10			ns	D0-D7
Input Data Setup Time	tDSW	Fig. 1-2 Fig. 1-5	60			ns	D0-D7
Input Data Hold Time	tDHW	Fig. 1-2 Fig. 1-5	40			ns	D0-D7
IRQT Release Time	tIRQT	Fig. 1-2				ns	IRQT
$\overline{DACKI}$ Setup Time	tAS	Fig. 1-5	70			ns	$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tAH	Fig. 1-5	30			ns	$\overline{DACKI}$
DRQTO Release Time	tDRQTO	Fig. 1-5				ns	DRQTO

1.3.2.2 Using and Intel Type MPU (8086, 8080, etc.)

(VDD=5.0V±5%, Vss=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Address Setup Time	tAR	Fig. 1-3	70				$\overline{CS}$, A0-A2,
Address Hold Time	tRA	Fig. 1-3	30				$\overline{CS}$, A0-A2,
Output Data Delay Time	tRD	Fig. 1-3 Fig. 1-6			180		D0-D7
Output Data Hold Time	tDR	Fig. 1-3 Fig. 1-6	10				D0-D7
Read Pulse Width	tRW	Fig. 1-3 Fig. 1-6	200				DS
Adress Setup Time	tAW	Fig. 1-4	70				$\overline{CS}$, A0-A2
Address Hold Time	tWA	Fig. 1-4	30				$\overline{CS}$, A0-A2
Input Data Setup Time	tWD	Fig. 1-4 Fig. 1-7	60				D0-D7
Input Data Hold Time	tDW	Fig. 1-4 Fig. 1-7	40				D0-D7
Write Pulse Width	tWW	Fig. 1-4 Fig. 1-7	200				R/$\overline{W}$
IRQT Release Time	tIRQT	Fig. 1-3					IRQT
$\overline{DACKI}$ Setup Time	tAR	Fig. 1-6	70				$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tRA	Fig. 1-6	30				$\overline{DACKI}$
$\overline{DACKI}$ Setup Time	tAW	Fig. 1-7	70				$\overline{DACKI}$
$\overline{DACKI}$ Hold Time	tWA	Fig. 1-8	30				$\overline{DACKI}$
DRQTO Release Time	tDRQTO	Fig. 1-6 Fig. 1-7					DRQTO

1.3.3 Document Image Bus Timing

(VDD=5.0V±5%, Vss=0V, Ta=0 to +70°C, Cout=140pF unless otherwise noted.
However, the values in the parentheses are the values at Cout=50pF.)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Address Enable Active Delay Time	tDAEL	Fig. 1-8 Fig. 1-9		(70)	150	ns	$\overline{\text{MAEN}}$
Address Enable Inactive Delay Time	tDAEH	Fig. 1-8 Fig. 1-9		(70)	140	ns	$\overline{\text{MAEN}}$
Address Strobe Active Delay Time	tDASH	Fig. 1-8 Fig. 1-9		(70)	140	ns	MAS
Address Strobe Inactive Delay Time	tDASL	Fig. 1-8 Fig. 1-9		(60)	120	ns	MAS
Data Strobe Valid Delay Time	tDDSV	Fig. 1-8 Fig. 1-9		(60)	140	ns	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$
Data Strobe Active Delay Time	tDDSL	Fig. 1-8 Fig. 1-9		(75)	140	ns	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$
Data Strobe Inactive Delay Time	tDDSH	Fig. 1-8 Fig. 1-9		(75)	140	ns	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$
Data Strobe Float Delay Time	tDDSX	Fig. 1-8 Fig. 1-9		( )		ns	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$
Data Enable Active Delay Time	tDDEL	Fig. 1-8		(80)	130	ns	$\overline{\text{MDEN}}$
Data Enable Inactive Delay Time	tDDEH	Fig. 1-8		(75)	140	ns	$\overline{\text{MDEN}}$
Read Valid Delay Time	tDRDV	Fig. 1-8 Fig. 1-9		(60)	140	ns	$\overline{\text{IOR}}$, $\overline{\text{MR}}$
Read Active Delay Time	tDRDL	Fig. 1-8 Fig. 1-9		(70)	140	ns	$\overline{\text{IOR}}$, $\overline{\text{MR}}$
Read Inactive Delay Time	tDRDH	Fig. 1-8 Fig. 1-9		(75)	140	ns	$\overline{\text{IOR}}$, $\overline{\text{MR}}$
Read Float Delay Time	tDRDX	Fig. 1-8 Fig. 1-9		( )		ns	$\overline{\text{IOR}}$, $\overline{\text{MR}}$

(to be continued)

(continued)

Item	Symbol	Test Condition	min	typ	max	Unit	Application Terminal
Write Valid Delay Time	tDWRV	Fig. 1-8 Fig. 1-9		(60)	140	ns	$\overline{IOW}$, $\overline{MW}$
Write Active Delay Time	tDWRL	Fig. 1-8 Fig. 1-9		(70)	140	ns	$\overline{IOW}$, $\overline{MW}$
Write Inactive Delay Time	tDWRH	Fig. 1-8 Fig. 1-9		(80)	140	ns	$\overline{IOW}$, $\overline{MW}$
Write Float Delay Time	tDWRX	Fig. 1-8 Fig. 1-9		( )		ns	$\overline{IOW}$, $\overline{MW}$
Address Valid Delay Time	tMAV	Fig. 1-8 Fig. 1-9		(75)	140	ns	MA/MD0 - MA/MD15
Address Hold Delay Time	tMAH	Fig. 1-8 Fig. 1-9	25	(50)		ns	MA/MD0 - MA/MD15
Data Setup Time (Read)	tDSR	Fig. 1-8	10	(10)		ns	MA/MD0 - MA/MD15
Data Hold Time (Read)	tDHR	Fig. 1-8	70	(70)		ns	MA/MD0 - MA/MD15
Data Delay Time (Write)	tDDW	Fig. 1-8		(95)	170	ns	MA/MD0 - MA/MD15
Data Hold Time (Write)	tDHW	Fig. 1-8	15	(15)		ns	MA/MD0 - MA/MD15
DMA Acknowlege Active Delay Time	tDAKL	Fig. 1-9		(60)	140	ns	$\overline{DACKO}$
DMA Acknowlege Inactive Delay Time	tDAKH	Fig. 1-9		(65)	140	ns	$\overline{DACKO}$
DMA Active Delay Time	tDDMAL	Fig. 1-9		(80)	140	ns	$\overline{DMA}$
DMA Inactive Delay Time	tDDMAH	Fig. 1-9		(70)	140	ns	$\overline{DMA}$
DTC Active Delay Time	tDDTCH	Fig. 1-9		4CLK + 75	4CLK +140	ns	DTC
DTC Inactive Delay Time	tDDTCL	Fig. 1-9		(50)	130	ns	DTC

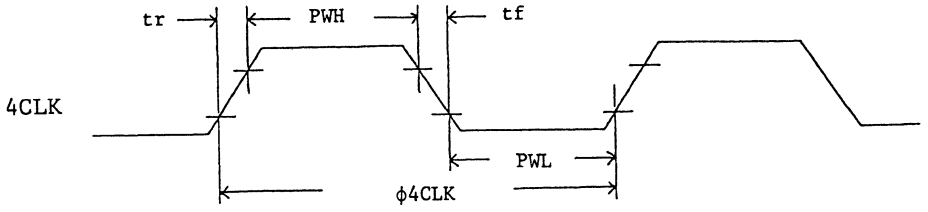


Fig. 1-1 Clock Timing

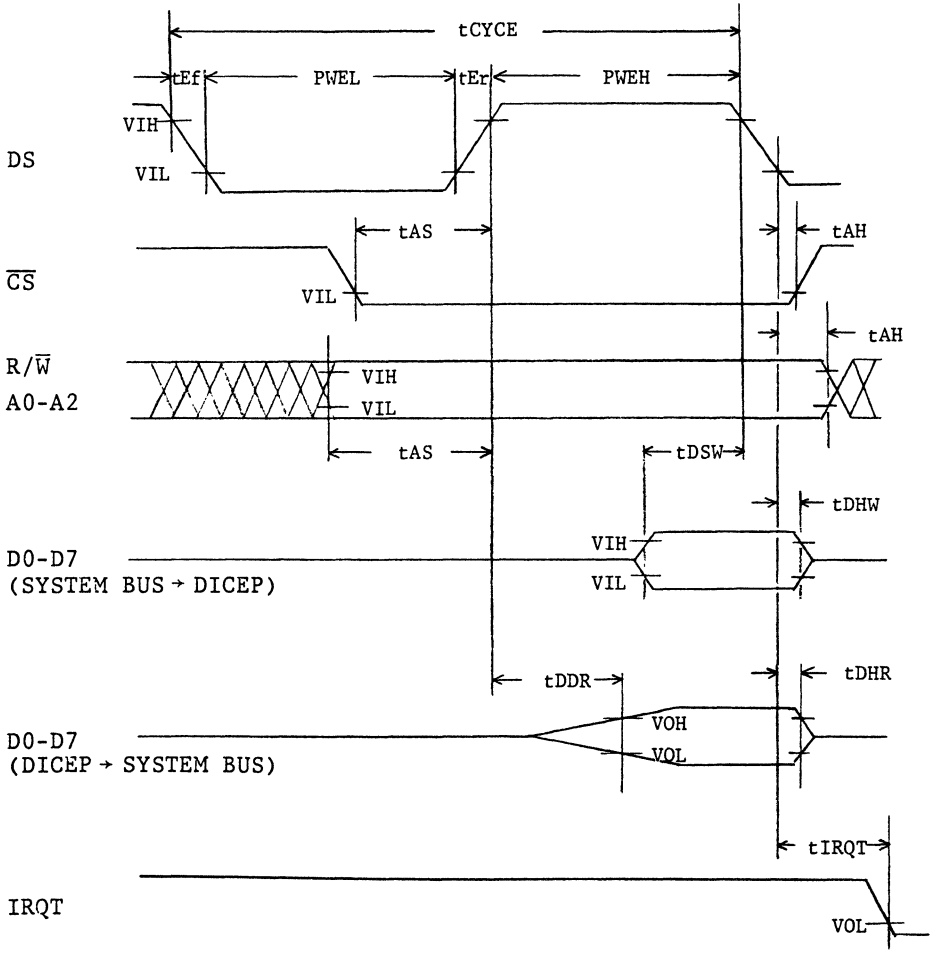


Fig. 1-2 System Bus Read/Write Timing

(68 Type MPU)

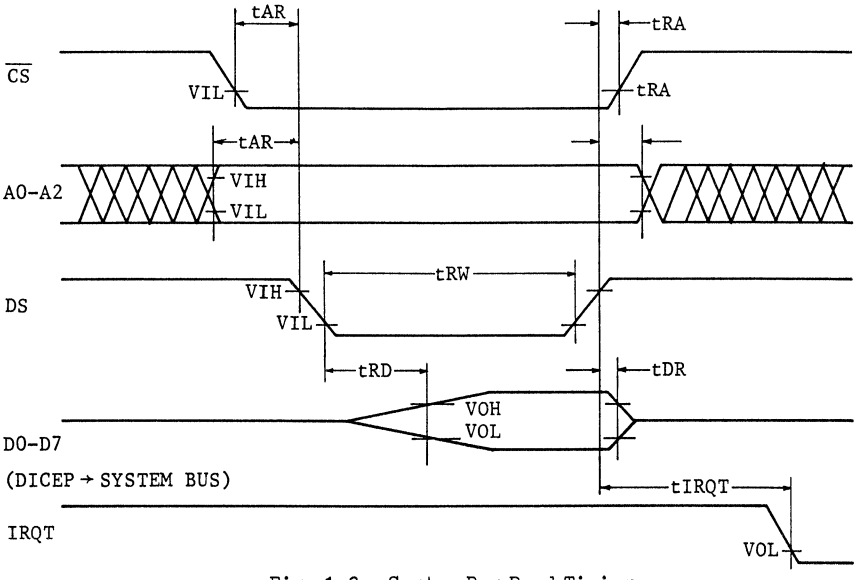


Fig. 1-3 System Bus Read Timing
(80 Type MPU)

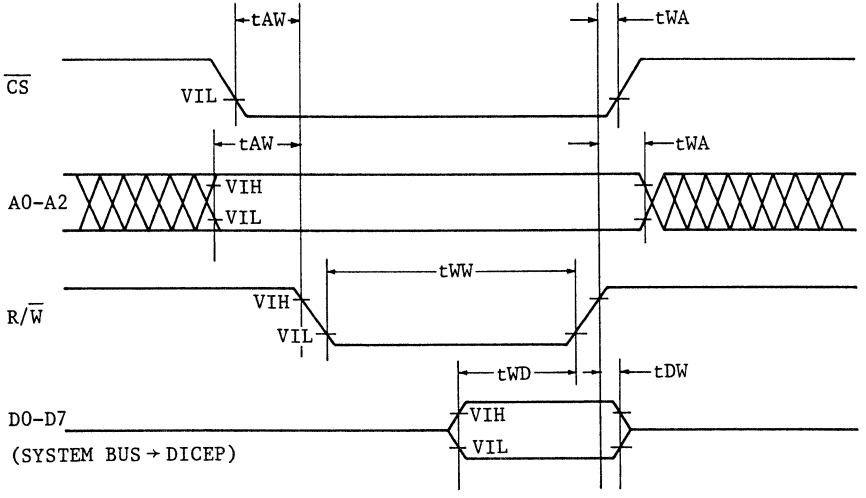


Fig. 1-4 System Bus Write Timing
(80 Type MPU)

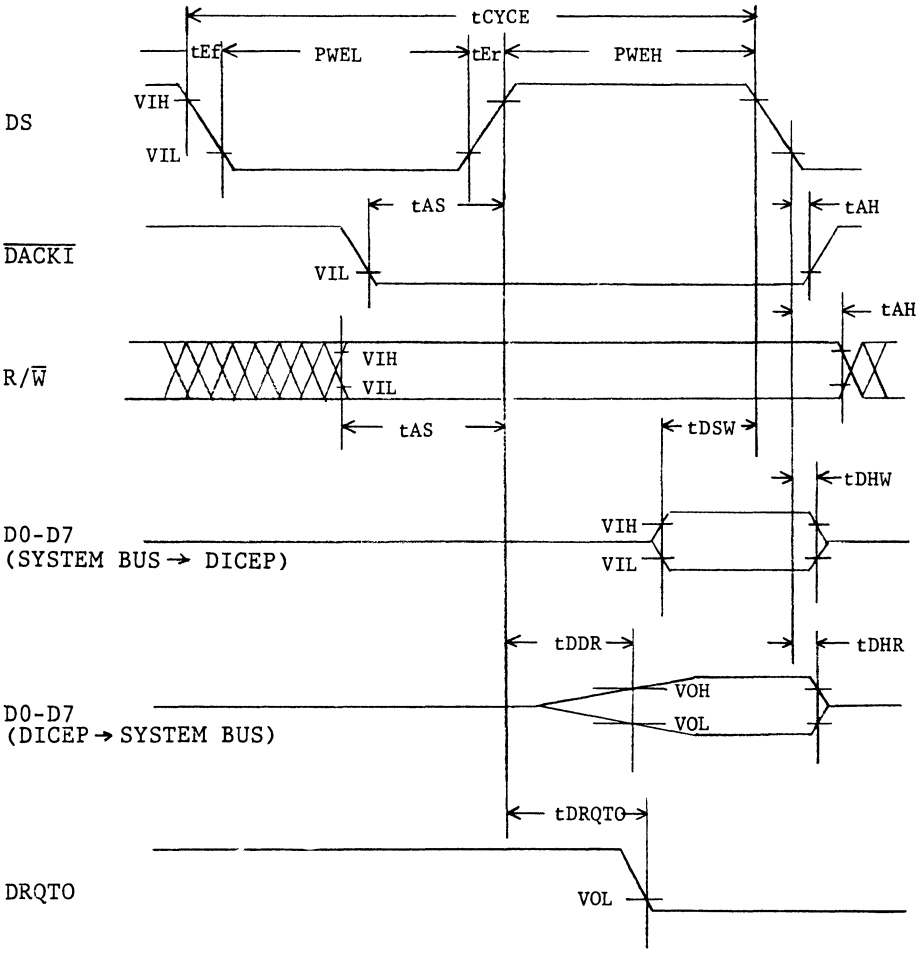


Fig. 1-5 System Bus DMA Timing
(Motorola Type MPU)

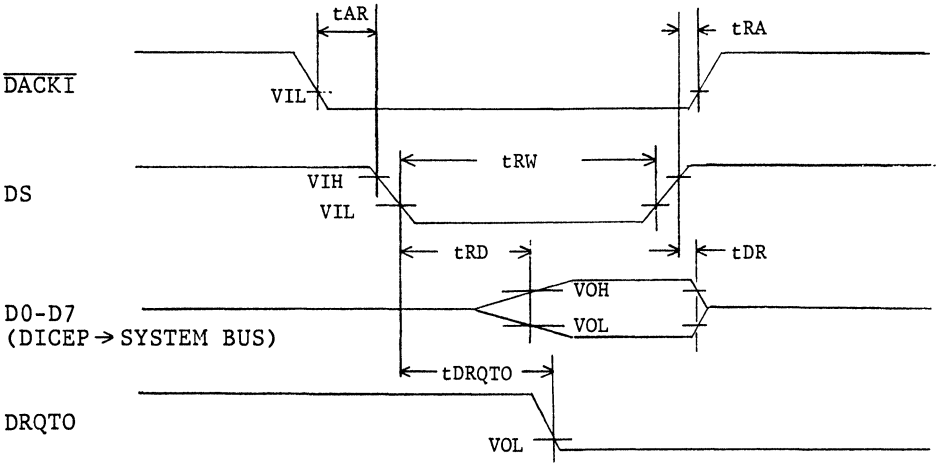


Fig. 1-6 System Bus DMA Timing
(DICEP→SYSTEM BUS)
(80 Type MPU)

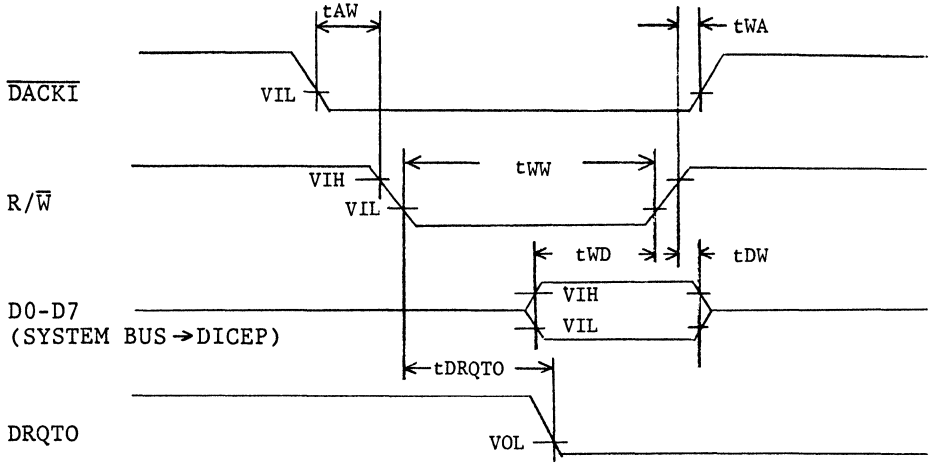


Fig. 1-7 System Bus DMA Timing
(SYSTEM BUS→DICEP)
(Intel Type MPU)

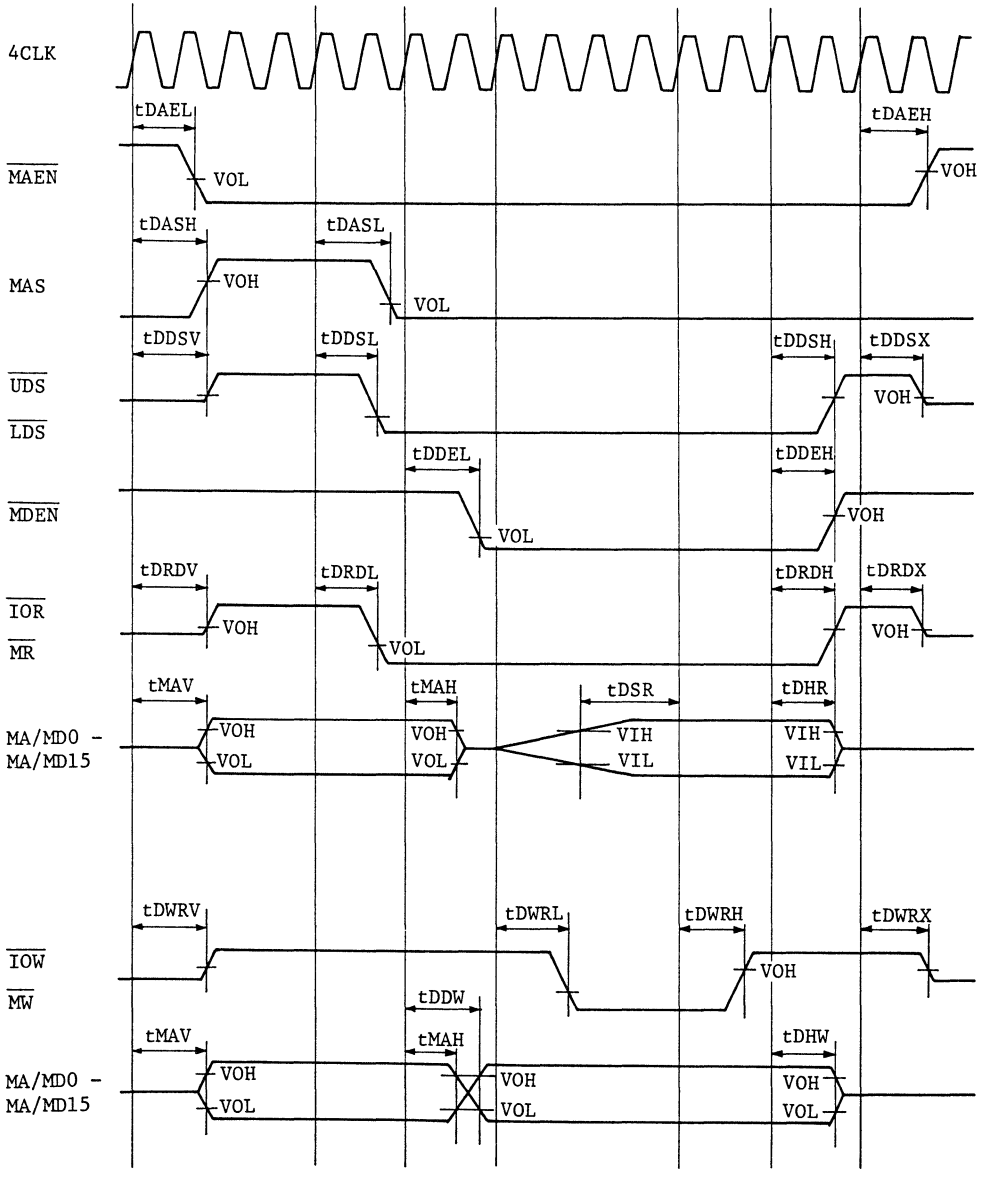


Fig. 1-8 Document Image Bus Read/Write Timing

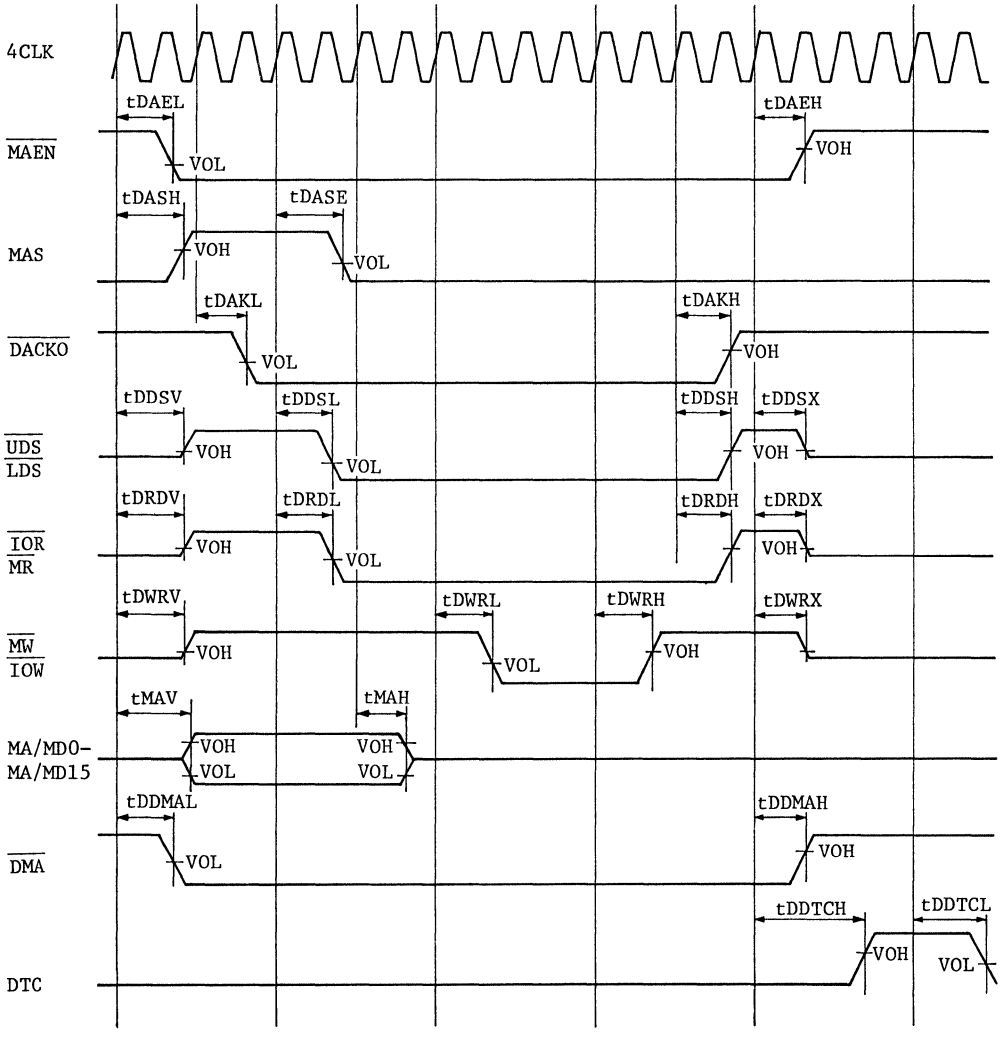


Fig. 1-9 Document Image Bus DMA Timing