HD63310 S-DPRAM (Smart Dual Port RAM)

The HD63310 (S-DPRAM) is a high intelligent DPRAM, which provide a communication path between multiprocessor systems.

The HD63310 has 1024 x 8 bit RAM, 62 x 8 bit registers and individual dual I/O ports. The dual ports perform read/write operations independently and simultaneously.

User can select one of the two mode (DPRAM or FIFO mode) by the program. This architecture makes it possible to communicate efficiently according to applications.

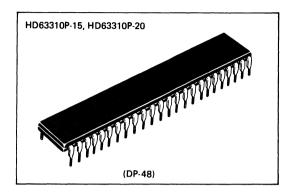
■ FEATURES

- 2 independent asynchronous bus operation Address/Data bus configurable as multiplexed or non-multiplexed bus.
- Dual port large scale data buffer space
 - Dual port RAM mode: 1024 byte
 - · FIFO mode: 2 FIFOs for 1024 byte
- 62 internal registers
 - Semaphore registers which support multi-processing (8 bit)
- · 32 registers which user can use freely
- Access Time
 - 150 ns/200 ns
- Low power consumption 2 μm full CMOS circuit

■ TYPE OF PRODUCTS

Type No.	Access Time	
HD63310P-15	150 ns	
HD63310P-20	200 ns	

-ADVANCE INFORMATION-

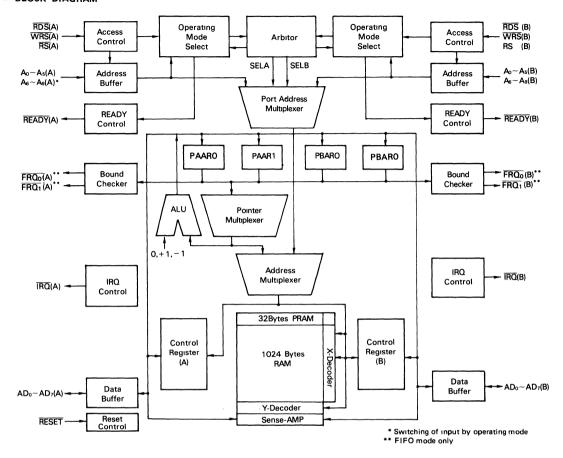


■ PIN ARRANGEMENT

V _∞ I	48	RESET
A ₀ (A) 2	47	A ₀ (B)
A,(A) 3	46	A,(B)
A ₂ (A) 4	45	A ₂ (B)
A ₃ (A) 5	44	A ₃ (B)
A ₄ (A) 6	43	A ₄ (B)
A _s (A) 7	42	A _s (B)
$A_s(A)(A_s(A)/FRQ_s(A))$ 8	41	A (B)(A (B)/FRQ (B))
$A_7(A)(A_9(A)/FRQ_1(A))$ 9	40	A,(B)(A,(B)/FRQ,(B))
A ₆ (A)(AS(A)/ -) 10	39	A ₈ (B)(AS(B)/ -)
RS(A)	38	RS(B)
RDS(A) 12	37	RDS(B)
WRS(A) 13	36	WRS(B)
READY(A) 14	35	READY(B)
IRQ(A) [15	34	IRQ(B)
V _{ss} [16]	33	V _{ss}
AD ₀ (A) 17	32	AD₀(B)
AD ₁ (A) 18	31	AD _I (B)
AD₂(A) 19	30	AD ₂ (B)
AD ₃ (A) 20	29	AD ₃ (B)
AD ₄ (A) 21	28	AD₄(B)
AD ₅ (A) 22	27	AD _s (B)
AD ₆ (A) 23	26	AD ₆ (B)
AD ₇ (A) 24	25	AD ₇ (B)

(Top View)

■ BLOCK DIAGRAM



■ SYSTEM BLOCK DIAGRAM

