HD63450, HD63450Y, HD63450P
HD63450PS, HD63450CP
CMOS Direct Memory Access Controller

SEPTEMBER, 1989

HITACHI

The HD63450 is a CMOS Direct Memory Access Controller (DMAC). It is upwardly compatible with the NMOS DMAC HD68450.

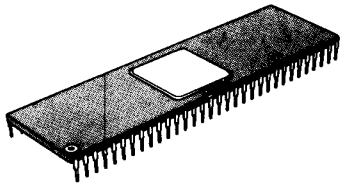
In addition to the NMOS DMAC HD68450 features, the HD63450 performs one or several blocks of data transfer (Operand; byte, word, or long word) between memory and peripheral device at high speed. The block transfer restart operation is provided (Multi-Block Transfer with $\overline{\text{DONE}}$ Mode). The number of operands in a block is determined by a transfer count.

Fabricated in CMOS for lower power dissipation.

■ FEATURES

- HD68000 Bus Compatible
- 4 independent DMA Channels with Programmable Priority
- Memory-to-Memory, Memory-to-Device, Device-to-Memory Transfers
- Programmable 8-Bit or 16-Bit I/O Device Types
- Auto-Request and External-Request Transfer Modes
- Interface Lines for Requesting, Acknowledging, and Incidental Control of the Peripheral Devices
- Block Transfer Operation
  - In Single-Block : ● Unchaining Transfer
  - In Multi-Block : ● Continue Mode Transfer
    - ● Array-Chaining and Linked-Array-Chaining Transfers
    - ● Multi-Block Transfer with $\overline{\text{DONE}}$
- 68000 Bus Exception Processing Support
- 2 Vectored Interrupts for each Channel
- Variable System Bus Bandwidth Rate Utilization
- Fast Transfer Rates: Up to 6.25 Mbytes/sec. at 12.5MHz
- CMOS +5 Volts Operation

HD63450-8,
HD63450-10,
HD63450-12



(DC-64)

HD63450Y-8,
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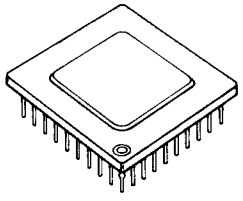

(PGA-68)

HD63450P-8,
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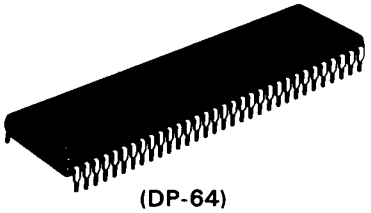

(DP-64)

HD63450PS-8,
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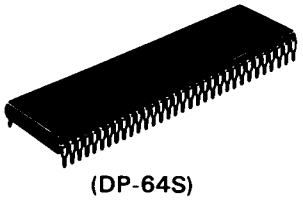

(DP-64S)

HD63450CP-8,
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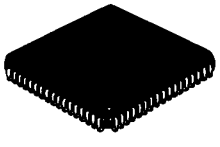


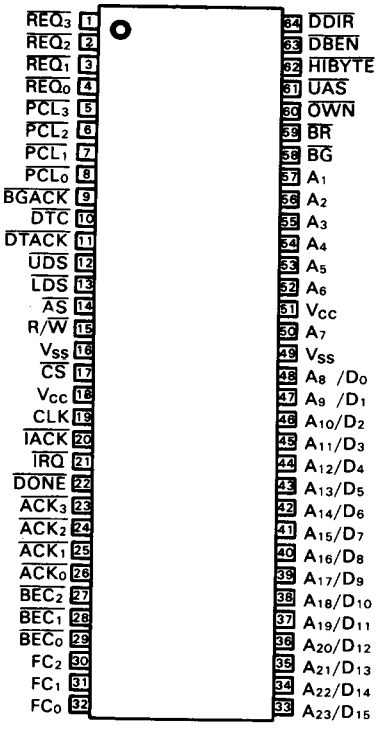
(CP-68)

■ TYPE OF PRODUCTS

Type No.	Bus Timing	Packaging
HD63450-8	8MHz	DC-64
HD63450-10	10MHz	
HD63450-12	12.5MHz	
HD63450Y-8	8MHz	PGA-68
HD63450Y-10	10MHz	
HD63450Y-12	12.5MHz	
HD63450P-8	8MHz	DP-64
HD63450Y-10	10MHz	
HD63450Y-12	12.5MHz	
HD63450PS-8	8MHz	DP-64S
HD63450PS-10	10MHz	
HD63450PS-12	12.5MHz	
HD63450CP-8	8MHz	CP-68
HD63450CP-10	10MHz	
HD63450CP-12	12.5MHz	

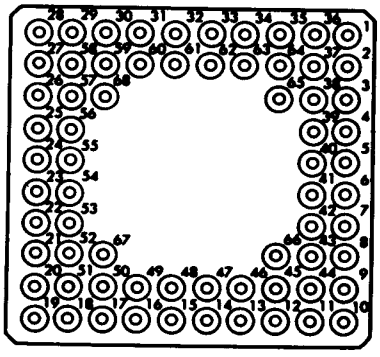
■ PIN ARRANGEMENT

● HD63450, HD63450P, HD63450PS



(Top View)

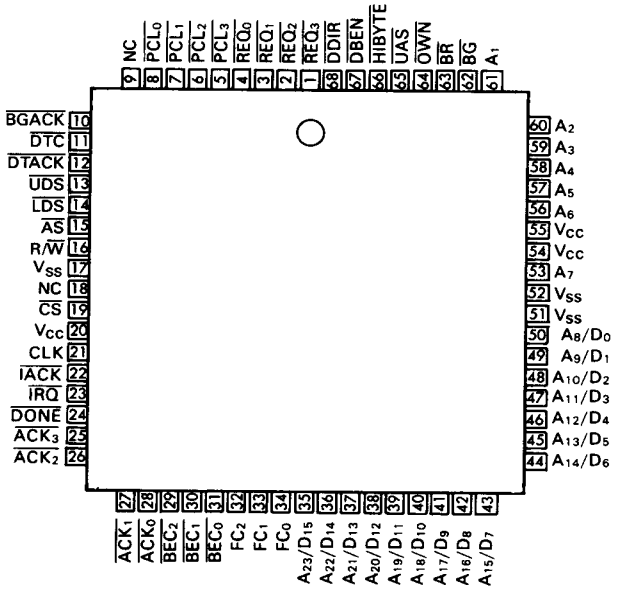
● HD63450Y



(Bottom View)

Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N/C	18	$\overline{PCL_1}$	35	A_{19}/D_{11}	52	$\overline{BGACK}$
2	A_{13}/D_5	19	$\overline{DTACK}$	36	A_{17}/D_9	53	$\overline{LDS}$
3	A_{11}/D_3	20	$\overline{UDS}$	37	A_{15}/D_7	54	V_{SS}
4	A_{10}/D_2	21	$\overline{AS}$	38	A_{12}/D_4	55	V_{CC}
5	A_8/D_0	22	$R/\overline{W}$	39	A_9/D_1	56	$\overline{DONE}$
6	A_7	23	N/C	40	V_{SS}	57	$\overline{IRQ}$
7	A_6	24	$\overline{CS}$	41	V_{CC}	58	$\overline{ACK_2}$
8	A_5	25	CLK	42	A_4	59	$\overline{BEC_2}$
9	A_3	26	$\overline{IACK}$	43	A_2	60	$\overline{BEC_0}$
10	N/C	27	$\overline{ACK_3}$	44	$\overline{BG}$	61	FC_0
11	$\overline{BR}$	28	$\overline{ACK_0}$	45	$\overline{OWN}$	62	A_{21}/D_{13}
12	$\overline{UAS}$	29	$\overline{BEC_1}$	46	$\overline{HIBYTE}$	63	A_{18}/D_{10}
13	$\overline{DBEN}$	30	FC_2	47	$\overline{DDIR}$	64	A_{16}/D_8
14	$\overline{REQ_3}$	31	FC_1	48	$\overline{REQ_1}$	65	A_{14}/D_6
15	$\overline{REQ_2}$	32	A_{23}/D_{15}	49	$\overline{PCL_2}$	66	A_1
16	$\overline{REQ_0}$	33	A_{22}/D_{14}	50	$\overline{PCL_0}$	67	$\overline{DTC}$
17	$\overline{PCL_3}$	34	A_{20}/D_{12}	51	N/C	68	$\overline{ACK_1}$

● HD63450CP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3～+7.0	V
Input Voltage	V_{in}*	−0.3～V_{CC}+0.3	V
Operating Temperature Range	T_{opr}	0～+70	°C
Storage Temperature	T_{stg}	−55～+150	°C

*With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent damage to the device may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditons. If these conditions are exceeded, it could affect reliability of the device.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input Voltage	V_{IH}*	2.0		V_{CC}	V
	V_{IL}*	−0.3		0.8	V
Operating Temperature	T_{opr}	0	25	70	°C

*With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{CC}=5V±5%, V_{SS}=0V, T_a=0～+70°C, unless otherwise noted.)

Item		Symbol	Test Condition	min	typ	max	Unit
Input "High" Voltage		V_{IH}		2.0		V_{CC}	V
Input "Low" Voltage		V_{IL}		V_{SS}−0.3		0.8	V
Input Leakage Current	$\overline{CS}$, $\overline{IACK}$, $\overline{BG}$, CLK, $\overline{BEC_0}$～$\overline{BEC_2}$, $\overline{REQ_0}$～$\overline{REQ_3}$	I_{in}				10	μA
Three-State (Off State) Input Current	A_1～A_7, D_0～D_{15}/A_8～A_{23}, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{UAS}$, $\overline{DTACK}$, $\overline{BGACK}$, $\overline{OWN}$, $\overline{DTC}$, $\overline{HIBYTE}$, $\overline{DDIR}$, $\overline{DBEN}$, FC_0～FC_2, $\overline{PCL_0}$～$\overline{PCL_3}$	I_{TSI}				10	μA
Open Drain (Off State) Input Current	$\overline{IRQ}$, $\overline{DONE}$	I_{ODI}				20	μA
Output "High" Voltage	A_1～A_7, D_0～D_{15}/A_8～A_{23}, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{UAS}$, $\overline{DTACK}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{OWN}$, $\overline{DTC}$, $\overline{HIBYTE}$, $\overline{DDIR}$, $\overline{DBEN}$, $\overline{ACK_0}$～$\overline{ACK_3}$, $\overline{PCL_0}$～$\overline{PCL_3}$, FC_0～FC_2	V_{OH}	I_{OH}=−400μA	V_{CC}−2.0			V
Output "Low" Voltage	A_1～A_7, FC_0～FC_2	V_{OL}	I_{OL}=3.2mA			0.5	V
	D_0～D_{15}/A_8～A_{23}, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{DTACK}$, $\overline{BR}$, $\overline{OWN}$, $\overline{DTC}$, $\overline{HIBYTE}$, $\overline{DDIR}$, $\overline{DBEN}$, $\overline{ACK_0}$～$\overline{ACK_3}$, $\overline{UAS}$, $\overline{PCL_0}$～$\overline{PCL_3}$, $\overline{BGACK}$	V_{OL}	I_{OL}=5.3mA			0.5	V
	$\overline{IRQ}$, $\overline{DONE}$	V_{OL}	I_{OL}=8.9mA			0.5	V
Power Dissipation		P_D	f=8MHz, V_{CC}=5.0V, T_a=25°C		0.5	1.0	W
Capacitance		C_{in}	V_{in}=0V, T_a=25°C, f=1MHz			15	pF

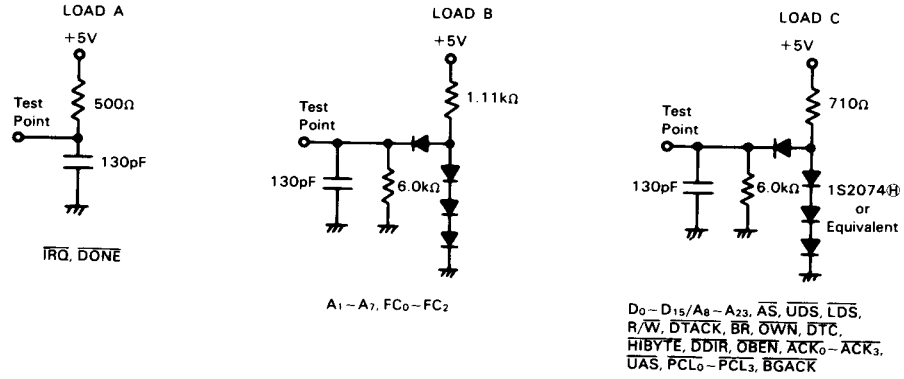


Figure 1 Test Loads

● AC ELECTRICAL SPECIFICATIONS (V_{CC}=5V±5%, V_{SS}=0V, T_a=0~+70°C, unless otherwise noted.)

No.	Item	Symbol	Test Condition	8MHz Version		10MHz Version		12.5MHz Version		Unit
				min	max	min	max	min	max	
	Frequency of Operation	f		4.0	8.0	4.0	10.0	4.0	12.5	MHz
1	Clock Period	t_{cyc}		125	250	100	250	80	250	ns
2	Clock Width Low	t_{CL}		55	125	45	125	35	125	ns
3	Clock Width High	t_{CH}		55	125	45	125	35	125	ns
4	Clock Fall Time	t_{Cf}			10		10		5	ns
5	Clock Rise Time	t_{Cr}			10		10		5	ns
6	Asynchronous Input Setup Time	t_{ASI}		20		15		15		ns
7	Data in to $\overline{DBEN}$ Low	t_{DIDBL}		0		0		0		ns
8	$\overline{DTACK}$ Low to Data Invalid	t_{DTLDI}		0		0		0		ns
9	Address in to $\overline{AS}$ in Low	t_{AIASL}		0		0		0		ns
10	$\overline{AS}$, $\overline{DS}$ in High to Address in Invalid	t_{SIHAIV}		0		0		0		ns
10A	$\overline{DS}$ in High to $\overline{CS}$ High	t_{DSHCSH}			1.0		1.0	clk.per.	1.0	clk.per.
11	Clock High to $\overline{DDIR}$ Low	t_{CHDRL}			70		60		55	ns
12	Clock High to $\overline{DDIR}$ High	t_{CHDRH}			70		60		55	ns
13	$\overline{DS}$ in High to $\overline{DDIR}$ High Impedance	t_{DSHDRZ}	Figure1		120		110		110	ns
14	Clock Low to $\overline{DBEN}$ Low	t_{CLDBL}			70		60		55	ns
15	Clock Low to $\overline{DBEN}$ High	t_{CLDBH}	~		70		60		55	ns
16	$\overline{DS}$ in High to $\overline{DBEN}$ High Impedance	t_{DSHDBZ}			120		110		110	ns
17	Clock High to Data Out Valid (MPU read)	t_{CHDVM}	Figure8		180		160		140	ns
18	$\overline{DS}$ in High to Data Out Invalid	t_{DSHDZn}		0		0		0		ns
19	$\overline{DS}$ in High to Data High Impedance	t_{DSHDZ}			120		110		110	ns
20	Clock Low to $\overline{DTACK}$ Low	t_{CLDTL}			70		60		55	ns
21	$\overline{DS}$ in High to $\overline{DTACK}$ High	t_{DSHDTH}			110		110		110	ns
22	$\overline{DTACK}$ Width High	t_{DTH}		10		10		10		ns
23	$\overline{DS}$ in High to $\overline{DTACK}$ High Impedance	t_{DSHDTZ}			180		160		160	ns
24	$\overline{DTACK}$ Low to $\overline{DS}$ in High	t_{DTLDSH}		0		0		0		ns
25	$\overline{REQ}$ Width Low	t_{REQL}		2.0		2.0		2.0		clk.per.
26	$\overline{REQ}$ Low to $\overline{BR}$ Low	t_{RELBRL}		250		200		160		ns
27	Clock High to $\overline{BR}$ Low	t_{CHBRL}			70		60		55	ns
28	Clock High to $\overline{BR}$ High	t_{CHBRH}			70		60		55	ns
29	$\overline{BG}$ Low to $\overline{BGACK}$ Low	t_{BGLBL}		4.5		4.5		4.5		clk.per.
30	$\overline{BR}$ Low to MPU Cycle End ($\overline{AS}$ in High)	t_{BRLASH}		0		0		0		ns

(continued next page)

No.	Item	Symbol	Test Condition	8MHz Version		10MHz Version		12.5MHz Version		Unit
				min	max	min	max	min	max	
31	MPU Cycle End ($\overline{AS}$ in High) to $\overline{BGACK}$ Low	t_{ASHBL}	Figure1 ~ Figure8	4.5	5.5	4.5	5.5	4.5	5.5	clk.per.
32	$\overline{REQ}$ Low to $\overline{BGACK}$ Low	t_{REQLBL}		6.5		6.5		6.5		clk.per.
33	Clock High to $\overline{BGACK}$ Low	t_{CHBL}			70		60		55	ns
34	Clock High to $\overline{BGACK}$ High	t_{CHBH}			70		60		55	ns
35	Clock Low to $\overline{BGACK}$ High Impedance	t_{CLBZ}			80		70		65	ns
36	Clock High to FC Valid	t_{CHFCV}			100		90		90	ns
37	Clock High to Address Valid	t_{CHAV}			120		110		100	ns
38	Clock High to Address/FC/Data High Impedance	t_{CHAZx}			100		100		100	ns
39	Clock High to Address/FC/Data Invalid	t_{CHAZn}		0		0		0		ns
40	Clock Low to Address High Impedance	t_{CLAZ}			100		90		80	ns
41	Clock High to $\overline{UAS}$ Low	t_{CHUL}			70		60		55	ns
42	Clock High to $\overline{UAS}$ High	t_{CHUH}			70		60		55	ns
43	Clock Low to $\overline{UAS}$ High Impedance	t_{CLUZ}			80		70		65	ns
44	$\overline{UAS}$ High to Address Invalid	t_{UHAI}		30		20		15		ns
45	Clock High to $\overline{AS}$, $\overline{DS}$ Low	t_{CHSL}			60		55		55	ns
46	Clock Low to $\overline{DS}$ Low (write)	t_{CLDSL}			60		55		55	ns
47	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}			70		60		60	ns
48	Clock Low to $\overline{AS}$, $\overline{DS}$ High Impedance	t_{CLSZ}			80		70		65	ns
49	$\overline{AS}$ Width Low	t_{ASL}		255		195		160		ns
50	$\overline{DS}$ Width Low	t_{DSL}		190		145		120		ns
51	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}		150		105		65		ns
52	Address/FC Valid to $\overline{AS}$, $\overline{DS}$ Low	t_{AVSL}		30		20		0		ns
53	$\overline{AS}$, $\overline{DS}$ High to Address/FC/Data Invalid	t_{SHAZ}		30		20		15		ns
54	Clock High to R/$\overline{W}$ Low	t_{CHRL}			70		60		55	ns
55	Clock High to R/$\overline{W}$ High	t_{CHRH}			70		60		55	ns
56	Clock Low to R/$\overline{W}$ High Impedance	t_{CLRZ}			80		70		65	ns
57	Address/FC Valid to R/$\overline{W}$ Low	t_{AVRL}		20		10		0		ns
58	R/$\overline{W}$ Low to $\overline{DS}$ Low (write)	t_{RLSL}		120		90		70		ns
59	$\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}		40		20		15		ns
60	Clock Low to $\overline{OWN}$ Low	t_{CLOL}			70		60		55	ns
61	Clock Low to $\overline{OWN}$ High	t_{CLOH}			70		60		55	ns
62	Clock High to $\overline{OWN}$ High Inpedance	t_{CHOZ}			80		70		65	ns
63	$\overline{OWN}$ Low to $\overline{BGACK}$ Low	t_{OLBL}		30		20		15		ns
64	$\overline{BGACK}$ High to $\overline{OWN}$ High	t_{BHOH}		30		20		15		ns
65	$\overline{OWN}$ Low to $\overline{UAS}$ Low	t_{OLUL}		30		20		15		ns
66	Clock High to $\overline{ACK}$ Low	t_{CHACL}			70		60		55	ns
67	Clock Low to $\overline{ACK}$ Low	t_{CLACL}			70		60		55	ns
68	Clock High to $\overline{ACK}$ High	t_{CHACH}			70		60		55	ns
69	$\overline{ACK}$ Low to $\overline{DS}$ Low	t_{ACLDSL}		100		80		60		ns
70	$\overline{DS}$ High to $\overline{ACK}$ High	t_{DSHACH}		30		20		15		ns
71	Clock High to $\overline{HIBYTE}$ Low	t_{CHHIL}			70		60		55	ns
72	Clock Low to $\overline{HIBYTE}$ Low	t_{CLHIL}			70		60		55	ns
73	Clock High to $\overline{HIBYTE}$ High	t_{CHHIH}			70		60		55	ns
74	Clock Low to $\overline{HIBYTE}$ High Impedance	t_{CLHIZ}			80		70		65	ns
75	Clock High to $\overline{DTC}$ Low	t_{CHDTL}			70		60		55	ns
76	Clock High to $\overline{DTC}$ High	t_{CHDTH}			70		60		55	ns

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HITACHI

No.	Item	Symbol	Test Condition	8MHz Version		10MHz Version		12.5MHz Version		Unit
				min	max	min	max	min	max	
77	Clock Low to $\overline{DTC}$ High Impedance	t_{CLDTZ}			80		70		65	ns
78	$\overline{DTC}$ Width Low	t_{DTCL}		105		80		60		ns
79	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{DTLDH}		30		20		15		ns
80	Clock High to $\overline{DONE}$ Low	t_{CHDOL}			70		60		55	ns
81	Clock Low to $\overline{DONE}$ Low	t_{CLDOL}			70		60		55	ns
82	Clock High to $\overline{DONE}$ High	t_{CHDOH}			130		120		120	ns
83	Clock Low to $\overline{DDIR}$ High Impedance	t_{CLDRZ}			80		70		65	ns
84	Clock Low to $\overline{DBEN}$ High Impedance	t_{CLDBZ}			80		70		65	ns
85	$\overline{DDIR}$ Low to $\overline{DBEN}$ Low	t_{DRLDBL}		30		20		15		ns
86	$\overline{DBEN}$ High to $\overline{DDIR}$ High	t_{DBHDRH}		30		20		15		ns
87	$\overline{DBEN}$ Low to Address/Data High Impedance	t_{DBLAZ}			17		17		17	ns
88	Clock Low to $\overline{PCL}$ Low (1/8 clock)	t_{CLPL}			70		60		55	ns
89	Clock Low to $\overline{PCL}$ High (1/8 clock)	t_{CLPH}	Figure1		70		60		55	ns
90	$\overline{PCL}$ Width Low (1/8 clock)	t_{PCLL}		4.0		4.0		4.0		clk.per.
91	$\overline{DTACK}$ Low to Data In (setup time)	t_{DALDI}	~		150		115		85	ns
92	$\overline{DS}$ High to Data Invalid (hold time)	t_{SHDI}		0		0		0		ns
93	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	Figure8	0	120	0	90	0	70	ns
94	Data Out Valid to $\overline{DS}$ Low	t_{DOSL}		0		0		0		ns
95	Data In to Clock Low (setup time)	t_{DICL}		15		15		15		ns
96	$\overline{BEC}$ Low to $\overline{DTACK}$ Low	t_{BECDAL}		50		50		50		ns
97	$\overline{BEC}$ Width Low	t_{BECL}		2.0		2.0		2.0		clk.per.
98	Clock High to $\overline{IRQ}$ Low	t_{CHIRL}			70		60		55	ns
99	Clock High to $\overline{IRQ}$ High	t_{CHIRH}			130		120		120	ns
100	$\overline{READY}$ In to $\overline{DTC}$ Low (Read)	t_{RALDTL}		145		120		100		ns
101	$\overline{READY}$ In to $\overline{DS}$ Low (Write)	t_{RALDSL}		205		170		140		ns
102	$\overline{DS}$ High to $\overline{READY}$ High	t_{DSHRAH}		0	120	0	90	0	70	ns
103	$\overline{DONE}$ In Low to $\overline{DTACK}$ Low	t_{DOLDAL}		50		50		50		ns
104	$\overline{DS}$ High to $\overline{DONE}$ In High	t_{DSHDOH}		0	120	0	90	0	70	ns
105	Asynchronous Input Hold Time	t_{ASIH}		15		15		15		ns

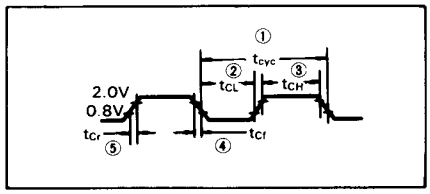


Figure 2 Input Clock Waveform

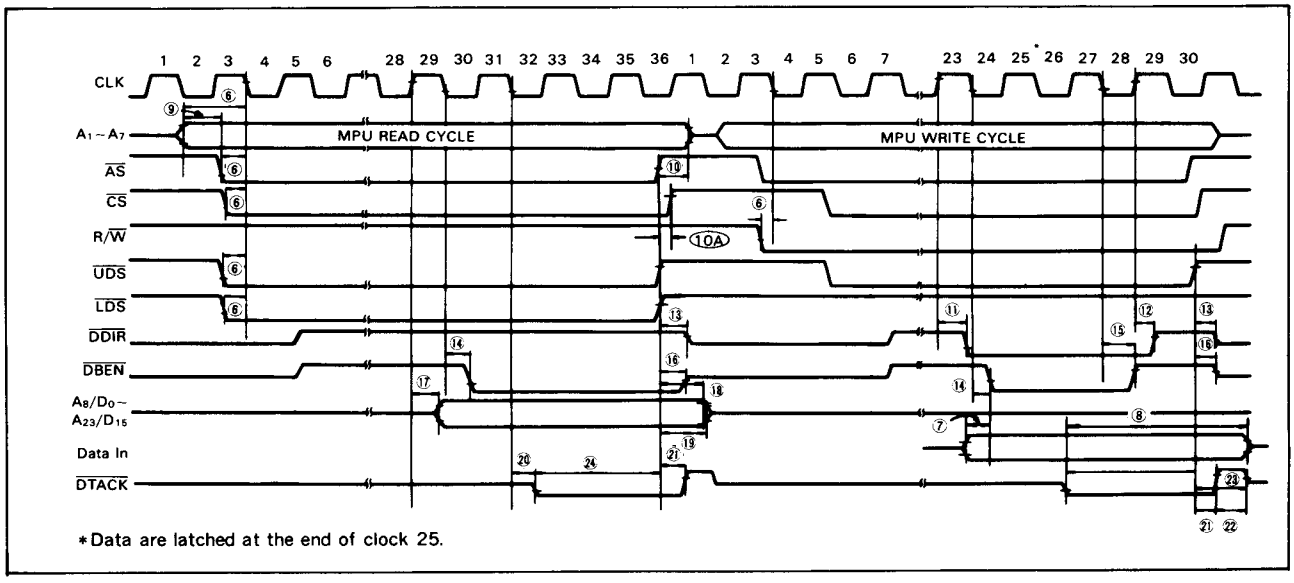


Figure 3 AC Electrical Waveforms-MPU Read/Write

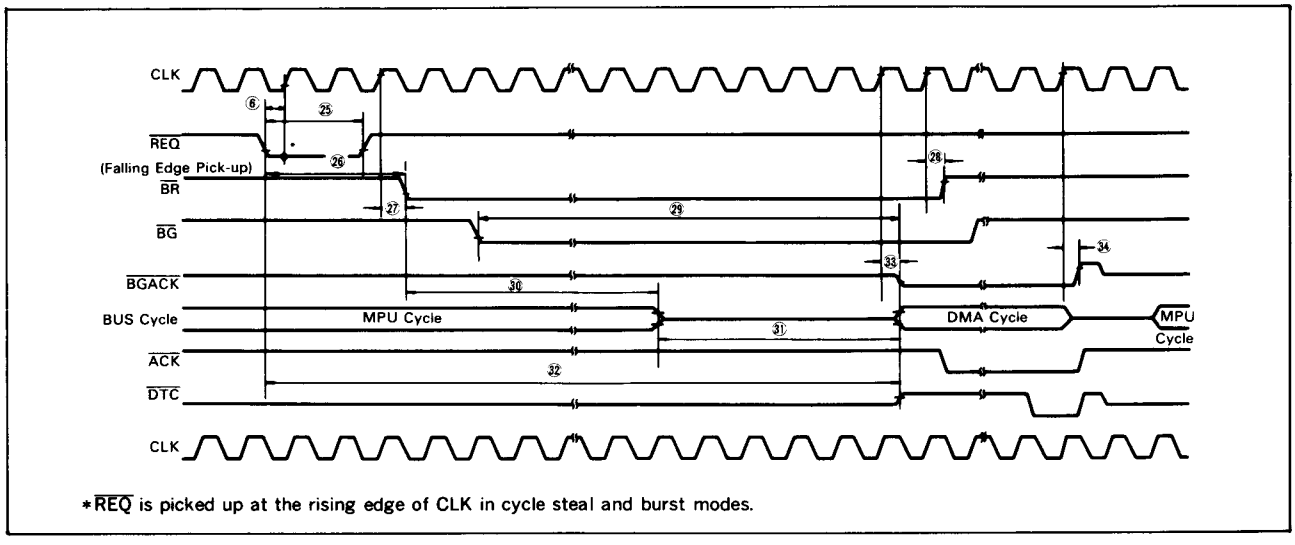
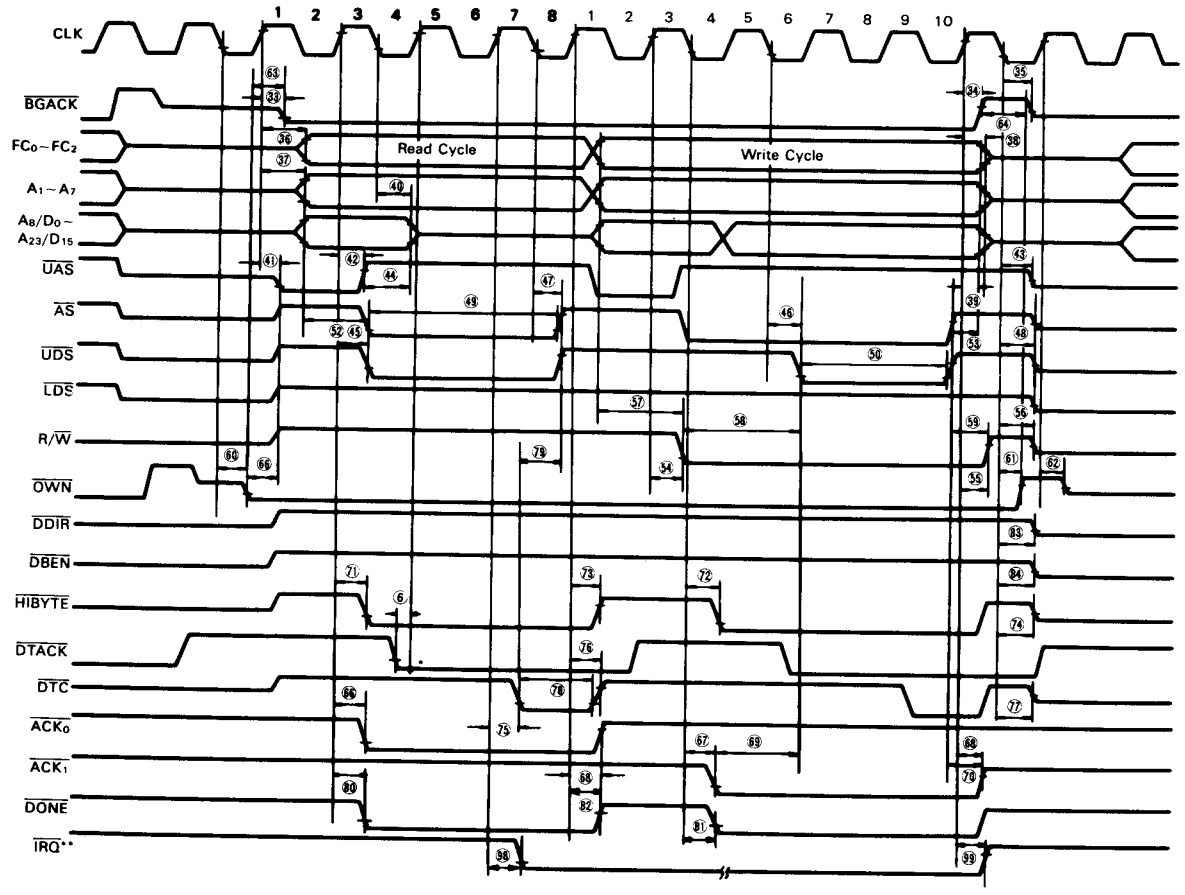
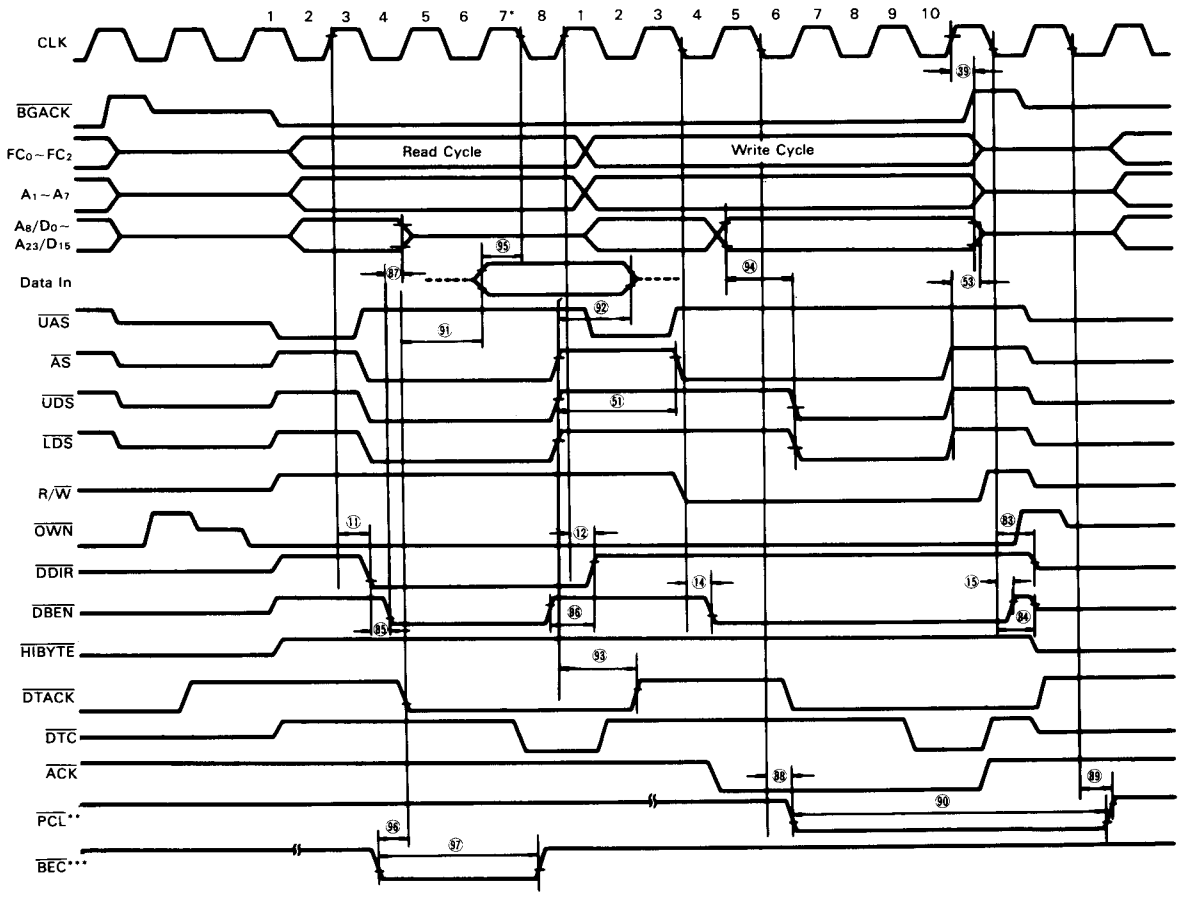


Figure 4 AC Electrical Waveforms-Bus Arbitration



*$\overline{\text{DTACK}}$ is picked up at the rising edge of CLK. This is different from HD68000.
**This timing is not related to DMA Read/Write (Single Cycle) sequence.

Figure 5 AC Electrical Waveforms-DMA Read/Write (Single Cycle)



*Data are latched at the end of clock 7. This timing is the same as HD68000.
**This timing is not related to DMA Read/Write (Dual Cycle) sequence. This timing is only applicable when 1/8 clock pulse mode is selected.
***This timing is applicable when a bus exception occurs.

Figure 6 AC Electrical Waveforms-DMA Read/Write (Dual Cycle)

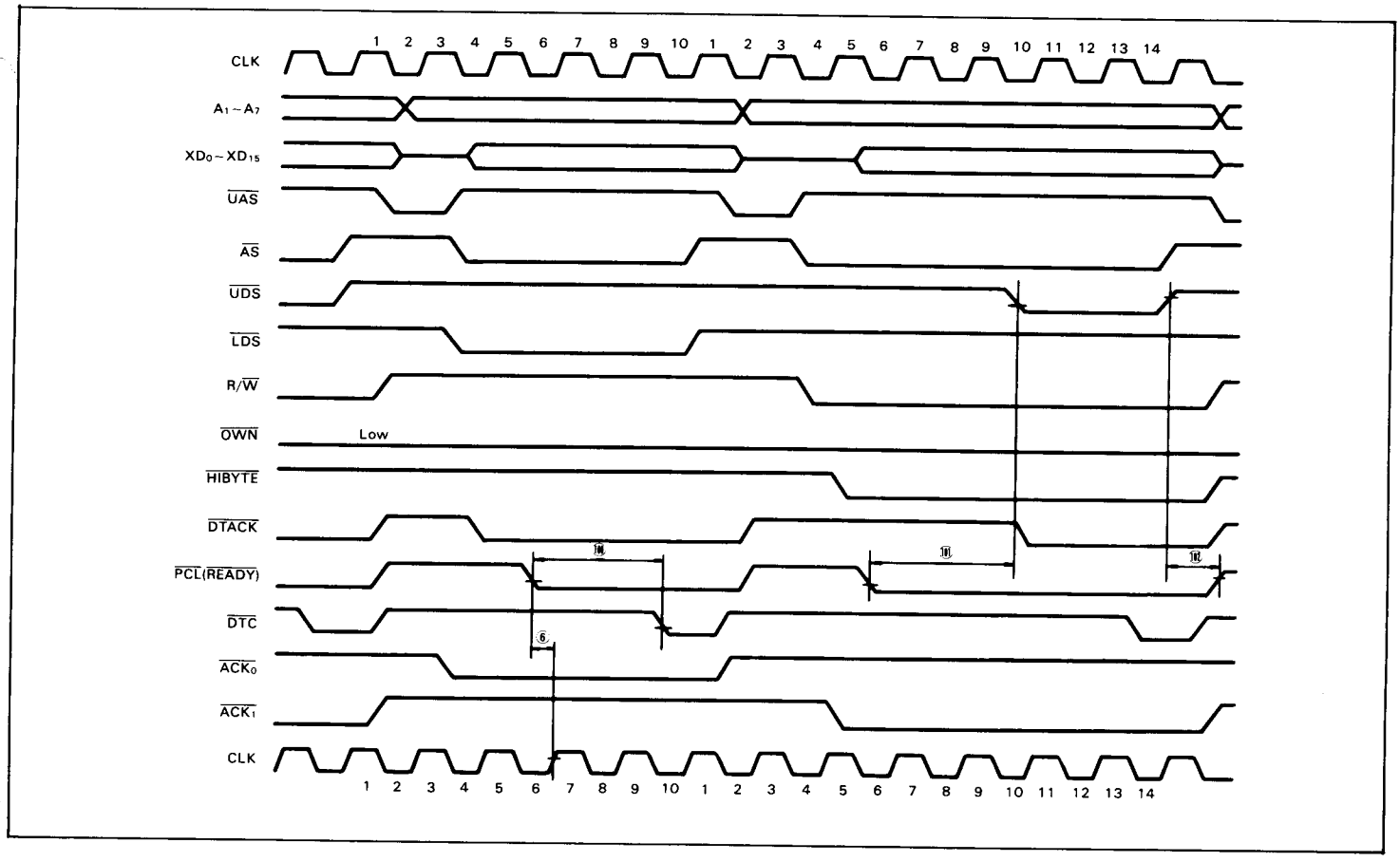


Figure 7 AC Electrical Waveforms-DMA Read/Write (Single Cycle with $\overline{ACK}$ and $\overline{READY}$)

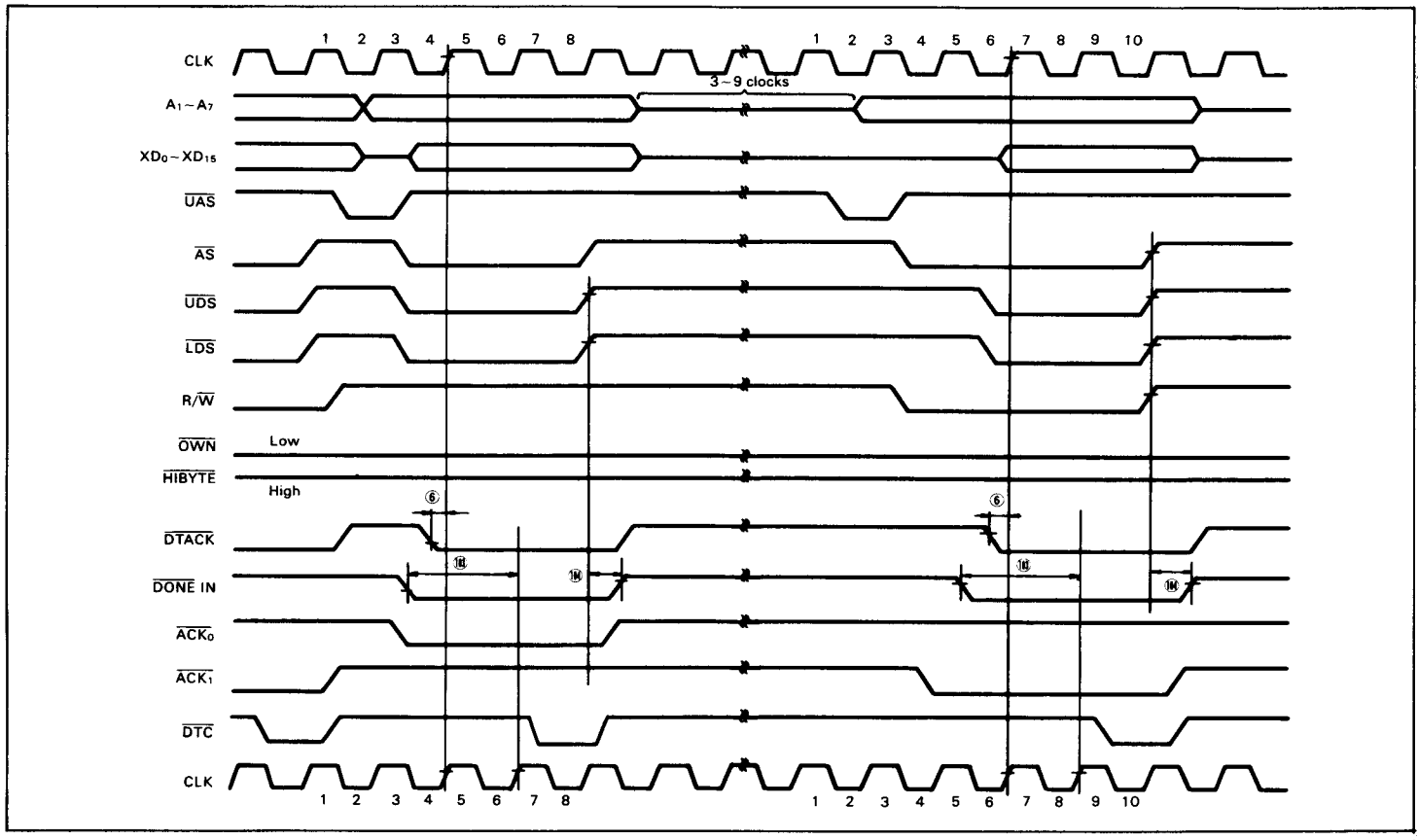


Figure 8 AC Electrical Waveforms-$\overline{\text{DONE}}$ Input

(NOTES for Figure 3 through 8)

1) Setup time for the asynchronous inputs $\overline{\text{BG}}$, $\overline{\text{BGACK}}$, $\overline{\text{CS}}$, $\overline{\text{IACK}}$, $\overline{\text{AS}}$, $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, and R/$\overline{\text{W}}$ guarantees their recognition at the next falling edge of the clock. Setup time for $\overline{\text{BEC0}}$~$\overline{\text{BEC2}}$, $\overline{\text{REQ0}}$~$\overline{\text{REQ3}}$, $\overline{\text{PCL0}}$~$\overline{\text{PCL3}}$, $\overline{\text{DTACK}}$, and $\overline{\text{DONE}}$ guarantees their recognition at the next rising edge of the clock.
2) Timing measurements are referred to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts.
3) These waveforms should only be referred in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

■ INTRODUCTION

The main purpose of a direct memory access (DMA) controller is to perform memory-to-memory, device-to-memory, and memory-to-device data transfers at high speed. The DMAC is required in any system including the device for data input/output like a floppy disk, a hard disk, a display terminal etc..

Figure 9 illustrates a typical system configuration using the DMAC. In this figure, the DMAC transfers blocks of data between the HDC and memory in a quick and efficient manner. Memory-to-memory data transfer is also provided by using data registers in the DMAC. Both 8-bit and 16-bit I/O devices are supportable. 8-/16-/32-bit data can be accessed in the DMA data transfer.

■ OPERATION MODES

The HD63450 DMAC operates through the MPU's writing operation into the internal control registers, then the DMAC will be in one of three operating modes:

1) MPU mode
   This is the state that the DMAC is chip-selected by another bus master in the system (MPU etc.), or that it is asserting the vector number during the interrupt acknowledge cycle.
2) DMA mode
   This is the state that the DMAC is acting as a bus master to perform an operand transfer. The DMA bus cycle refers to the bus cycle that is executed by the DMAC in the DMA mode.
3) IDLE mode
   This is the state that the DMAC is reset by an external device. The DMAC is waiting for an access by MPU or an operand transfer request from a peripheral. Many of the bus control signals are three-stated.

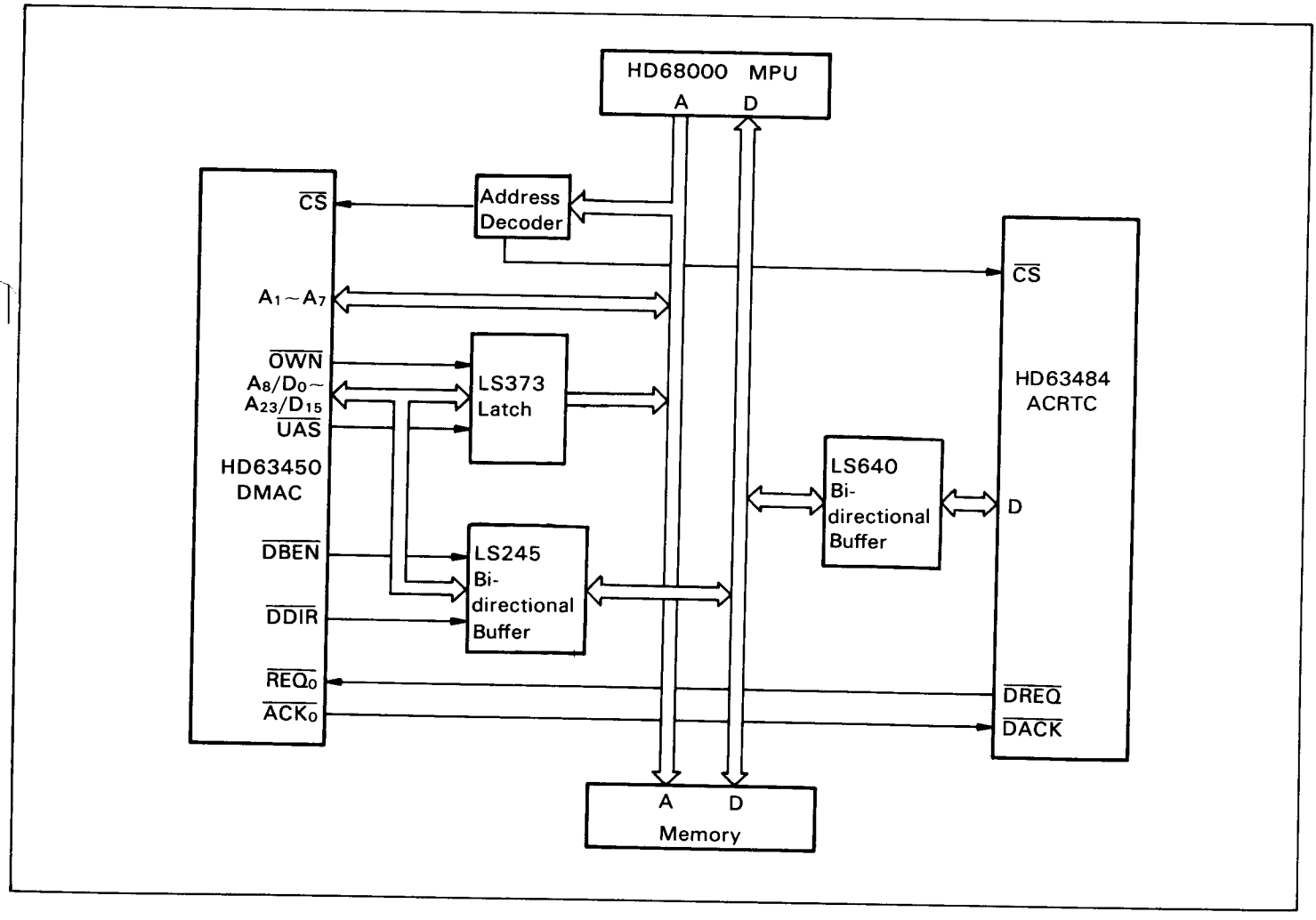


Figure 9 Typical System Configuration

■ SIGNAL DESCRIPTION

In this data sheet, the state of the signals is described with "active/inactive" or "assert/negate".
Figure 10 illustrates the input and output signals. Each function is described in the following.

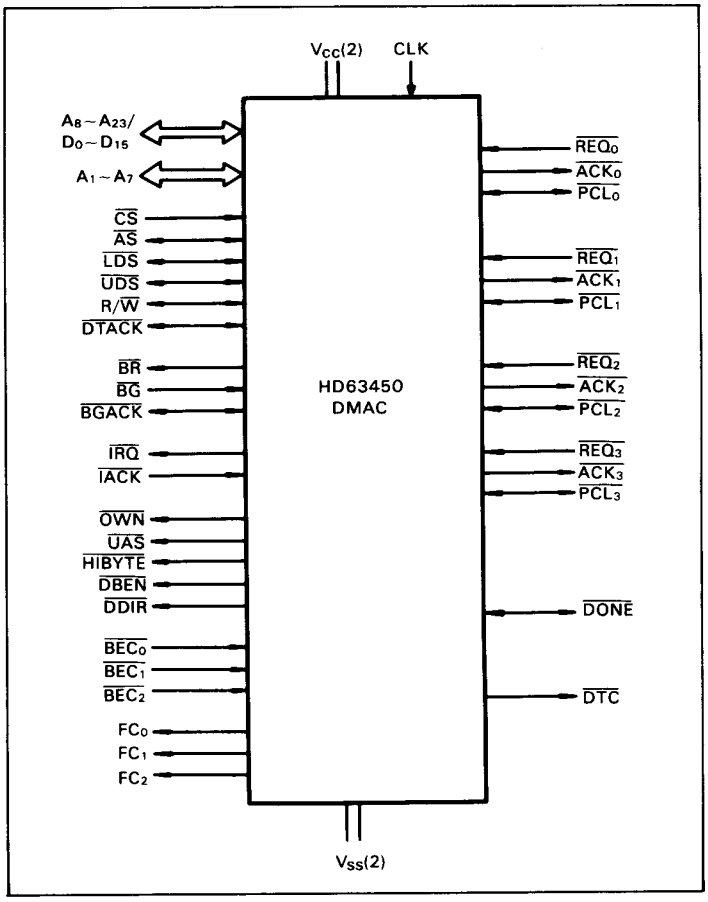


Figure 10 Input and Output Signals

● Address/Data Bus (A_8/D_0 through A_{23}/D_{15})

Input/Output	Three-statable

These lines are time multiplexed for address and data bus. The lines $\overline{DDIR}$, $\overline{DBEN}$, $\overline{UAS}$ and $\overline{OWN}$ are used to control the demultiplexing of the data and address lines externally. Demultiplexing is explained in the later section. The bi-directional data bus is used to transfer data between DMAC, MPU, memory and I/O devices.

Address lines are outputs to address memory and I/O devices.

● Address Bus (A_1 through A_7)

Input/Output	Three-statable

In the MPU mode, the DMAC internal registers are accessed with these lines and $\overline{LDS}$, $\overline{UDS}$. The address map for these registers is shown in Table 1. During a DMA bus cycle, A_1-A_7 are outputs containing the low order address bits of the location being accessed.

● Function Code (FC_0 through FC_2)

Output	Three-statable

These output signals provide the function codes during DMA bus cycles. They are three-stated except in the DMA bus cycles. They are used to control the HD68000 memories.

● Clock (CLK)

Input

This is the input clock to the HD63450, and should never be terminated at any time. This clock can be different from the MPU clock since HD63450 operates completely asynchronously.

● Chip Select ($\overline{CS}$)

Input

This input signal is used to chip select the DMAC in "MPU" mode. If the $\overline{CS}$ input is asserted during a bus cycle which is generated by the DMAC, the DMAC internally terminates the bus cycle and signals an address error. This function protects the DMAC from accessing its own register.

● Address Strobe ($\overline{AS}$)

Input/Output	Three-statable

In the "MPU mode", this line is an input indicating valid address input, and during the DMA bus cycle it is an output indicating valid address output from the DMAC on the address bus.

The DMAC monitors these input lines during bus arbitration to determine the completion of the bus cycle by the MPU or other bus masters.

● Upper Address Strobe ($\overline{UAS}$)

Output	Three-statable

This line is an output to latch the upper address lines on the multiplexed data/address lines. It is three-stated except in the "DMA mode".

● Own ($\overline{OWN}$)

Output	Three-statable

This line is asserted by the DMAC during DMA mode, and is used to control the output of the address line latch. This line may also be used to control the direction of bi-directional buffers when loads on $\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$, R/$\overline{W}$ and other signals exceed the drive capability. It is three-stated in the "MPU mode" and the "IDLE mode".

● Data Direction ($\overline{DDIR}$)

Output	Three-statable

This line controls the direction of data through the bi-directional buffer which is used to demultiplex the data/address lines. It is three-stated during the "IDLE mode".

● Data Bus Enable ($\overline{DBEN}$)

Output	Three-statable

This line controls the output enable line of bi-directional buffers on the multiplexed data/address lines. It is three-stated during the "IDLE mode".

● High Byte ($\overline{HIBYTE}$)

Output	Three-statable

This line is used when the operand size is byte in the single addressing mode. It is asserted when data is present on the upper eight bits of the data bus. It is used to control the output of bidirectional buffers which connects the upper eight bits of the data bus with the lower eight bits. It is three-stated during the "MPU mode" and the "IDLE mode".

● Read/Write (R/$\overline{W}$)

Input/Output	Three-statable

This line is an input during the "MPU mode" and an output during the "DMA mode". It is three-stated during the "IDLE mode". It is used to control the direction of data flow.

● Upper Data Strobe ($\overline{UDS}$), Lower Data Strobe ($\overline{LDS}$)

Input/Output	Three-statable

These lines are extensions of the address lines indicating which byte or bytes of data of the addressed word are being addressed. These lines combined corresponds to address line A_0 in table 1.

● Data Transfer Acknowledge ($\overline{DTACK}$)

Input/Output	Three-statable

In the "MPU mode", this line is an output indicating the completion of Read/Write bus cycle by the MPU.

In the "DMA mode", the DMAC monitors this line to determine when a data transfer has completed. In the event that a bus exception is requested, except for $\overline{HALT}$, prior to or concurrent with $\overline{DTACK}$, the $\overline{DTACK}$ response is ignored and the bus exception is honored. In the "IDLE mode", this signal is three-stated.

● Bus Exception Controls ($\overline{BEC_0}$ through $\overline{BEC_2}$)

Input

These lines provide an encoded signal input indicating an exceptional condition in the DMA bus cycle. See bus exception section for details.

● Bus Request ($\overline{BR}$)

Output

This output line is used to request ownership of the bus by the DMAC.

● Bus Grant ($\overline{BG}$)

Input

This line is used to indicate to the DMAC that it is to be the next bus master. The DMAC cannot assume bus ownership until both $\overline{AS}$ and $\overline{BGACK}$ become inactive. Once the DMAC acquires the bus, it dose not continue to monitor the $\overline{BG}$ input.

● Bus Grant Acknowledge ($\overline{BGACK}$)

Input/Output	Three-statable

Bus Grant Acknowledge ($\overline{BGACK}$) is a bi-directional control line. As an output, it is generated by the DMAC to indicate that it is the bus master.

As an input, $\overline{BGACK}$ is monitored by the DMAC, in limited rate auto-request mode, to determine whether or not the current bus master is a DMA device or not. $\overline{BGACK}$ is also monitored during bus arbitration in order to assume bus ownership.

● Interrupt Request ($\overline{IRQ}$)

Output	Open drain

This line is used to request an interrupt to the MPU.

● Interrupt Acknowledge ($\overline{IACK}$)

Input

This line is an input to the DMAC indicating that the current bus cycle is an interrupt acknowledge cycle by the MPU. The DMAC responds the interrupt vector of the channel with the highest priority requesting an interrupt. There are two kinds of the interrupt vectors for each channel: normal (NIV) or error (EIV). $\overline{IACK}$ is not serviced if the DMAC has not generated $\overline{IRQ}$.

● Channel Request ($\overline{REQ_0}$ through $\overline{REQ_3}$)

Input

These lines are the DMA transfer request inputs from the peripheral devices.

These lines are falling edge sensitive inputs when the request mode is cycle steal. They are low-level sensitive when the request mode is burst.

● Channel Acknowledge ($\overline{ACK_0}$ through $\overline{ACK_3}$)

Output

These lines indicate to the I/O device requesting a transfer that the request is acknowledged and the transfer is to be performed. These lines may be used as a part of the enable circuit for bus interface to the peripheral.

● Peripheral Control Line ($\overline{PCL_0}$ through $\overline{PCL_3}$)

Input/Output	Three-statable

The four lines ($\overline{PCL_0}$~$\overline{PCL_3}$) are multi-purpose lines which may be individually programmed to be a START output, an Enable Clock input, a READY input, an ABORT input, a STATUS input, or an INTERRUPT input.

$\overline{REQ_x}$, $\overline{ACK_x}$, and $\overline{PCL_x}$ are provided for each channel.

● Done ($\overline{DONE}$)

Input/Output	Open Drain

As an output, this line is asserted concurrently with the $\overline{ACK_x}$ timing to indicate the last data transfer to the peripheral device. As an input, it allows the peripheral device to request a normal termination of the DMA transfer.

● Device Transfer Complete ($\overline{DTC}$)

Output	Three-statable

This line is asserted when the DMA bus cycle has terminated normally with no exceptions. It may be used to supply the data latch timing to the peripheral device. In this case, data is valid at the falling edge of $\overline{DTC}$.

■ INTERNAL ORGANIZATION

The DMAC has four independent DMA channels. Each channel has its own set of channel registers. These registers define and control the activity of the DMAC in processing a channel operation.

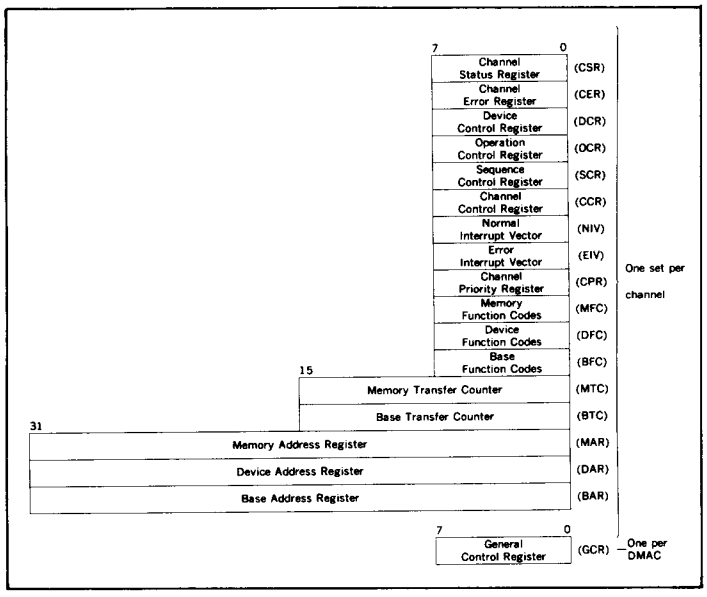


Figure 11 Internal Registers

● Register Organization

The internal register addresses are represented in Table 1. Address space not used within the address map is reserved for future expansion. A read from an unused location in the map results in a normal bus cycle with all ones for data. A write to one of these locations results in a normal bus cycle but no write occurs.

Unused bits of the defined registers in Table 1 are read as zeros.

Table 1 Internal Register Addressing Assignments

Register	Address Bits 7 6 5 4 3 2 1 0	Mode
Channel Status Register	c c 0 0 0 0 0 0	R/W*
Channel Error Register	c c 0 0 0 0 0 1	R
Device Control Register	c c 0 0 0 1 0 0	R/W
Operation Control Register	c c 0 0 0 1 0 1	R/W
Sequence Control Register	c c 0 0 0 1 1 0	R/W
Channel Control Register	c c 0 0 0 1 1 1	R/W
Memory Transfer Counter	c c 0 0 1 0 1 b	R/W
Memory Address Register	c c 0 0 1 1 s s	R/W
Device Address Register	c c 0 1 0 1 s s	R/W
Base Transfer Counter	c c 0 1 1 0 1 b	R/W
Base Address Register	c c 0 1 1 1 s s	R/W
Normal Interrupt Vector	c c 1 0 0 1 0 1	R/W
Error Interrupt Vector	c c 1 0 0 1 1 1	R/W
Channel Priority Register	c c 1 0 1 1 0 1	R/W
Memory Function Codes	c c 1 0 1 0 0 1	R/W
Device Function Codes	c c 1 1 0 0 0 1	R/W
Base Function Codes	c c 1 1 1 0 0 1	R/W
General Control Register	1 1 1 1 1 1 1 1	R/W

cc: 00-Channel #0, 01-Channel #1, 10-Channel #2, 11-Channel #3

ss: 00-High-order, 01-Upper middle, 10-Lower middle, 11-Low-order

b: 0-High-order, 1-Low-order

*see Channel Status Register section in page 17

● Device Control Register (DCR)

The DCR is a device oriented control register. The XRM bits specify whether the channel is in burst or cycle steal request mode. The DTYP bits define what type of device is on the channel. If the DTYP bits are programmed to be a HMCS6800 device, the PCL definition is ignored and the $\overline{PCL}$ line is an Enable clock input. If the DTYP bits are programmed to be a device with $\overline{READY}$, the PCL definition is ignored and the $\overline{PCL}$ line is a $\overline{READY}$ input. The DPS bit defines the port size (eight or sixteen bits) of the peripheral device. (A port size is the largest data which the peripheral device can transfer during a DMA bus cycle.) The PCL bits define the function of the $\overline{PCL}$ line. If the DTYP bits are programmed to be HMCS6800 device, or Device with $\overline{ACK}$ and $\overline{READY}$, these definitions are ignored. The XRM bits are ignored if an auto-request mode (REQG=00 or 01 in Operation Control Register) is selected.

7	6	5	4	3	2	1	0
XRM		DTYP		DPS	0	PCL	

XRM (EXTERNAL REQUEST MODE)
- 00 Burst Transfer Mode
- 01 (undefined, reserved)
- 10 Cycle Steal Mode without Hold
- 11 Cycle Steal Mode with Hold

DTYP (DEVICE TYPE)
- 00 HD68000 compatible device, explicitly addressed (dual addressing mode)
- 01 HD6800 compatible device, explicitly addressed (dual addressing mode)
- 10 Device with $\overline{ACK}$, implicitly addressed (single addressing mode)
- 11 Device with $\overline{ACK}$ and $\overline{READY}$, implicitly addressed (single addressing mode)

DPS (DEVICE PORT SIZE)
- 0 8 bit port
- 1 16 bit port

PCL (PERIPHERAL CONTROL LINE)
- 00 Status Input
- 01 Status Input with Interrupt
- 10 1/8 Start Pulse
- 11 Abort Input

Bit 2 Not Used

● Operation Control Register (OCR)

The OCR is an operation control register. The DIR bit defines the direction of the transfer. The BTD bit defines the execution of the multi-block transfer with $\overline{DONE}$. The SIZE bits define the size of the operand. The CHAIN bits define the type of the CHAIN mode. The REQG bits define how requests for transfers are generated.

7	6	5	4	3	2	1	0
DIR	BTD	SIZE		CHAIN		REQG	

DIR (DIRECTION)
- 0 Transfer from memory to device (transfer from MAR address to DAR address)
- 1 Transfer from device to memory (transfer from DAR address to MAR address)

BTD (MULTI BLOCK TRANSFER WITH $\overline{\text{DONE}}$ MODE)
- 0 Terminates channel operation after the current DMA bus cycle completion
- 1 Restarts next block transfer after the current DMA bus cycle completion

See Page 47 Note 2 for details

SIZE (OPERAND SIZE)
- 00 Byte (8 bits)
- 01 Word (16 bits)
- 10 Long Word (32 bits)
- 11 Byte Transfer without Packing (Port size : 8 bits)

CHAIN (CHAINING OPERATION)
- 00 Chain operation is disabled
- 01 (undefined, reserved)
- 10 Array Chaining
- 11 Linked Array Chaining

REQG (DMA REQUEST GENERATION METHOD)
- 00 Auto-request at transfer rate limited by General Control Register (Limited Rate Auto-Request)
- 01 Auto-request at maximum rate
- 10 $\overline{\text{REQ}}$ line requests an operand transfer
- 11 Auto-request the first operand, external request for subsequent operands

See Page 47 Note 2 for details

● Sequence Control Register (SCR)

The SCR is used to define the sequencing of memory and device addresses.

7	6	5	4	3	2	1	0
0	0	0	0	MAC		DAC	

MAC (MEMORY ADDRESS COUNT)
- 00 Memory address register does not count
- 01 Memory address register counts up
- 10 Memory address register counts down
- 11 (undefined, reserved)

DAC (DEVICE ADDRESS COUNT)
- 00 Device address register does not count
- 01 Device address register counts up
- 10 Device address register counts down
- 11 (undefined, reserved)

Bits 7, 6, 5, 4 Not Used

● Channel Control Register (CCR)

The CCR is used to start or terminate the operation of a channel. This register also determines if an interrupt request is to be generated. Setting the STR bit causes immediate activation of the channel; the channel will be ready to accept request immediately. The STR and CNT bits of the register cannot be reset by a write to the register. The SAB bit is used to terminate the operation forcedly. Setting the SAB bit will reset STR and CNT. Setting the HLT bit will halt the channel operation, and clearing the HLT bit will resume the operation. Setting start bit must be done by byte access. Otherwise, timing error occurs.

7	6	5	4	3	2	1	0
STR	CNT	HLT	SAB	INT	0	0	0

STR (START OPERATION)
- 0 No operation is pending
- 1 Start operation

CNT (CONTINUE OPERATION)
- 0 No continuation is pending
- 1 Continue operation

HLT (HALT OPERATION)
- 0 Operation not halted
- 1 Operation halted

SAB (SOFTWARE ABORT)
- 0 Channel operation not aborted
- 1 Abort channel operation

INT (INTERRUPT ENABLE)
- 0 No interrupts enabled
- 1 Interrupts enabled

Bits 2, 1, 0 Not Used

● Channel Status Register (CSR)

The CSR is a register containing the status of the channel.

7	6	5	4	3	2	1	0
COC	BTC	NDT	ERR	ACT	DIT	PCT	PCS

COC (CHANNEL OPERATION COMPLETE)
- 0 Channel operation incomplete
- 1 Channel operation complete

BTC (BLOCK TRANSFER COMPLETE)
- 0 Block transfer incomplete
- 1 Block transfer complete

NDT (NORMAL DEVICE TERMINATION)
- 0 No normal device termination by $\overline{\text{DONE}}$ input
- 1 Device terminated operation normally by $\overline{\text{DONE}}$ input

ERR (ERROR BIT)
- 0 No errors
- 1 Error as coded in CER

ACT (CHANNEL ACTIVE)
- 0 Channel not active
- 1 Channel active

DIT ($\overline{\text{DONE}}$ INPUT TRANSITION)
- 0 No $\overline{\text{DONE}}$ input transition occurred
- 1 $\overline{\text{DONE}}$ input transition occurred when BTD bit is set

PCT ($\overline{\text{PCL}}$ TRANSITION)
- 0 No $\overline{\text{PCL}}$ transition occurred
- 1 $\overline{\text{PCL}}$ transition occurred

PCS (THE STATE OF THE $\overline{\text{PCL}}$ INPUT LINE)
- 0 $\overline{\text{PCL}}$ "Low"
- 1 $\overline{\text{PCL}}$ "High"

● Channel Error Register (CER)

The CER is an error condition status register. The ERR bit of CSR indicates if there is an error or not. Bits 0-4 indicate what type of error has occurred.

7	6	5	4	3	2	1	0
0	0	0	ERROR CODE				

Error Code

00000	No error
00001	Configuration error
00010	Operation timing error
00101	Address error in MAR
00110	Address error in DAR
00111	Address error in BAR
01001	Bus error in MAR
01010	Bus error in DAR
01011	Bus error in BAR
01101	Count error in MTC
01111	Count error in BTC
10000	External abort
10001	Software abort

Bits 7, 6, 5 Not Used

● Channel Priority Register (CPR)

The CPR is used to define the priority level of the channel. Priority level 0 is the highest and priority level 3 is the lowest priority.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CP	

CP (CHANNEL PRIORITY)

00	Priority level 0
01	Priority level 1
10	Priority level 2
11	Priority level 3

Bit 7 through 2 Not Used

● General Control Register (GCR)

The GCR is used to define what portion of the bus cycles is available to the DMAC for limited rate auto-request generation. GCR is also used to specify the hold time for cycle steal mode with hold.

7	6	5	4	3	2	1	0
0	0	0	0	BT		BR	

BT (BURST TIME)

The number of DMA clock cycles per burst that the DMAC allows in the auto-request at a limited rate of transfer is controlled by these two bits. The number is $2^{(BT+4)}$ (two to the BT +4 power).

BT	Clock Cycle
00	16 Clocks
01	32 Clocks
10	64 Clocks
11	128 Clocks

BR (BANDWIDTH RATIO)

The amount of the bandwidth utilized by the auto-request at a limited rate transfer is controlled by these two bits. The ratio is $2^{(BR+1)}$ (two to the BR+1 power).

BR	Bandwidth Ratio
00	50.00%
01	25.00%
10	12.50%
11	6.25%

The hold time for cycle steal mode with hold is defined to be minimum of 1 sample interval and maximum of 2 sample intervals. A sample interval is defined to be $2^{(BT+BR+5)}$ (two to the BT+BR+5 power) clock cycles.

Bit 7 through 4 Not Used

● Address Registers (MAR, DAR, BAR)

Three 32-bit registers are utilized to implement the Memory Address Register, Device Address Register, and the Base Address Register. Only the least significant twenty-four bits are connected to the address output pins. The content of the MAR is outputted when the memory is accessed in single or dual addressing mode. The content of the DAR is outputted when the peripheral device is accessed. The contents of the BAR is outputted when reading chain information from memory in the Array Chaining Mode or the Linked Array Chaining Mode. It is also used to set the top address of the next block transfer in Continue mode.

● Function Code Registers (MFC, DFC, BFC)

The DMAC has three function code register per channel: the Memory Function Code Register (MFC), Device Function Code Register (DFC), and the Base Function Code Register (BFC). The contents of these registers are outputted from FC_0 through FC_2 lines when an address is outputted from MAR. DAR, or BAR, respectively. The BFC is also used to set the MFC for the transfer of the next data block in the Continue mode.

7	6	5	4	3	2	1	0
0	0	0	0	0	FC2	FC1	FC0

Bit 3 through 7 Not Used

● Transfer Count Registers (MTC, BTC)

Each channel has two 16-bit counters: the Memory Transfer Counter (MTC) and the Base Transfer Counter (BTC). The MTC counts the number of transfer words in one block, and is decreased by one for every operand transfer.

The BTC is used to count the number of data blocks in the Array Chaining Mode. BTC is also used to set the number of operands to transfer for the next data block in the Continue Mode.

The specifiable number is up to "2^{16}-1".

● Interrupt Vector Registers (NIV, EIV)

Each channel has a Normal Interrupt Vector register and an Error Interrupt Vector register.

When an interrupt acknowledge cycle occurs, an interrupt vector is outputted from one of those registers. If the error bit (CSR) is set for the channel with interrupt pending, then content of EIV is outputted, otherwise content of NIV is outputted.

■ OPERATION DESCRIPTION

A DMAC channel operation proceeds in three principal phases. During the initialization phase, the MPU sets the channel control registers, supplies the initial address and the number of transfer words, and starts the channel. During the tranfer phase, the DMAC accepts requests for data operand transfers, and provides addressing and bus controls for the trasnfers. The termination phase occurs after the operation is completed.

This section describes DMAC operations. A description of the MPU/DMAC communication is given first. Next, the transfer phase is covered, including how the DMAC recognizes requests and how the DMAC arranges for data transfer. Following this, the initialization phase is described. The termination phase is covered, introducing chaining, error signaling, and bus exceptions. A description of the channel priority scheme rounds out the section.

■READ/WRITE OF THE DMAC REGISTERS BY MPU

The MPU reads and writes the DMAC internal registers and controls the DMA transfer.

Figure 12 indicates the timing diagram when the MPU reads the contents of the DMAC register. The MPU outputs A_1-A_{23}, FC_0-FC_2, $\overline{AS}$, R/$\overline{W}$, $\overline{UDS}$, and $\overline{LDS}$, and accesses the DMAC internal register. The specific internal register is selected by A_1-A_7, $\overline{LDS}$ and $\overline{UDS}$. The $\overline{CS}$ and $\overline{IACK}$ lines are generated by the external circuit with A_8-A_{23} and FC_0-FC_2. The DMAC outputs data on the data bus, together with $\overline{DDIR}$, $\overline{DBEN}$ and $\overline{DTACK}$. The $\overline{DDIR}$ and $\overline{DBEN}$ control the bi-directional buffer on the bus and the $\overline{DTACK}$ indicates that the data has been sent or received by the DMAC. Read Cycle is eighteen CLKs.

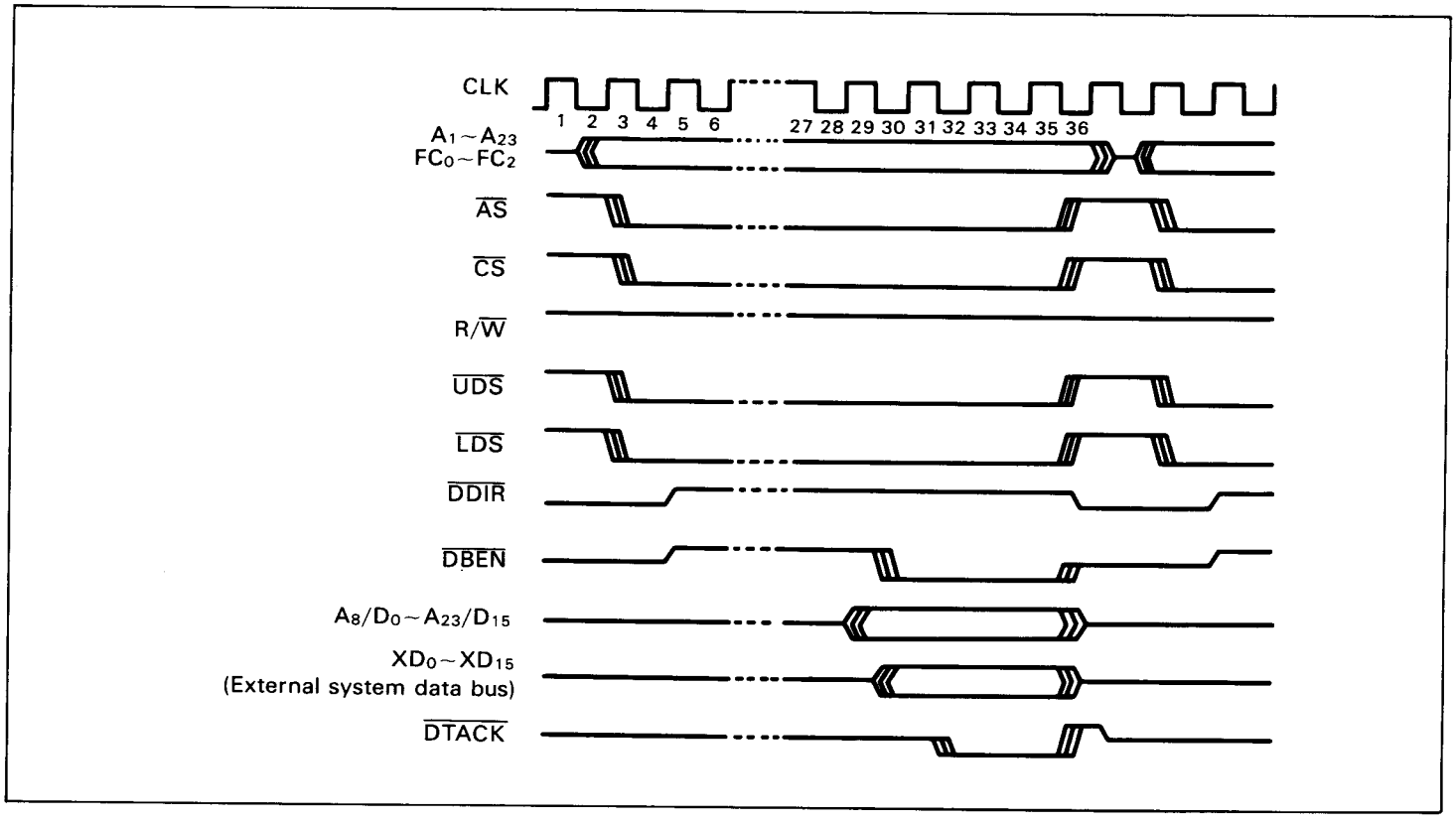


Figure 12 MPU Read from DMAC-Word

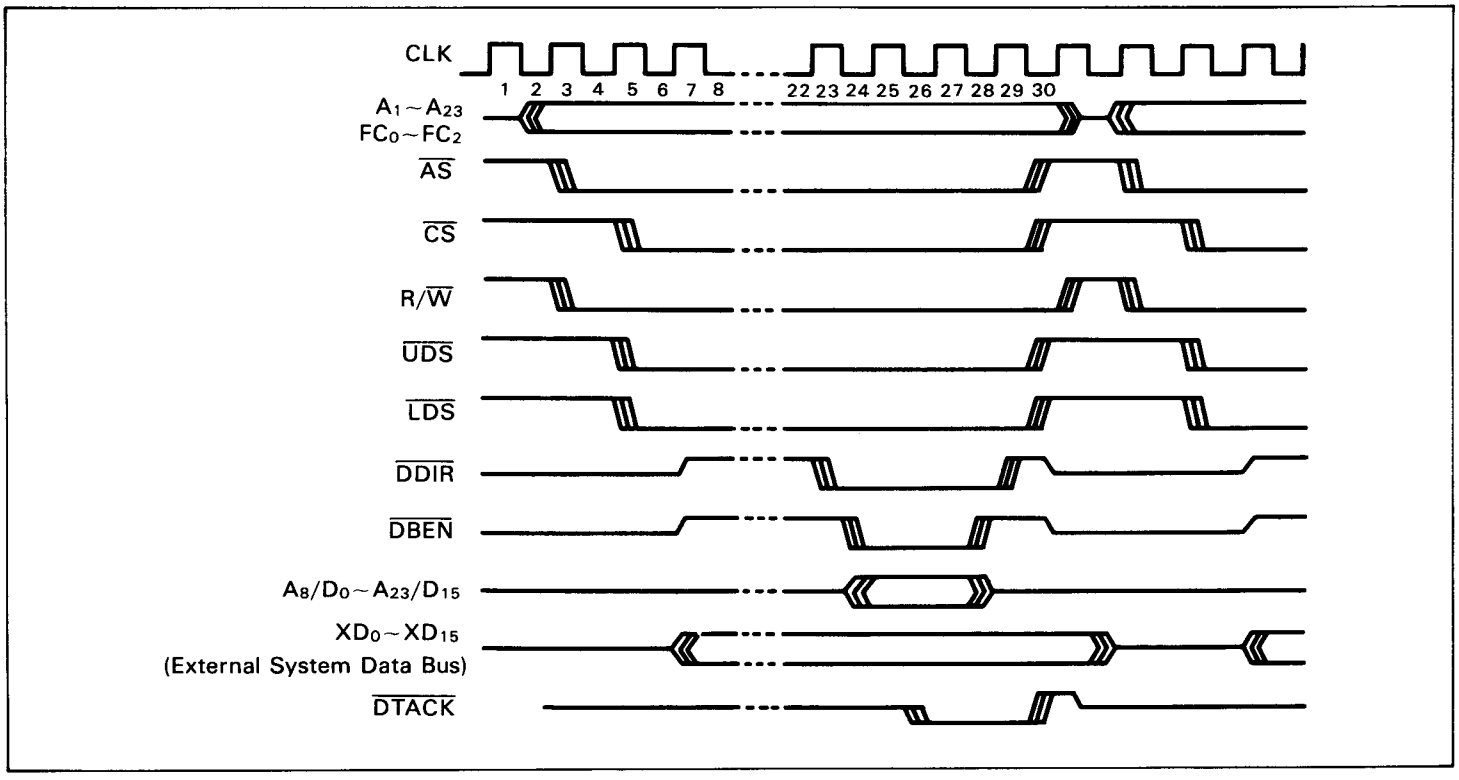


Figure 13 MPU Write to DMAC-Word

Figure 13 shows the MPU write cycle. Write cycle is fifteen CLKs.

Note the following points.

(1) The clock reference shown in this figure is the DMAC input clock.
(2) The $\overline{DDIR}$ and the $\overline{DBEN}$ are three-stated at the beginning which detects $\overline{CS}$ and the ending of the cycle.
(3) During the MPU read cycle, the $\overline{DTACK}$ is asserted after the data is valid on the system bus.
(4) During the MPU write cycle, the $\overline{DDIR}$ line will be driven low to direct the data buffers toward to DMAC before the buffers are enabled.
(5) During the MPU write cycle, the DMAC will latch the data before asserting $\overline{DTACK}$. Then it will negate $\overline{DBEN}$ and $\overline{DDIR}$ in the proper order.
(6) After the MPU cycle and the $\overline{LDS}$ and the $\overline{UDS}$ are negated by the MPU, the DMAC will put $\overline{DBEN}$, $\overline{DDIR}$ and the address data lines to a high impedance state.
(7) $\overline{DTACK}$ will once go "High" and then to a high impedance state after negating $\overline{LDS}$ and $\overline{UDS}$.

■BUS ARBITRATION

The followings are the description of the bus arbitration. The DMAC must obtain the ownership of the bus in order to transfer data. Figure 14 indicates the DMAC bus arbitration timing. It is completely compatible with that of HD68000 MPU. The DMAC asserts the Bus Grant ($\overline{BG}$) to request the bus mastership. The

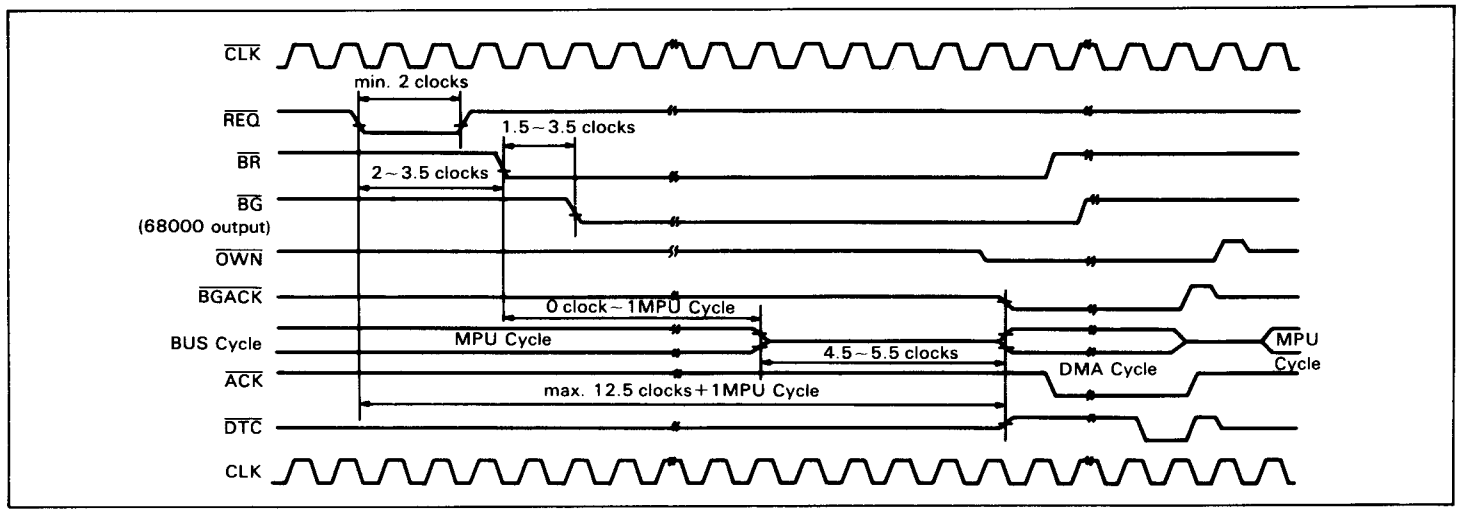


Figure 14 DMAC Bus Arbitration Timing

MPU recognizes the request and asserts $\overline{BG}$, then it grants the ownership in the next bus cycle. After the end of the current cycle ($\overline{AS}$ is negated), the MPU relinquishes the bus to the DMAC. The DMAC asserts the bus grant acknowledge ($\overline{BGACK}$) to indicate that it has the bus ownership. A half clock before $\overline{BGACK}$ is asserted, the DMAC asserts $\overline{OWN}$. $\overline{OWN}$ is kept asserted for a half clock after $\overline{BGACK}$ is negated at the end of the DMA cycle. $\overline{BR}$ is negated one clock after $\overline{BGACK}$ is asserted.

■DEVICE/DMAC COMMUNICATION

Communication between peripheral devices and the DMAC is accomodated by five signal lines. Each channel has $\overline{REQ}$, $\overline{ACK}$ and $\overline{PCL}$, and the last two lines, the $\overline{DONE}$ and $\overline{DTC}$ lines, are shared among the four channels.

● Request ($\overline{REQ}$)

The peripheral devices assert $\overline{REQ}$ to request data transfers. See the "Requests" section for details.

● Acknowledge ($\overline{ACK}$)

This line is used to implicitly address the device which is transferring the data (This device is not selected by address lines). It is also asserted when the content of DAR is outputted during memory-to-memory transfer except for the auto-request mode at a limited rate or at the maximum rate.

● Peripheral Control Line ($\overline{PCL}$)

The function of this line is quite flexible and is determined by the DCR (Device Control Register).

The DTYP bits of the DCR define what type of device is on the channel. If the DTYP bits are programmed to be a HMCS6800 device, the PCL difinition is ignord and the $\overline{PCL}$ line is an Enable clock (E clock) input. If the DTYP bits are programmed to be a device with $\overline{READY}$, the PCL definition is ignored and the $\overline{PCL}$ line is a ready input.

(1) $\overline{PCL}$ as a Status Input

The $\overline{PCL}$ line may be programmed as a status input. The status level of this line can be determined by the PCS bit in the CSR, regardless of the PCL function determined by the DCR. If a negative transition occurs and remains stable for a minimum of two clocks, the PCT bit of the CSR is set. This PCT bit is cleared by resetting the DMAC or writing "1" to the PCT bit.

(2) $\overline{PCL}$ as an Interrupt

The $\overline{PCL}$ line may be programmed to generate an interrupt on a negative transition. This enables an interrupt which is requested if the PCT bit of the CSR is set. When using this function, it is necessary to reset the PCT bit in the CSR before the PCL bit in the DCR is set to interrupt, in order to avoid assertion of IRQ line at this time.

(3) $\overline{PCL}$ as a 1/8 Starting Pulse

The $\overline{PCL}$ line may be programmed to output a 1/8 starting pulse. This active low starting pulse is outputted when a channel is activated, and is "Low" for a period of four clock cycles.

(4) $\overline{PCL}$ as an Abort Input

The $\overline{PCL}$ line may be programmed to be a negative transition abort input which terminates an operation by setting the external abort error in CER. It is necessary to reset the PCT bit in the CSR before activating the channel (Setting the ACT bit of CCR) so that the channel operation is not immediately aborted.

(5) $\overline{PCL}$ as an Enable Clock (E Clock) Input

If the DTYP bits are programmed to be a HMCS6800 device, the PCL definition is ignored and the $\overline{PCL}$ line is an Enable Clock input. The Enable clock downtime must be as long as five clock cycles, and must be high for a minimum of three DMAC clock cycles, but need not be synchronous with the DMAC's clock.

(6) $\overline{PCL}$ as a $\overline{READY}$ Input

If the DTYP bits are programmed to be a device with $\overline{READY}$, the PCL definition is ignored and the $\overline{PCL}$ line is a $\overline{READY}$ input. The $\overline{READY}$ is an active low input.

● DONE ($\overline{DONE}$)

This line is an active low Input/Output signal with an open drain. It is asserted when the memory transfer count is exhausted in a single block transfer. In the chaining operation, $\overline{DONE}$ is asserted only at the last transfer to the peripheral device of the last data block. In the continue mode, $\overline{DONE}$ is asserted for each data block. It is asserted and negated in coincident with the $\overline{ACK}$ line for the last data transfer to the peripheral device. It is also outputted in coincident with the $\overline{ACK}$ line of the last bus cycle, in which the address is outputted from the DAR, in the memory-to-memory transfer (dual addressing mode) that uses the $\overline{ACK}$ line.

The DMAC also monitors the state of the $\overline{DONE}$ line during the DMA bus cycle. If the device asserts $\overline{DONE}$ during $\overline{ACK}$ active, the DMAC will terminate the operation after the transfer of the current operand. If $\overline{DONE}$ is asserted on the first byte of 2-byte operation or the first word of long word operation, the DMAC does not terminate the operation before the whole operand transfer is completed. If $\overline{DONE}$ is asserted, then the DMAC terminates the operation by clearing the ACT bit of the CSR, and setting the COC and NDT bits of the CSR. If both the DMAC and the device assert $\overline{DONE}$, the device termination is not recognized, but the channel operation does terminate. $\overline{DONE}$ is outputted again for the retry exceptions bus cycles.

The case that the multi-block transfer with $\overline{DONE}$ mode is set is described later.

● Data Transfer Complete ($\overline{DTC}$)

$\overline{DTC}$ is an active low signal which is asserted when the actual data transfer is accomplished. It is also asserted in the bus cycle which read a chain information from memory in the Chaining mode. However, if exceptions are generated and the DMA bus cycle terminates, $\overline{DTC}$ is not asserted. $\overline{DTC}$ is asserted one half clock before $\overline{LDS}$ and $\overline{UDS}$ are negated, and negated one half clock after $\overline{LDS}$ and $\overline{UDS}$ are negated.

■REQUESTS

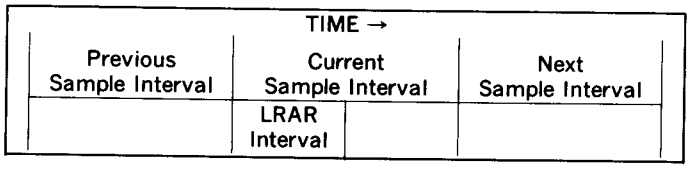
Requests may be externally generated by circuitry in the peripheral device, or internally generated by the auto-request mechanism. The REQG bits of the OCR determine these modes. The DMAC also supports an operation in which the DMAC auto-requests the first transfer and then waits for the peripheral device to request the following transfers.

● Auto-request Transfers

The auto-request mechanism provides generation of requests within the DMAC. These requests can be generated at either of two rates: maximum-rate and limited-rate. In the former case, the channel always has a request pending.

The limited rate auto-request functions by monitoring the bus utilization.

(1) Limited-rate Auto-request



In the limited-rate auto-request, the DMAC devides time into equal length sample intervals by counting clock cycles. The end of one sample interval makes the beginning of the next. During a sample interval, the DMAC monitors, by means of $\overline{BGACK}$ pin, the system bus activity of the DMAC and other bus master devices. At the end of the sample interval, decision is made whether or not to perform the channel's data transfer during the next sample interval. Namely, based on the activity of the DMAC or other bus master devices during the current sample interval, the DMAC allows limited-rate auto-requests for some initial portion of the next sample interval.

The length of the sample interval, and the lenght of the limited-rate auto-request generation period (the limited-rate auto-request interval) are controlled by the BT and BR bits in the GCR. The length in clock cycles of the limited-rate auto-request interval is $2^{(BT+4)}$ (2 raised to the BT+4 power). For example, if BT equals 2 and the DMA utilization of the bus was low during the previous sample interval, then the DMAC generates the auto-request transfers during the first 64 clock cycles.

The ratio of the length of the sample interval to the length of the limited-rate auto-request interval is controlled by the BR bits. The ratio of the system bus utilization of the MPU to other bus master devices including the DMAC is $2^{(BR+1)}$ (2 raised to the BR +1 power). If the fraction of DMA clock cycles during the sample interval exceeds the programmed utilization level, the DMAC will not allow limited-rate auto-requests during the next sample interval.

For example, if BR equals 3, then at most one out of 16 clock cycles during a sample interval can be used by the DMAC and other bus master devices, and still the DMAC would allow limited rate auto-request during the next sample interval. Therefore, from the viewpoint of long period, the ratio of the system bus utilization of the MPU to I/O devices including the DMAC is about 16 : 1. The sample interval length is not a direct parameter, but it is equal to $2^{(BT+BR+5)}$ clock cycles. Thus, the sample interval can be programmed between 32 and 2048 clock cycles.

The DMAC uses the $\overline{BGACK}$ to differentiate between the MPU bus cycle and DMAC or other bus master devices. If $\overline{BGACK}$ is active, then the DMAC assumes that the bus is used by a DMAC or other bus master devices. If it is inactive, then the DMAC assumes that it is used by the MPU.

(2) Maximum-rate Auto-request

If the REQG bits in the OCR indicate auto-request at the maximum rate, the DMAC acquires the bus after the start bit is set and keeps it until the data transfer is completed.

If a request is made by another channel of higher priority, the DMAC services that channel and then resumes the auto-request sequence. If two or more channels are set to equal priority level and maximum rate auto-request, then the channels will rotate in a "round robbin" fashion.

If the HMCS68000 compatible device is connected to a channel, the $\overline{ACK}$ line is held inactive during an auto-request operation. Consequently, any channel may be used for the memory-to-memory transfer with the auto-request function in addition to the operation of data transfer between memory and peripheral device with using the $\overline{REQ}$ pin. Refer to Figure 15 for the timing of the memory-to-memory transfer. In this mode, the $\overline{ACK}$, $\overline{HIBYTE}$ and $\overline{DONE}$ outputs are always inactive.

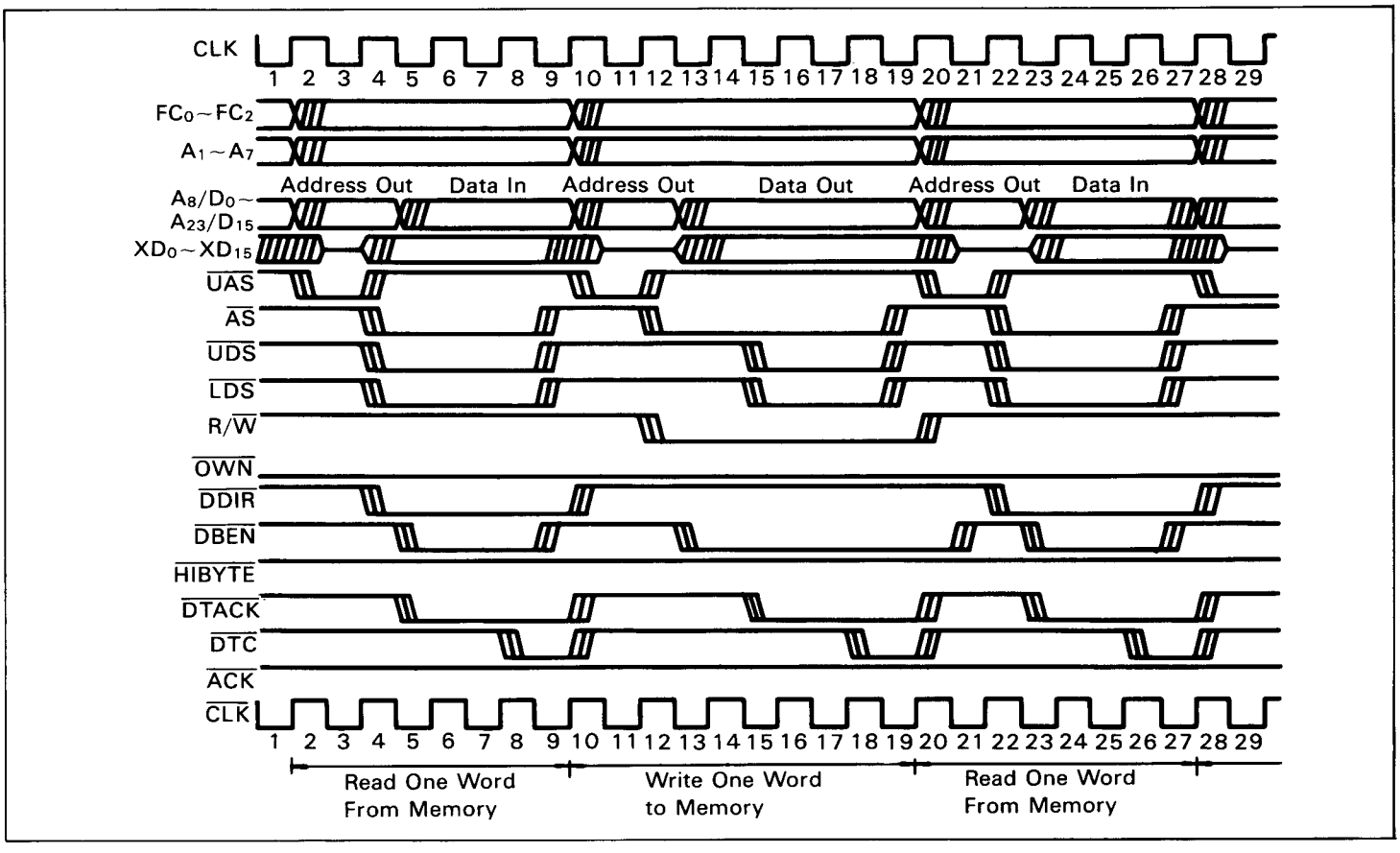


Figure 15 Memory-to-Memory Transfer Read-Write-Read Cycles

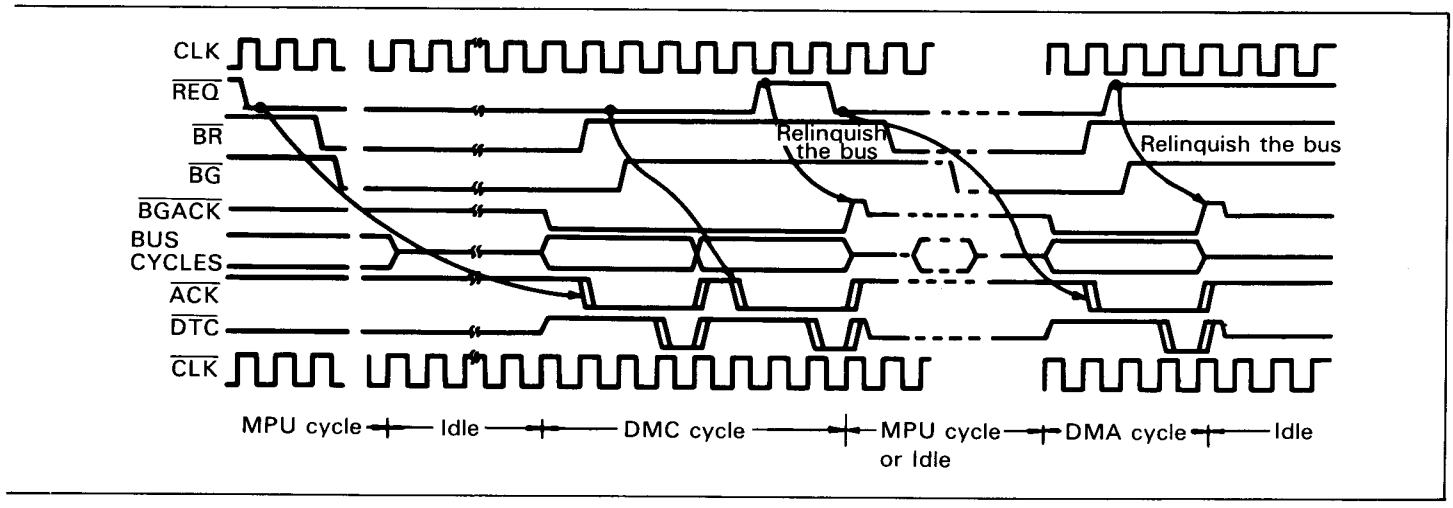


Figure 16 Burst Mode Request Timing (Only one channel is active)

● External Requests

If the REQG bits of the OCR indicate that the $\overline{REQ}$ line generates requests, the transfer requests are generated externally. The request line associated with each channel allows the device to externally generate requests for DMA transfers. When the device wants an operand transferred, it makes a request by asserting the request line. The external request mode is determined by the XRM bits of the DCR, which allows both burst and cycle steal request modes. The burst request mode allows a channel to request the transfer of multiple operands using consecutive bus cycles. The cycle steal request mode allows a channel to request the transfer of a single operand. The followings are the description of the burst and the cycle steal modes.

(1) Burst Request Recognition

In the burst request mode, the $\overline{REQ}$ line is an active low input. The level sampled at the rising edge of the clock. Once the burst request is asserted, it needs to be held low until the first DMA bus cycle starts in order to insure at least one data transfer operation. In order to stop the burst mode transfer after the current bus cycle, the $\overline{REQ}$ line has to be negated one clock before the $\overline{DTC}$ output clock of this cycle. Refer to Figure 16 or the burst mode timing.

(2) Cycle Steal Request Recognition

In the cycle steal request mode, the peripheral device requests the DMA transfer by generating an falling edge at the $\overline{REQ}$ line. The $\overline{REQ}$ line needs to be held "low" for at least 2 clock cycles. In the cycle steal mode, if the $\overline{REQ}$ line changes from "High" to "Low" between $\overline{ACK}$ output and one clock before the clock that outputs $\overline{DTC}$, then the next DMA transfer is performed without relinquishing the bus. If the bus is not relinquished, then maximum of 5 idle clocks is inserted between bus cycles.

Refer to Figure 17 for the request timing of the cycle steal mode. If the XRM bits specify cycle steal without hold, the DMAC will relinquish the bus. If the XRM bits specify cycle steal with hold, the DMAC will hold the bus and wait for the next $\overline{REQ}$ input for at least 1 sample interval after the current bus cycle completion. The allowable hold time is up to 2 sample intervals.

Figure 18 shows the request timing in the cycle steal bus hold. If the $\overline{REQ}$ is inputted during the hold time, the $\overline{ACK}$ is outputted after a maximum of 7.5 clock cycles from the picked-up clock.On the cycle steal with hold mode, the DMAC will hold the bus even when the transfer count is exhausted and the last data has been transferred. If DMA transfer is requested from other channel during this period, they are executed normally.

(3) Request Recognition in Dual-address Transfers

In a following section, dual-address transfers are defined. Dual address transfer is an exception to the request recognition rules

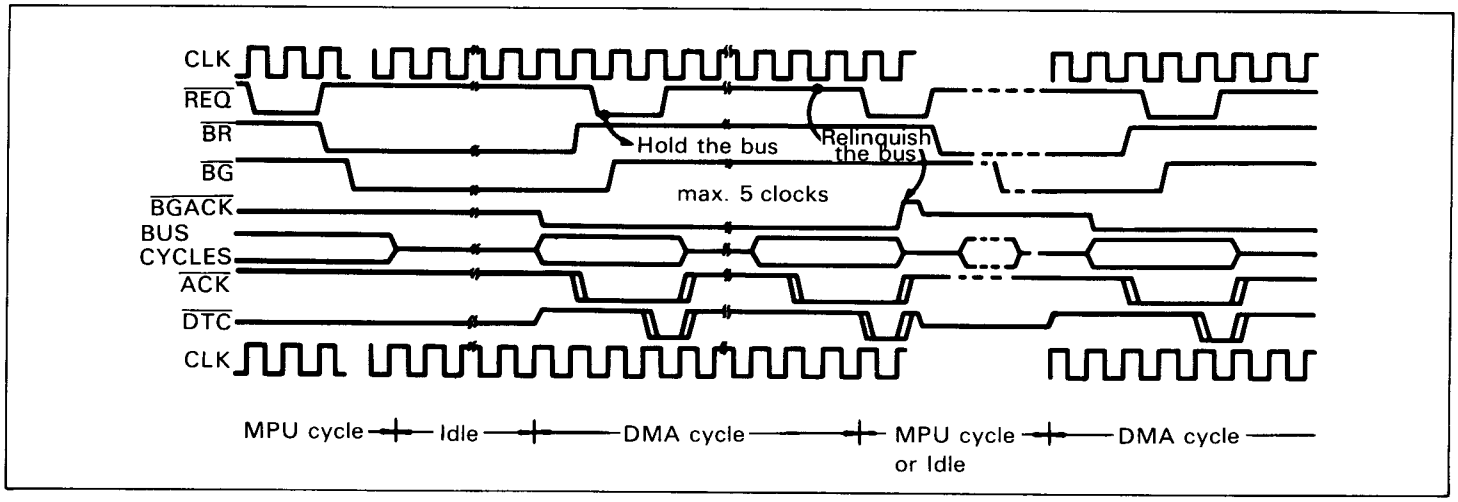


Figure 17 Cycle Steal Mode Request Timing

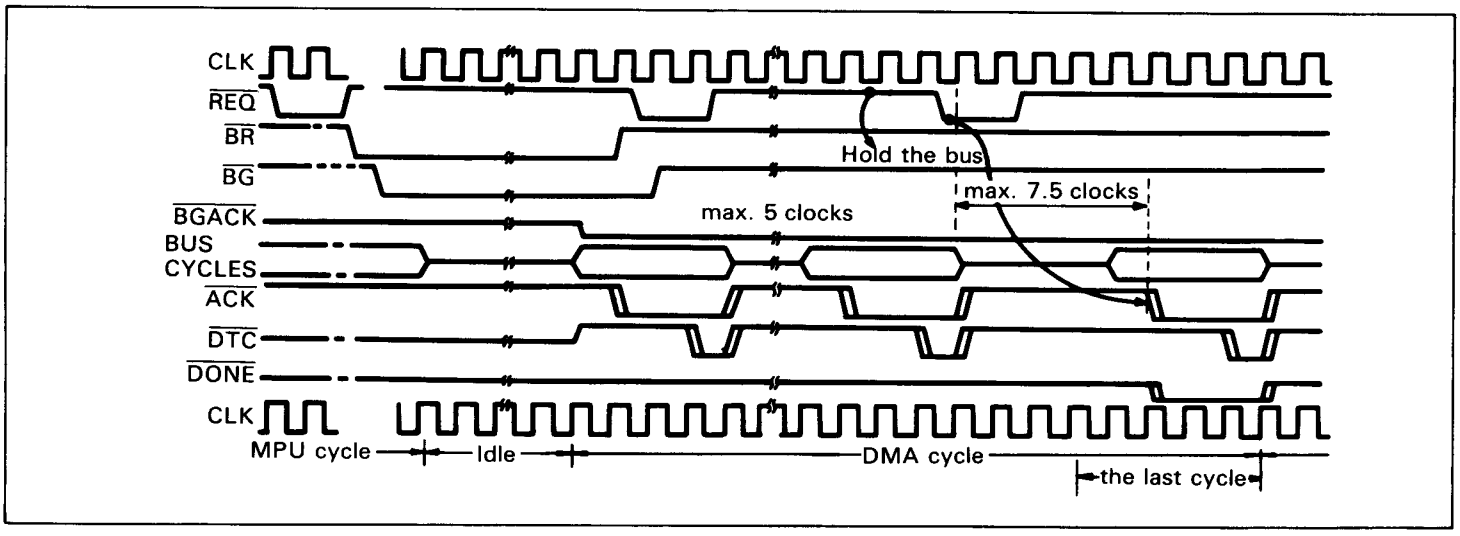


Figure 18 Cycle Steal Bus Hold Mode Request Timing

in the previous paragraphs. In the cycle steal request mode, when there are two or more transfers between the DMAC and the peripheral device during one operand transfer, the request is not recognized until the last transfer between the DMAC and the I/O device starts.

● Mixed Request Generation

A single channel can mix two request generation methods. By programming the REQG bits of the OCR to "11", when the channel is started, the DMAC auto-requests the first transfer. Subsequent requests are then generated externally by the device. The $\overline{ACK}$ and $\overline{PCL}$ lines perform their normal functions in this operation.

■DATA TRANSFERS

All DMAC data transfers are assumed to be between memory and the peripheral device. The word "memory" means a 16-bit HD68000 bus compatible device. By programming the DCR, the characteristics of the peripheral device may be assigned. Each channel can communicate using any of the following protocols.

DTYP	Device Type	
00	HD68000 compatible device	Dual Addressing
01	HD6800 compatible device	
10	Device with $\overline{ACK}$	Single Addressing
11	Device with $\overline{ACK}$ and $\overline{READY}$	

● Dual Addressing

HD68000 and HD6800 compatible devices may be explicity addressed. This means that before the peripheral transfers data, a data register within the device must be addressed. Because the address bus is used to address the peripheral, the data cannot be directly transferred to/from the memory because the memory also requires addressing. Instead, the data is transferred from the source to the DMAC and held in an internal DMAC holding register. A second bus transfer between the DMAC and the destination is then required to complete the operation. Because both the source and destination of the transfer are explicitey addressed, this protocol is called dual addressing.

(1) HD68000 Compatible Device Transfers

In this operation, when a request is received, the bus is obtained and the transfer is completed using the protocol as shown in Figures 19 and 20. Figures 21 through 24 show the transfer timings. Figures 21 and 24 show the operation when the memory is the source and the peripheral device is the destination. Figures 22 and 23 show the transfer in the opposite direction. The peripheral device is a 16-bit device in Figures 21 and 22, and a 8-bit device in Figures 23 and 24.

(2) HD6800 Compatible Device Transfers

When a channel is programmed to perform HD6800 compatible transfers, the $\overline{PCL}$ line for that channel is defined as an Enable clock input. The DMAC performs data transfers between itself and the peripheral device using the HD6800 bus protocol, with the $\overline{ACK}$ output providing the $\overline{VMA}$ (valid memory address) signal. Figure 25 illustrates this protocol. Refer to Figure 26 for the read cycle timing and Figure 27 for the write cycle timing. In Figure 26, the DMAC latches the data at the falling edge of clock 19, so a latch to hold the data is necessary as shown in the figure.

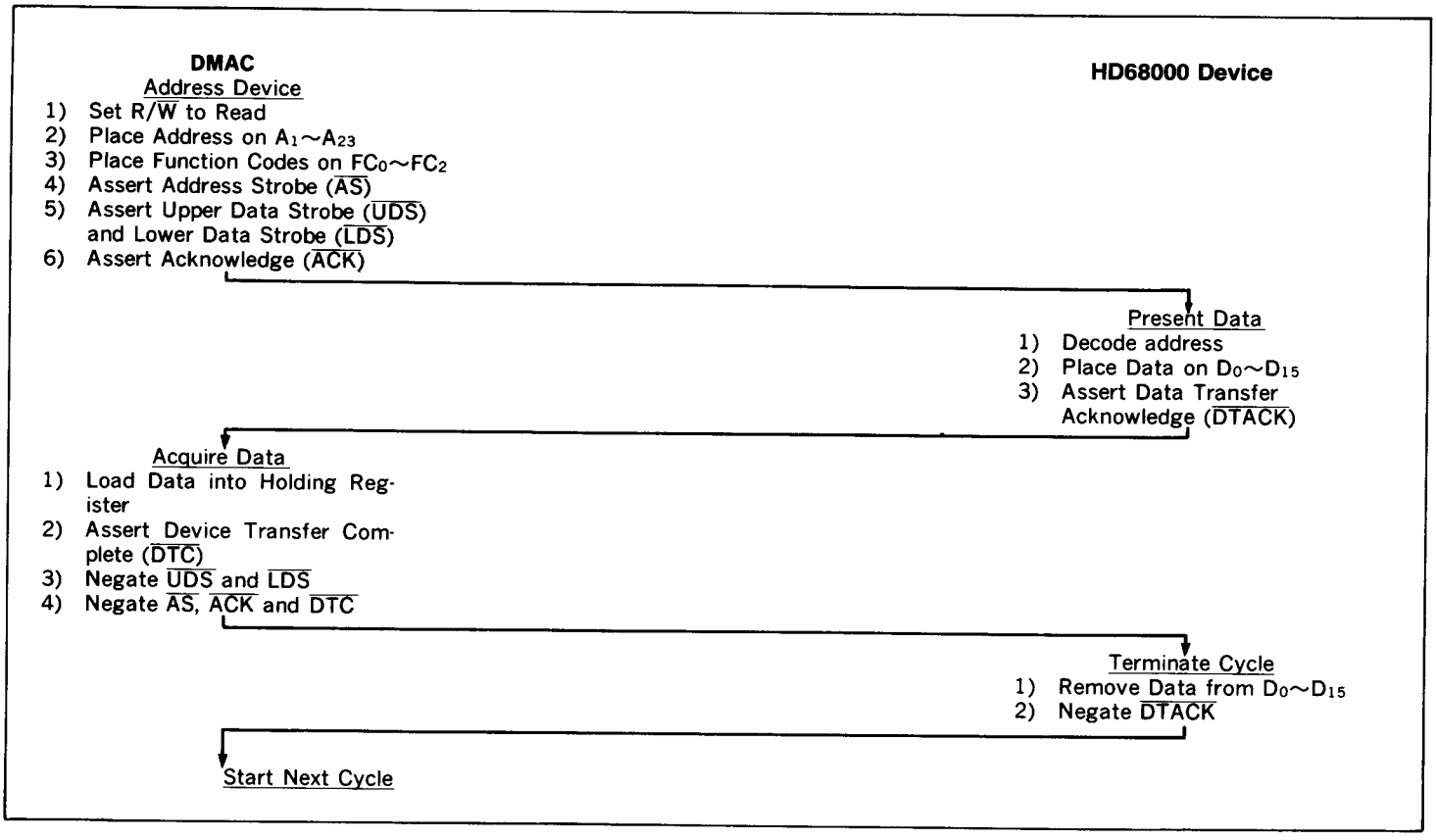


Figure 19 Word Read Cycle Flowchart HD68000 Type Device

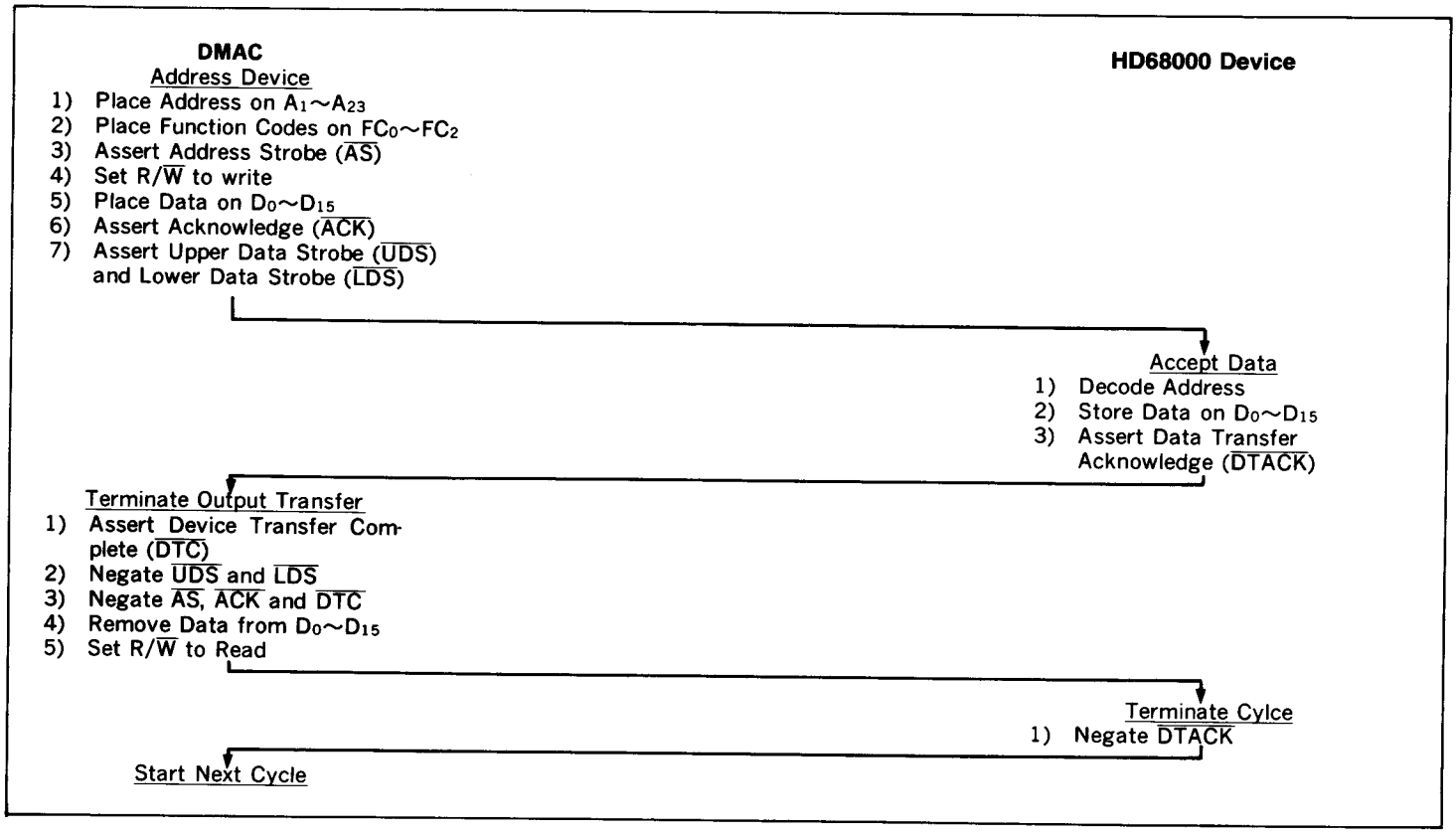


Figure 20 Word Write Cycle Flowchart HD68000 Type Device

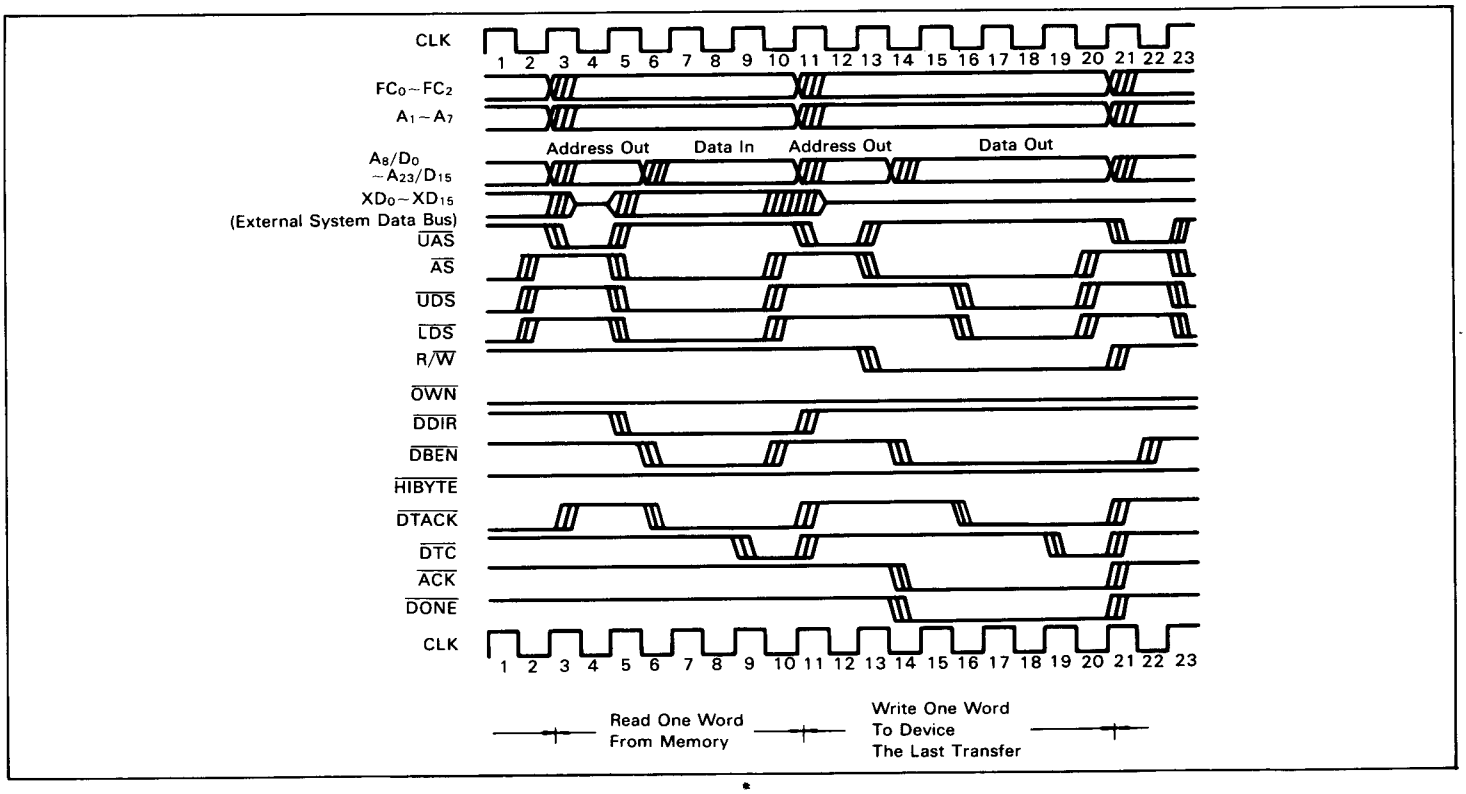


Figure 21 Dual Addressing Mode, Read/Write Cycle, Destination=16-bit Device, Word Operand

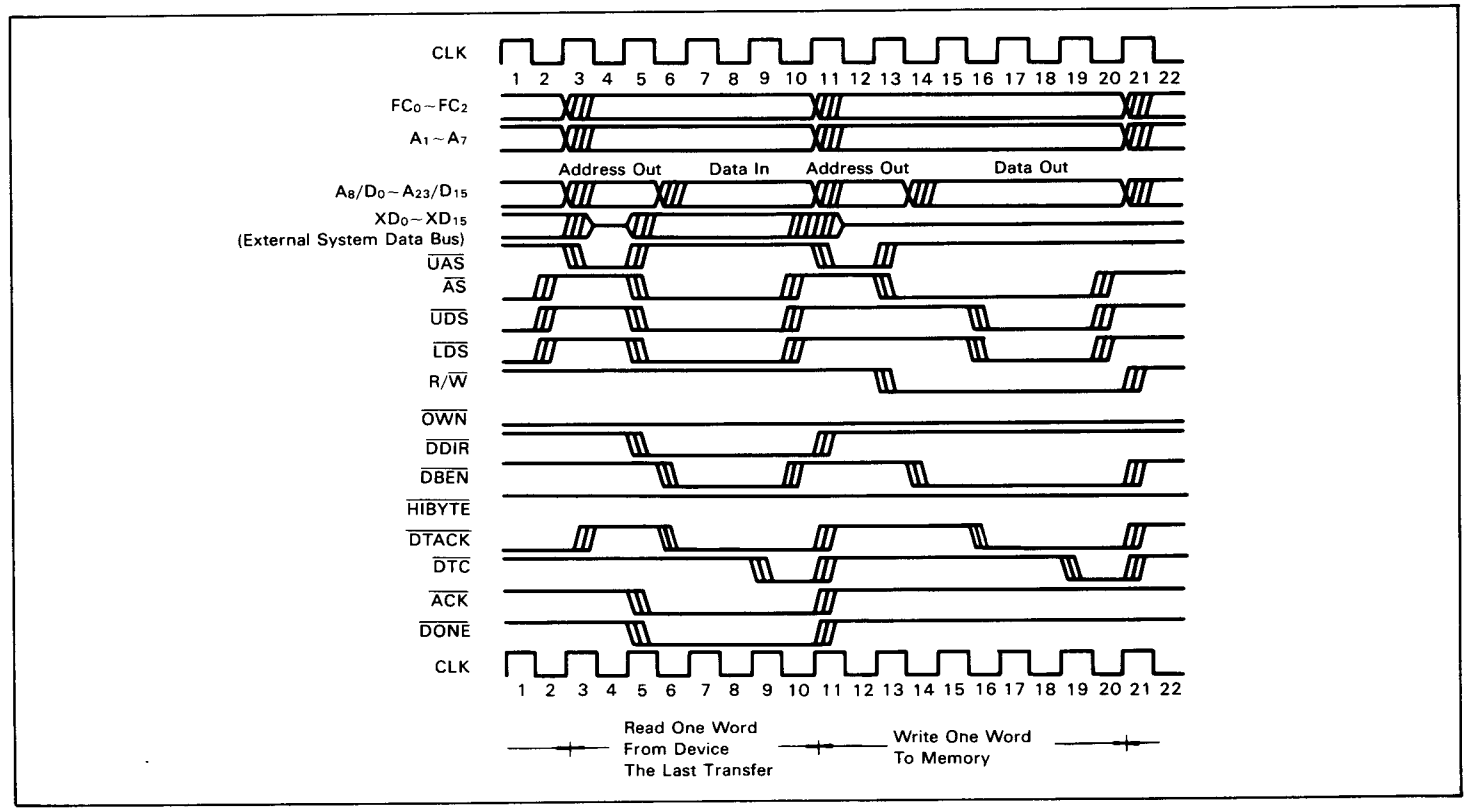


Figure 22 Dual Addressing Mode, Read/Write Cycle, Source=16-bit Device, Word Operand

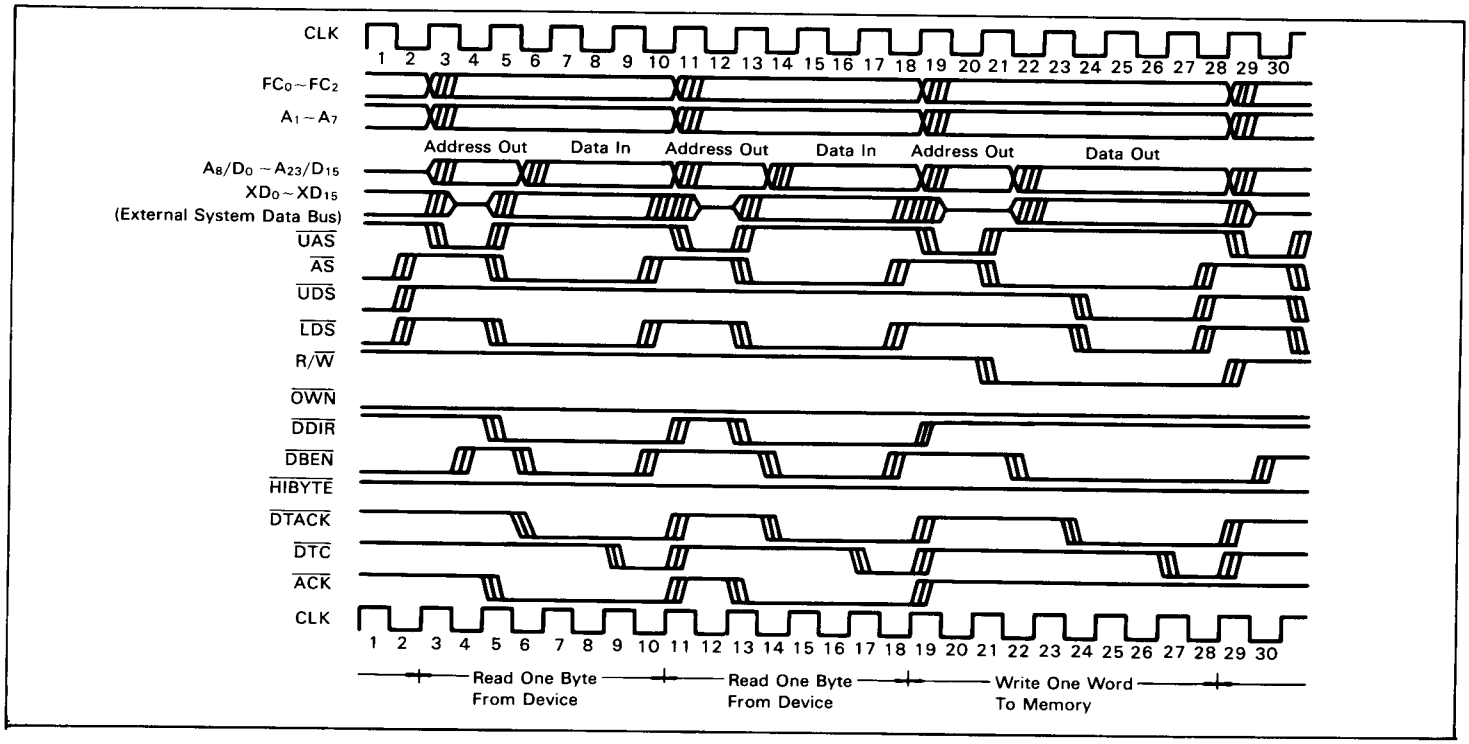


Figure 23 Dual Addressing Mode, Read/Write Cycle, Source=8-bit Device, Word Operand

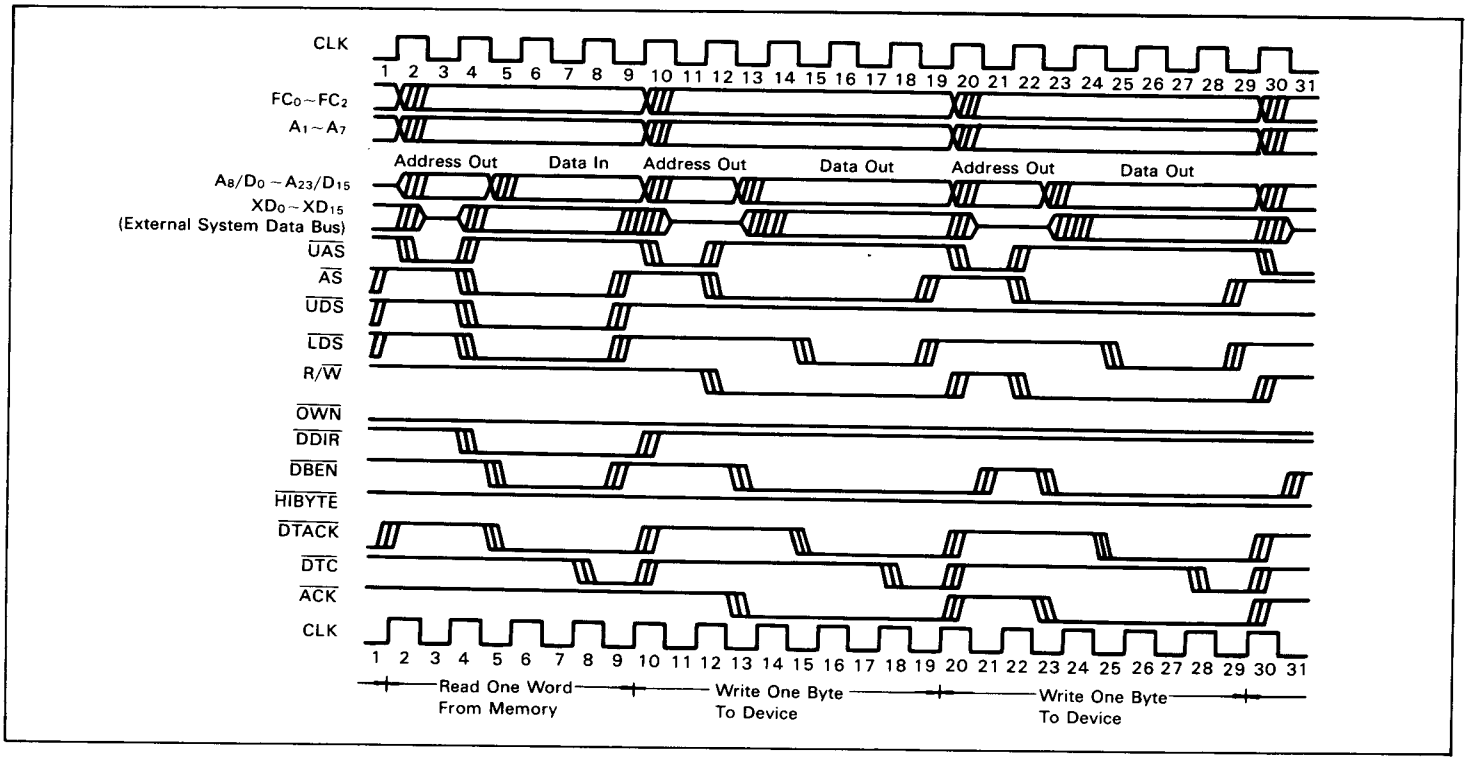


Figure 24 Dual Addressing Mode, Read/Write Cycle, Destination=8-bit Device, Word Operand

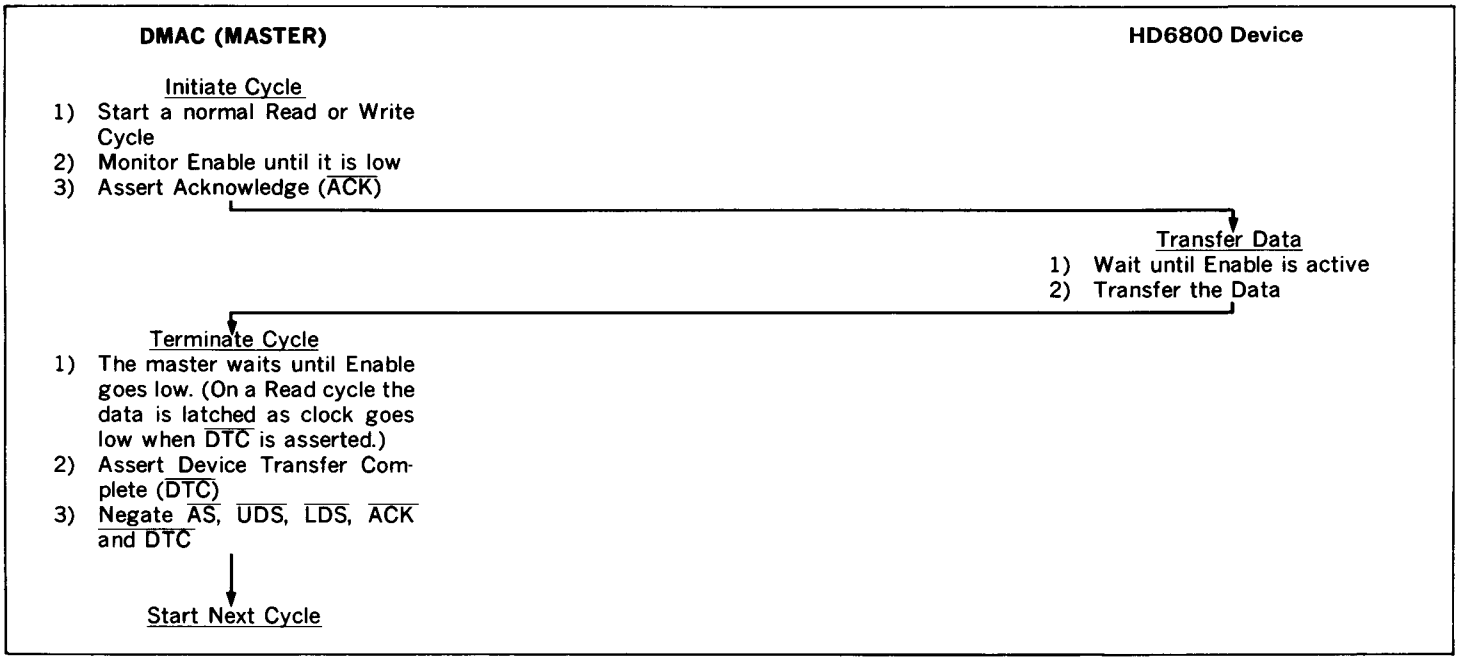


Figure 25 HD6800 Cycle Flowchart

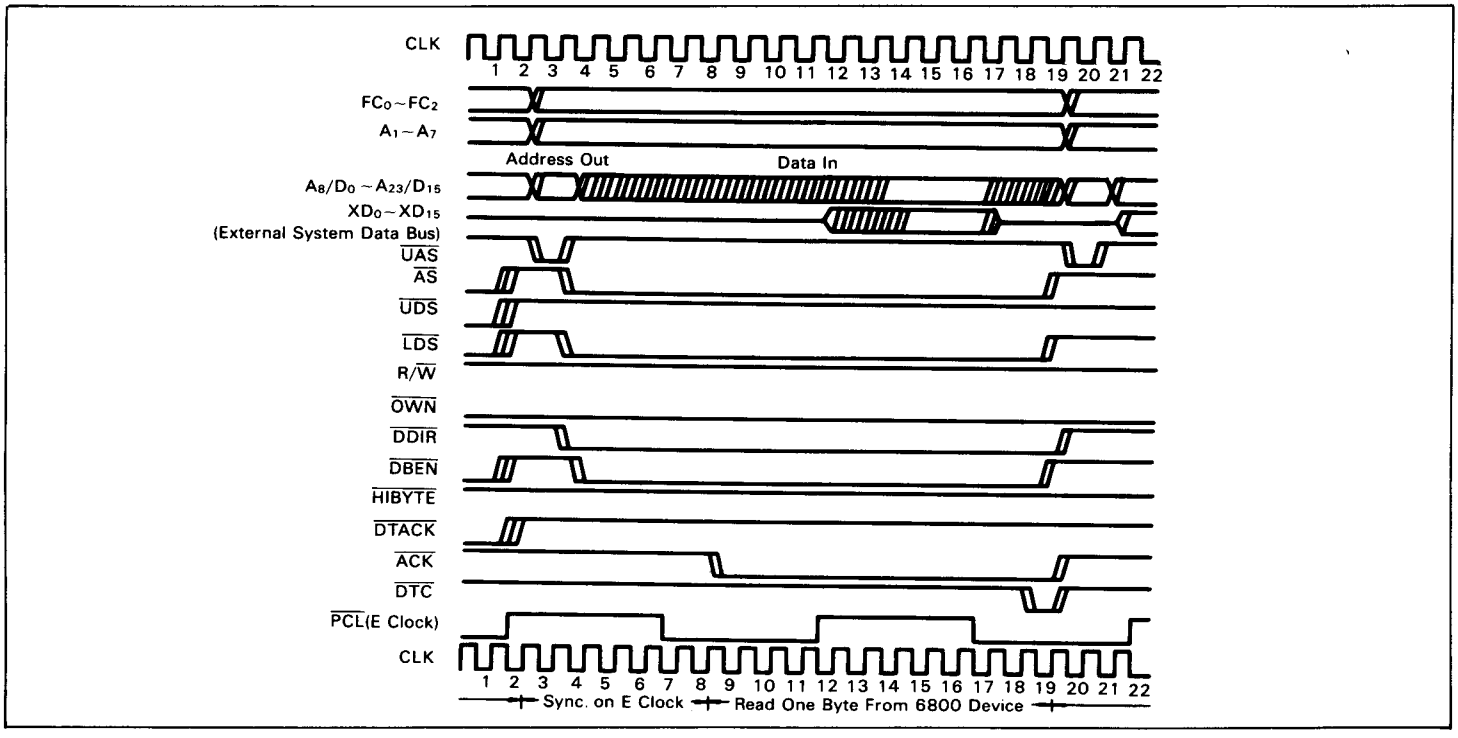


Figure 26 Dual Addressing Mode, HD6800 Compatible Device, Read Cycle

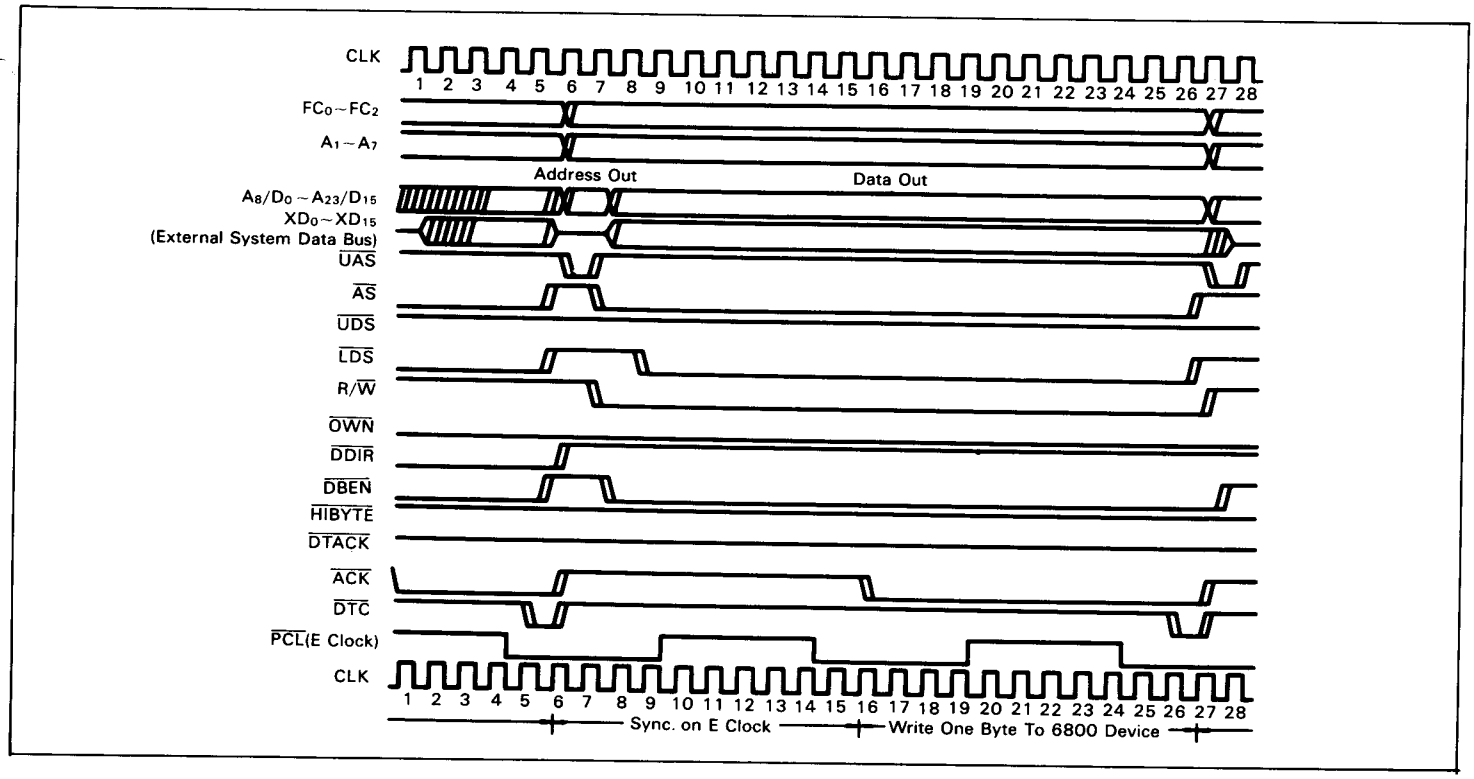


Figure 27 Dual Addressing Mode, HD6800 Compatible Device, Write Cycle

(3) An Example of a Dual Address Transfer

This scetion contains an example of a dual address transfer using Table 2 of Dual-Address Sequencing. The transfer mode of this example is the following.

1. Device Port size=8 bits
2. Operand size=Long Word (32 bits)
3. Memory to Device Transfer
4. Source (Memory) Counts up, Destination (Device) Counts Down

In this mode, a data transfer from the source (memory) is done according to the 6th row of Table 2, since the port size of the memory is always 16 bits. A data transfer to the destination (device) is done according to the 3rd row of Table 2. Table 3 shows the data transfer sequence.

The port size in Table 2 is not related to the DPS bit of the DCR. The DPS defines the port size of the device only. The DPS is set to "0" in this example as the device port size is 8 bits.

The memory map of this example is shown in Table 4. The operand consists of BYTE A through BYTE D in memory of Table 4. Prior to the transfer, MAR and DAR are set to 00000012 and 00000108 respectively. The operand is transferred to the 8-bit port device according to the order of transfer number in Table 3.

Table 2 Dual-Address Sequencing

Row No.	Port Size	Operand Size	Operand Part Size	Operand Part Addresses	Address Increment		
					+	=	−
1	8	BYTE	BYTE	A	+2	0	−2
2	8	WORD	BYTE	A, A+2	+4	0	−4
③	8	LONG	BYTE *4	A, A+2, A+4, A+6 *3 *5 *7 *8	+8	0	−8 *10
4	16	BYTE	PACK (BYTE or WORD)**	A	+P	0	−P
5	16	WORD	WORD	A	+2	0	−2
⑥	16	LONG	WORD *2	A, A+2 *1 *6	+4 *9	0	−4

*Numbers in Table 2 correspond to ones in Tables 3 and 4.
**Refer to Address Sequencing on Operand Part Size and PACK.

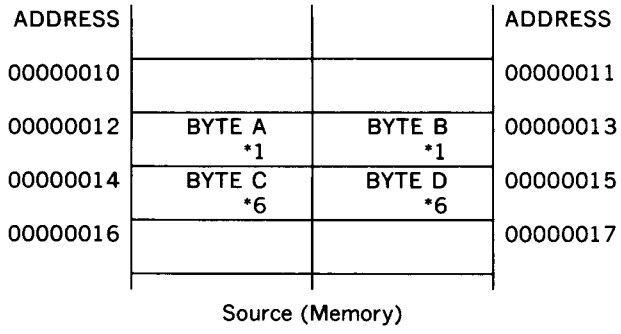
Table 3 An Example of a Data Transfer for One Operand

SRC: Source (Memory), DST Destination (Device), HR: Holding Register (DMAC Internal Reg.)

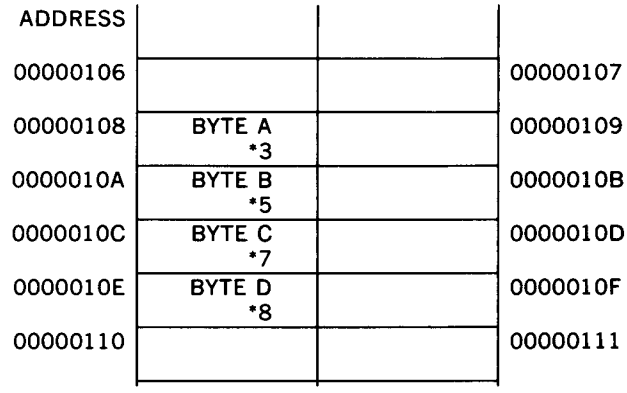
Transfer No.	Data Transfer	Address Output	Data Size on Bus	DMAC Registers after Transfer		Comment
				MAR	DAR	
0	—	—	—	00000012	00000108	Initial Register Setting
1	SRC→HR	00000012 *1	WORD *2	00000014	00000108	Higher order 16 bits of operand is fetched.
2	HR →DST	00000108 *3	BYTE *4	00000014	0000010A	Higher order 16 bits of operand is transferred.
3	HR →DST	0000010A *5	BYTE *4	00000014	0000010C *10	
4	SRC→HR	00000014 *6	WORD *2	00000016 *9	0000010C	Lower order 16 bits of operand is fetched.
5	HR →DST	0000010C *7	BYTE *4	00000016	0000010E	Lower order 16 bits of operand is transferred.
6	HR →DST	0000010E *8	BYTE *4	00000016	00000110 *10	
6′	—	—	—	00000016	00000110	MAR, DAR are pointing the next operand addresses when the transfer is complete.

Mode: Port size=8, operand size=Long Word, Memory to Device, Source (Memory) Counts Up, Destination (Device) Counts Down

Table 4 Memory Map for the Example of the Data Transfer



Source (Memory)



Destination (Device)

● Single Addressing Mode

Implicitly addressed devices are peripheral devices selected not by address but by $\overline{ACK}$. They do not require addressing of data register during data transfer. Transfers between memory and these devices are controlled by the request/acknowledge protocol. Such peripherals require only one bus cycle to transfer data, and the DMAC internal holding register is not used. Because only the memory is addressed during a data transfer and a transfer is done in only one bus cycle, this protocol is called single-addressing.

(1) Device with $\overline{ACK}$ Transfers

Under this protocol, the communication between peripheral device and the DMAC is performed with a two signal $\overline{REQ}/\overline{ACK}$ handshake. When a request is generated using the request method programmed in the DMAC's internal control registers, the DMAC obtains the bus and responds with $\overline{ACK}$. The DMAC asserts all the bus control signals required for the memory access. Refer to Figure 28 for the flowchart of the data transfer from memory to the device with $\overline{ACK}$. Figure 29 shows the flowchart of the data transfer from the device with $\overline{ACK}$ to memory. Receiving the transfer request, the DMAC obtains the bus. Then the DMAC outputs the memory address and asserts $\overline{ACK}$ to inform the I/O device that the transfer request has been acknowledged. When the DMAC accepts $\overline{DTACK}$ from memory, it asserts $\overline{DTC}$ and informs the peripheral device of the transfer termination.

Figures 30 and 31 show the transfer timings of the device with $\overline{ACK}$: the port size for the former figure is 8-bit and the latter is 16-bit respectively.

When the transfer is from memory to a device, data is valid when $\overline{DTACK}$ is asserted and remains valid until the data strobes are negated. The assertion of $\overline{DTC}$ from the DMAC may be used to latch the data as data strobes are not negated half clock period after the assertion of $\overline{DTC}$.

When the transfer is from device to memory, data must be valid on the HD68000 bus before the DMAC asserts the data strobes. The data strobes are asserted one clock period after $\overline{ACK}$ is asserted. When the DMAC obtains the bus and starts a DMA cycle, the three-state of the $\overline{OWN}$ line is cancelled a half clock earlier than other control lines. If the DMA Cycle terminates and the DMAC relinquishes the bus, all the control signals get three-stated a half clock before $\overline{OWN}$. The $\overline{DDIR}$ and

$\overline{DBEN}$ lines are not asserted in the single addressing mode. Four-clock cycle is the smallest bus cycle for the transfer from memory to device. Five-clock cycle is the smallest bus cycle for the transfer from device to memory. If the device port size is 8bits, either $\overline{LDS}$ or $\overline{UDS}$ is asserted. In the single addressing mode, $A_8/D_0 \sim A_{23}/D_{15}$ are outputted for only one and a half clock from the beginning of the DMA bus cycle. Therefore, A_8/D_0 through A_{23}/D_{15} need to be latched externally just like in the dual addressing mode.

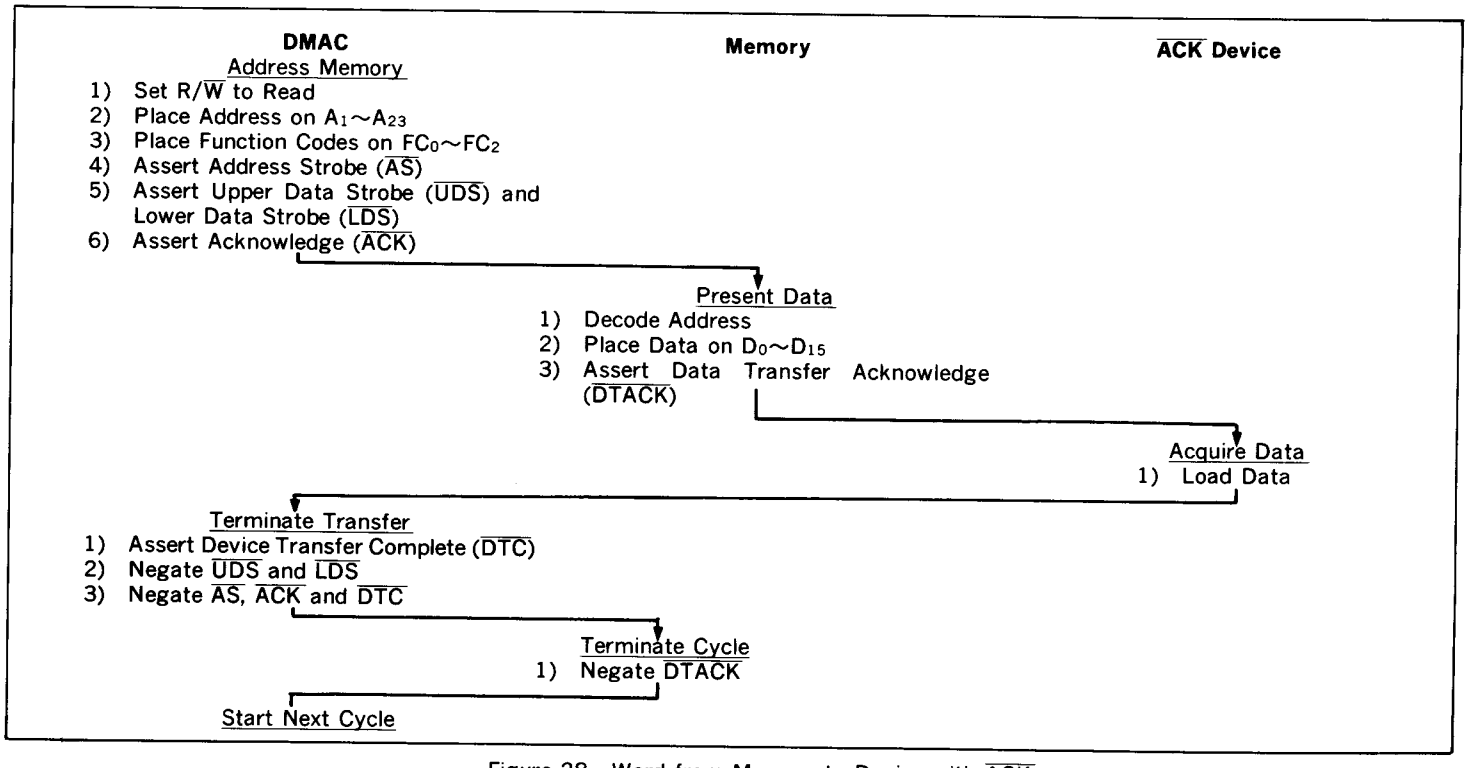


Figure 28 Word from Memory to Device with $\overline{ACK}$

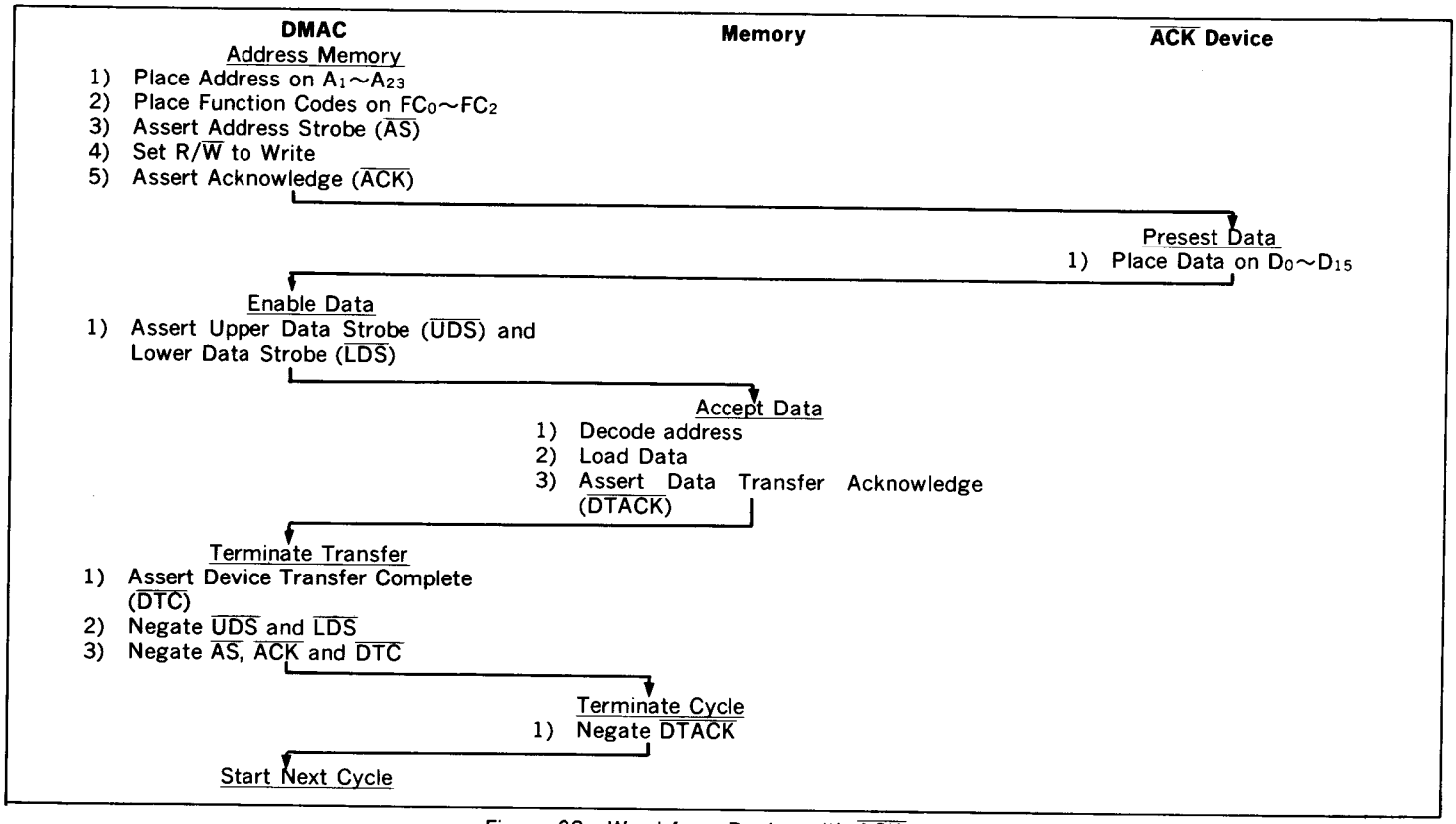


Figure 29 Word from Device with $\overline{ACK}$ to Memory

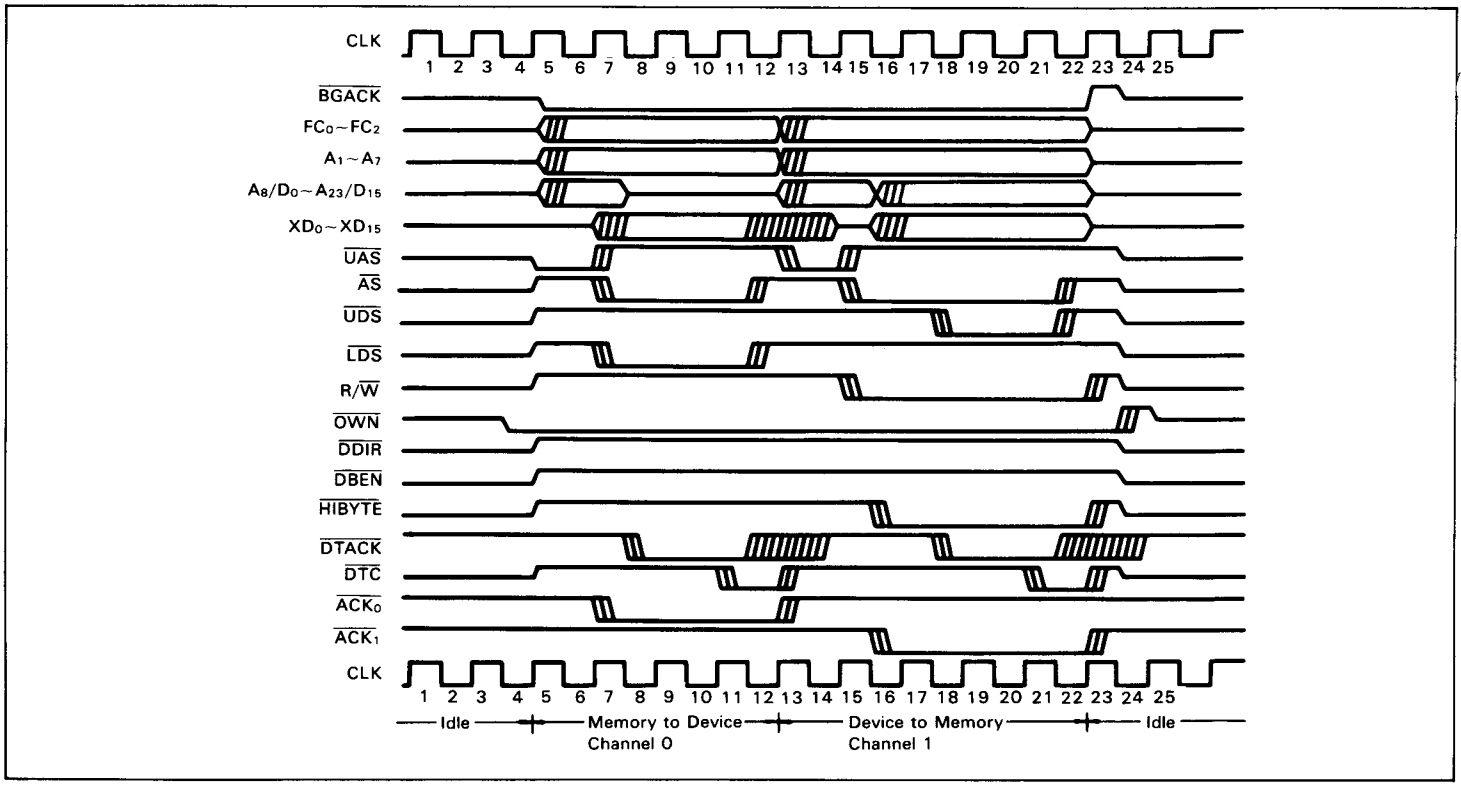


Figure 30 Single Addressing Mode with 8-Bit Devices as Source and Destination (Read-Write Cycles)

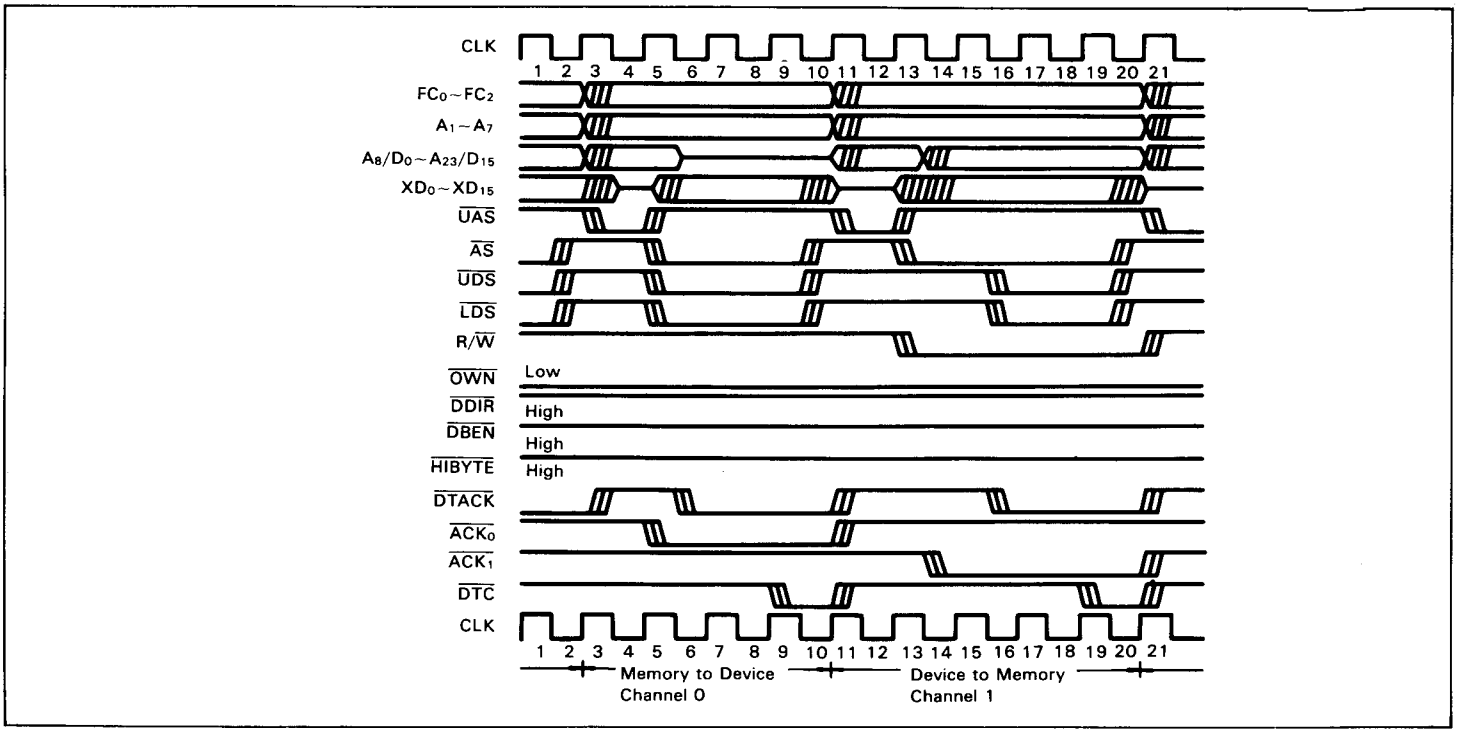


Figure 31 Single Addressing Mode with 16-bit Devices as Source and Destination (Read-Write Cycles)

(2) Device with $\overline{ACK}$ and $\overline{READY}$ Transfers

Under this protocol, the communication between peripheral device and the DMAC is performed using a three signal $\overline{REQ}$/$\overline{ACK}$/$\overline{READY}$ handshake. The $\overline{READY}$ input to the DMAC is provided by the $\overline{PCL}$ line. The $\overline{READY}$ line is active low. When a request is generated using the request method programmed in the control registers, the DMAC obtains the bus and asserts $\overline{ACK}$ to notify the device that the transfer is to take place. The DMAC waits for $\overline{READY}$ ($\overline{PCL}$ input), which is a response from the device, in addition to $\overline{DTACK}$ which is a response from memory.

When the DMAC accepts both signals, it terminates the transfer. Refer to Figures 34 and 35 for the flowcharts of the data transfer between memory and the device with $\overline{ACK}$ and $\overline{READY}$. Refer to Figure 36 for the transfer timing of the 8-bit device. When the data transfer is from memory to a device, data is valid from the assertion of $\overline{DTACK}$ to the negation of $\overline{LDS}$ and $\overline{UDS}$. $\overline{DTC}$ is asserted a half clock before $\overline{LDS}$ and $\overline{UDS}$ are negated, so this line may be used for latching the data by the peripheral device. In this case, $\overline{READY}$ ($\overline{PCL}$ input) indicates that the device has received the data. Both $\overline{DTACK}$ and $\overline{READY}$ ($\overline{PCL}$ input) signals are needed for terminating the DMA cycle.

When the data transfer is from the device to memory, data must be valid on the bus before the DMAC asserts $\overline{LDS}$ and $\overline{UDS}$. Therefore, $\overline{READY}$ ($\overline{PCL}$ input) is used as the signal to indicate that the peripheral device has outputted the data on the bus. When the DMAC detects PCL ($\overline{READY}$ input), then it asserts $\overline{LDS}$ and $\overline{UDS}$. After asserting $\overline{LDS}$ and $\overline{UDS}$, the DMAC terminates the cycle when $\overline{DTACK}$ signal from the memory is detected.

As mentioned above, the I/O device and the DMAC communicate each other through three handshake signals in Figure 32.

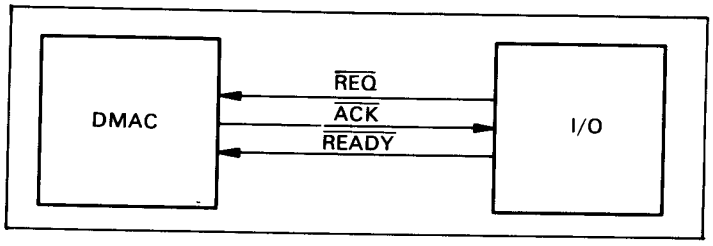
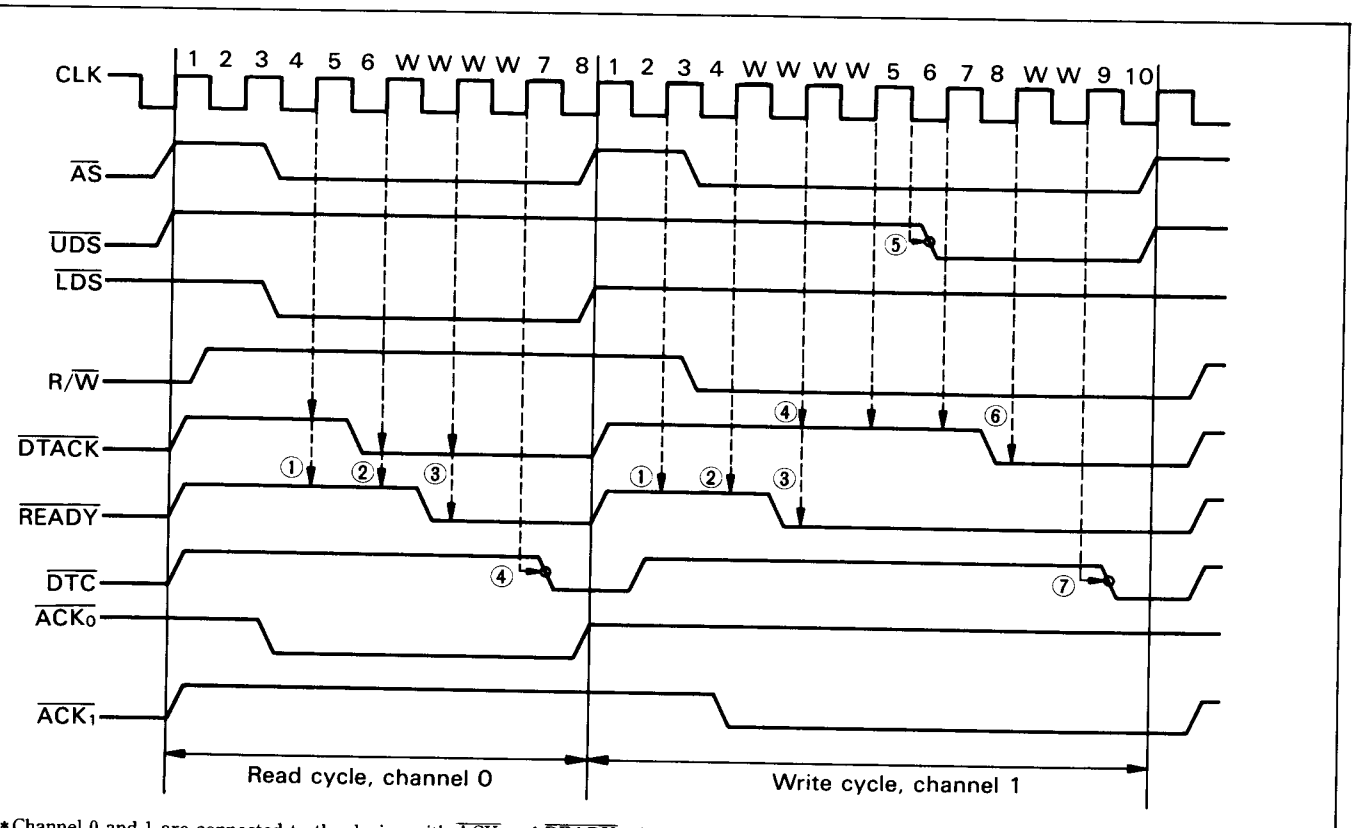


Figure 32 Device with $\overline{ACK}$ and $\overline{READY}$, and DMAC transfer protocol

Figure 33 shows the timing of transfers between the memory and the device with $\overline{ACK}$ and $\overline{READY}$. The detail is as Follows.



*Channel 0 and 1 are connected to the device with $\overline{ACK}$ and $\overline{READY}$ whose port size is 8 bits

Figure 33 Device with $\overline{ACK}$ and $\overline{READY}$ Mode Timing

(i) Data transfer from the memory to the I/O device (read cycle)

The DMAC samples both $\overline{DTACK}$ and $\overline{READY}$ signals at the rising edge of CLK 5 (Figure 33 ①).

Until both signals are asserted, the DMAC repeats wait cycles and samples those signals at each rising edge of the clock : the DMAC does not proceed to CLK 7 and 8 (Figure 33 ②).

When both $\overline{DTACK}$ and $\overline{READY}$ signals are asserted (Figure 33 ③), the DMAC proceeds to CLK 7 and 8, asserts $\overline{DTC}$ at the rising edge of CLK 7 (Figure 33 ④), and terminates the bus cycle. The bus cycle is 4-clock long when there is no wait cycles.

(ii) Data transfer from the I/O device to the memory (write cycle)

The DMAC samples $\overline{READY}$ signal at the rising edge of CLK 3 (Figure 33 ①). Until $\overline{READY}$ signal is asserted, the DMAC repeats wait cycles and samples the signal at each rising edge of the clock : the DMAC does not proceed to CLK 5 and 6 (Figure 33 ②).

When $\overline{READY}$ signal is asserted (Figure 33 ③), the DMAC proceeds to CLK 5~8, and asserts $\overline{DS}$ at the falling edge of CLK 5 (Figure 33 ⑤).

Table 5 indicates the combinations of port size and operand size of the peripheral devices supported by the DMAC in the single and dual addressing modes. In the single addressing mode, port size and operand size must be the same. In the dual addressing mode, byte operand cannot be used when the port size is sixteen and the REQG bit is 10 or 11.

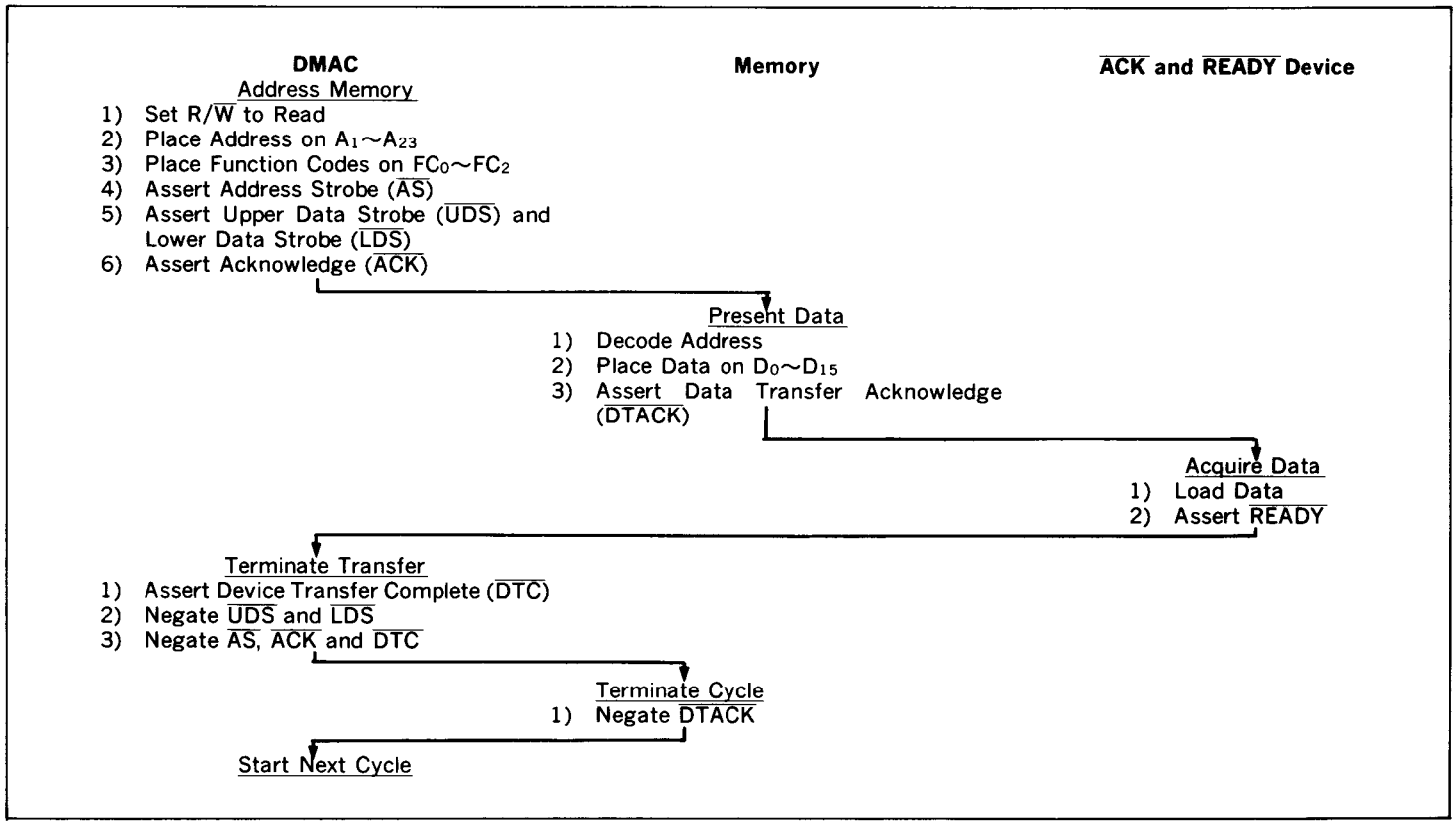


Figure 34 Word from Memory to Device with $\overline{ACK}$ and $\overline{READY}$

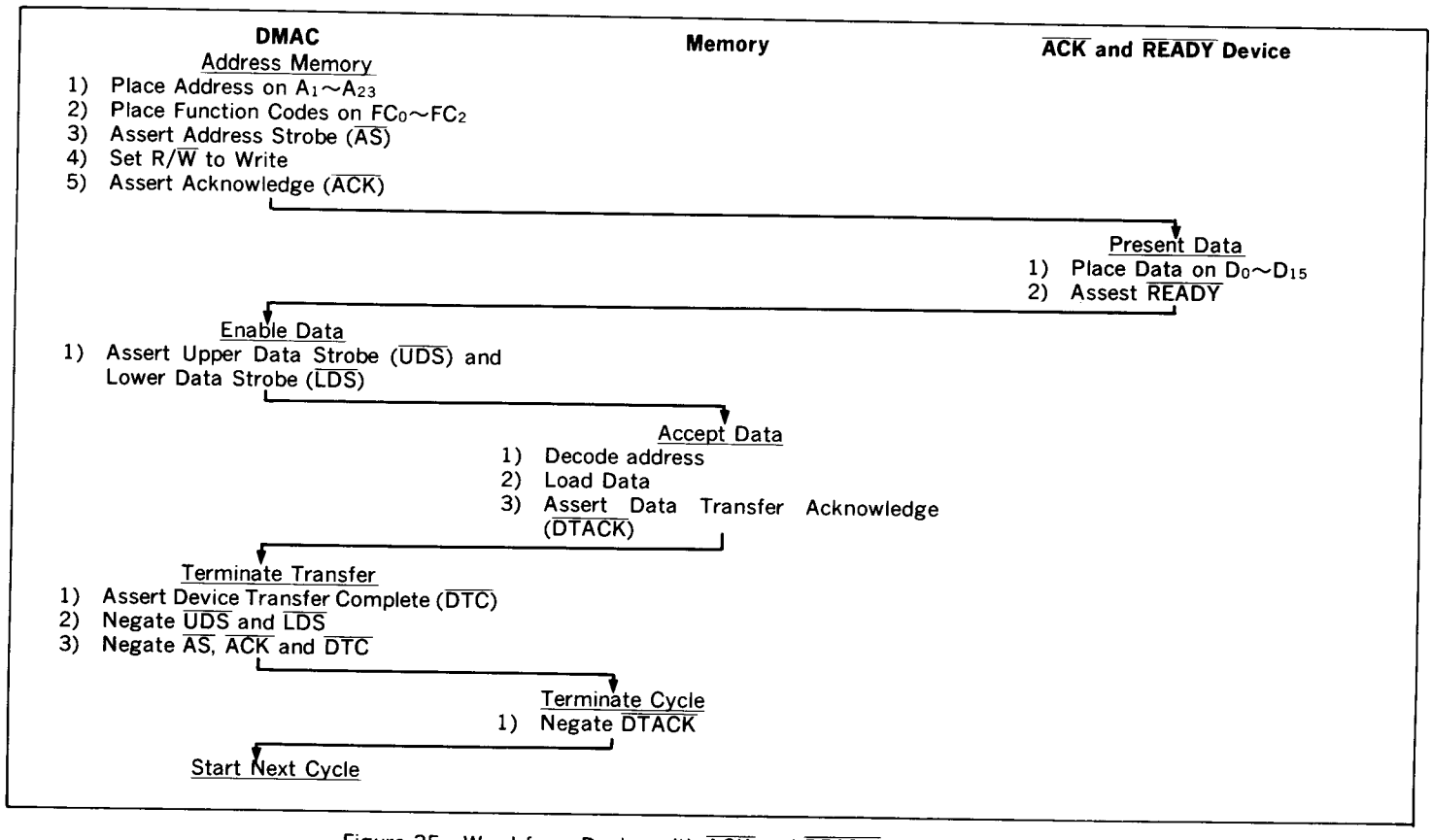


Figure 35 Word from Device with $\overline{ACK}$ and $\overline{READY}$ to Memory

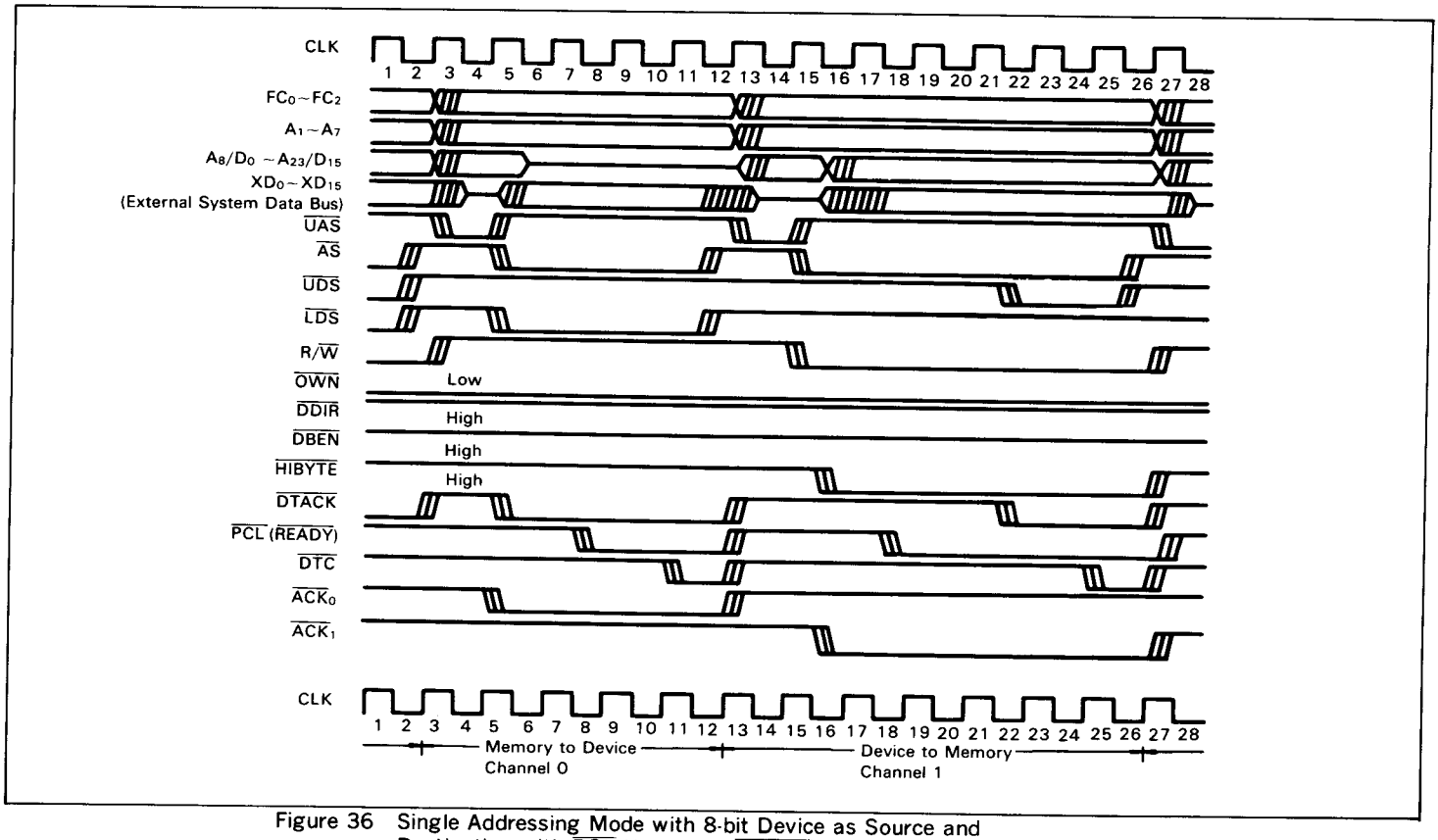


Figure 36 Single Addressing Mode with 8-bit Device as Source and Destination with $\overline{PCL}$ Used as a $\overline{READY}$ input (Read-Write Cycles)

Table 5 Operation Combinations

Addressing	Device Type	Port	Operand			REQG bits of OCR
			Byte	Word	Long Word	
Dual	68000, 6800	8	○	○	○	00, 01, 10, 11
Dual	68000, 6800	16	○	○	○	00, 01
Dual	68000, 6800	16	×	○	○	10, 11
Single	with $\overline{ACK}$ or $\overline{ACK}$ & $\overline{READY}$	8	○	×	×	00, 01, 10, 11
		16	×	○	×	00, 01, 10, 11

○ : supported × : not supported

REQG
- 00: Auto request at a limited rate
- 01: Auto request at a maximum rate
- 10: $\overline{REQ}$ line requests the operand transfer
- 11: First operand is auto requested, and subsequent operands are externally requested.

● Address Sequencing

The sequence of addresses generated depends upon the port size, whether the addresses are to count up, down or not change and whether the transfer is executed in the single addressing mode or the dual addressing mode. The memory address count method and the peripheral device address count method is programmed using the Memory address count (MAC) bit and the Device address count (DAC) bit in the Sequence Control Register (SCR).

(i) Single addressing mode
In the single addressing mode, memory address sequencing is shown in Table 6. If the operand size is byte, the memory address increment is one (1). If the operand size is word, the memory address increment is two (2). If the memory address register does not count, the memory address is unchanged after the transfer.

(ii) Dual addressing mode
In the dual addressing mode, the operand size need not match the port size. Thus the transfer of an operand may require several DMA bus cycles. Each DMA bus cycle, between memory and DMAC and between DMAC and the device, is called the operand part and transfers a portion or all of the operand. The addresses of the operand parts are in a linear increasing sequence. The step between the addresses of the operand is two. The size of the operand part is the minimum of the port size and the operand size. The number of the operand part is the operand size divided by the port size.

In the dual addressing mode, memory is regarded as a device whose port size is 16 bits and the operand size is a byte or a word. When the operand is transferred to the memory from the I/O device whose port size is 8 bits and the operand size is byte, the DMAC reads 2-byte operand one byte at a time from the I/O device and writes 2 bytes at the same time to the memory, or reads one byte from the I/O device and writes one byte to the memory. Thus, when the port size is 8 bits and the operand size is byte, two-operand transfer which is performed at the same time is called PACK. Utilizing the PACK, the DMAC may improve the DMA bus efficiency. However, packing is not performed if the address does not count. When the port size is 8 bits and the operand size is byte (port size : 8 bits, without PACK) with the DMAC in the dual addressing mode, the DMAC repeats the following cycles :

① READ BYTE (reads data from the I/O device or the memory)
② WRITE BYTE (writes data to the I/O device or the memory)

Table 7 shows the dual addressing sequencing

Table 6 Single Address Sequencing

Port Size	Operand Size	Memory Address Increment		
		+(increment)	=(unchanged)	−(decrement)
8	Byte	+1	0	−1
16	Word	+2	0	−2

Table 7 Dual Address Sequencing

Port Size	Operand Size	Part Size	Operand Part Address	Address Increment		
				+	=	−
8	Byte	Byte	A	+2	0	−2
8	Word	Byte	A, A+2	+4	0	−4
8	Long	Byte	A, A+2, A+4, A+6	+8	0	−8
16	Byte	Pack	A	+P	0	−P
16	Word	Word	A	+2	0	−2
16	Long	Word	A, A+2	+4	0	−4

P = 1 if packing is not done
= 2 if packing is done

Pack = byte if packing is not done
= word if packing is done

■INITIATION AND CONTROL OF CHANNEL OPERATION

● Operation Initiation

To initiate the operation of a channel, the STR bit of the CCR is set to start the operation. Setting the STR bit causes the immediate activation of the channel, the channel will be ready to accept requests immediately. The channel initiates the operation by resetting the STR bit and setting the channel active bit in the CSR. Any pending requests are cleared, and the channel is then ready to receive requests for the new operation. If the channel is configured for an illegal operation, the configuration error is signaled, and no channel operation is run. The illegal operations include the selection of any of the options marked "(undefined, reserved)". If the MTC is set to zero in any mode other than the chaining mode, or BTC is set to zero in the array chaining mode, then the count error is signaled and the channel is not activated. The channel cannot be started if any of the ACT, COC, BTC, NDT or ERR bit is set in the CSR. In this case, the channel signals the operation timing error.

● Operation Continuation (Continue Mode)

When the STR bit or the ACT bit in the CSR is set, setting the CNT (Continue) bit in the CCR allows multiple blocks to be transferred as in the chaining modes. The CNT bit is set in order to continue the current channel operation. To set the CNT bit, the initial address of the next block to be transferred, the corresponding function code, and the number of words to be transferred must be previously set to the BAR, BFC and BTC. If the CNT bit is set when either the STR or the ACT bit is not set, the operation timing error is signaled. The configuration error is signaled when the CNT bit is set in the chaining modes.

● Operation Halting (Halt)

The CCR has a halt bit which allows suspension of the operation of the channel. If this bit is set, a request may still be generated and recognized, but the DMAC does not attempt to acquire the bus or to make transfers for the halted channel. When this bit is reset, the channel resumes operation and services any request that may have been received while the channel was halted. However, in the burst request mode, the transfer request should be kept asserted until the initiation of the first transfer after clearing the halt bit.

● Operation Abort by Software (Software Abort)

Setting the software abort bit (SAB) in the CCR allows the current operation of the channel to be aborted. In this case, the ERR bit and the COC bit in the CSR are set and the ACT bit is reset. The error code for the software abort is set in the CER. The SAB bit is designed to be reset if the ERR bit is reset. When the CCR is read, the SAB always reads as zero(0).

■CHANNEL OPERATION TERMINATION

As part of the transfer of an operand, the DMAC decrements the memory transfer counter(MTC). If the chaining mode is not used and the CNT bit is not set or the last block is transferred in the chaining mode, the operation of the channel is complete when the last operand transfer is completed and the MTC is zero. The DMAC notifies the peripheral device of the channel completion via the $\overline{\text{DONE}}$ output.

However, in the continue mode, $\overline{\text{DONE}}$ is outputted at the termination of every data block transfer. When the channel operation has been completed, the ACT bit of the CSR is cleared, and the COC bit of the CSR is set.

The occurrence of errors, such as the bus error, during the DMA bus cycle also terminates the channel operation. In this case, the ACT bit in the CSR is cleared, the ERR and the COC bits are set, and at the same time the code corresponding to the error that occurred is set in the CER.

● Channel Status Register (CSR)

The channel status register contains the status of the channel at the channel operation termination. The register is cleared by writing a one (1) into each bit of the register to be cleared.

COC

The channel operation complete (COC) bit is set if the channel operation has completed. The COC bit must be cleared in order to start another channel operation. The COC bit is cleared only by writing a one to this bit or resetting the DMAC.

PCS

The peripheral status (PCS) bit reflects the level of the $\overline{\text{PCL}}$ line regardless of its programmed function. If $\overline{\text{PCL}}$ is at "High" level, the PCS bit reads as one. If $\overline{\text{PCL}}$ is at "Low" level, the PCS bit reads as zero. The PCS bit is unaffected by writing to the CSR.

PCT

The peripheral control transition (PCT) bit is set, if a falling edge transition has occurred on the $\overline{\text{PCL}}$ line. (The $\overline{\text{PCL}}$ line must remain at "low" level for at least two clock cycles.) The PCT bit is cleared by writing a one to this bit or resetting the DMAC.

BTC

Block transfer complete (BTC) bit is set when the continue (CNT) bit of CCR is set and the memory transfer counter (MTC) is exhausted. The BTC bit must be cleared before the another continuation is attempted (namely, setting the CNT bit again), otherwise an operation timing error occurs. The BTC bit is cleared by writing a one to this bit or resetting the DMAC.

NDT

Normal device termination (NDT) bit is set when the peripheral device terminates the channel operation by asserting the $\overline{\text{DONE}}$ line while the peripheral device was being acknowledged. The NDT bit is cleared by writing a one to this bit or resetting the DMAC.

ERR

Error (ERR) bit is set if any errors have been signaled, When the ERR bit is set, the code corresponding to the kind of the error that occured is set in the CER. The ERR bit is clered by writing a one to this bit or resetting the DMAC.

ACT

The active (ACT) bit is asserted after the STR bit has been set and the channel operation has started. This bit remains set until the channel operation is terminated. The ACT bit is unaffected by write operations. This bit is cleared by the termination of the channel or resetting the DMAC.

DIT

Done input transition (DIT) bit is set if the $\overline{\text{DONE}}$ input is generated while the multiple block transfer mode with $\overline{\text{DONE}}$ is being set. The DIT bit is cleared by writing a one to this bit or resetting the DMAC.

● Interrupts

The DMAC can signal the termination of the channel operation by generating an interrupt request. The interrupt request is generated by the following condition.

① INT=1
and
② COC=1 or BTC=1 or ERR=1 or NDT=1 or PCT=1
(the $\overline{PCL}$ line is an interrupt input)
This may be represented as
$\overline{IRQ}=INT \cdot (COC+BTC+ERR+NDT+PCT^*)$
(*PCL line is programmed as an interrupt input.)

When the $\overline{IRQ}$ line is asserted, changing the INT bit from one to zero to one will cause the $\overline{IRQ}$ output to change from "low" to "high" to "low" again. The $\overline{IRQ}$ should be negated by clearing the COC, the BTC, the ERR, the NDT and the PCT bits.

If the DMAC receives $\overline{IACK}$ from the MPU during asserting the $\overline{IRQ}$, the DMAC provides an interrupt vector. If multiple channels have interrupt requests, the determination of which channel presents its interrupt vector is made using the same priority scheme defined for the channel operations.

The bus cycle in which the DMAC provides the interrupt vector when receiving an $\overline{IACK}$ from the MPU is called the interrupt acknowledge cycle. The interrupt vector returned to the MPU comes from either the nomal or the error interrupt vector register. The normal interrupt register is used unless the ERR bit of CSR is set, in which case the error interrupt vector register is used. The content of the interrupt vector register is placed on $A_8/D_0 \sim A_{15}/D_7$, and $\overline{DTACK}$ is asserted to indicate that the vector is on the data bus. If a reset occurs, all interrupt vector registers are set to $(00001111)_2$, the value of the uninitialized interrupt vector of the HD68000 MPU. The timing of the interrupt acknowledge cycle is shown in Figure 36. The HD68000 MPU outputs the interrupt level into A_1-A_3 and "1" into A_4-A_7 during the interrupt acknowledge cycle, but the HD63450 DMAC ignores these signals.

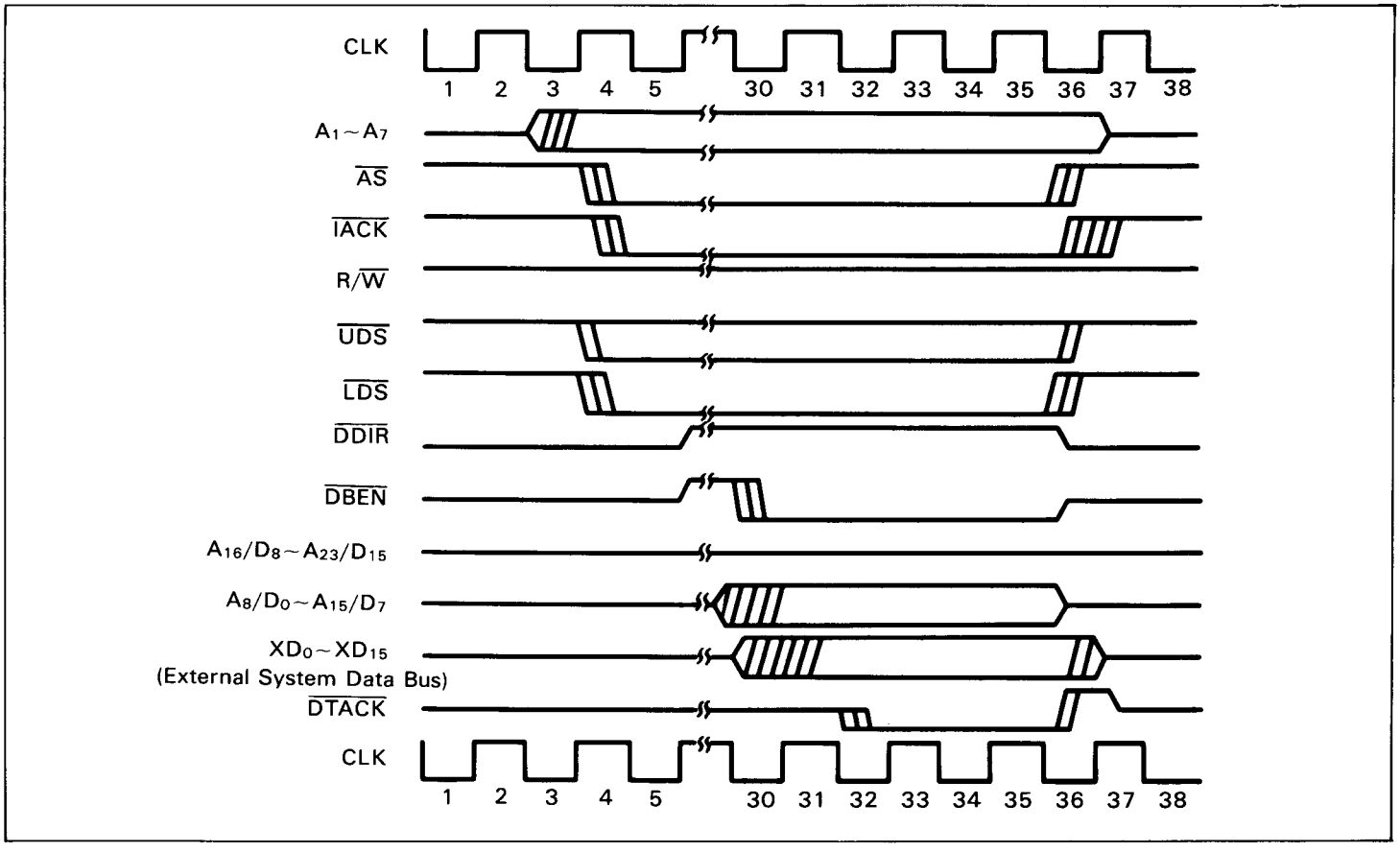


Figure 37 MPU $\overline{IACK}$ Cycle to DMAC

● Multiple Data Block Transfer Operation

When the memory transfer counter (MTC) is exhausted, the channel operation still continues if the channel is set to the array chaining mode or the linked array chaining mode, and the chain is not exhausted. The channel operation also continues if the continue bit (CNT) of the CCR is set. The DMAC provides the initialization of the memory address register and the memory transfer counter in these cases so that the DMAC can transfer the multiple blocks.

Continued Operation

The continued operation is described in the Initiation and the Control of the Channel Operation section.

Array Chaining

This type of chaining uses an array in memory consisting of memory addresses and transfer counts. Each entry in the array is six bytes long and, consists of four bytes of address followed by two bytes of transfer count. The beginning address of this array is in the base address register, and the number of entries in the array is in the base transfer counter. Before starting any block transfers, the DMAC fetches the entry currently pointed to by the base address register. The address information is placed in the memory address register, and the count information is placed in the memory transfer counter. As each chaining entry is fetched, the base transfer counter is decremented by one. After the chaining entry is fetched, the base address register is incremented

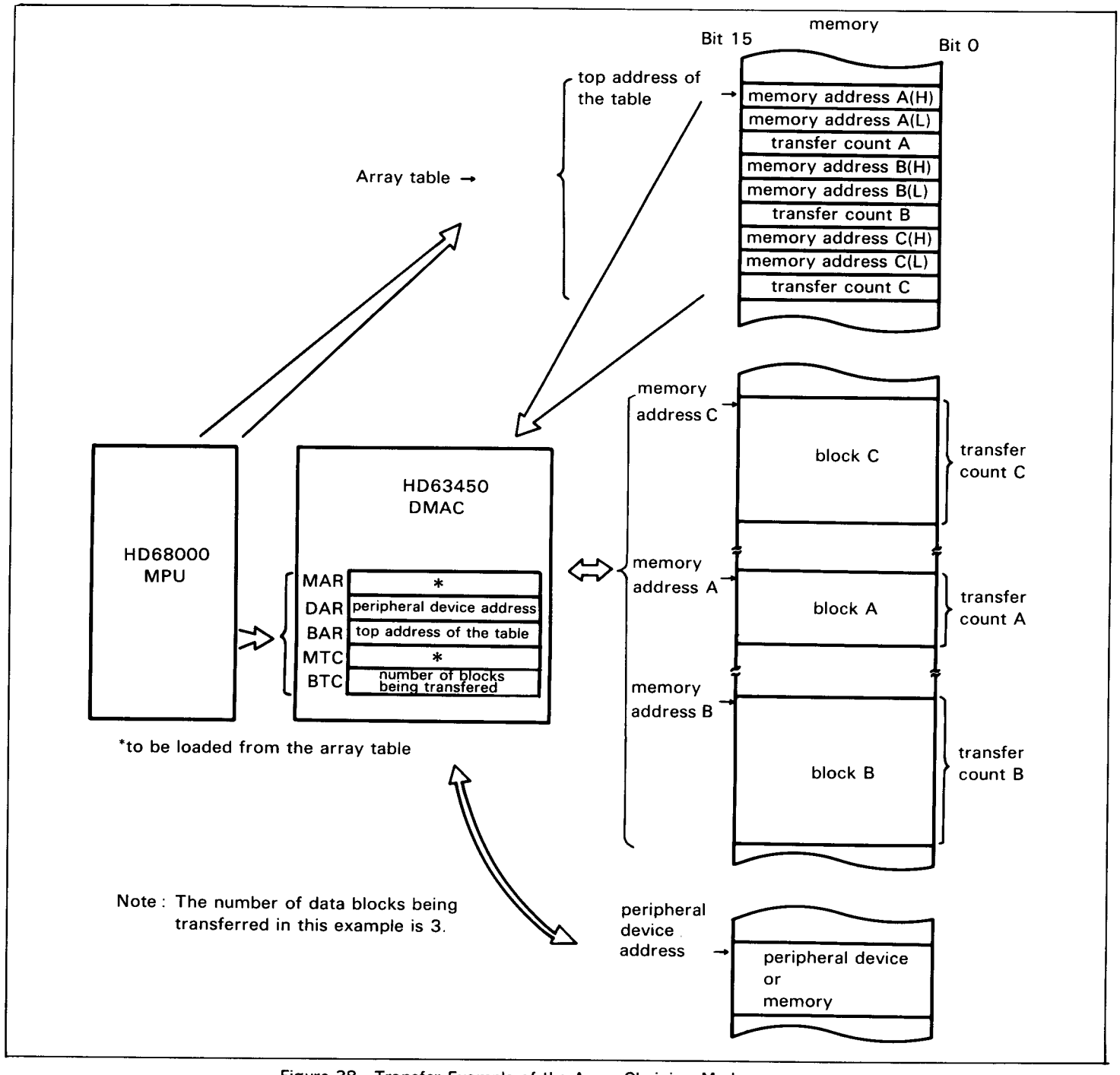


Figure 38 Transfer Example of the Array Chaining Mode

to point the next entry. When the base transfer counter reaches a terminal count of zero, the chain is exhausted, and the entry just fetched determines the last block of the channel operation.

An example of the array chaining mode operation and the memory format for supporting for array chaining is shown in Figure 38. The array must start at an even address, or the entry fetch results in an address error. If a terminal count is loaded into the memory transfer counter or the base transfer counter, the count error is signaled.

Linked Array Chaining

This type of chaining uses a list in memory consisting of memory address, transfer counts, and link addresses. Each entry in the chain list is ten bytes long, and consists of four bytes of memory address, two bytes of transfer count and four bytes of link address. The address of the first entry in the list is in the base address register, and the base transfer counter is unused. Before starting any block transfers, the DMAC fetches the entry currently pointed to by the base address register. The address information is placed in the memory address register, the count information is placed in the memory transfer counter, and the link address replaces the current contents of the base address

register. The channel then begins a new block transfer. As each chaining entry is fetched, the update base address register is examined for the terminal link which has all 32 bits equal to zero. When the new base address is the terminal address, the chain is exhausted, and the entry just fetched determines the last block of the channel operation.

An example of the linked array chaining mode operation and the memory format for supporting it is shown is Figure 39.

In Figure 39, the DMAC transfers data blocks in the order of Block A, Block B, and Block C. In the linked array chaining mode, the BTC is not used. When the DMAC refers to the linked array table, the value of the BFC is outputted as the function code. The values of the function code registers are unchanged by the linked array chaining operation.

This type of chaining allows entries to be easily removed or inserted without having to reorganize data within the chain. Since the end of the chain is indicated by a terminal link, the number of entries in the array need not be specified to the DMAC.

The linked array table must start at an even address in the linked array chaining mode. Starting the table at an odd address results in an address error. If "0" is initially loaded to the MTC, the count error is signaled. Because the MPU can read all of the DMAC registers, all necessary error recovery information is available to the operating system.
The comparison of both chaining modes is shown in Table 8.

Table 8 Chaining Mode Address/Count Information

Chaining Mode	Base Address Register	Base Transfer Counter	Completed When
Array Chaining	address of the array table	number of data blocks being transferred	Base Transfer Count=0
Linked Array Chaining	address of the linked array table	(not used)	Linked Address=0

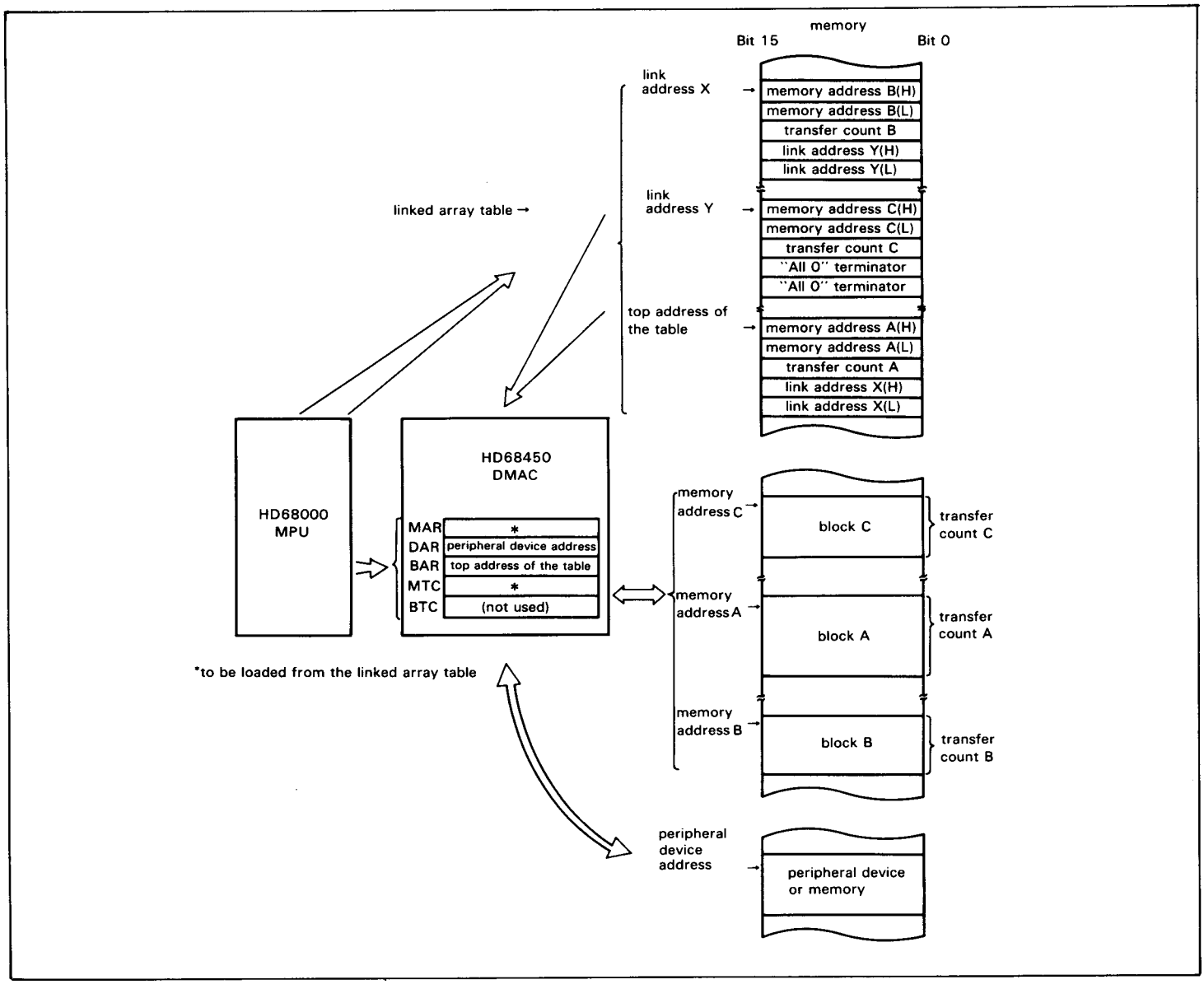


Figure 39 Transfer Example of the Linked Array Chaining Mode

Multi-Block Transfer with $\overline{\text{DONE}}$ Mode

The multi-block transfer with $\overline{\text{DONE}}$ mode is set by setting BTD bit of the OCR. In this mode, data block transfer continues even if the $\overline{\text{DONE}}$ signal is inputted during the DMA bus cycle. If $\overline{\text{DONE}}$ is inputted during the DMA bus cycle when the multi-block transfer is not performed, the DMAC resets ACT bit of the CSR, sets NDT and COC bits, and terminates the DMA operation.

When $\overline{\text{DONE}}$ is inputted from the I/O device during the DMA bus cycle in which $\overline{\text{ACK}}$ is outputted, the DMAC terminates the operand transfer and then the current block transfer. Then, maintaining the bus, the DMAC sets DIT bit of the CSR and reads the data block transfer information from the memory. After that, the DMAC transfers the next block as required.

In the continue mode, if $\overline{\text{DONE}}$ is inputted from the I/O device during the DMA bus cycle in which $\overline{\text{ACK}}$ is outputted, the DMAC terminates the operand transfer and terminates the current block transfer. Then the DMAC shifts the data in BAR, BFC and BTC to MAR, MFC and MTC, waits for the transfer request, and transfers the next block. If the value of BAR, BFC and BTC is the same as that of MAR, MFC and MTC, the DMAC repeats transferring the same block.

As stated above, the multi-block transfer with $\overline{\text{DONE}}$ mode realizes termination (stops the current block transfer) and restart (starts transferring the next block) of the multi-block transfer in the high-speed data transfer system without MPU interposition.

• Bus Exception Conditions

The DMAC has three lines for inputting bus exception conditions called $\overline{\text{BEC}_0}$, $\overline{\text{BEC}_1}$, and $\overline{\text{BEC}_2}$. The priority encoder can be used to generate these signals externally. These lines are encoded as shown in Table 9.

Table 9 BEC Bus Exception Condition

$\overline{\text{BEC}_2}$	$\overline{\text{BEC}_1}$	$\overline{\text{BEC}_0}$	Exception Condition
1	1	1	No exception condition
1	1	0	Halt
1	0	1	Bus error
1	0	0	Retry
0	1	1	Relinquish bus and retry
0	1	0	(undefined, reserved)
0	0	1	(undefined, reserved)
0	0	0	Reset

In order to guarantee reliable decoding, the DMAC verifies that the incoming code has been stable for two DMAC clock cycles before acting on it. The DMAC picks up $\overline{\text{BEC}_0}$-$\overline{\text{BEC}_2}$ at the rising edge of the clock. If $\overline{\text{BEC}_0}$-$\overline{\text{BEC}_2}$ is asserted to the undefined code, the operation of the DMAC does not proceed. For example, when the DMAC is waiting for $\overline{\text{DTACK}}$, inputting $\overline{\text{DTACK}}$ does not result in the termination of the cycle if $\overline{\text{BEC}_0}$-$\overline{\text{BEC}_2}$ is asserted to the undefined code. In addition, when the transfer request is received, $\overline{\text{BR}}$ is not output if the $\overline{\text{BEC}_0}$-$\overline{\text{BEC}_2}$ is not set to code (111).

If exception condition, except for HALT, is inputted during the DMA bus cycle prior to, or in coincidence with $\overline{\text{DTACK}}$, the DMAC terminates the current channel operation immediately. Here coincident means meeting the same set up requirements for the same sampling edge of the clock. $\overline{\text{BEC}_0}$~$\overline{\text{BEC}_2}$ is ignored in the current DMA bus cycle if it is input after $\overline{\text{DTACK}}$. If a bus exception condition exists, the DMAC does not generate any bus cycles until it is removed. However, the DMAC still recognizes requests.

Halt

The timing diagram of halt is shown in Figure 40. This diagram shows halt being generated during a read cycle from the 68000 compatible device in the dual addressing mode. If the halt exception is asserted during a DMA bus cycle, the DMAC does not terminate the bus cycle immediately. The DMAC waits for the assertion of $\overline{\text{DTACK}}$ before terminating the bus cycle so that the bus cycle is completed normally. In the halted state, the DMAC puts all the control signals to high impedance and relinquishes the bus to the MPU. The DMAC does not output the $\overline{\text{BR}}$ until halt exception is negated. When halt exception is negated, the DMAC acquires the bus again and proceeds the DMA operation. In order to insure a halt exception operation, the $\overline{\text{BEC}}$ lines must be set to halt at least until the assertion of $\overline{\text{DTC}}$.

If the halt is asserted when the DMAC has the bus but is not executing any bus cycle, the DMAC relinquishes the bus as soon as halt exception is asserted.

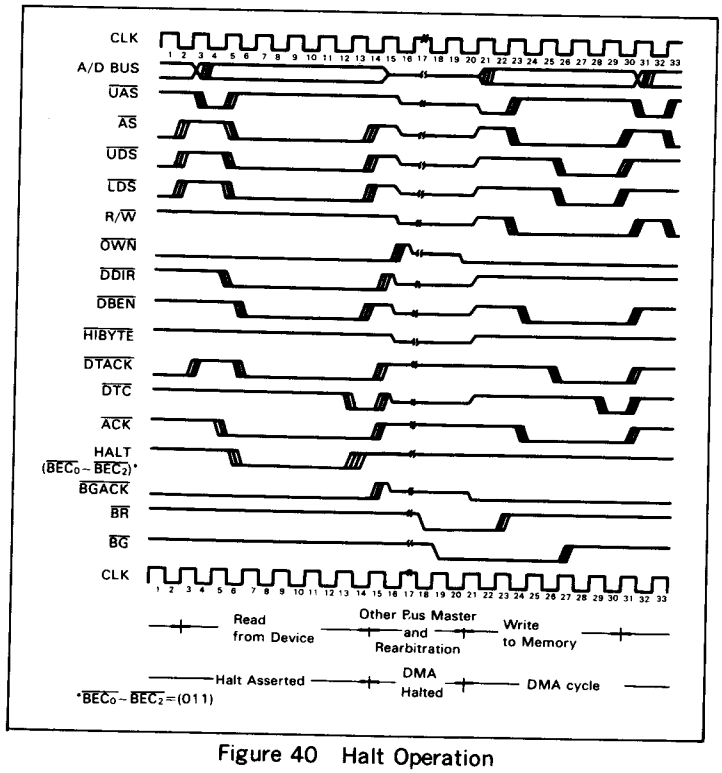


Figure 40 Halt Operation

Bus Error

The bus error exception is generated by external circuitry to indicate the current transfer cannot be successfully completed and is to be aborted. As soon as the DMAC recognizes the bus error exception, the DMAC immediately terminates the bus cycle and proceeds to the error recovery cycle. In this cycle, the DMAC adjusts the values of the MAR, the DAR, the MTC and the BTC to the values when the bus error exception occurred. 24 clocks are required for the error recovery cycle in the single addressing mode and in the read cycle of the dual addressing mode. 28 clocks are required in the write cycle of the dual addressing mode. If the DMAC does not have any transfer request in the other channels after the error recovery cycle, the DMAC relinquishes the bus.

The diagram of the bus error timing is shown in Figure 41.

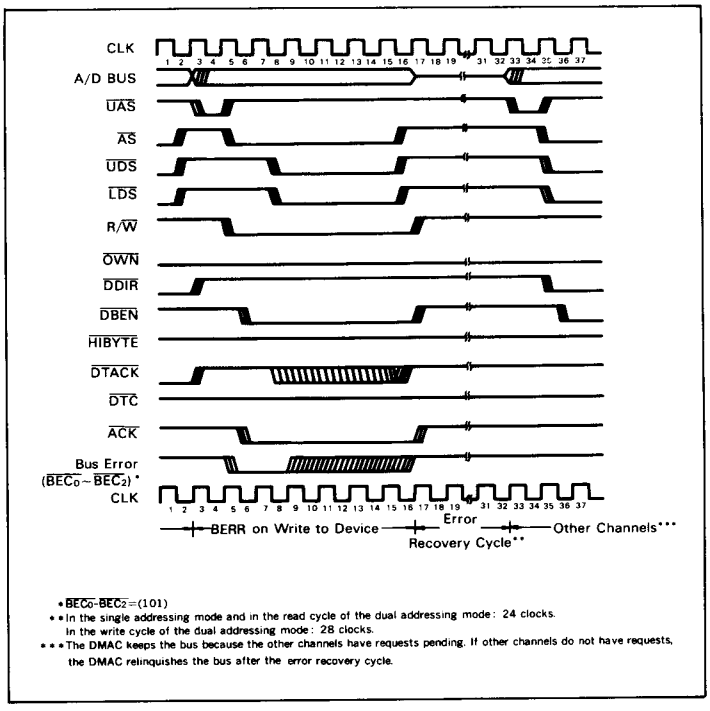


Figure 41 Bus Error Operation

Retry

The retry exception causes the DMAC to terminate the present operation and retry that operation when retry is removed, and thus will not honor any requests until it is removed. However, the DMAC still recognizes requests. The retry timing is shown in Figure 42.

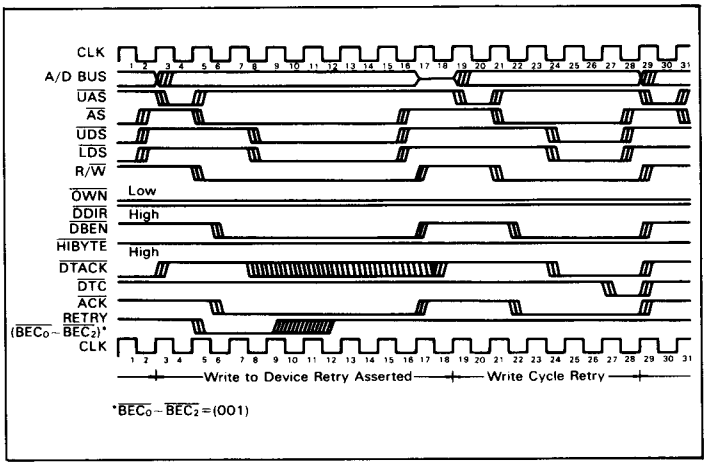


Figure 42 Retry Operation

Relinquish and Retry (R & R)

The relinquish and retry exception causes the DMAC to relinquish the bus and three-state all bus master controls and when the exception is removed, rearbitrate for the bus to retry the previous operation.

The diagram of the relinquish and retry timing is shown in Figure 43.

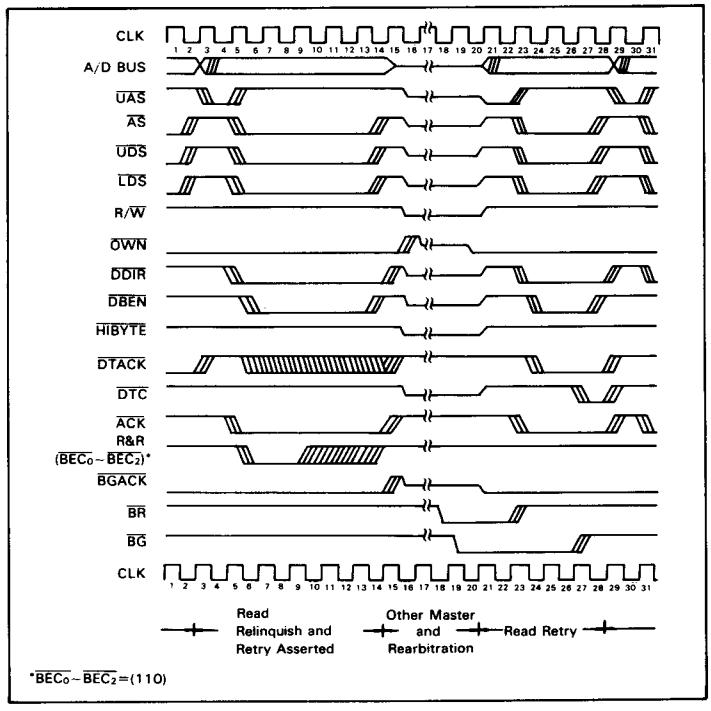


Figure 43 Relinquish and Retry Operation

Reset

The reset provides a means of resetting and initializing the DMAC. If the DMAC is bus master when the reset is asserted, the DMAC relinquishes the bus. Reset clears GCR, DCR, OCR, SCR, CCR, CSR, CPR, and CER for all channels. The NIV and the EIV are all set to $(OF)_{16}$, which is the uninitialized interrupt vector number for the HD68000 MPU. MTC, MAR, DAR, BTC, BAR, MFC, DFC, and BFC are not affected (see Table 10).

In order to insure a reset, $\overline{BEC_0}$~$\overline{BEC_2}$ must be kept at "Low" level for at least ten clocks.

Table 10 The Value after Resetting

Register	Value	Comments
MAR	××××××××	
DAR	××××××××	
BAR	××××××××	
MFC	×	
DFC	×	
BFC	×	
MTC	××××	
BTC	××××	
NIV	0 F	uninitialized vector
EIV	0 F	uninitialized vector
CPR	0 0	
DCR	0 0	
OCR	0 0	
SCR	0 0	
CCR	0 0	
CSR	0 0 or 0 1	depending on $\overline{PCL}$
CER	0 0	
GCR	0 0	

×—indefinite value, or the value before resetting

● Error Conditions

When an error is signaled on a channel, all activity on that channel is stopped. The ACT bit of the CSR is cleared, and the COC bit is set. The ERR bit of the CSR is set, and the error code is indicated in the CER. All pending operations are cleared, so that both the STR and CNT bits of CCR are cleared.

Enumerated below are the error signals and their sources.

(a) Configuration Error—This error occurs if the STR bit is set in the following cases.
  (i) The CNT bit is set at the same time STR bit in the chaining mode.
  (ii) DTYP specifies a single addressing mode, and the device port size is not the same as the operand size.
  (iii) DTYP specifies a dual addressing mode, DPS is 16 bits, SIZE is 8 bits and REQG is "10" or "11".
  (iv) An undefined configuration is set in the registers. The undefined configuraions are: XRM=01, MAC=11, DAC =11, CHAIN=01, and SIZE=11.
  When the port size is 8 bits, SIZE=11 is not an error in the dual addressing mode.

(b) Operation Timing Error—An operation timing error occurs in the following cases:
  (i) When the CNT bit is set after the ACT bit has been set by the DMAC in the chaining mode, or when the STR and the ACT bits are not set.
  (ii) The STR bit is set when ACT, COC, BTC, NDT or ERR is set.
  (iii) An attempt to write to the DCR, OCR, SCR, MAR, DAR, MTC, MFC, or DFC is made when the STR bit or the ACT bit is set.
  (iv) An attempt to set the CNT bit is made when the BTC and the ACT bits are set.

(c) Address Error—An address error occurs in the following cases:
  (i) An odd address is set for word or long word operands.
  (ii) $\overline{CS}$ or $\overline{IACK}$ is asserted during the DMA bus cycle.

(d) Bus Error—Bus error occurs when a bus error exception is signaled during a DMA bus cycle.

(e) Count Error—A count error occurs in the following cases:
  (i) The STR bit is set when zero is set in the MTC and the chaining mode is not used.
  (ii) The STR bit is set when zero is set in BTC for the array chaining mode.
  (iii) Zero is loaded from memory or the BTC to the MTC in the chaining modes or the continue mode.

(f) External Abort—External abort occurs if an abort is asserted by the external circuitry when the $\overline{PCL}$ line is configured as an abort input and the STR or the ACT bit is set.

(g) Software Abort—Software abort occurs if the SAB bit is set when the STR or the ACT bit is set.

Error Recovery Procedures

If an error occurs during a DMA transfer, appropriate information is available to the operating system (OS) to allow a software failure recovery operation. The operating system must be able to determine how much data was transferred, where the data was transferred to, and what type of error occurred.

The information available to the operating system consists of the present value of the Memory Address, Device Address and Base Address Register, the Memory Transfer and Base Transfer Counters, the channel status register, the channel error register. After the successful completion of any transfer, the memory and device address registers point to the location of the next operand to be transferred and the memory transfer counter contains the number of operands yet to be transferred. If an error occurs during a transfer, that transfer has not completed and the registers contain the values they had before the transfer was attempted. If the channel operation uses chaining, the Base Address Register points to the next chain entry to be serviced, unless the termination occurred while attempting to fetch an entry in the chain. In that case, the Base Address Register points to the entry being fetched. However, in the case of external abort, there are cases in which the previous values are not recovered.

Bus Exception Operating Flow

The bus exception operating flow in the case of multiple exception conditions occurring continuously in sequence is shown in Figure 44. Note that the DMAC can receive and execute the next exception condition before completing the current exception operation. For example, if the retry exception occurs, and next the relinquish and retry exception occurs while the DMAC is waiting for the retry condition to be cleared, the DMAC relinquishes the bus and waits for the exception condition to be cleared. If a bus error occurs during this period, the DMAC executes the bus error exception operation.

The flow diagram of the normal operation without exception operation or errors is shown in Figure 45.

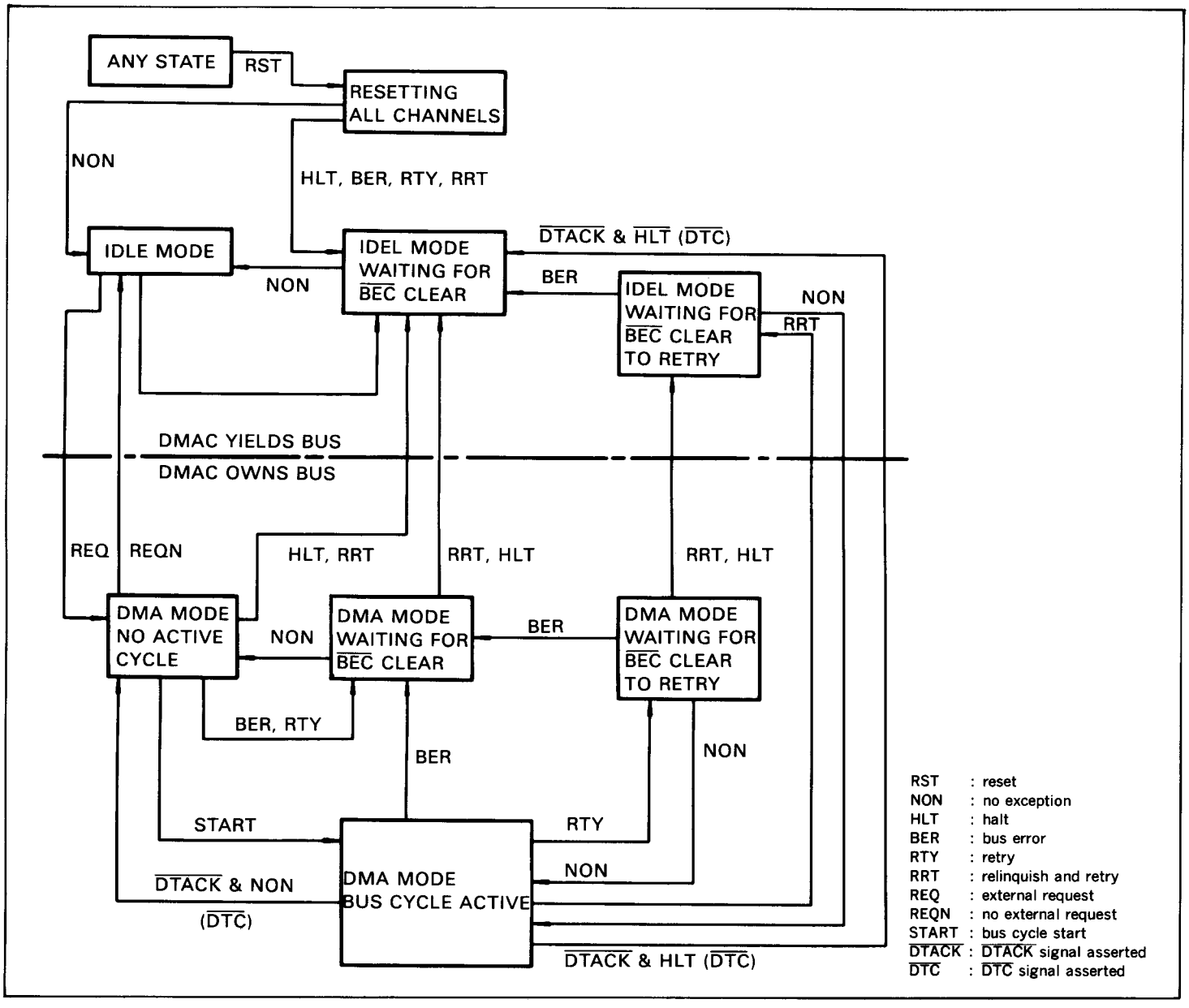


Figure 44 Bus Exception Flow Diagram

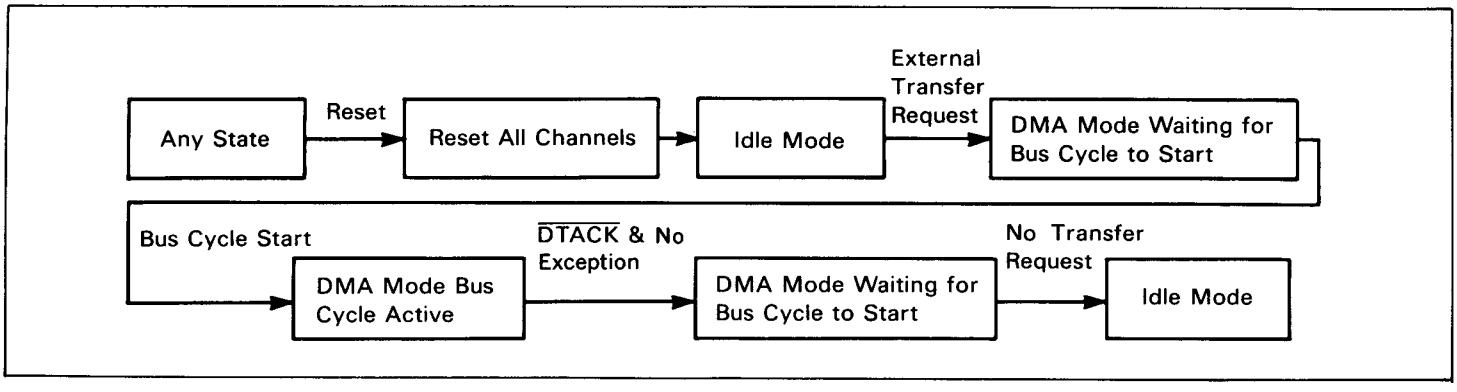


Figure 45 Flow of Normal Operation Without Exception or Error Condition

■CHANNEL PRIORITIES

Each channel has a priority level, which is determined by the contents of the Channel Priority Register (CPR). The priority of a channel is set by writing one of values $(00)_2$ through $(11)_2$, to CPR, $(00)_2$ being the highest priority level. When multiple requests are pending at the DMAC, the channel with the highest priority receives first service. The priority of a channel is independent of the device protocol or the request mechanism for that channel. If there are several requesting channels at the same priority level, a round-robin resolution is used, that is the DMAC does operand transfers in rotation starting form the channel of the lowest address.

Resetting the DMAC sets the priority level of all channels to "$(00)_2$", the highest priority level.

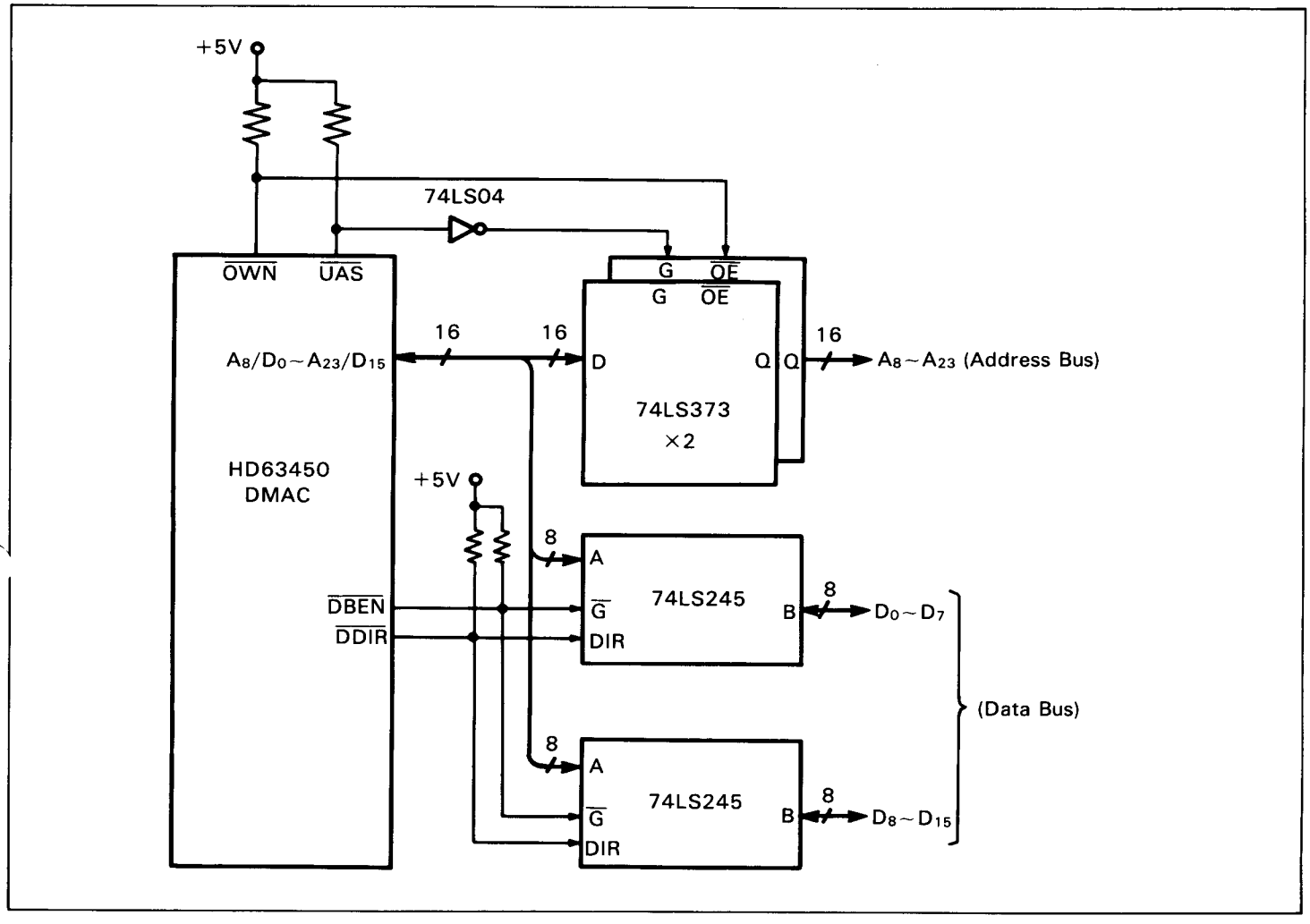


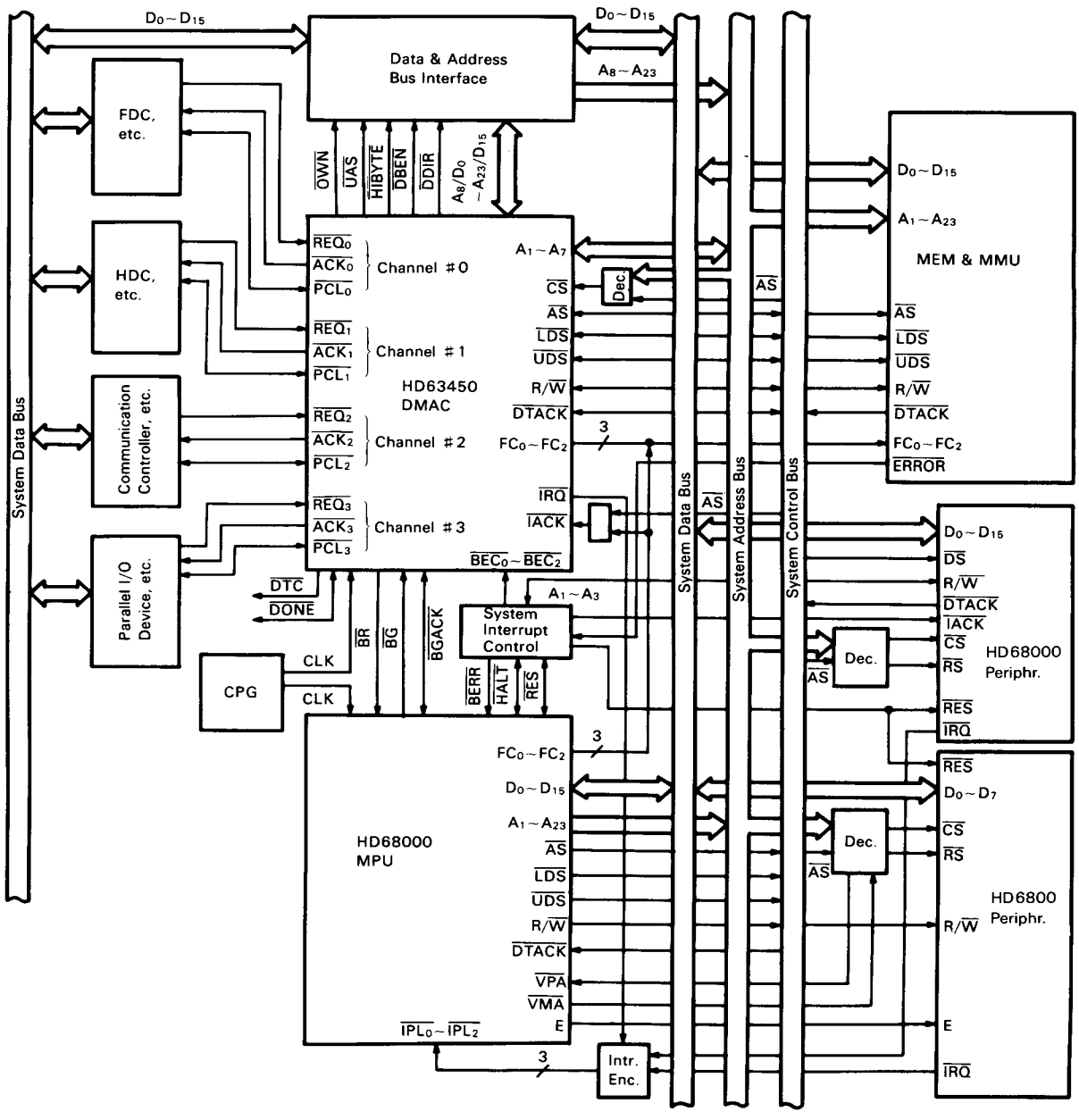
Figure 46 An Example of the Demultiplexed Address Data Bus

■ APPLICATIONS

Examples of how to interface HD63450 to an HD68000 based system are shown in Figures 46 and 47.

Figure 46 shows an example of how to demultiplex the address/data bus. $\overline{OWN}$ and $\overline{UAS}$ are used to control 74LS373 for latching the address. $\overline{DBEN}$ and $\overline{DDIR}$ are used to control the bi-directional buffer 74LS245. These signals are three-stated at active low, which requires pull-up resistors.

Figure 47 shows an example of inter-device connection in the HD68000 system. $\overline{REQ}$, $\overline{ACK}$, $\overline{PCL}$, $\overline{DTC}$, and $\overline{DONE}$ are used to control I/O devices.



The address bus and the system control bus in each device are omitted in this Figure

Figure 47 An Example of Inter-Device Connection in the HD68000 System

■ NOTES FOR USING HD63450

(1) I/O device connection in HD6800 mode.

When the DMAC is reading data from the HD6800 type peripheral device, the data is to be latched not at the falling edge of E clock but at that of CLK of $\overline{DTC}$ assertion. As shown in the figure below, the 74LS373 is externally required to keep this data on the bus of the DMAC.

(2) External abort during the $\overline{DONE}$ input cycle

In case of I/O device-to-Memory transfer under the dual addressing mode, the $\overline{DONE}$ input occurs during the read cycle of I/O device-to-DMAC registers.

The external abort ($\overline{PCL}$ is configured as an external abort input.) will be ignored during the write cycle which subsequently starts after the DMAC enters the $\overline{DONE}$ input cycle.

In this case, the registers CSR and CER indicate the normal transfer termination informed by the $\overline{DONE}$ input. When PCT = "1", ERR = "0", and NDT = "1" are set in CSR, an external abort has occurred.

(3) Multiple errors in one channel

In case of the sequential multiple errors in one channel, the DMAC indicates only the first one. The error code once set in CER is reserved until the ERR bit is reset.

(4) Attention for mounting the DMAC

The thick wiring is recommended to be used to connect the V_{SS} pin of the DMAC to the ground of the circuit board.

When using a socket, note that the V_{SS} pin should make a good contact with the socket.

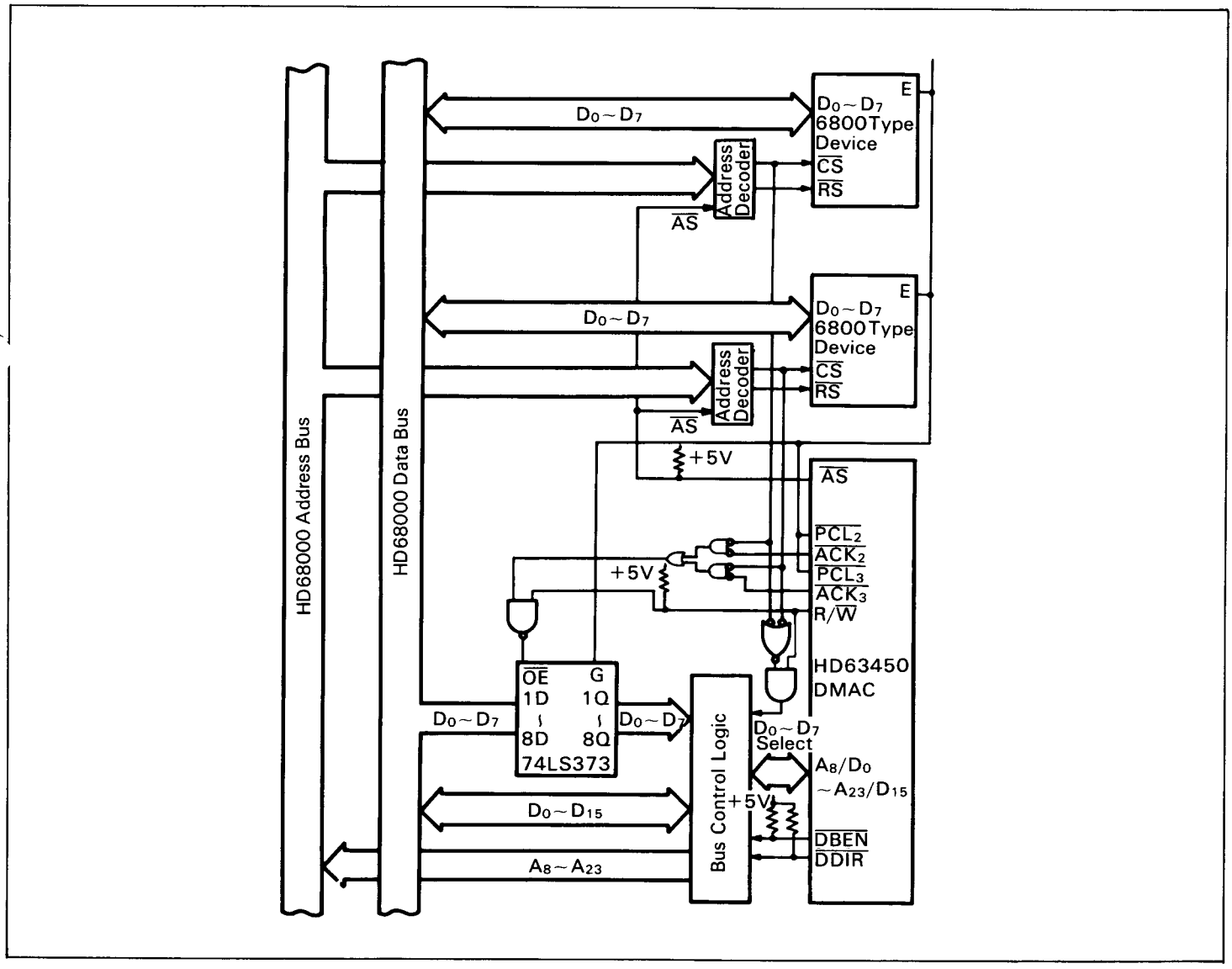
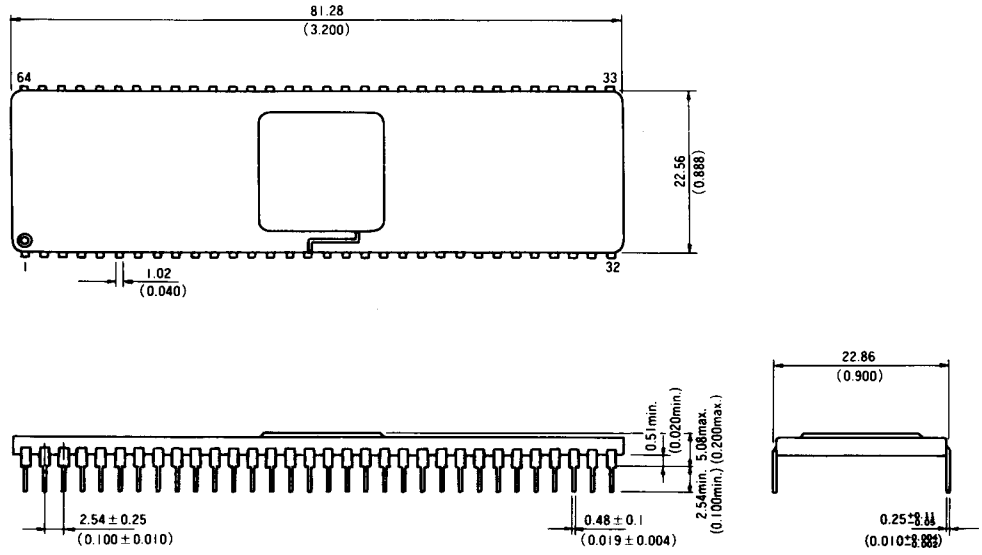


Figure 48 An Example of Connection with HD6800 type Peripheral Devices (channel 2 and 3 are used)

■ PACKGE DIMENSIONS (Unit : mm (inch))

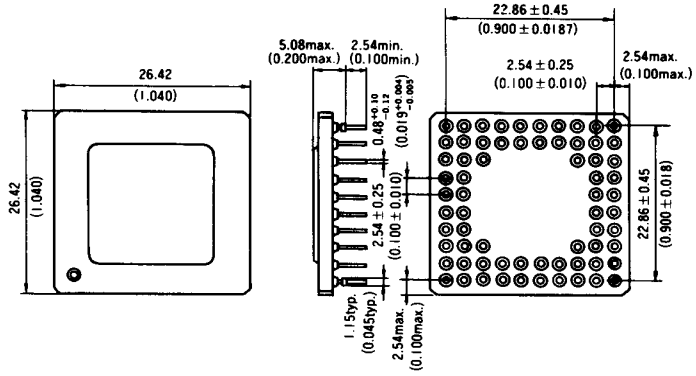
scale: 1/1

● DC-64



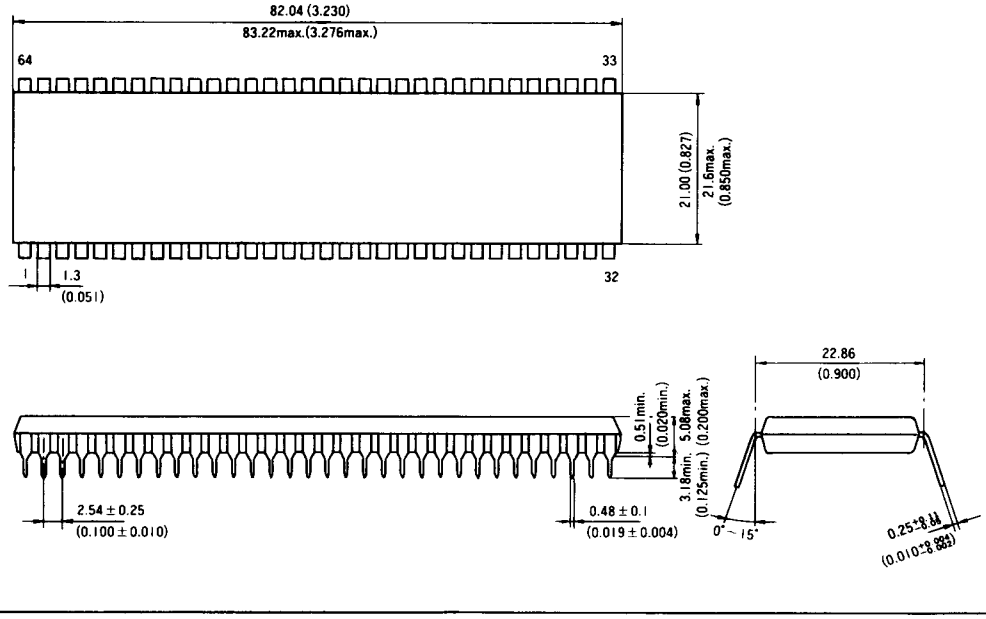
scale: 1/1

● PGA-68



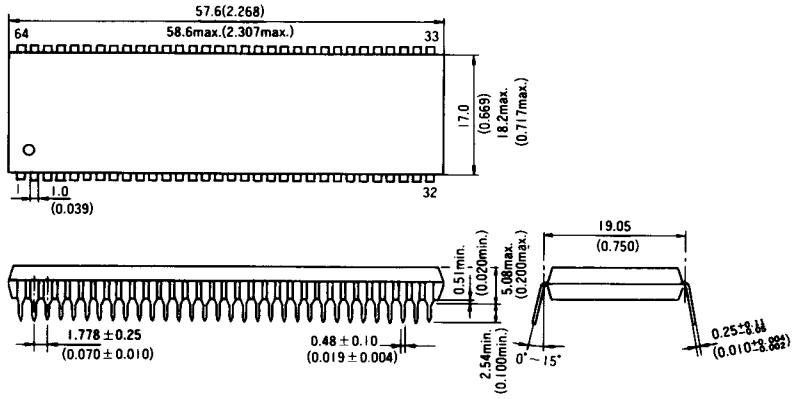
scale: 1/1

● DP-64



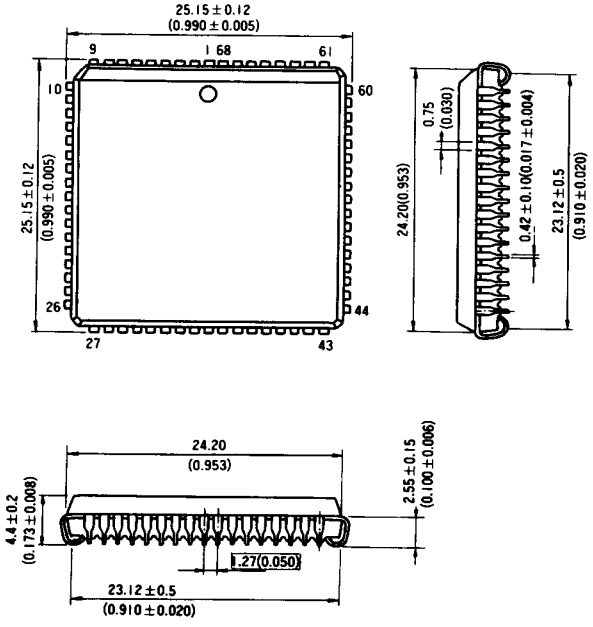
scale: 1/1

● **DP-64S**



scale: 3/2

● **PLCC-68**



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