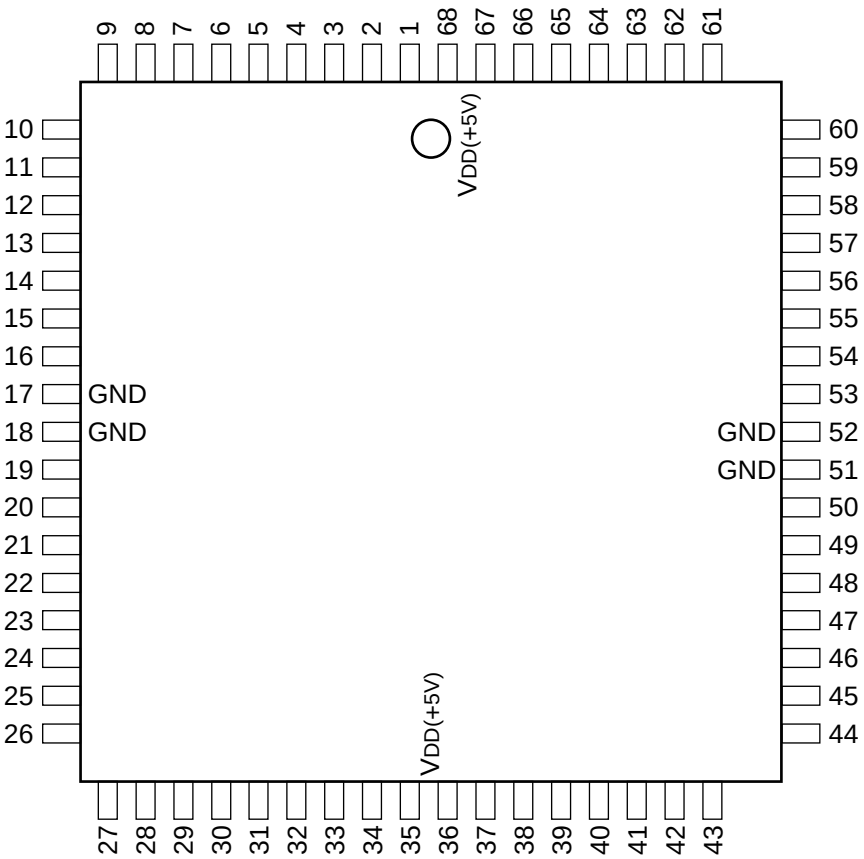
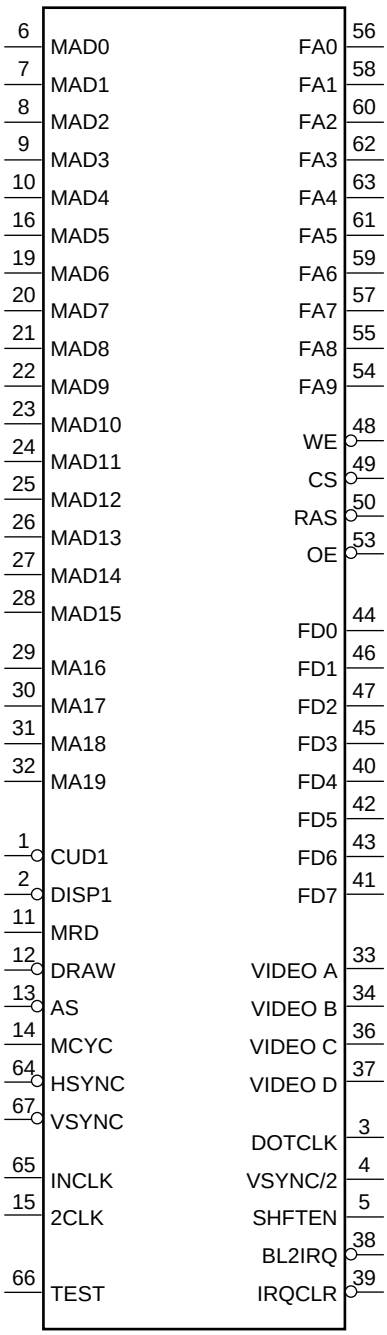
C-MOS MEMORY INTERFACE AND VIDEO ATTRIBUTE CONTROLLER

—TOP VIEW—



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	CUD1	18	—	GND	35	—	VDD V	52	—	GND
2	I	DISP1	19	I/O	MAD6	36	O	VIDEO C	53	O	OE
3	O	DOTCLK	20	I/O	MAD7	37	O	VIDEO D	54	O	FA9
4	O	VSYNC/2	21	I/O	MAD8	38	O	BL2IRQ	55	O	FA8
5	O	SHFTEN	22	I/O	MAD9	39	I	IRQCLR	56	O	FA0
6	I/O	MAD0	23	I/O	MAD10	40	I/O	FD4	57	O	FA7
7	I/O	MAD1	24	I/O	MAD11	41	I/O	FD7	58	O	FA1
8	I/O	MAD2	25	I/O	MAD12	42	I/O	FD5	59	O	FA6
9	I/O	MAD3	26	I/O	MAD13	43	I/O	FD6	60	O	FA2
10	I/O	MAD4	27	I/O	MAD14	44	I/O	FD0	61	O	FA5
11	I	MRD	28	I/O	MAD15	45	I/O	FD3	62	O	FA3
12	I	DRAW	29	I	MA16	46	I/O	FD1	63	O	FA4
13	I	AS	30	I	MA17	47	I/O	FD2	64	I	HSYNC
14	I	MCYC	31	I	MA18	48	O	WE	65	I	INCLK
15	O	2CLK	32	I	MA19	49	O	CS	66	I	TEST
16	I/O	MAD5	33	O	VIDEO A	50	O	RAS	67	I	VSYNC
17	—	GND	34	O	VIDEO B	51	—	GND	68	—	VDD



INPUT

AS	;	ADDRESS STROBE
CUD1	;	CURSOR DISPLAY
DISP1	;	DISPLAY TIMING
DRAW	;	DRAW
HSYNC	;	HORIZONTAL SYNC
INCLK	;	MASTER CLOCK
IRQCLR	;	BL2IRQ CLEAR
MA16 - MA19	;	MEMORY ADDRESS
MCYC	;	MEMORY CYCLE
MRD	;	MEMORY READ
TEST	;	TEST
VSYNC	;	VERTICAL SYNC

OUTPUT

2CLK	;	2 CLOCK
BL2IRQ	;	SETTED MA19
CS	;	CHIP SELECT
DOTCLK	;	DOT CLOCK
FA0 - FA9	;	FRAME BUFFER ADDRESS
OE	;	OUTPUT ENABLE
RAS	;	RAS TIMING FOR DRAM
SHFTEN	;	VIDEO SIGNAL OUTPUT ENABLE
VIDEO A - VIDEO D	;	VIDEO SIGNAL
VSYNC/2	;	HALF-VSYNC
WE	;	WRITE ENABLE

INPUT/OUTPUT

FD0 - FD7	;	FRAME BUFFER DATA
MAD0 - MAD15	;	MEMORY ADDRESS/DATA