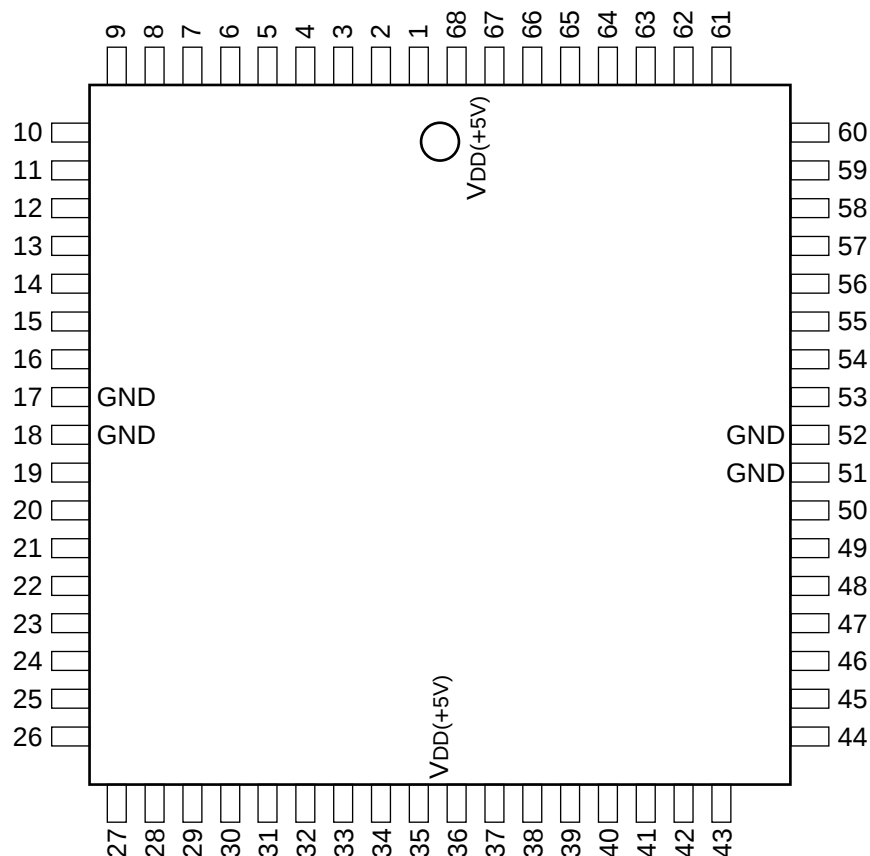

C-MOS MEMORY INTERFACE AND VIDEO ATTRIBUTE CONTROLLER

—TOP VIEW—



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	CUD1	18	—	GND	35	—	VDD V	52	—	GND
2	I	DISP1	19	I/O	MAD6	36	O	VIDEO C	53	O	OE
3	O	DOTCLK	20	I/O	MAD7	37	O	VIDEO D	54	O	FA9
4	O	VSYSNC/2	21	I/O	MAD8	38	O	BL2IRQ	55	O	FA8
5	O	SHFTEN	22	I/O	MAD9	39	I	IRQCLR	56	O	FA0
6	I/O	MAD0	23	I/O	MAD10	40	I/O	FD4	57	O	FA7
7	I/O	MAD1	24	I/O	MAD11	41	I/O	FD7	58	O	FA1
8	I/O	MAD2	25	I/O	MAD12	42	I/O	FD5	59	O	FA6
9	I/O	MAD3	26	I/O	MAD13	43	I/O	FD6	60	O	FA2
10	I/O	MAD4	27	I/O	MAD14	44	I/O	FD0	61	O	FA5
11	I	MRD	28	I/O	MAD15	45	I/O	FD3	62	O	FA3
12	I	DRAW	29	I	MA16	46	I/O	FD1	63	O	FA4
13	I	AS	30	I	MA17	47	I/O	FD2	64	I	HSYNC
14	I	MCYC	31	I	MA18	48	O	WE	65	I	INCLK
15	O	2CLK	32	I	MA19	49	O	CS	66	I	TEST
16	I/O	MAD5	33	O	VIDEO A	50	O	RAS	67	I	VSYSNC
17	—	GND	34	O	VIDEO B	51	—	GND	68	—	VDD

6	MAD0	FA0	56	INPUT	
7	MAD1	FA1	58	AS	; ADDRESS STROBE
8	MAD2	FA2	60	CUD1	; CURSOR DISPLAY
9	MAD3	FA3	62	DISP1	; DISPLAY TIMING
10	MAD4	FA4	63	DRAW	; DRAW
16	MAD5	FA5	61	HSYNC	; HORIZONTAL SYNC
19	MAD6	FA6	59	INCLK	; MASTER CLOCK
20	MAD7	FA7	57	IRQCLR	; BL2IRQ CLEAR
21	MAD8	FA8	55	MA16 - MA19	; MEMORY ADDRESS
22	MAD9	FA9	54	MCYC	; MEMORY CYCLE
23	MAD10			MRD	; MEMORY READ
24	MAD11	WE	48	TEST	; TEST
25	MAD12	CS	49	VSYNC	; VERTICAL SYNC
26	MAD13	RAS	50		
27	MAD14	OE	53	OUTPUT	
28	MAD15			2CLK	; 2 CLOCK
29	MA16	FD0	44	BL2IRQ	; SETTED MA19
30	MA17	FD1	46	CS	; CHIP SELECT
31	MA18	FD2	47	DOTCLK	; DOT CLOCK
32	MA19	FD3	45	FA0 - FA9	; FRAME BUFFER ADDRESS
		FD4	40	OE	; OUTPUT ENABLE
		FD5	42	RAS	; RAS TIMING FOR DRAM
1	CUD1	FD6	43	SHFTEN	; VIDEO SIGNAL OUTPUT ENABLE
2	DISP1	FD7	41	VIDEO A - VIDEO D	; VIDEO SIGNAL
11	MRD			VSYNC/2	; HALF-VSYNC
12	DRAW	VIDEO A	33	WE	; WRITE ENABLE
13	AS	VIDEO B	34		
14	MCYC	VIDEO C	36	INPUT/OUTPUT	
64	HSYNC	VIDEO D	37	FD0 - FD7	; FRAME BUFFER DATA
67	VSYNC			MAD0 - MAD15	; MEMORY ADDRESS/DATA
		DOTCLK	3		
65	INCLK	VSYNC/2	4		
15	2CLK	SHFTEN	5		
		BL2IRQ	38		
66	TEST	IRQCLR	39		

