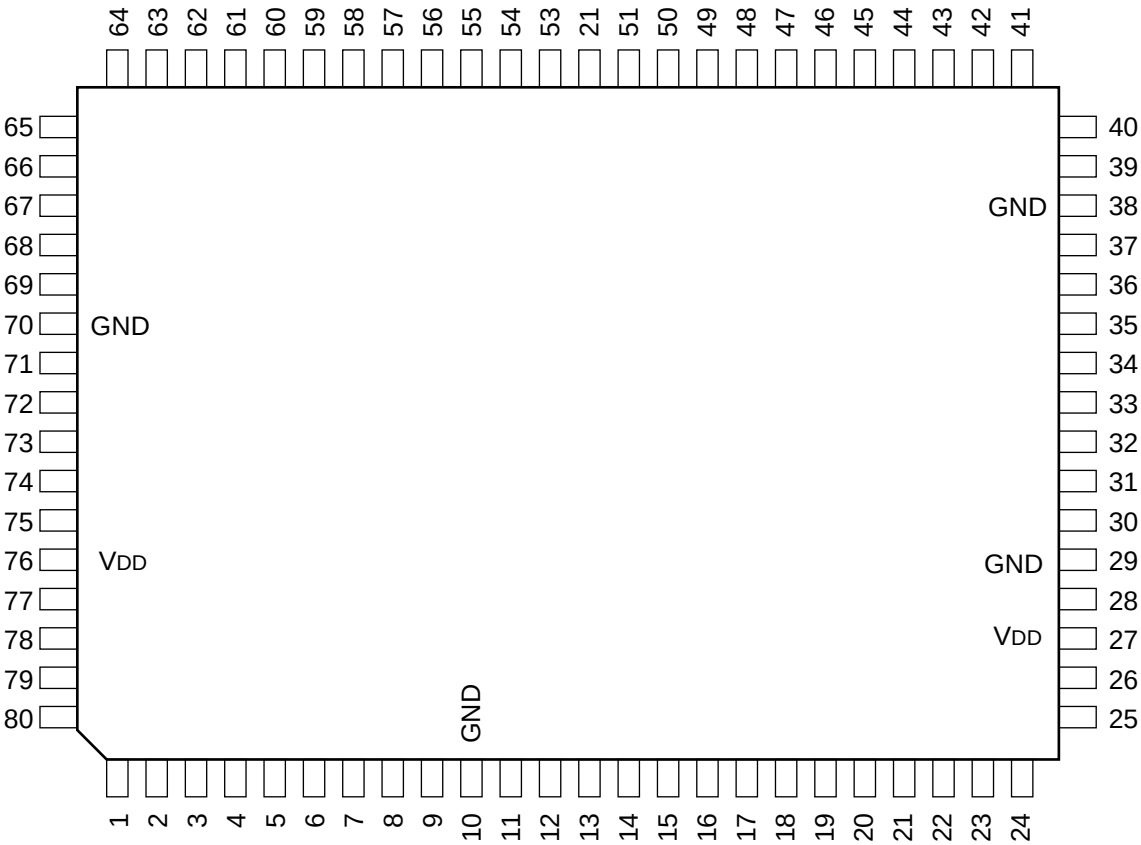
C-MOS 8-BIT MICRO PROCESSING UNIT

—TOP VIEW—



MODE 0 : HD643180X, HD647180X
MODE 1 : HD641180XF6, HD643180X, HD647180X, HD641180X-8L-FP80B
MODE 2 : HD643180X, HD647180X
PROM MODE : HD647180X

PIN No.	MODE 0		MODE 1		MODE 2		PROM MODE	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	I	$\overline{\text{NMI}}$	I	$\overline{\text{NMI}}$	I	$\overline{\text{NMI}}$	O	A9
2	I	$\overline{\text{INT0}}$	I	$\overline{\text{INT0}}$	I	$\overline{\text{INT0}}$	—	NC
3	I	$\overline{\text{INT1}}$	I	$\overline{\text{INT1}}$	I	$\overline{\text{INT1}}$	—	NC
4	I	$\overline{\text{INT2}}$	I	$\overline{\text{INT2}}$	I	$\overline{\text{INT2}}$	—	NC
5	I/O	PE4	O	ST	O	ST	—	NC
6	I/O	PC0	O	A0	O	A0	O	A0
7	I/O	PC1	O	A1	O	A1	O	A1
8	I/O	PC2	O	A2	O	A2	O	A2
9	I/O	PC3	O	A3	O	A3	O	A3
10	—	GND	—	GND	—	GND	—	GND
11	I/O	PC4	O	A4	O	A4	O	A4
12	I/O	PC5	O	A5	O	A5	O	A5
13	I/O	PC6	O	A6	O	A6	O	A6
14	I/O	PC7	O	A7	O	A7	O	A7
15	I/O	PD0	O	A8	I/O	A8/PD0	O	A8
16	I/O	PD1	O	A9	I/O	A9/PD1	—	NC
17	I/O	PD2	O	A10	I/O	A10/PD2	O	A10
18	I/O	PD3	O	A11	I/O	A11/PD3	O	A11
19	I/O	PD4	O	A12	I/O	A12/PD4	O	A12
20	I/O	PD5	O	A13	I/O	A13/PD5	O	A13
21	I/O	PD6	O	A14	I/O	A14/PD6	O	A14
22	I/O	PD7	O	A15	I/O	A15/PD7	I	OE
23	I/O	PE0	O	A16	I/O	A16/PE0	I	CE
24	I/O	PE1	O	A17	I/O	A17/PE1	—	NC
25	O	PE2	O	A18	I/O	A18/PE2	—	NC
26	—	TOUT1	O	TOUT1	O	TOUT1	—	NC
27	I/O	V_{DD}	—	V_{DD}	—	V_{DD}	—	V_{DD}
28		PE3	O	A19	I/O	A19/PE3	—	NC
29	—	GND	—	GND	—	GND	—	GND
30	I/O	PF0	I/O	D0	I/O	D0	O	O0
31	I/O	PF1	I/O	D1	I/O	D1	O	O1
32	I/O	PF2	I/O	D2	I/O	D2	O	O2
33	I/O	PF3	I/O	D3	I/O	D3	O	O3
34	I/O	PF4	I/O	D4	I/O	D4	O	O4
35	I/O	PF5	I/O	D5	I/O	D5	O	O5
36	I/O	PF6	I/O	D6	I/O	D6	O	O6
37	I/O	PF7	I/O	D7	I/O	D7	O	O7
38	—	GND	—	GND	—	GND	—	GND
39	I	PG0/AN0	I	PG0/AN0	I	PG0/AN0	—	NC
40	I	PG1/AN1	I	PG1/AN1	I	PG1/AN1	—	NC

PIN No.	MODE 0		MODE 1		MODE 2		PROM MODE	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
41	I	PG2/AN2	I	PG2/AN2	I	PG2/AN2	—	NC
42	I	PG3/AN3	I	PG3/AN3	I	PG3/AN3	—	NC
43	I	PG4/AN4	I	PG4/AN4	I	PG4/AN4	—	NC
44	I	PG5/AN5	I	PG5/AN5	I	PG5/AN5	—	NC
45	O	$\overline{\text{RTS0}}$	O	$\overline{\text{RTS0}}$	O	$\overline{\text{RTS0}}$	—	NC
46	I	$\overline{\text{CTS0}}$	I	$\overline{\text{CTS0}}$	I	$\overline{\text{CTS0}}$	—	NC
47	I	$\overline{\text{DCD0}}$	I	$\overline{\text{DCD0}}$	I	$\overline{\text{DCD0}}$	—	NC
48	O	TXA0	O	TXA0	O	TXA0	—	NC
49	I	RXA0	I	RXA0	I	RXA0	—	NC
50	I/O	CKA0/$\overline{\text{DREQ0}}$	I/O	CKA0/$\overline{\text{DREQ0}}$	I/O	CKA0/$\overline{\text{DREQ0}}$	—	NC
51	O	TOUT2	O	TOUT2	O	TOUT2	—	NC
52	O	TOUT3	O	TOUT3	O	TOUT3	—	NC
53	I	IC	I	IC	I	IC	—	NC
54	I/O	TXA1/PA0	I/O	TXA1/PA0	I/O	TXA1/PA0	—	NC
55	I/O	RXA1/PA1	I/O	RXA1/PA1	I/O	RXA1/PA1	—	NC
56	I/O	CKA1/$\overline{\text{TEND0}}$/PA2	I/O	CKA1/$\overline{\text{TEND0}}$/PA2	I/O	CKA1/$\overline{\text{TEND0}}$/PA2	—	NC
57	I/O	TXS/PA3	I/O	TXS/PA3	I/O	TXS/PA3	—	NC
58	I/O	RXS/$\overline{\text{CTS1}}$/PA4	I/O	RXS/$\overline{\text{CTS1}}$/PA4	I/O	RXS/$\overline{\text{CTS1}}$/PA4	—	NC
59	I/O	CKS/PA5	I/O	CKS/PA5	I/O	CKS/PA5	—	NC
60	I/O	$\overline{\text{DREQ1}}$/PA6	I/O	$\overline{\text{DREQ1}}$/PA6	I/O	$\overline{\text{DREQ1}}$/PA6	—	NC
61	I/O	$\overline{\text{TEND1}}$/PA7	I/O	$\overline{\text{TEND1}}$/PA7	I/O	$\overline{\text{TEND1}}$/PA7	—	NC
62	I/O	PB7	O	$\overline{\text{HALT}}$	O	$\overline{\text{HALT}}$	—	NC
63	I/O	PB6	O	$\overline{\text{REF}}$	O	$\overline{\text{REF}}$	—	NC
64	I/O	PB5	O	$\overline{\text{IOE}}$	O	$\overline{\text{IOE}}$	—	NC
65	I/O	PB4	O	$\overline{\text{ME}}$	O	$\overline{\text{ME}}$	—	NC
66	I/O	PB3	O	E	O	E	—	NC
67	I/O	PB2	O	$\overline{\text{LIR}}$	O	$\overline{\text{LIR}}$	—	NC
68	I/O	PB1	O	$\overline{\text{WR}}$	O	$\overline{\text{WR}}$	—	NC
69	I/O	PB0	O	$\overline{\text{RD}}$	O	$\overline{\text{RD}}$	—	NC
70	—	GND	—	GND	—	GND	—	GND
71	O	ø	O	ø	O	ø	—	NC
72	I	MP1	I	MP1	I	MP1	I	MP1
73	I	MP0	I	MP0	I	MP0	I	MP0
74	I	XTAL	I	XTAL	I	XTAL	I	XTAL
75	I	EXTAL	I	EXTAL	I	EXTAL	I	EXTAL
76	—	V_{DD}	—	V_{DD}	—	V_{DD}	—	V_{DD}
77	I/O	PE7	I	$\overline{\text{WAIT}}$	I	$\overline{\text{WAIT}}$	—	NC
78	I/O	PE6	O	$\overline{\text{BUSACK}}$	O	$\overline{\text{BUSACK}}$	—	NC
79	I/O	PE5	I	$\overline{\text{BUSREQ}}$	I	$\overline{\text{BUSREQ}}$	—	NC
80	I	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$	—	VPP

INPUT

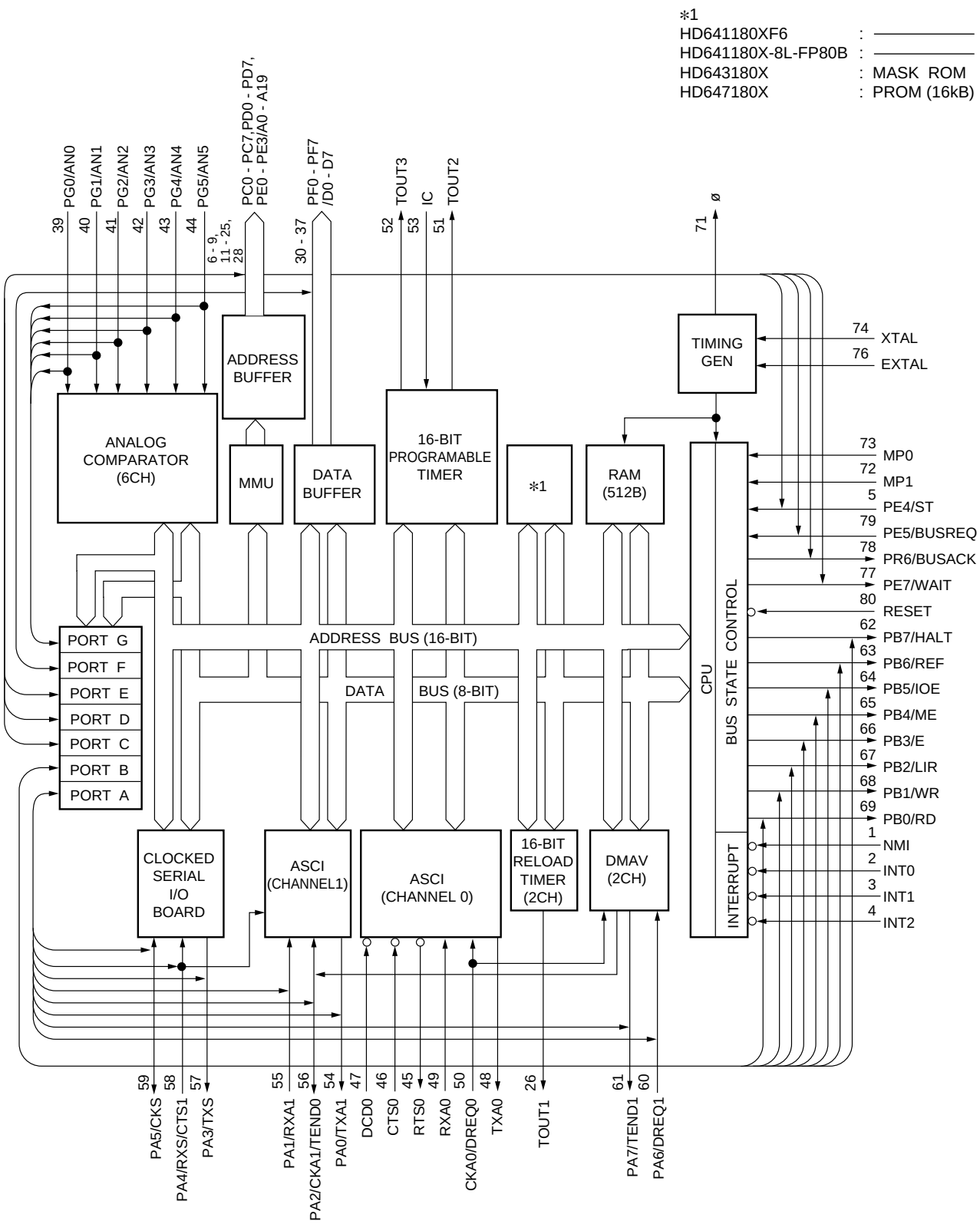
AN0 - AN5 : ANALOG INPUT
$\overline{\text{BUSREQ}}$: BUS REQUEST
$\overline{\text{CTS0}}$, $\overline{\text{CTS1}}$: CLEAR TO SEND GOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
$\overline{\text{DCD0}}$, $\overline{\text{DCD1}}$: DATA VARRIER DETECT FOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$: DMA REQUEST FOR CHANNEL n (n = 0 OR 1)
EXTAL : EXTERNAL CLOCK
IC : INPUT CAPTURE
$\overline{\text{INT0}}$ - $\overline{\text{INT2}}$: INTERRUPT
MP0, MP1 : MOD PROGRAM
$\overline{\text{NMI}}$: NON-MASKABLE INTERRUPT
$\overline{\text{RESET}}$: RESET
PG0 - PG5 : 6-BIT INPUT OF PORT G
RXA0, RXA1 : RECEIVE DATA FOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
RXS : RECIEVE DATA FOR SERIAL I/O PORT
XTAL : CLOCK

OUTPUT

A0 - A19 : ADDRESS BUS
BUSACK : BUS ACKNOULEDGE
E : ENABLE
$\overline{\text{IOE}}$: I/O ENABLE
$\overline{\text{LIR}}$: LOAD INSTRUCTION REGISTER
$\overline{\text{ME}}$: MEMORY ENABLE
$\overline{\text{RD}}$: READ
$\overline{\text{REF}}$: REFRESH
$\overline{\text{RTS0}}$, $\overline{\text{RTS1}}$: REQUEST TO SEND FOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
ST : STATUS
$\overline{\text{TEND0}}$, $\overline{\text{TEND1}}$: TRANFER END FOR CHANNEL n (n = 0 OR 1)
TOUT1 - TOUT3 : TIMER OUT
TXA0, TXA1 : TRANSFER DATA FOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
TXS : TRANSFER DATA FOR SERIAL I/O PORT
$\overline{\text{WR}}$: WRITE
Ø : SYSTEM CLOCK

INPUT/OUTPUT

CKA0, CKA1 : CLOCK FOR ASYNCHRONOUS SCI CHANNEL n (n = 0 OR 1)
CKS : CLOCK FOR SERIAL I/O PORT
D0 - D7 : DATA BUS
PA0 - PA7 : 8-BIT INPUT/OUTPUT OF PORT A
PB0 - PB7 : 8-BIT INPUT/OUTPUT OF PORT B
PC0 - PC7 : 8-BIT INPUT/OUTPUT OF PORT C
PD0 - PD7 : 8-BIT INPUT/OUTPUT OF PORT D
PE0 - PE7 : 8-BIT INPUT/OUTPUT OF PORT E
PF0 - PF7 : 8-BIT INPUT/OUTPUT OF PORT F


*1
HD641180XF6 : ————
HD641180X-8L-FP80B : ————
HD643180X : MASK ROM
HD647180X : PROM (16kB)
PG0/AN0
PG1/AN1
PG2/AN2
PG3/AN3
PG4/AN4
PG5/AN5
PC0 - PC7,PD0 - PD7,
PE0 - PE3/A0 - A19
PF0 - PF7
/D0 - D7
TOUT3
IC
TOUT2
ø
ADDRESS BUFFER
TIMING GEN
XTAL
EXTAL
ANALOG COMPARATOR (6CH)
MMU
DATA BUFFER
16-BIT PROGRAMABLE TIMER
*1
RAM (512B)
MP0
MP1
PE4/ST
PE5/BUSREQ
PR6/BUSACK
PE7/WAIT
RESET
PB7/HALT
PB6/REF
PB5/IOE
PB4/ME
PB3/E
PB2/LIR
PB1/WR
PB0/RD
PORT G
PORT F
PORT E
PORT D
PORT C
PORT B
PORT A
ADDRESS BUS (16-BIT)
DATA BUS (8-BIT)
CPU
BUS STATE CONTROL
INTERRUPT
NMI
INT0
INT1
INT2
CLOCKED SERIAL I/O BOARD
ASCI (CHANNEL1)
ASCI (CHANNEL 0)
16-BIT RELOAD TIMER (2CH)
DMAV (2CH)
PA5/CKS
PA4/RXS/CTS1
PA3/TXS
PA1/RXA1
PA2/CKA1/TEND0
PA0/TXA1
DCD0
CTS0
RTS0
RXA0
CKA0/DREQ0
TXA0
TOUT1
PA7/TEND1
PA6/DREQ1