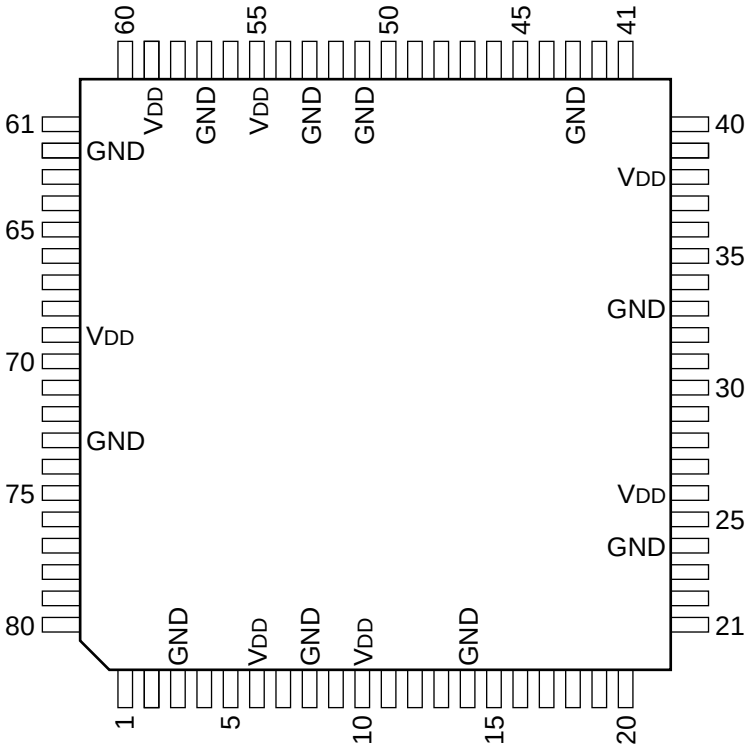
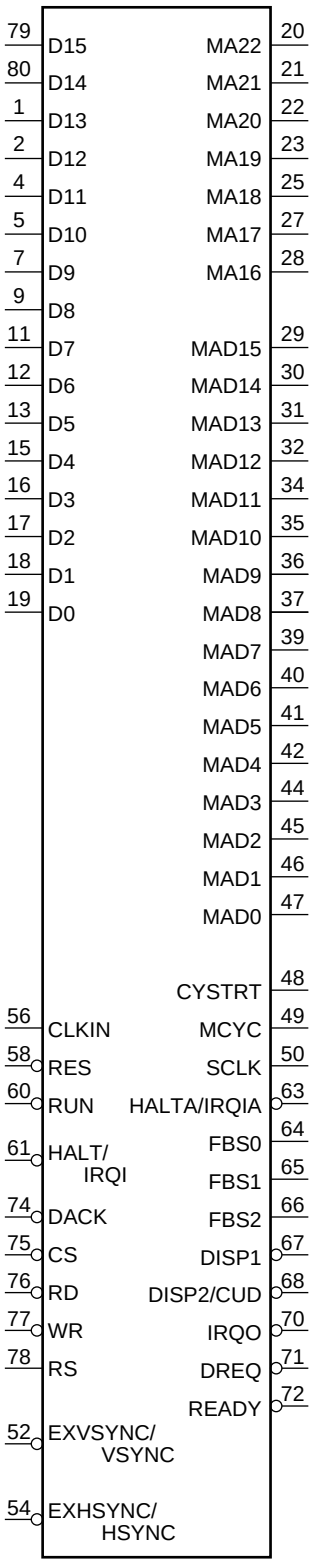
C-MOS 16-BIT GRAPHIC PROCESSOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	D13	17	I/O	D2	33	—	GND	49	O	MCYC	65	O	FBS1
2	I/O	D12	18	I/O	D1	34	I/O	MAD11	50	O	SCLK	66	O	FBS2
3	—	GND	19	I/O	D0	35	I/O	MAD10	51	—	GND	67	O	$\overline{\text{DISP1}}$
4	I/O	D11	20	O	MA22	36	I/O	MAD9	52	I/O	$\overline{\text{EXVSYNC}}$/$\overline{\text{VSYNC}}$	68	O	$\overline{\text{DISP2}}$/$\overline{\text{CUD}}$
5	I/O	D10	21	O	MA21	37	I/O	MAD8	53	—	GND	69	—	VDD
6	—	VDD	22	O	MA20	38	—	VDD	54	I/O	$\overline{\text{EXHSYNC}}$/$\overline{\text{HSYNC}}$	70	O	$\overline{\text{IRQO}}$
7	I/O	D9	23	O	MA19	39	I/O	MAD7	55	—	VDD	71	O	$\overline{\text{DREQ}}$
8	—	GND	24	—	GND	40	I/O	MAD6	56	I	CLKIN	72	O	$\overline{\text{READY}}$
9	I/O	D8	25	O	MA18	41	I/O	MAD5	57	—	GND	73	—	GND
10	—	VDD	26	—	VDD	42	I/O	MAD4	58	I	$\overline{\text{RES}}$	74	I	$\overline{\text{DACK}}$
11	I/O	D7	27	O	MA17	43	—	GND	59	—	VDD	75	I	$\overline{\text{CS}}$
12	I/O	D6	28	O	MA16	44	I/O	MAD3	60	I	$\overline{\text{RUN}}$	76	I	$\overline{\text{RD}}$
13	I/O	D5	29	I/O	MAD15	45	I/O	MAD2	61	I	$\overline{\text{HALT}}$/$\overline{\text{IRQI}}$	77	I	$\overline{\text{WR}}$
14	—	GND	30	I/O	MAD14	46	I/O	MAD1	62	—	GND	78	I	RS
15	I/O	D4	31	I/O	MAD13	47	I/O	MAD0	63	O	$\overline{\text{HALTA}}$/$\overline{\text{IRQIA}}$	79	I/O	D15
16	I/O	D3	32	I/O	MAD12	48	O	CYSTRT	64	O	FBS0	80	I/O	D14



INPUT

CLKIN	;	CLOCK
$\overline{CS}$	;	CHIP SELECT
$\overline{DACK}$	;	DMA TRANSLATE REQUEST ACKNOWLEDGE
$\overline{EXHSYNC}$	;	EXTERNAL HORIZONTAL SYNC
$\overline{EXVSYNC}$	;	EXTERNAL VERTICAL SYNC
$\overline{HALT}$	;	HALT
$\overline{IRQI}$	;	INTERRUPT REQUEST
$\overline{RD}$	;	READ
$\overline{RES}$	;	RESET
RS	;	REGISTER SELECT
$\overline{RUN}$	;	RUN
$\overline{WR}$	;	WRITE

OUTPUT

$\overline{CUD}$	;	CURSOR DISPLAY TIMING
CYSTRT	;	CYCLE START
$\overline{DISP1}$, $\overline{DISP2}$	;	DISPLAY TIMING
$\overline{DREQ}$	;	DMA TRANSLATE REQUEST
FBS0-FBS2	;	FRAME BUFFER STATUS
$\overline{HALTA}$	;	HALT ACKNOWLEDGE
$\overline{HSYNC}$	;	HORIZONTAL SYNC
$\overline{IRQIA}$	;	INTERRUPT REQUEST INPUT ACKNOWLEDGE
$\overline{IRQO}$	;	INTERRUPT REQUEST
MA16 - MA22	;	FRAME BUFFER ADDRESS BUS
MCYC	;	MEMORY CYCLE
$\overline{READY}$	;	READY
SCLK	;	S CLOCK
$\overline{VSYNC}$	;	VERTICAL SYNC

INPUT/OUTPUT

D0 - D15	;	DATA BUS
MAD0 - MAD15	;	FRAME BUFFER ADDRESS/DATA BUS