HD64460

CRT Controller Plus (CRTC+)

The CRTC+ is a single-chip CRT controller implementing graphic and character display functions which correspond to the VGA (Video Graphics Adapter™) for IBM personal computers.

Since the CRTC+ combines a video signal generator using a color palette, the graphics functions of the IBM-VGA, and control functions for a dynamic RAM frame buffer into a single chip, it provides the total system control required to implement graphic and character display with one chip.

In addition, the CPU can access the frame buffer up to four times faster with the CRTC+ than with the IBM-VGA. Graphics can therefore be created faster and CPU wait time is reduced.

In addition to the VGA features, the CRTC+ includes additional extended features, and it also has enhanced 6845 modes which correspond to the IBM-CGA (Color Graphics Adapter™), IBM-MDA (Monochrome Display Adapter™), or HGA (Hercules Graphics Adapter™).
These features enable the design of a multi-function personal computer graphic system using one CRTC+ chip.

In addition to the VGA functions, the CRTC+ supports many extended functions, including 132-column text display, frame buffer bank switching, additional text fonts, monochrome reverse video, and non-wait display/CPU access (smart access) for more efficient graphics drawing. These extended functions greatly simplify support for future products.

Notes:
1. IBM-PC, IBM-PS/2, VGA, CGA, and MDA are registered trademarks of International Business Machines Corporation.
2. Hercules Graphics is a registered trademark of Hercules Computer Technologies Corporation.

Features

Compatibility

- Hardware- and software-compatible with the IBM-VGA board
- Software-compatible with the IBM-MDA, IBM-CGA, and HGA modes*
- Compatible with IBM-EGA at the BIOS level**

* Functions provided by the CRTC+ but not by the VGA.
** EGA software can be used via BIOS (Basic Input Output System) software.

Display Control Functions

- Both bit-mapped graphics and code refresh supported
- Variety of resolutions supported:
  640 × 480 (VGA), 640 × 200 and 320 × 200 (CGA), 720 × 350 (MDA), 720 × 348 (HGA), 640 × 350 (EGA), and 800 × 600 (extended function)
- Dot clock speeds of up to 37 MHz (132-column text display mode)
- 2-partition screen splitting
- Programmable underlining, programmable cursor display (underline and cursor control by hardware)
- Flashless vertical smooth scroll, flashless horizontal panning scroll
- Interrupt generated at the start of the vertical retrace period

Ordering Information

Type	Clock Frequency [MHz]	Package
HD64460F28	32.0	FP-136
HD64460F37	37.0	

Graphics Assist Functions

- Bit shift and color logic operations on graphics data in the frame buffer
- Programmable bit masking and memory plane masking
- Copying of graphics using byte-boundary data in the frame buffer
- Writing of a specified color in the frame buffer
- Color data comparison in the frame buffer

Frame Buffer Access

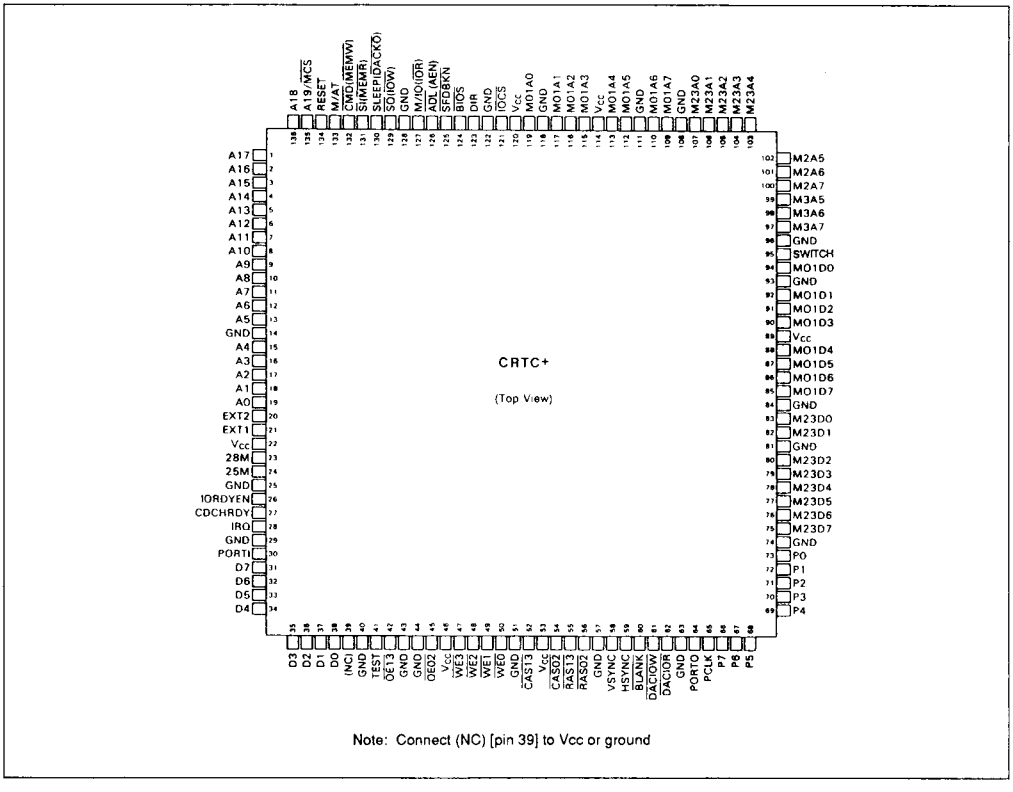
- Direct interface with a 256-kbyte memory using 64k × 4-type dynamic RAM chips (HM50464 or equivalent)
- Generation of dynamic RAM control signals ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)
- Generation of dynamic RAM refresh addresses
- Improved efficiency in CPU graphics drawing access through non-wait display/CPU access (smart access)

Other Features

- Switching to HD6845 (CRTC) compatible register configurations (MDA, CGA, and HGA modes)*
- 132-column text display (7 dots per character)* (available only in the HD64460F37 version.)
- Frame buffer bank switching*
- Additional text fonts*
- BIOS ROM bank switching*
- BIOS signal output masking*
- Three-state control of video pins*
- Monochrome reverse video (in MDA and HGA modes)*
- Port input*

* Functions provided by the CRTC+ but not by the VGA.

Pin Arrangement



Note: Connect (NC) [pin 39] to Vcc or ground

Pin Description

Power

Signal	Pin No.	Input/Output	Function
Vcc	22, 46, 53, 89, 114, 120	—	Power supply for the CRTC+: 5 V ±5%
Vss	14, 25, 29, 40, 43, 44, 51,57, 63, 74, 81, 84, 93, 96, 108, 111, 118, 122, 128	—	Ground for the CRTC+

Note: Connect all 25 Vcc and Vss power pins of the CRTC+ to the power supply or ground. Connect a bypass capacitor across Vcc and Vss as close to the pins as possible, as a noise killer.

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CPU Interface

Signal	Pin No.	Input/Output	Function
$A_{19}/\overline{MCS}$	135	I	$A_{19}/\overline{MCS}$ is used to input the A_{19} address signal or the $\overline{MCS}$ signal derived from a higher address decoder when the frame buffer is acessed. $A_{19}/\overline{MCS}$ is switched to A_{19} when bit 3 of extended register 2 is 0, and to $\overline{MCS}$ when bit 3 of extended register 2 is 1.
A_{18}-A_0	136,1-13, 15-19	I	A_{18}-A_0 are the address input signals from the system bus. Address information input to these pins is used to access the frame buffer, BIOS ROM, color palette, and internal registers.
D_7-D_0	31-38	I/O	D_7-D_0 are used to transfer data between the CPU system and the CRTC+. The frame buffer and CRTC+ registers can be accessed through these lines.
$\overline{IOCS}$	121	I	$\overline{IOCS}$ selects the I/O address mapping function of the CRTC+. If $\overline{IOCS}$ is high when reset input is negated, the A_{15}-A_0 lines are used for accessing the I/O address. If $\overline{IOCS}$ is low when reset is negated, $\overline{IOCS}$ functions as I/O chip select after the reset. In this case, I/O addresses can be mapped to the area specified by the $\overline{IOCS}$ in place of the A_{15}-A_8 lines.
DIR	123	O	DIR indicates the data transfer direction on the system bus. Data is transferred from the system bus to the CRTC+ when DIR is high, and is transferred from the CRTC+ to the system bus when DIR is low.
M/IO ($\overline{IOR}$)	127	I	M/IO switches between I/O access and frame buffer access in the micro channel bus mode. High indicates frame buffer access; low indicates I/O access. $\overline{IOR}$ controls reading of the CRTC+ registers (I/O read command) in the I/O channel bus mode.

Signal	Pin No.	Input/Output	Function
$\overline{S0}$ ($\overline{IOW}$)	129	I	$\overline{S0}$ indicates access status 0 when the micro channel bus mode is used: M/IO: 0 0 0 1 1 1 1 1 — $\overline{S0}$: 0 0 1 1 0 0 1 1 — $\overline{S1}$: 0 1 0 1 0 1 0 1 — Status: Reserved A; I/O write; I/O read; Reserved B; Reserved C; Memory write; Memory read; Reserved D 0: Low level 1: High level $\overline{IOW}$ controls writing to the CRTC+ registers in the I/O channel bus mode.
$\overline{S1}$ ($\overline{MEMR}$)	131	I	$\overline{S1}$ indicates access status 1 in the micro channel bus mode (see description of $\overline{S0}$). $\overline{MEMR}$ controls the reading of frame buffer data and BIOS ROM in the I/O channel bus mode.
$\overline{CMD}$ ($\overline{MEMW}$)	132	I	$\overline{CMD}$ indicates that valid data is present on the data bus (D_7-D_0) in the micro channel bus mode. $\overline{MEMW}$ controls the writing of frame buffer data in the I/O channel bus mode.
$\overline{ADL}$ (AEN)	126	I	$\overline{ADL}$ is the latch command for address signals on the address bus (A_{19}-A_0) in the micro channel bus mode. When AEN is asserted in the I/O channel bus mode, I/O access to the CRTC+ is ignored in the I/O channel bus mode. AEN assertion indicates that DMA transfer is being performed on the system bus.
SLEEP ($\overline{DACK0}$)	130	I	SLEEP disables both I/O access and memory access in the micro channel bus mode. $\overline{DACK0}$ inhibits the system from accessing the frame buffer in I/O channel bus mode.
$\overline{SFDBKN}$	125	O	$\overline{SFDBKN}$ indicates that either an I/O address or memory address mapped by the CRTC+ has ben accessed in the micro channel bus mode. $\overline{SFDBKN}$ must be left disconnected in I/O channel bus mode.
CDCHRDY	27	O	CDCHRDY indicates the data transfer completion/wait status between the system and the CRTC+. The CRTC+ performs the CPU wait control by driving the CDCHRDY pin low when the CPU attempped to access the frame buffer during the CRTC+ display access.

Signal	Pin No.	Input/Output	Function
CDCHRDY	27	O	The CRTC+ performs the CPU wait control against the I/O access when the IORDYEN pin is high. The wait control function for I/O access can be disabled by driving the IORDYEN pin low when the CPU does not need high-speed operation.
IRQ	28	O	IRQ is an interrupt request to the system.
$\overline{\text{BIOS}}$	124	O	$\overline{\text{BIOS}}$ output is used to access the BIOS ROM in the I/O channel bus mode (M/AT pin = low). $\overline{\text{BIOS}}$ output is kept to be High in the micro channel bus mode.

Operation Mode Interface

Signal	Pin No.	Input/Output	Function
RESET	134	I	RESET initializes the internal status of the CRTC+.
25M	24	I	25M is the input pin for a 25.175-MHz clock source. 25M is used to display a horizontal 640-dot screen.
28M	23	I	28M is the input pin for a 28.322-MHz clock source. 28M is used to display a horizontal 720-dot screen.
EXT1	21	I	An external clock other than 25 MHz, 28 MHz, and EXT2 can be input to EXT1. The EXT1 clock is selected when the CRTC+ is in external clock mode1, and also in the CGA mode.
EXT2	20	I	An external clock other than 25 MHz, 28 MHz, and EXT1 can be input to EXT2. The EXT2 clock is selected when the CRTC+ is in external clock mode2, and also in the MDA or HGA mode.
M/AT	133	I	M/AT selects either the micro channel bus mode or I/O channel bus mode. High selects the micro channel bus mode; low selects the I/O channel bus mode.
IORDYEN	26	I	IORDYEN determines whether wait control for CPU access is enabled or disabled when I/O access is performed. When IORDYEN is low, CDCHRDY stays in the high inpedance state. When IORDYEN is high, CDCHRDY goes low (not ready) in order to make the system wait.
SWITCH	95	I	Input to SWITCH sets bit 4 in the input status register 0. Normally, SWITCH is used to indicate either monochrome or color monitor.
PORT0, PORT1	64, 30	I	Inputs to port0 and port1 set bits 0 and 1 in the port register (POT).

Signal	Pin No.	Input/Output	Function
TEST	41	I	TEST is used for chip testing. The TEST pin must always be low.

Frame Buffer Interface

Signal	Pin No.	Input/Output	Function
$\overline{\text{RAS02}}$	56	O	$\overline{\text{RAS02}}$ outputs the row address strobe to memory planes 0 and 2.
$\overline{\text{RAS13}}$	55	O	$\overline{\text{RAS13}}$ outputs the row address strobe to memory planes 1 and 3.
$\overline{\text{CAS02}}$	54	O	$\overline{\text{CAS02}}$ outputs the column address strobe to memory planes 0 and 2.
$\overline{\text{CAS13}}$	52	O	$\overline{\text{CAS13}}$ outputs the column address strobe to memory planes 1 and 3.
$\overline{\text{OE02}}$	45	O	$\overline{\text{OE02}}$ outputs the read enable signal to memory planes 0 and 2.
$\overline{\text{OE13}}$	42	O	$\overline{\text{OE13}}$ outputs the read enable signal to memory planes 1 and 3.
$\overline{\text{WE0}}$-$\overline{\text{WE3}}$	50-47	O	$\overline{\text{WE0}}$-$\overline{\text{WE3}}$ output write enable signals to memory planes 0-3, respectively.
M01A0 - M01A7	119, 117-115, 113, 112, 110, 109	O	M01A0-M01A7 provide row and column addresses to memory planes 0 and 1 in a time-sharing manner.
M23A0 - M23A4	107-103	O	M23A0-M23A4 provide the 5 low-order bits of row and column addresses to memory planes 2 and 3 in a time-sharing manner.
M2A5 - M2A7	102-100	O	M2A5-M2A7 provide the 3 high-order bits of row and column addresses to memory plane 2 in a time-sharing manner.
M3A5 - M3A7	99-97	O	M3A5-M3A7 provide the 3 high-order bits of row and column addresses to memory plane 3 in a time-sharing manner.
M01D0 - M01D7	94, 92-90 88-85	I/O	M01D0-M01D7 transfer display data between memory planes 0 and 1 in a time-sharing manner.
M23D0 - M23D7	83, 82, 80-75	I/O	M23D0-M23D7 transfer display data between memory planes 2 and 3 in a time-sharing manner.

Video Interface

Signal	Pin No.	Input/Output	Function
P7-P0	66-73	O	P7-P0 output video signals. These are TTL-level outputs.
$\overline{\text{DACIOR}}$	62	O	$\overline{\text{DACIOR}}$ controls reading of the external color palette DAC.
$\overline{\text{DACIOW}}$	61	O	$\overline{\text{DACIOW}}$ controls writing to the external color palette DAC.
PCLK	65	O	PCLK provides the dot clock to the external color palette DAC.
$\overline{\text{BLANK}}$	60	O	$\overline{\text{BLANK}}$ provides the blanking signal to the external color palette DAC.
HSYNC	59	O	HSYNC provides the horizontal synchronization timing signal required by the CRT display. The polality of HSYNC is programmable in the VGA mode, and always active-high in the other modes.
VSYNC	58	O	VSYNC provides the vertical synchronization timing signal required by the CRT display. The polality of VSYNC is programmable in the VGA mode, and active-high in the CGA mode, and active-low in the other modes.

Internal Block Diagram

Figure 1 is the CRTC+ internal block diagram.

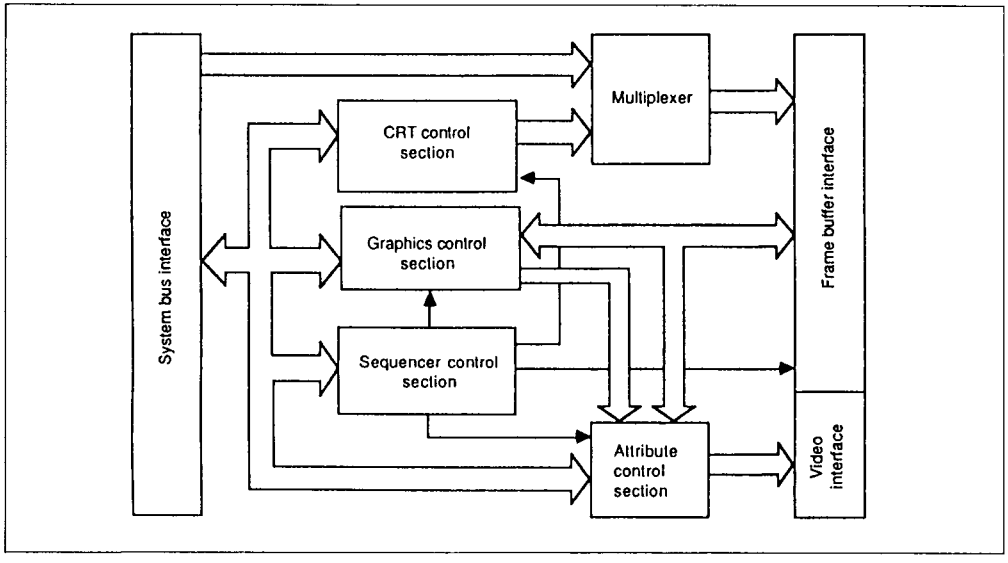

Figure 1 Internal Structure of the CRTC+

CRT Control Section: generates CRT control timing signals, frame buffer addresses, raster addresses, and refresh addresses. It also controls cursor and underline output.

Graphics Control Section: performs logic operations on graphics data, bit rotation and bit masking, memory plane masking, and other functions to support the CPU in creating graphics in the frame buffer. (CRTC+ does not support these functions in MDA, CGA, and HGA modes)

Sequencer Control Section: controls the timing of access to the frame buffer.

Attribute Control Section: controls the color palette, horizontal panning scroll, and other video functions.

Multiplexer: multiplexes the CPU address (the frame buffer address received from the CPU) and the frame buffer address generated by the CRT control section in the CRTC+.

System bus Interface: controls the interface with the system bus. The interface is easy to set up because it is compatible with both the I/O channel bus of the IBM-PC and the micro channel bus of the IBM-PS/2.

Frame Buffer Interface: direct interface to eight 64k × 4-type dynamic RAM (HM50464 or equivalent) chips.

Video Interface: outputs a TTL-level video signal and an external color palette control signal.

System Configuration

Figure 2 shows the configuration of a VGA system using the CRTC+. The CPU interface is compatible with both the I/O channel bus of the IBM-PC and the micro channel bus of the IBM-PS/2 and has an eight-bit data width, so there should be no interfacing problems. The bus type selection is made with the M/AT pin.

The frame buffer interface can directly control eight 64k × 4-type dynamic RAM (HM50464) chips, so a 256-kbyte frame buffer can be interfaced without going through an external circuit. The frame buffer consists of four memory planes (numbered 0 to 3), so the CPU can write 32 bits to the frame buffer at a time.

Use of the CRTC+ enables the parts count on a VGA graphics board to be greatly reduced.

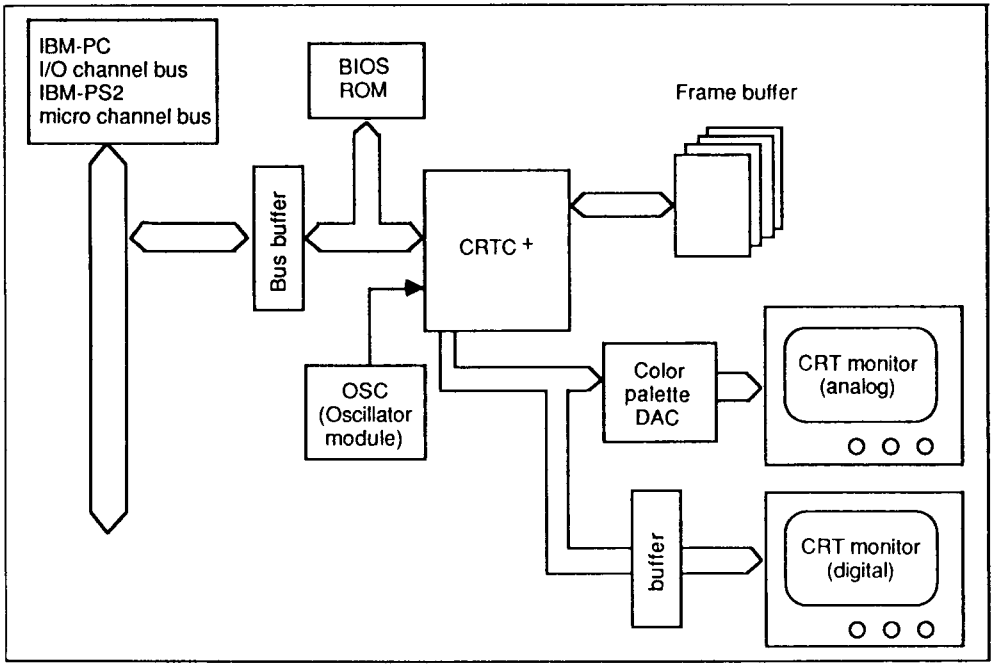

Figure 2 System Configuration

VGA-Mode Register Configuration

(1) General Control Registers

The general control registers of the VGA mode can be accessed directly by I/O port addresses.

Table 1 General Control Registers

Port*1 Address	Index Address	Register No.	Register Name	R/W	Data Bits*2							
					7	6	5	4	3	2	1	0
3C2 (3CC)	—	OR0	Output operation register	R/W								
3XA (3CA)	—	OR1	Feature control register	R/W								
3C2	—	OR2	Input status register 0	R								
3XA	—	OR3	Input status register 1	R								
3C3	—	OR4	Chip enable register	R/W								

*1 X is B in monochrome mode and D in color mode. The addresses in parentheses are read addresses.

*2 The shaded data bits are always read as 0, regardless of what value is written in them, except that bit 2 of OR3 is read as 1.

*3 The Chip enable register (OR4) is available only in the micro channel bus mode.

(2) CRT Control Registers

Table 2 CRT Control Registers

Port*1 Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X4	—	CRA	CRT address	R/W								
3X5	00	CR0	Horizontal total characters	R/W								
3X5	01	CR1	Horizontal displayed characters	R/W								
3X5	02	CR2	Horizontal blanking start position	R/W								
3X5	03	CR3	Horizontal blanking stop position	R/W								

Table 2 CRT Control Registers (cont)

Port*1 Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X5	04	CR4	Horizontal sync pulse start position	R/W								
3X5	05	CR5	Horizontal sync pulse stop position	R/W								
3X5	06	CR6	Vertical total rasters	R/W								
3X5	07	CR7	MSB	R/W								
3X5	08	CR8	First raster address	R/W								
3X5	09	CR9	Maximum raster address	R/W								
3X5	0A	CR10	Cursor start raster	R/W								
3X5	0B	CR11	Cursor end raster	R/W								
3X5	0C	CR12	Start address (H)	R/W								
3X5	0D	CR13	Start address (L)	R/W								
3X5	0E	CR14	Cursor (H)	R/W								
3X5	0F	CR15	Cursor (L)	R/W								
3X5	10	CR16	Vertical sync pulse start position	R/W								
3X5	11	CR17	Vertical sync pulse stop position	R/W								
3X5	12	CR18	Vertical displayed rasters	R/W								
3X5	13	CR19	Memory width	R/W								
3X5	14	CR20	Underline	R/W								
3X5	15	CR21	Vertical blanking start position	R/W								
3X5	16	CR22	Vertical blanking stop position	R/W								
3X5	17	CR23	CRTC mode control	R/W								
3X5	18	CR24	Screen split postion	R/W								

*1 X is B in monochrome mode and D in color mode.

(3) Graphics Control Registers

Table 3 Graphics Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3CE	——	GRA	Graphics address	R/W								
3CF	00	GR0	Set/reset	R/W								
3CF	01	GR1	Enable set/reset	R/W								
3CF	02	GR2	Color compare	R/W								
3CF	03	GR3	Data rotate	R/W								
3CF	04	GR4	Read plane select	R/W								
3CF	05	GR5	Graphic mode control	R/W								
3CF	06	GR6	Graphics	R/W								
3CF	07	GR7	Color compare enable	R/W								
3CF	08	GR8	Bit mask	R/W								
3CF	09	GR9*1	Processor latch 0	R								
3CF	0A	GR10*1	Processor latch 1	R								
3CF	0B	GR11*1	Processor latch 2	R								
3CF	0C	GR12*1	Processor latch 3	R								

*1 The processor latch 0-3 are the extended registers of CRTC+.

(4) Sequencer Control Registers

Table 4 Sequencer Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3C4	—	SRA	Sequencer address	R/W								
3C5	00	SR0	Reset	R/W								
3C5	01	SR1	Clock mode	R/W								
3C5	02	SR2	Memory plane mask	R/W								
3C5	03	SR3	Character font select	R/W								
3C5	04	SR4	Memory mode	R/W								

(5) Attribute Control Registers

Table 5 Attribute Control Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3C0	—	ARA	Attribute address	R/W								
3C0(3C1)	00-0F	AR0-AR15	Palette	R/W								
3C0(3C1)	10	AR16	Attribute mode control	RW								
3C0(3C1)	11	AR17	Border color	R/W								
3C0(3C1)	12	AR18	Color plane enable	R/W								
3C0(3C1)	13	AR19	Horizontal panning scroll	R/W								
3C0(3C1)	14	AR20	Color select	R/W								

Note: The addresses in parentheses are read addresses.

(6) Extended Registers

The extended registers listed in table 6 support the extended functions of the CRTC*. These registers are internal registers of the CRT control section, and are each accessed by an index address placed in the CRT address register (CRA).

Table 6 Extended Registers

Port* Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X5	FD	EM0	Extended register 1	R/W								
3X5	FE	EM1	Extended register 2	R/W								
3X5	FC	POT	Port register	R/W								

*: X is B in monochrome mode and D in color mode.

(7) External Palette DAC Control

External palette DAC control is provided at the port addresses listed in table 7. External Palette DAC Control Registers, for details of the register functions.

Table 7 External Palette DAC Control Registers

Port Address*1	Register No.	Register Name	R/W
3C8	DCWA	DAC write address*1	R/W
3C7	DCRA	DAC read address*1	W
3C7	DC0	DAC status*2	R
3C9	DC1	DAC data*1	R/W
3C6	DC2	DAC pel mask*1	R/W

1 DAC write address registers, the DAC read address register, DAC data registers, and DAC pel mask register are located in the external palette DAC. The CRTC outputs the $\overline{\text{DACIOR}}$, $\overline{\text{DACIOW}}$ control signals by decoding the port address given above.

2 The DAC status register is located in the CRTC.

6845-Mode Register Configuration

(1) 6845-Mode Registers

Table 8 lists the 6845-mode registers, which are used in all three modes: MDA, HGA, and CGA. Although they are not listed in the table, the extended registers are also accessed by specifying an index address in the CRT address register, as in the VGA mode.

Table 8 6845-Mode Registers (Used in CGA, MDA, and HGA Modes)

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3X4	—	CRA	CRT address register	R/W								
3X5	00	CR0	Horizontal total characters register	R/W								
3X5	01	CR1	Horizontal displayed characters register	R/W								
3X5	02	CR62	Horizontal sync position register	R/W								
3X5	03	CR63	Sync pulse width register	R/W								
3X5	04	CR64	Vertical total characters register	R/W								
3X5	05	CR65	Total raster adjust register	R/W								
3X5	06	CR66	Vertical displayed characters register	R/W								
3X5	07	CR67	Vertical sync position register	R/W								
3X5	08	CR68	Skew register *2	R/W								
3X5	09	CR9	Maximum raster address register	R/W								
3X5	0A	CR10	Cursor start raster address *3	R/W								
3X5	0B	CR11	Cursor end raster address	R/W								
3X5	0C	CR12	Start address register (H) *4	R/W								
3X5	0D	CR13	Start address register (L)	R/W								
3X5	0E	CR14	Cursor register (H) *4	R/W								
3X5	0F	CR15	Cursor register (L)	R/W								

*1 X is [B] in the MDA and HGA modes and [D] in the CGA mode.
*2 The CRTC+ supports only the noninterlaced mode.
*3 The CRTC+ does not support cursor blinking.
*4 In the CRTC+, the start address register and cursor address register are 16-bit registers.

(2) MDA- and HGA-Compatible Registers

The MDA- and HGA-compatible registers are provided to make the 6845 modes of the CRTC+ compatible with MDA and HGA.

Table 9 MDA- and HGA-Compatible Registers

Port Address	Index Address	Register No.	Register Name		R/W	Data Bits							
						7	6	5	4	3	2	1	0
3B8	—	MH0	Mode control register	MDA	R/W								
				HGA									
3BA	—	MH1	CRT status register	MDA	R								
				HGA									
3BF*	—	MH2	Hercules configuration register		R/W								

* The Hercules configuration register [3BF] is used only in the HGA mode.

(3) CGA-Compatible Registers

The CGA-compatible registers are provided to make the 6845 modes of the CRTC+ compatible with CGA.

Table 10 CGA-Compatible Registers

Port Address	Index Address	Register No.	Register Name	R/W	Data Bits							
					7	6	5	4	3	2	1	0
3D8	—	CG0	Mode control register	R/W								
3D9	—	CG1	Color select register	R/W								
3DA	—	CG2	CRT status register	R								

(4) Extended Registers

Extended registers 1 and 2 (EM0 and EM1) and the port register (POT) are used in the 6845 modes as well as the VGA mode. These registers have the same functions in the 6845 modes as in the VGA mode.

Absolute Maximum Ratings

Table 11 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC} *1	-0.3 to +6.7	V
Input voltage	V_{in} *1	-0.3 to (V_{CC} + 0.3)	V
Allowable output current	$\|I_0\|$ *2	5	mA
Total allowable output current	$\|\Sigma I_0\|$ *3	200	mA
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

*1 This value is referenced to V_{SS} = 0 V.
*2 Allowable output current is the maximum current that may be drawn from or sunk into one output pin or one input/output pin.
*3 Total allowable output current is the total sum of the currents that may be drawn from or sunk into all the output and input/output pins.

Notes 1. Using this chip beyond its maximum ratings may degrade its reliability or permanently destroy it. Use this chip under the conditions recommended in Recommended Operating Conditions.
2. Unused input pins should be pulled up.

Recommended Operating Conditions

Table 12 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*	4.75	5.0	5.25	V
Low input level	V_{IL}*	0	–	0.7	V
High input level	V_{IH}*	2.2	–	V_{CC}	V
Reset low input level	V_{ILR}*	0	–	0.5	V
Reset high input level	V_{IHR}*	2.5	–	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	C°

* This value is referenced to V_{SS} = 0 V.

■ Timing measurements

- The timing measurement point for low output levels in these specifications is defined to be 0.8 V.
- The low output level for stable conditions (DC characteristics) is defined to be 0.5 V.
- The high output level is defined to be V_{CC} - 2.0 V.

DC Characteristics

Table 13 DC Characteristics

(V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Conditions
Input high level (except RESET)	V_{IH}	2.2	V_{CC}	V	
Input low level (except RESET)	V_{IL}	-0.3	0.7	V	
Reset input high level	V_{IHR}	2.5	V_{CC}	V	
Reset input low level	V_{ILR}	-0.3	0.5	V	
Input leakage current	I_{IN}	-2.5	+2.5	µA	V_{in} = 0 - V_{CC}
Three-state input current	I_{TSI}	-10	+10	µA	V_{in} = 0.4 - V_{CC}
Output high level	V_{OH}	3.5*4	–	V	I_{OH} = -350 µA
		–	–	–	–
Output low level	V_{OL}	–	0.5*3	V	I_{OL} = 2.2 mA*1
		–	0.5*3	V	I_{OL} = 1.6 mA*2
Input capacity	C_{in}	–	15	pF	V_{in} = 0 V, T_a =25°C, f = 1 MHz
Current consumption	I_{CC}	–	280	mA	f = 32 MHz

*1 CDCHRDY, IRQ, and $\overline{\text{SFDBKN}}$ pins
*2 Other pins
*3 The AC timing measurement point for output low levels is defined to be 0.8 V.
*4 The AC timing measurement point for output high level is defined to be V_{CC} - 2.0 V.

AC Characteristics

(1) Clock Timing

Table 14 Clock Timing

(Vcc = 5.0 V ±5%, Vss = 0 V, Ta = 0 to 70°C, unless otherwise noted)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
1	Operating frequency	f_C	5	32	5	37	MHz	Figure 3
2	Clock cycle	T_C	31	200	27	200	ns	
3	Clock high pulse width	t_{CH}	13	–	11	–	ns	
4	Clock low pulse width	t_{CL}	13	–	11	–	ns	
5	Clock rise time	t_{CR}	–	6	–	5	ns	
6	Clock fall time	t_{CF}	–	6	–	5	ns	

(2) CPU Read/Write Cycle Timing

Table 15 (1) to (3) gives the CPU read/write cycle timing for I/O channel bus mode.

Table 15 (1) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
11	$\overline{IOR}$ low pulse width	t_{IRLW}	$3M_C$	–	$3M_C$	–	Cycles*1	Figure 4 (a),
12	$\overline{IOR}$ high pulse width	t_{IRHW}	$2M_C$	–	$2M_C$	–	Cycles*1	Figure 4 (b)
13	$\overline{IOW}$ low pulse width	t_{IWLW}	$3M_C$	–	$3M_C$	–	Cycles*1	
14	$\overline{IOW}$ high pulse width	t_{IWHW}	$2M_C$	–	$2M_C$	–	Cycles*1	
15	$\overline{IOR}$ input inhibit time	t_{IRIH}	$2M_C$	–	$2M_C$	–	Cycles*1	
16	$\overline{IOW}$ input inhibit time	t_{IWIH}	$2M_C$	–	$2M_C$	–	Cycles*1	
17	Address setup time (from $\overline{IOR}$)	t_{ASIR}	0	–	0	–	ns	
18	Address hold time (from $\overline{IOR}$)	t_{AHIR}	10	–	10	–	ns	

*1 M_C: Clock cycle on the 28M pin

Table 15 (1) CPU Read/Write Cycle Timing (I/O Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
19	Address setup time (from $\overline{IOW}$)	t_{ASIW}	0	–	0	–	ns	
20	Address hold time (from $\overline{IOW}$)	t_{AHIW}	10	–	10	–	ns	
21	I/O read data access time	t_{IRAC}	–	70	–	70	ns	
22	I/O read data hold time	t_{IRDH}	5	–	5	–	ns	
23	I/O read data turnoff time 1	t_{IRTF1}	–	35	–	35	ns	
24	I/O write data setup time 1	t_{IWDS1}	0	–	0	–	ns	
25	I/O write data hold time 1	t_{IWDH1}	0	–	0	–	ns	
31	I/O read data setup time	t_{IRDS}	$1M_C$	–	$1M_C$	–	Cycles*1	Figure 4 (b)
36	CDCHRDY low delay (from $\overline{IOR}$)	t_{RDIR}	0	70	0	70	ns	
37	CDCHRDY low delay (from $\overline{IOW}$)	t_{RDIW}	0	70	0	70	ns	

Table 15 (2) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
41	$\overline{MEMR}$ low pulse width							Figure 5
	Text, graphics	t_{MRLW}	$10T_C$	–	$10T_C$	–	Cycles*2	
	132-column mode	t_{MRLW}	$12T_C$	–	$12T_C$	–	Cycles*2	
42	$\overline{MEMR}$ high pulse width	t_{MRHW}	$2M_C$	–	$2M_C$	–	Cycles*1	
43	$\overline{MEMW}$ low pulse width							
	Text, graphics	t_{MWLW}	$10T_C$	–	$10T_C$	–	Cycles	
	132-column mode	t_{MWLW}	$12T_C$	–	$12T_C$	–	Cycles	
44	$\overline{MEMW}$ high pulse width	t_{MWHW}	$2M_C$	–	$2M_C$	–	Cycles*1	

*1 M_C: Clock cycle on the 28M pin
*2 T_C: Clock cycle used as pixel clock

Table 15 (2) CPU Read/Write Cycle Timing (I/O Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
45	$\overline{\text{MEMR}}$ input inhibit time	t_{MRIH}	$2M_C$	–	$2M_C$	–	ns*1	
46	$\overline{\text{MEMW}}$ input inhibit time	t_{MWIH}	$2M_C$	–	$2M_C$	–	ns*1	
47	$\overline{\text{MEMR}}$ hold time (from CDCHRDY)	t_{MRH}	0	–	0	–	ns	
48	$\overline{\text{MEMW}}$ hold time (from CDCHRDY)	t_{MWH}	0	–	0	–	ns	
49	Address hold time (from CDCHRDY)	t_{AHRD}	0	–	0	–	ns	
50	Address hold time (from $\overline{\text{MEMR}}$)	t_{AHMR}	10	–	10	–	ns	
51	Address hold time (from $\overline{\text{MEMW}}$)	t_{AHMW}	10	–	10	–	ns	
52	Address setup time (from $\overline{\text{MEMR}}$)	t_{ASMR}	0	–	0	–	ns	
53	Address setup time (from $\overline{\text{MEMW}}$)	t_{ASMW}	0	–	0	–	ns	
54	Memory read data setup time	t_{MRDS}	$1T_C$	–	$1T_C$	–	Cycles	Figure 5
55	Memory read data hold time	t_{MRDH}	5	–	5	–	ns	
56	Memory read data turnoff time	t_{MRDT}	–	35	–	35	ns	
57	Memory write data setup time	t_{MWDS}	0	–	0	–	ns	
58	Memory write data hold time	t_{MWDH}	0	–	0	–	ns	
59	CDCHRDY low delay (from $\overline{\text{MEMR}}$)	t_{RDMR}	0	70	0	70	ns	
60	CDCHRDY low delay (from $\overline{\text{MEMW}}$)	t_{RDMW}	0	70	0	70	ns	

*1 M_C: Clock cycle on the 28M pin

Table 15 (3) CPU Read/Write Cycle Timing (I/O Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
61	CDCHRDY low pulse width							
	Memory access	t_{RDLW}	$10T_C$	–	$10T_C$	–	Cycles*2	
	I/O or BIOS access	t_{RDLW}	$2M_C$	–	$2M_C$	–	Cycles*1	
62	CDCHRDY high hold time	t_{RDHH}	0	–	0	–	ns	
71	AEN setup time (from $\overline{IOR}$)	t_{AESR}	20	–	20	–	ns	Figure 6
72	AEN setup time (from $\overline{IOW}$)	t_{AESW}	20	–	20	–	ns	
73	AEN hold time (from $\overline{IOR}$)	t_{AEHR}	5	–	5	–	ns	
74	AEN hold time (from $\overline{IOW}$)	t_{AEHW}	5	–	5	–	ns	
75	$\overline{DACK0}$ setup time (from $\overline{MEMR}$)	t_{DKSR}	20	–	20	–	ns	
76	$\overline{DACK0}$ setup time (from $\overline{MEMW}$)	t_{DKSW}	20	–	20	–	ns	
77	$\overline{DACK0}$ hold time (from $\overline{MEMR}$)	t_{DKHR}	5	–	5	–	ns	
78	$\overline{DACK0}$ hold time (from $\overline{MEMW}$)	t_{DKHW}	5	–	5	–	ns	
79	$\overline{BIOS}$ delay (from $\overline{MEMR}$)	t_{BSMR}	0	50	0	50	ns	
80	DIR delay (from $\overline{IOR}$ and $\overline{MEMR}$)	t_{DRIM}	0	55	0	55	ns	

*1 M_C: Clock cycle on the 28M pin
*2 T_C: Clock cycle used as pixel clock

Table 16 gives the CPU read/write cycle timing for micro channel bus mode.

Table 16 CPU Read/Write Cycle Timing (Micro Channel Bus Mode)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
91	Address setup time (from S0 or S1)	t_{ASST}	5	–	5	–	ns	Figure 7
92	Status setup time (from CMD)	t_{SSCM}	50	–	50	–	ns	
99	Address hold time (from CMD)	t_{AHCM}	25	–	25	–	ns	
100	Status hold time (from CMD)	t_{STHC}	25	–	25	–	ns	
101	$\overline{\text{SFDBKN}}$ delay	t_{SFDD}	–	50	–	50	ns	
102	Address setup time (from CMD)	t_{ASCM}	80	–	80	–	ns	
103	$\overline{\text{CMD}}$ low pulse width	t_{CMLW}	90	–	90	–	ns	
104	Write data setup time	t_{WDSC}	0	–	0	–	ns	Figure 7
105	Write data hold time	t_{WDHC}	25	–	25	–	ns	
106	Read data access time (from $\overline{\text{S0}}$ or $\overline{\text{S1}}$)	t_{ACST}	–	100	–	100	ns	
107	Read data access time (from CMD)	t_{ACCM}	–	45	–	45	ns	
108	Read data access time (from CDCHRDY)	t_{ACRD}	–	45	–	45	ns	
109	Read data hold time (from CMD)	t_{RDHC}	0	–	0	–	ns	
110	$\overline{\text{CMD}}$ input inhibit time 1	t_{CIH1}	180	–	180	–	ns	
111	$\overline{\text{CMD}}$ input inhibit time 2	t_{CIH2}	$1.5M_C$	–	$1.5M_C$	–	Cycles*1	
113	Status input inhibit time	t_{STIH}	35	–	35	–	ns	
114	$\overline{\text{CMD}}$ negate time (to next $\overline{\text{S0}}$ or $\overline{\text{S1}}$)	t_{CMNG}	–	5	–	5	ns	

Table 16 CPU Read/Write Cycle Timing (Micro Channel Bus Mode) (cont)

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
115	CDCHRDY low delay (from address)	t_{RDAD}	–	60	–	60	ns	
116	CDCHRDY low delay (from S0 or S1)	t_{RDSD}	0	30	0	30	ns	
117	Read data turnoff time	t_{RDTF}	–	35	–	35	ns	
123	DIR delay (from $\overline{CMD}$)	t_{DRCM}	0	35	0	35	ns	Figure 7
124	SLEEP setup time	t_{SLS}	5	–	5	–	ns	
125	SLEEP hold time	t_{SLH}	10	–	10	–	ns	

(3) IRQ and RESET Timing

Table 17 IRQ and RESET Timing

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
131	IRQ delay 1 (Hi-Z to low)	t_{IQD1}	–	80	–	70	ns	Figure 8
132	IRQ delay 2 (low to high)	t_{IQD2}	–	80	–	70	ns	
133	RESET pulse width	t_{RSTW}	$10T_C$	–	$10T_C$	–	Cycles	
134	RESET rise time	t_{RSTR}	–	100	–	100	ns	
135	RESET fall time	t_{RSTF}	–	100	–	100	ns	

*1 M_C: Clock cycle on the 28M pin

(4) Frame Buffer Memory Interface Timing

Table 18 (1) Frame Buffer Memory Interface Timing

No.	Item		Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
141	$\overline{RAS}$ delay		t_{RD}	10	80	10	65	ns	Figure 9 (a),
142	$\overline{RAS}$ low pulse width *1	Text, graphics (CPU)	t_{RSLW}	$(4T_c-10)(4T_c+10)$		$(4T_c-10)(4T_c+10)$		ns	Figure 9 (b)
		Graphics (display) 25M, 28M		$(4T_c-10)$	$(125T_c+10)$	$(4T_c-10)$	$(125T_c+10)$		
		Graphics (display) EXT1, EXT2		$(4T_c-10)$	$(253T_c+10)$	$(4T_c-10)$	$(253T_c+10)$		
		132-column (CPU)		$(5T_c-10)(5T_c+10)$		$(5T_c-10)(5T_c+10)$			
		132-column (display) 25M, 28M		$(5T_c-10)$	$(125T_c+10)$	$(5T_c-10)$	$(125T_c+10)$		
		132-column (display) EXT1, EXT2		$(5T_c-10)$	$(253T_c+10)$	$(5T_c-10)$	$(253T_c+10)$		
143	$\overline{RAS}$ high pulse width	Text, graphics	t_{RSHW}	$(3T_c-10)(3T_c+10)$		$(3T_c-10)(3T_c+10)$		ns	
		132-column		$(4T_c-10)(4T_c+10)$		$(4T_c-10)(4T_c+10)$			
144	$\overline{CAS}$ delay		t_{CD}	$(2T_c-10)(2T_c+10)$		$(2T_c-10)(2T_c+10)$		ns	
145	$\overline{CAS}$ low pulse width	Text, graphics	t_{CSLW}	$(3T_c-10)(3T_c+10)$		$(3T_c-10)(3T_c+10)$		ns	
		132-column		$(4T_c-10)(4T_c+10)$		$(4T_c-10)(4T_c+10)$			
146	$\overline{CAS}$ high pulse width	Text, graphics	t_{CSHW}	$(4T_c-10)(4T_c+10)$		$(4T_c-10)(4T_c+10)$		ns	
		Graphics (display)		$(2T_c-10)(2T_c+10)$		$(2T_c-10)(2T_c+10)$			
		132-column (CPU)		$(5T_c-10)(5T_c+10)$		$(5T_c-10)(5T_c+10)$			
		132-column (display)		$(3T_c-10)(3T_c+10)$		$(3T_c-10)(3T_c+10)$			

*1: Page mode access is used for graphics display and 132-column text display. t_{RSLW} differs according to the master clock selection (specified in the output operation register).

Table 18 (2) Frame Buffer Memory Interface Timing

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
151	Row address setup time	t_{RAS}	0	–	0	–	ns	Figure 9 (a),
152	Row address hold time	t_{RAH}	$1/2T_C-5$	–	$1/2T_C-5$	–	ns	Figure 9 (b)
153	Column address setup time	t_{CAS}	0	–	0	–	ns	
154	Column address hold time	t_{CAH}	T_C-10	–	T_C-10	–	ns	
155	RAM read data setup time	t_{RRS}	10	–	10	–	ns	
156	RAM read data hold time	t_{RRH}	5	–	5	–	ns	
157	$\overline{OE}$ delay	t_{OED}	$(t_{RD}-10)(t_{RD}+10)$		$(t_{RD}-10)(t_{RD}+10)$*1		ns	
158	$\overline{OE}$ low pulse width — Text, graphics	t_{OEW}	$(2T_C-10)(2T_C+10)$		$(2T_C-10)(2T_C+10)$		ns	
	132-column		$(3T_C-10)(3T_C+10)$		$(3T_C-10)(3T_C+10)$			
159	RAM write data setup time	t_{RWS}	0	–	0	–	ns	
160	RAM write data hold time	t_{RWH}	$(1.5T_C-10)$	–	$(1.5T_C-5)$	–	ns	
161	$\overline{WE}$ delay	t_{WED}	$(t_{RD}-10)(t_{RD}+10)$		$(t_{RD}-10)(t_{RD}+10)$*1		ns	
162	$\overline{WE}$ low pulse width — Text, graphics	t_{WEW}	$(2T_C-10)(2T_C+10)$		$(2T_C-10)(2T_C+10)$		ns	
	132-column		$(3T_C-10)(3T_C+10)$		$(3T_C-10)(3T_C+10)$			

*1 t_{RD} : No. 141 $\overline{RAS}$ delay time.

(5) Video Interface Timing

Table 19 Video Interface Timing

No.	Item	Symbol	F28 Min	F28 Max	F37 Min	F37 Max	Unit	Reference
171	$\overline{\text{DACIOR}}$ delay (from $\overline{\text{IOR}}$)	t_{DRIR}	–	55	–	55	ns	Figure 10 (a), Figure 10 (b)
172	$\overline{\text{DACIOR}}$ delay (from $\overline{\text{CMD}}$)	t_{DRCM}	–	45	–	45	ns	
173	$\overline{\text{DACIOW}}$ delay (from $\overline{\text{IOW}}$)	t_{DWIW}	–	55	–	55	ns	
174	$\overline{\text{DACIOW}}$ delay (from $\overline{\text{S0}}$ or $\overline{\text{S1}}$)	t_{DWST}	–	45	–	45	ns	
175	$\overline{\text{DACIOW}}$ low pulse width	t_{DWLI}	$1M_C$–10	–	$1M_C$–10	–	ns*1	
176	PCLK delay	t_{PCD}	–	45	–	45	ns	Figure 11
177	Video data setup time	t_{PDS}	6	–	6	–	ns	
178	Video data hold time	t_{PDH}	6	–	6	–	ns	
179	$\overline{\text{BLANK}}$ delay time	t_{BLD}	–	60	–	55	ns	
181	HSYNC delay	t_{HSD}	–	60	–	55	ns	
182	VSYNC delay	t_{VSD}	–	60	–	55	ns	

*1 M_C: Clock cycle on the 28M pin

Timing Charts

(1) Clock Timing

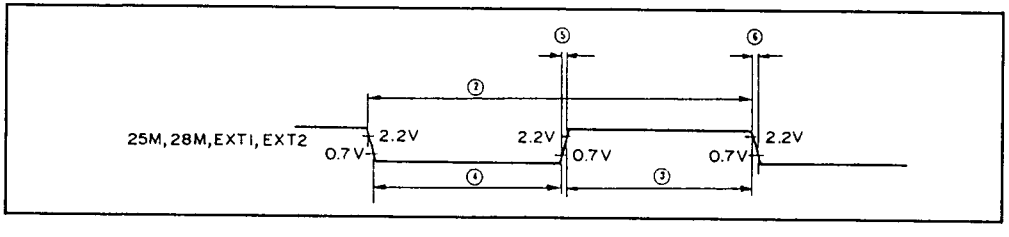

Figure 3 Clock Timing

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(2) I/O Access Timing (I/O Channel Bus Mode)

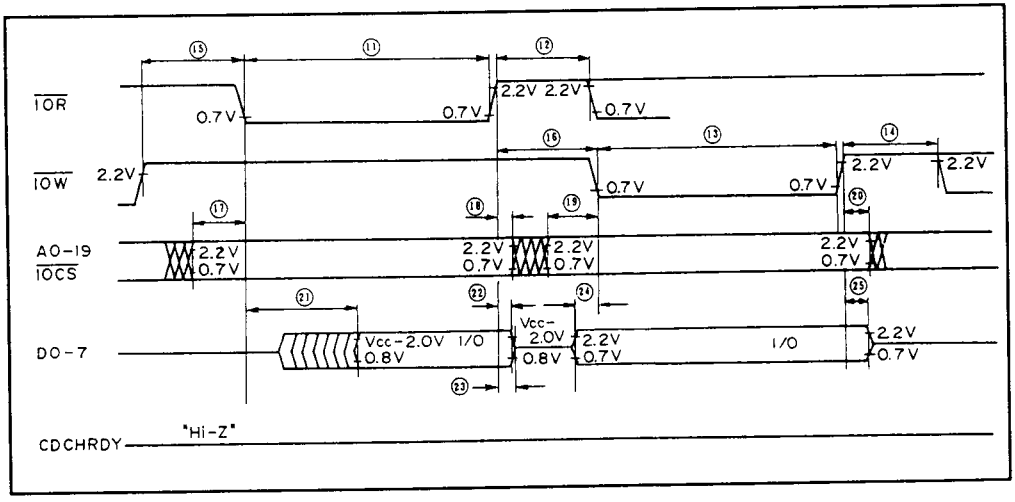

Figure 4 (a) I/O Access Timing (IORDYEN Pin Low)

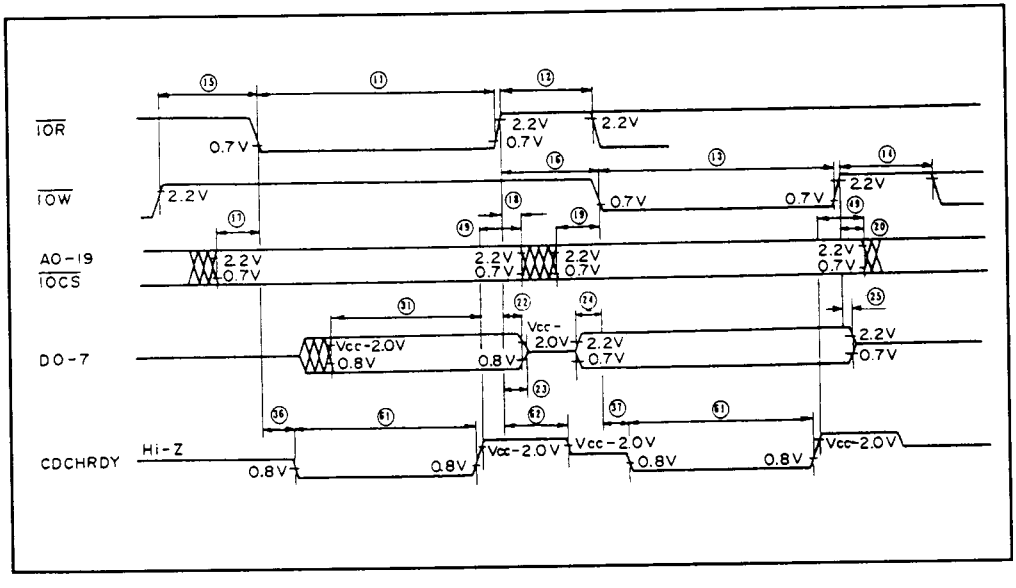

Figure 4 (b) I/O Access Timing (IORDYEN Pin High)

(3) Memory Access Timing (I/O Channel Bus Mode)

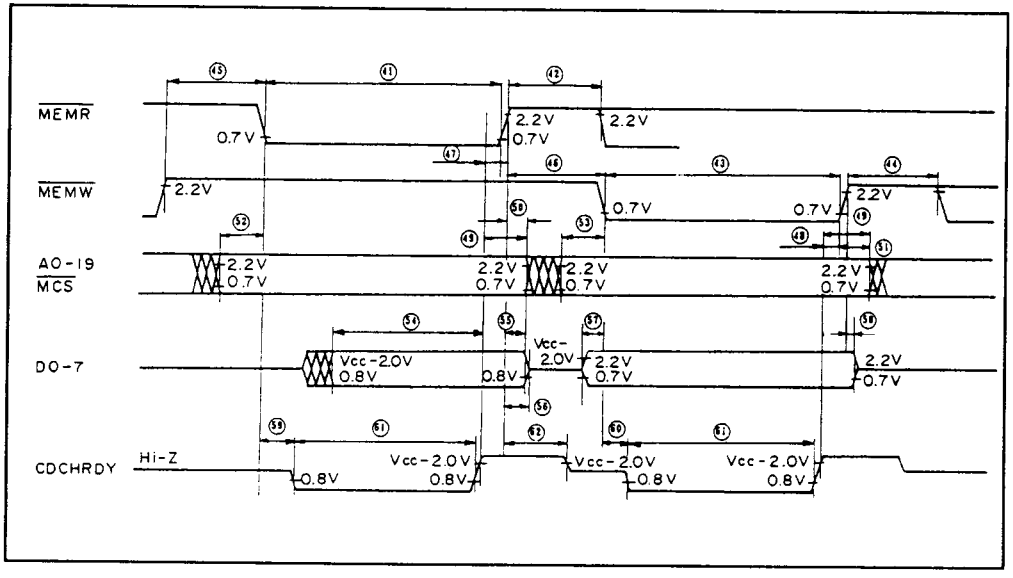

Figure 5 Memory Access Timing

(4) System Bus Interface Timing (I/O Channel Bus Mode)

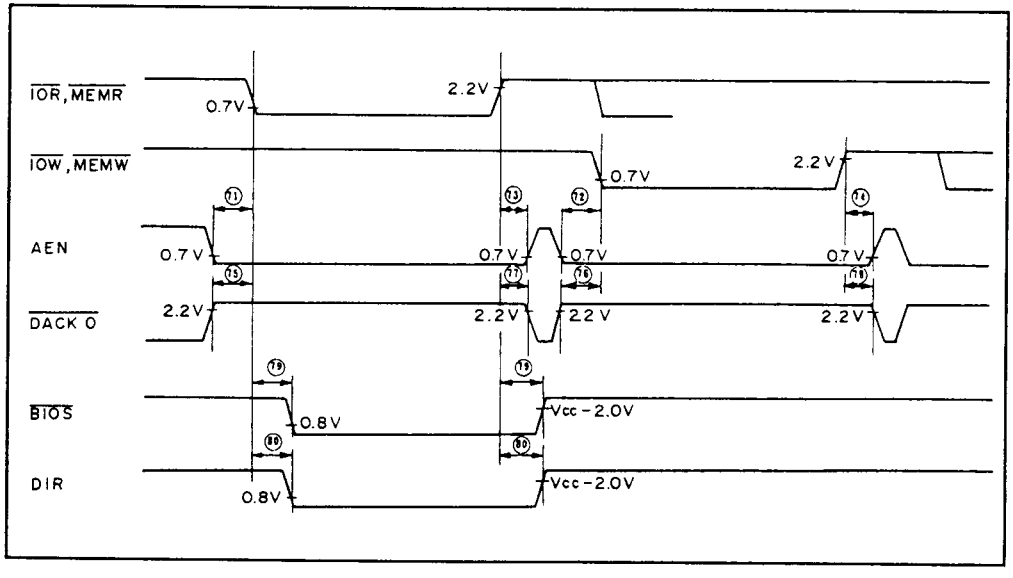

Figure 6 I/O Channel Bus Control Signal Timing

(5) Micro Channel Access Timing (Micro Channel Bus Mode)

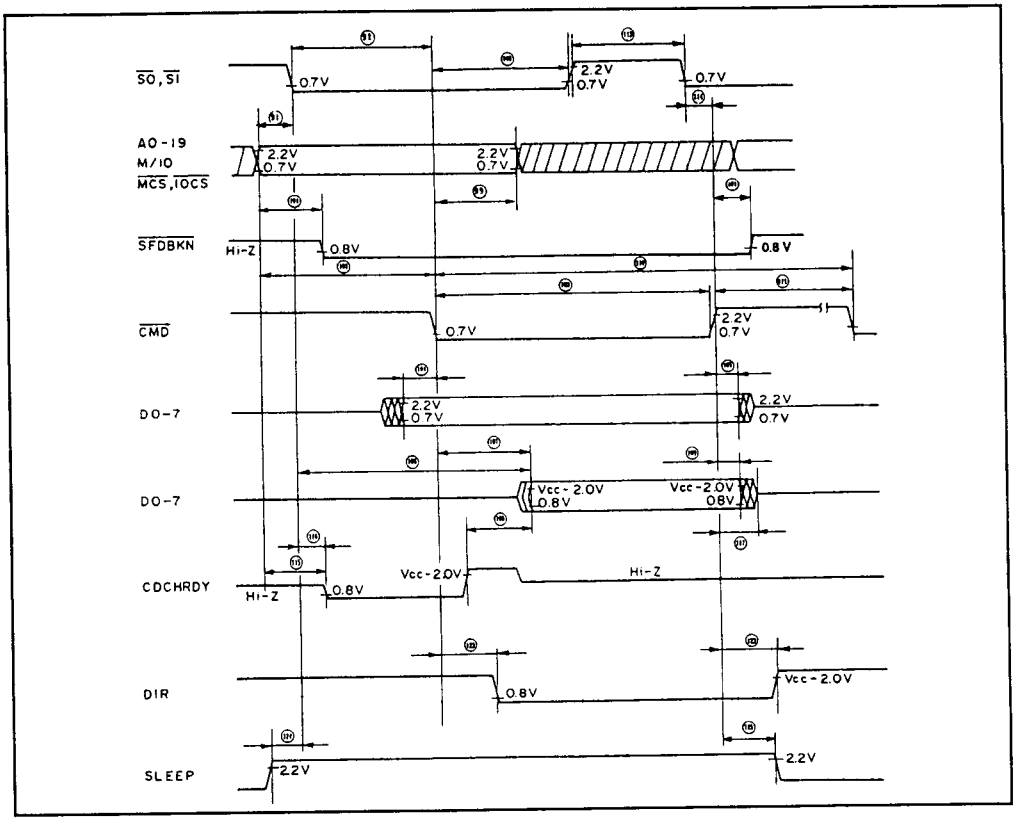

Figure 7 Micro Channel Bus Access Timing

(6) IRQ and RESET Timing

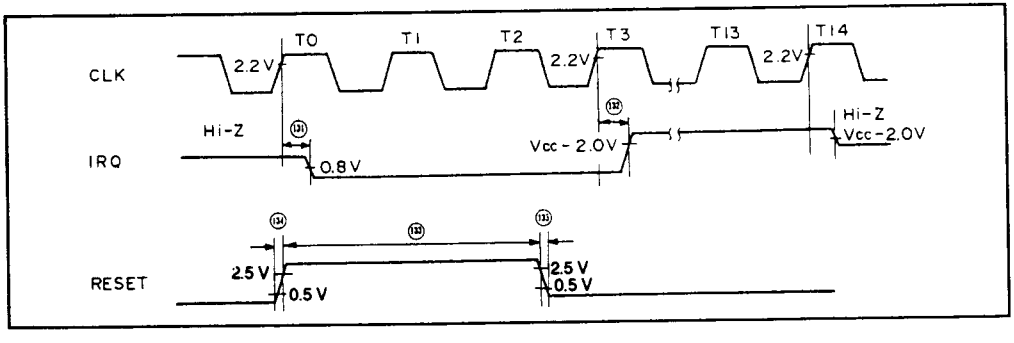

Figure 8 IRQ and RESET Timing

(7) Display Memory Read/Write Cycle Timing

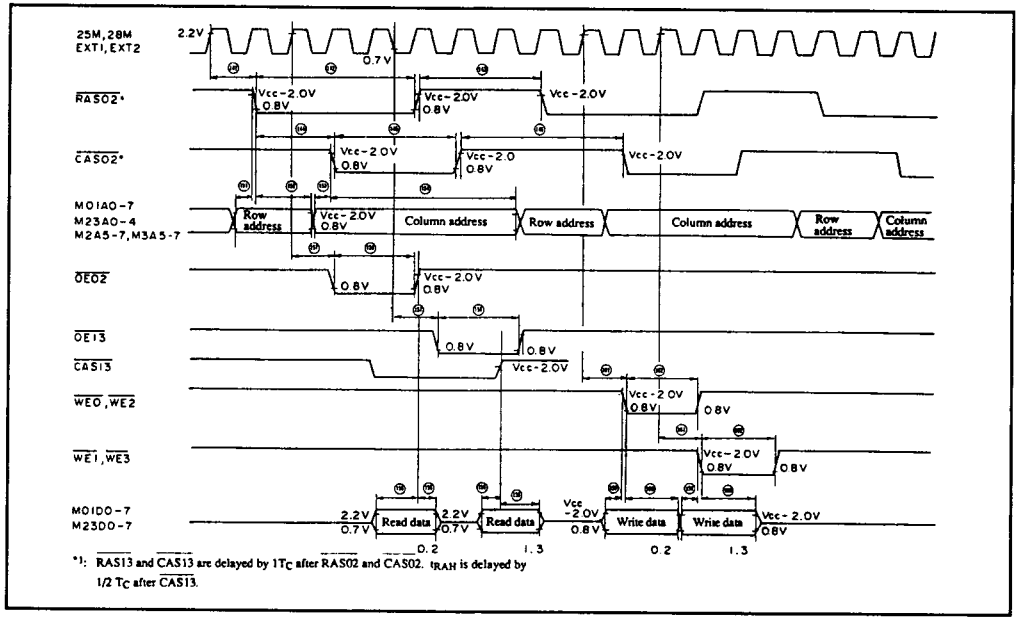

Figure 9 (a) Display Memory Normal Read/Write Timing
(Display or CPU access in non-132-column text mode)
(CPU access in graphics mode (smart access))
(CPU access in 132-column text mode)

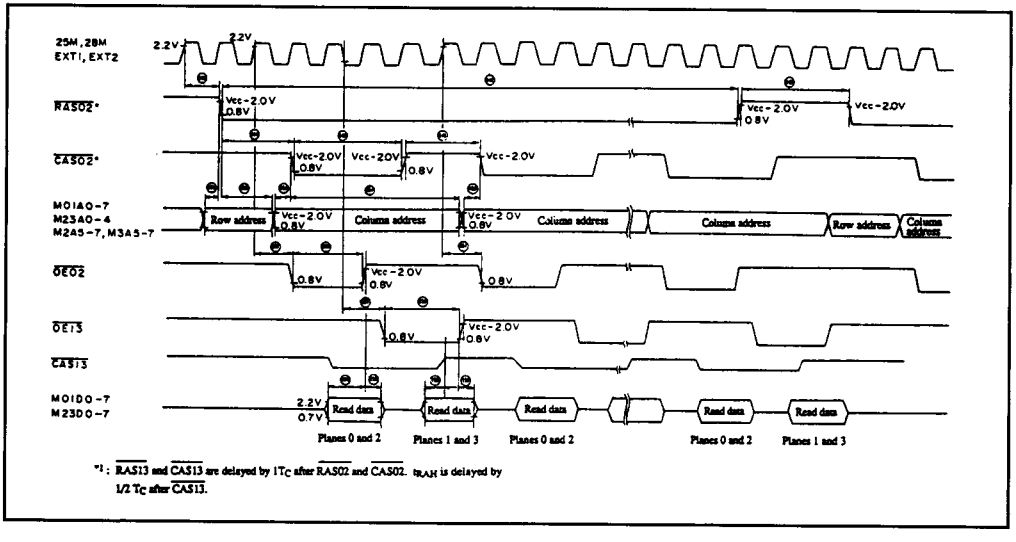

Figure 9 (b) Display Memory Page-Mode Read Timing
(Display access in graphics mode (smart access) and 132-column text mode)

(8) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing

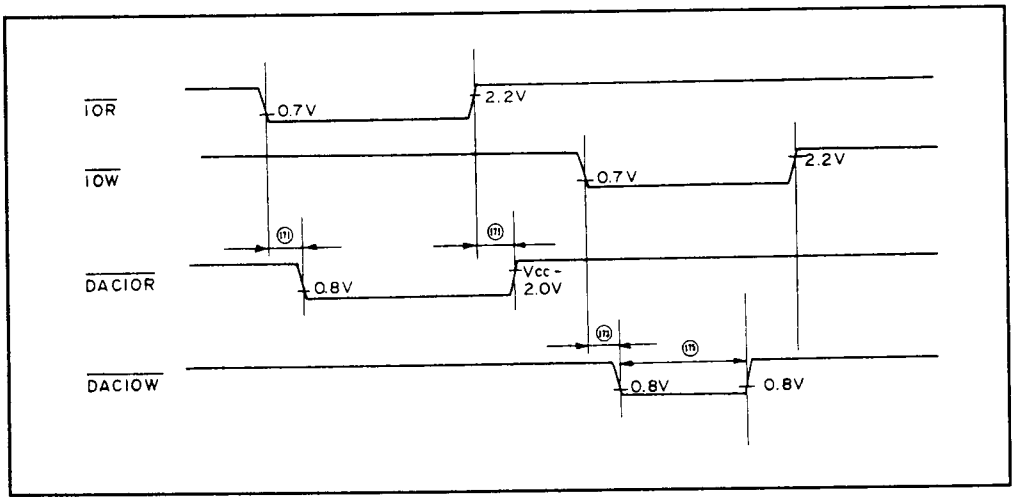

Figure 10 (a) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing (I/O Channel Bus Mode)

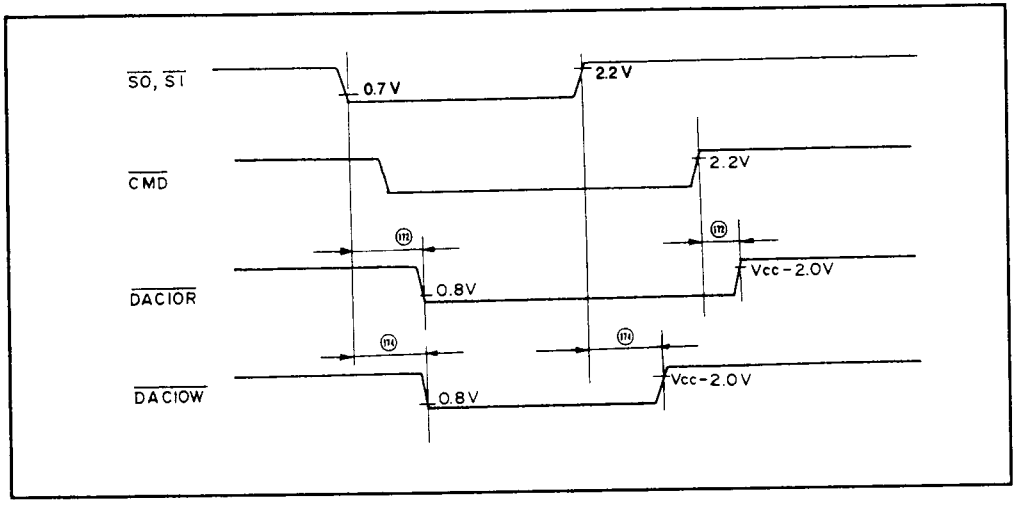

Figure 10 (b) $\overline{\text{DACIOR}}$ and $\overline{\text{DACIOW}}$ Timing (Micro Channel Bus Mode)

(9) Video Interface Timing

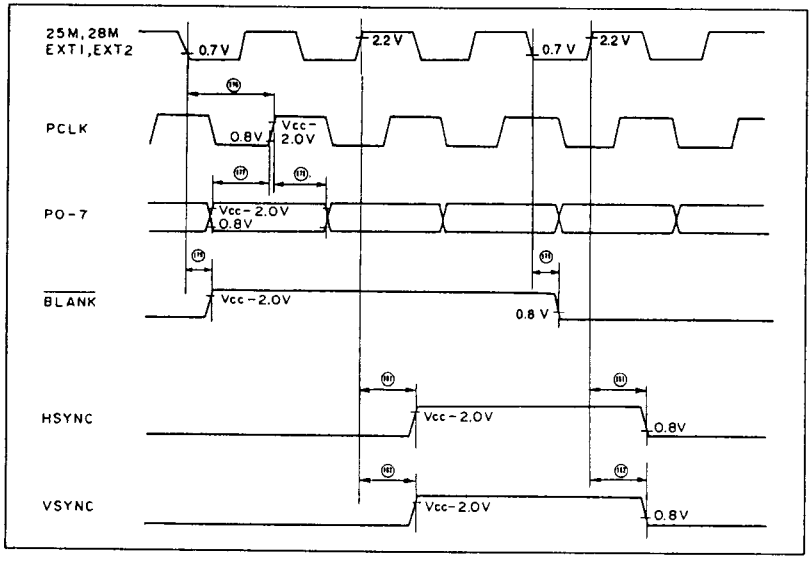

Figure 11 Video Interface Timing

Test Load Conditions

Load	Pin	Condition	Unit
R_L	$\overline{SFDBKN}$, CDCHRDY, IRQ	1.8	kΩ
	Other pins	2.4	kΩ
C	$\overline{SFDBKN}$, CDCHRDY, IRQ	100	pF
	Other pins	40	pF
R	$\overline{SFDBKN}$, CDCHRDY, IRQ	10	kΩ
	Other pins	10	kΩ

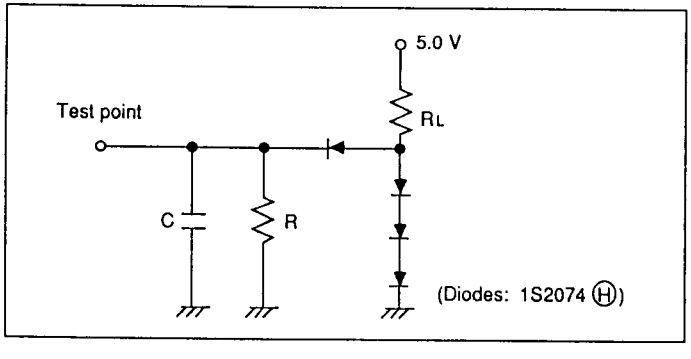

Figure 12 Test Load Conditions