Section 18 Electrical Specifications

18.1 Absolute Maximum Ratings

Table 18-1 lists the absolute maximum ratings.

Table 18-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +0.7	V
Programming voltage	V_{PP}	–0.3 to +13.5	V
Input voltage (except port 6)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (port 6)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: Permanent damage to the chip may result if the absolute maximum ratings shown in table 18-1 are exceeded.

18.2 Electrical Characteristics

18.2.1 DC Characteristics

Table 18-2 lists the DC characteristics.

Table 18-2 DC Characteristics

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$*1, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to 75°C (Regular specifications)
$T_a = -40$ to 85°C (Wide-range specifications)

Item		Symbol	min	typ	max	Unit	Test Conditions
Input high voltage	$\overline{RES}$, MD_2, MD_1, MD_0	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 6		2.2	—	$AV_{CC} + 0.3$	V	
	Other input pins (except port 5)		2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, MD_2, MD_1, MD_0	V_{IL}	−0.3	—	0.5	V	
	Other input pins (except port 5)		−0.3	—	0.8		
Schmitt trigger input voltage	Port 5	V_T^-	1.0	—	2.5	V	
		V_T^+	2.0	—	3.5	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} − 0.5 V
	NMI, MD_2, MD_1, MD_0,		—	—	1.0	µA	
	Port 6		—	—	1.0	µA	V_{in} = 0.5 to AV_{CC} − 0.5 V
Leakage current in 3-state (off state)	Port 7, ports 5 to 1	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} − 0.5 V
Input pull-up MOS current	Ports 3 and 4	$-I_P$	50	—	200	µA	V_{in} = 0 V
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	I_{OH} = −200 µA
			3.5	—	—	V	I_{OH} = −1 mA
Output low voltage	All output pins (except $\overline{RES}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Port 3		—	—	1.0	V	I_{OL} = 8 mA
			—	—	1.2	V	I_{OL} = 10 mA
	$\overline{RES}$		—	—	0.4	V	I_{OL} = 2.6 mA
Input capacitance	$\overline{RES}$	C_{in}	—	—	60	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$		—	—	15	pF	T_a = 25°C

Table 18-2 DC Characteristics (cont)

Item		Symbol	min	typ	max	Unit	Test Conditions
Current dissipation*	Normal operation	Icc	—	20	30	mA	f = 6 MHz
			—	25	40	mA	f = 8 MHz
			—	30	50	mA	f = 10 MHz
			—	12	20	mA	f = 6 MHz
	Sleep mode		—	16	25	mA	f = 8 MHz
			—	20	30	mA	f = 10 MHz
	Standby		—	0.01	5.0	µA	
Analog supply current	During A/D conversion	AIcc	—	0.6	2.0	mA	
	While waiting		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: AVcc must be connected to a power supply even when the A/D converter is not used.
* Current dissipation values assume that V_{IH} min = Vcc – 0.5 V, V_{IL} max = 0.5 V, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 18-3 Allowable Output Current Sink Values

Conditions: Vcc = AVcc = 5.0 V ± 10%, Vss = AVss = 0 V,
T_a = –20 to 75°C (Regular specifications)
T_a = –40 to 85°C (Wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Port 3	I_{OL}	—	—	10	mA
	$\overline{RES}$		—	—	2.6	mA
	Other output pins		—	—	2.0	mA
Allowable output low current sink (total)	Port 3, total of 8 pins	ΣI_{OL}	—	—	40	mA
	Total of all other output pins		—	—	80	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Allowable output high current sink (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 18-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 18-1 and 18-2.

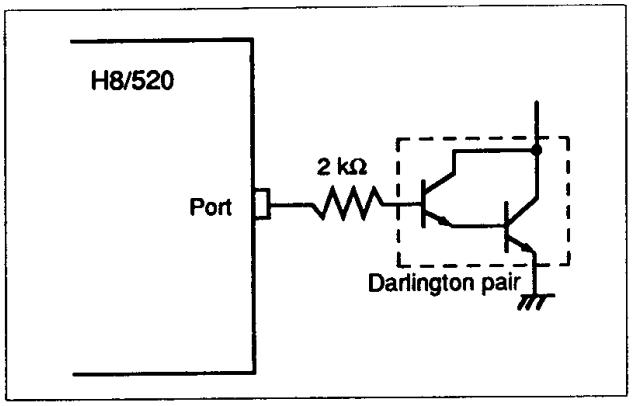

Figure 18-1 Example of Circuit for Driving a Darlington Transistor Pair

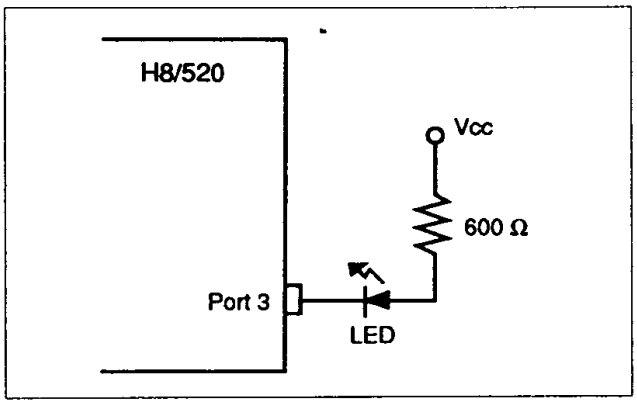

Figure 18-2 Example of Circuit for Driving an LED

18.2.2 AC Characteristics

The AC characteristics of the H8/520 chip are listed in three tables. Bus timing parameters are given in table 18-4, control signal timing parameters in table 18-5, and timing parameters of the on-chip supporting modules in table 18-6. See figure 18-3 for the output load circuit.

Table 18-4 Bus Timing

Conditions: V_{CC} = 5.0 V ± 10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to 75°C (Regular specifications)
T_a = –40 to 85°C (Wide-range specifications)

		6 MHz		8 MHz		10 MHz			Test
Item	Symbol	min	max	min	max	min	max	Unit	Conditions
Clock cycle time	t_{cyc}	166.7	2000	125	2000	100	2000	ns	See figure 18-4
Clock pulse width low	t_{CL}	65	—	45	—	35	—	ns	
Clock pulse width high	t_{CH}	65	—	45	—	35	—	ns	
Clock rise time	t_{Cr}	—	15	—	15	—	15	ns	
Clock fall time	t_{Cf}	—	15	—	15	—	15	ns	
Address delay time	t_{AD}	—	70	—	60	—	55	ns	
Address hold time	t_{AH}	30	—	25	—	20	—	ns	
$\overline{RD}$ delay time 1	t_{RDD1}	—	70	—	60	—	40	ns	
$\overline{RD}$ delay time 2	t_{RDD2}	—	70	—	60	—	50	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	70	—	60	—	50	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	70	—	60	—	50	ns	
Write data strobe pulse width	t_{DSWW}	200	—	150	—	120	—	ns	
Address setup time 1	t_{AS1}	25	—	20	—	15	—	ns	
Address setup time 2	t_{AS2}	105	—	80	—	65	—	ns	See figure 18-4
Read data setup time	t_{RDS}	60	—	50	—	40	—	ns	

Table 18-4 Bus Timing (cont)

Item	Symbol	6 MHz min	6 MHz max	8 MHz min	8 MHz max	10 MHz min	10 MHz max	Unit	Test Conditions
Read data hold time	t_{RDH}	0	—	0	—	0	—	ns	See figure 18-4
Read data access time	t_{ACC}	—	280	—	190	—	160	ns	
Write data delay time	t_{WDD}	—	70	—	60	—	60	ns	
Write data setup time	t_{WDS}	30	—	15	—	10	—	ns	
Write data hold time	t_{WDH}	30	—	25	—	20	—	ns	
Wait setup time	t_{WTS}	40	—	40	—	40	—	ns	See figure 18-5
Wait hold time	t_{WTH}	10	—	10	—	10	—	ns	

Table 18-5 Control Signal Timing

Conditions: V_{CC} = 5.0 V ± 10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to 75°C (Regular specifications)
T_a = –40 to 85°C (Wide-range specifications)

Item	Symbol	6 MHz min	6 MHz max	8 MHz min	8 MHz max	10 MHz min	10 MHz max	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	200	—	ns	See figure 18-6
$\overline{RES}$ pulse width 1*	t_{RESW1}	6.0	—	6.0	—	6.0	—	t_{cyc}	
$\overline{RES}$ pulse width 2*	t_{RESW2}	520	—	520	—	520	—	t_{cyc}	
$\overline{RES}$ output delay time	t_{RESD}	—	100	—	100	—	100	ns	See figure 18-7
$\overline{RES}$ output pulse width	t_{RESOW}	132	—	132	—	132	—	t_{cyc}	
Mode programming setup time	t_{MDS}	4.0	—	4.0	—	4.0	—	t_{cyc}	See figure 18-6
$\overline{NMI}$ setup time	t_{NMIS}	150	—	150	—	150	—	ns	See figure 18-8
$\overline{NMI}$ hold time	t_{NMIH}	10	—	10	—	10	—	ns	
$\overline{IRQ_0}$ setup time	t_{IRQ0S}	50	—	50	—	50	—	ns	
$\overline{IRQ_1}$ to $\overline{IRQ_7}$ setup time	t_{IRQ1S}	50	—	50	—	50	—	ns	
$\overline{IRQ_1}$ to $\overline{IRQ_7}$ hold time	t_{IRQ1H}	10	—	10	—	10	—	ns	
$\overline{NMI}$ pulse width (for recovery from software standby mode)	t_{NMIW}	200	—	200	—	200	—	ns	
A/D trigger setup time	t_{TRGS}	50	—	50	—	50	—	ns	See figure 18-18
A/D trigger hold time	t_{TRGH}	10	—	10	—	10	—	ns	
Crystal oscillator settling time (reset)	t_{OSC1}	20	—	20	—	20	—	ms	See figure 18-9
Crystal oscillator settling time (software standby)	t_{OSC2}	10	—	10	—	10	—	ms	See figure 17-1

Note: * t_{RESW2} applies when the RSTOE bit in the reset control/status register (RSTCR) is set to 1. t_{RESW1} applies when RSTOE is cleared to 0. t_{RESW1} also applies at power-up.

Table 18-6 Timing Conditions of On-Chip Supporting Modules

Conditions: V_{CC} = 5.0 V ± 10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to 75°C (Regular specifications)
T_a = –40 to 85°C (Wide-range specifications)

Item			Symbol	6 MHz min	6 MHz max	8 MHz min	8 MHz max	10 MHz min	10 MHz max	Unit	Test Conditions
FRT	Timer output delay time		t_{FTOD}	—	100	—	100	—	100	ns	See figure 18-11
	Timer input setup time		t_{FTIS}	50	—	50	—	50	—	ns	
	Timer clock input setup time		t_{FTCS}	50	—	50	—	50	—	ns	See figure 18-12
	Timer clock pulse width		t_{FTCW}	1.5	—	1.5	—	1.5	—	t_{cyc}	
TMR	Timer output delay time		t_{TMOD}	—	100	—	100	—	100	ns	See figure 18-13
	Timer clock input setup time		t_{TMCS}	50	—	50	—	50	—	ns	See figure 18-14
	Timer clock pulse width		t_{TMCW}	1.5	—	1.5	—	1.5	—	t_{cyc}	
	Timer reset input setup time		t_{TMRS}	50	—	50	—	50	—	ns	See figure 18-15
SCI	Input clock cycle	(Async)	t_{Scyc}	2	—	2	—	2	—	t_{cyc}	See figure 18-16
		(Sync)		4	—	4	—	4	—	t_{cyc}	
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	
	Transmit data delay time	(Sync)	t_{TXD}	—	100	—	100	—	100	ns	See figure 18-17
	Receive data setup time	(Sync)	t_{RXS}	100	—	100	—	100	—	ns	
	Receive data hold time	(Sync)	t_{RXH}	—	100	—	100	—	100	ns	
Ports	Output data delay time		t_{PWD}	—	100	—	100	—	100	ns	See figure 18-10
	Input data setup time		t_{PRS}	50	—	50	—	50	—	ns	
	Input data hold time		t_{PRH}	50	—	50	—	50	—	ns	

- **Measurement Conditions for AC Characteristics**

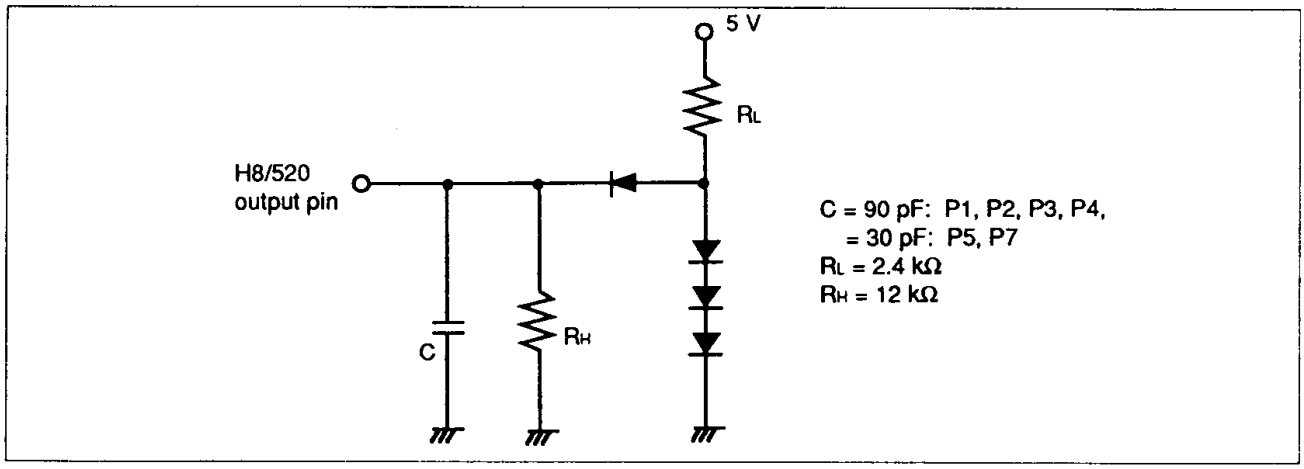

Figure 18-3 Output Load Circuit

18.2.3 A/D Converter Characteristics

Table 18-7 lists the characteristics of the on-chip A/D converter.

Table 18-7 (1) A/D Converter Characteristics

Conditions: V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V,
T_a = –40 to 85°C (Wide-range specifications)

	6 MHz			8 MHz			10 MHz			
Item	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±2.0	—	—	±2.0	—	—	±2.0	LSB
Offset error	—	—	±2.0	—	—	±2.0	—	—	±2.0	LSB
Full-scale error	—	—	±2.0	—	—	±2.0	—	—	±2.0	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±2.5	—	—	±2.5	—	—	±2.5	LSB

Table 18-7 (2) A/D Converter Characteristics

Conditions: V_{CC} = AV_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to 75°C (Regular specifications)

	6 MHz			8 MHz			10 MHz			
Item	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±3.5	—	—	±3.5	—	—	±3.5	LSB
Offset error	—	—	±3.5	—	—	±3.5	—	—	±3.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	—	—	±3.5	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	—	—	±4.0	LSB

18.3 MCU Operational Timing

This section provides the following timing charts:

18.3.1 Bus Timing

1. Basic Bus Cycle (without Wait States) in Expanded Modes

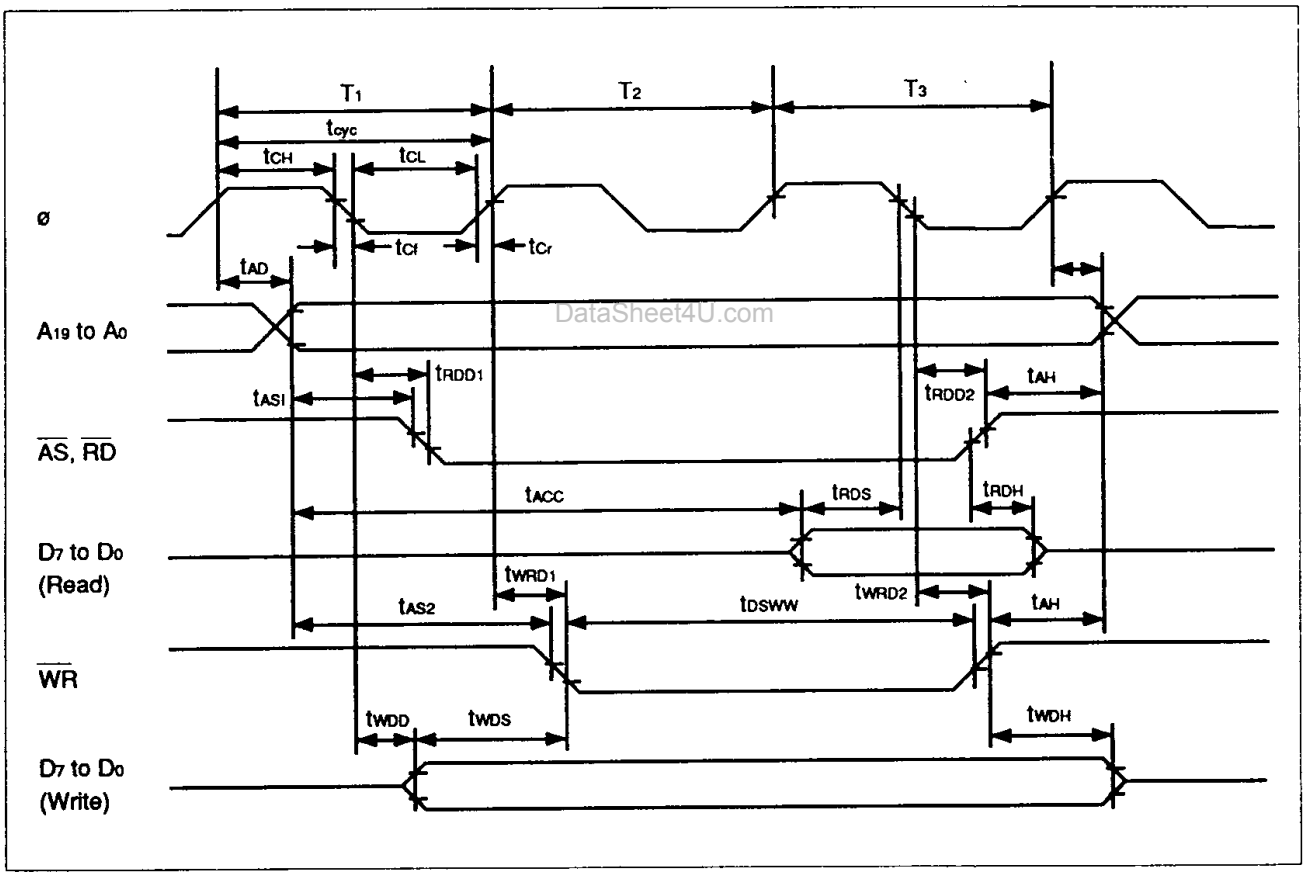

Figure 18-4 Basic Bus Cycle (without Wait States) in Expanded Modes

2. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

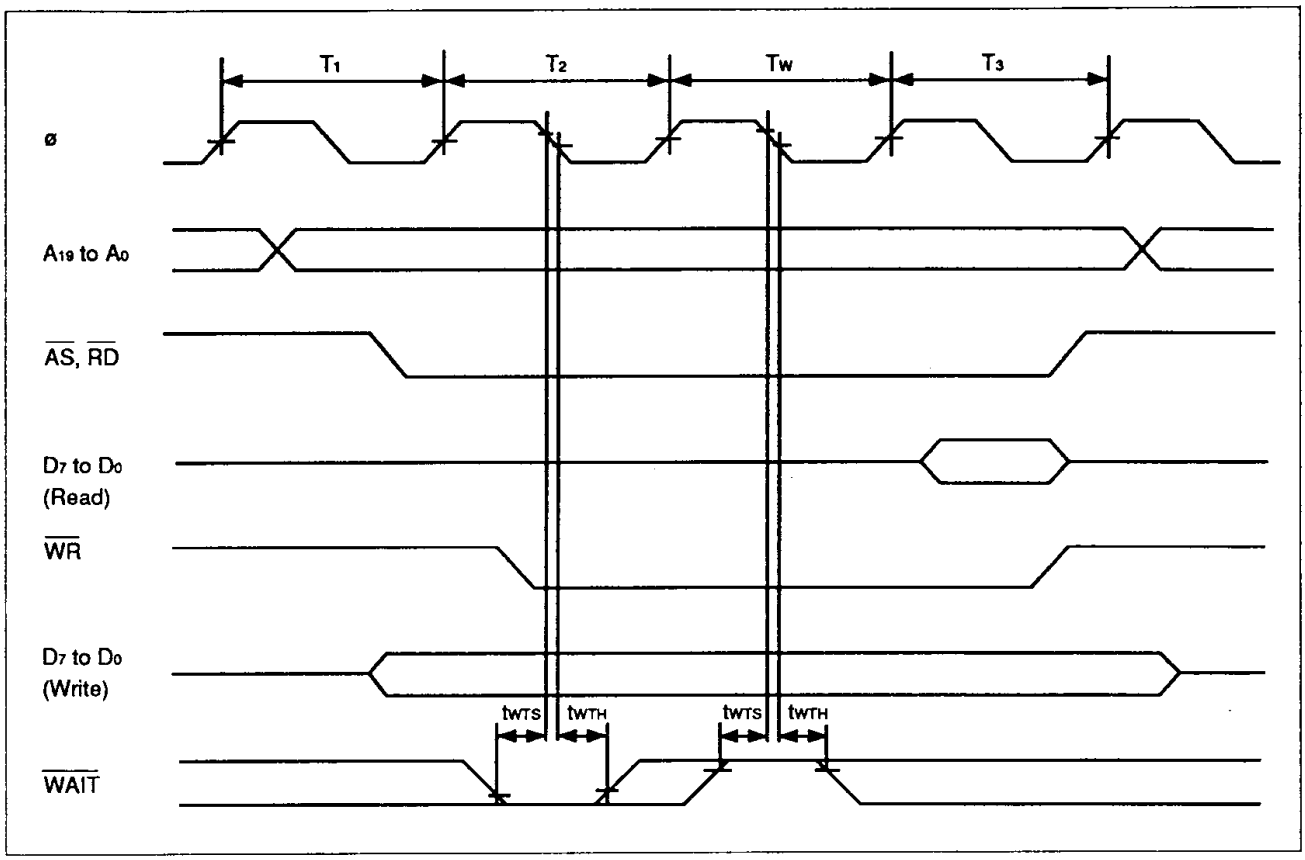

Figure 18-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes

18.3.2 Control Signal Timing

1. Reset Input Timing

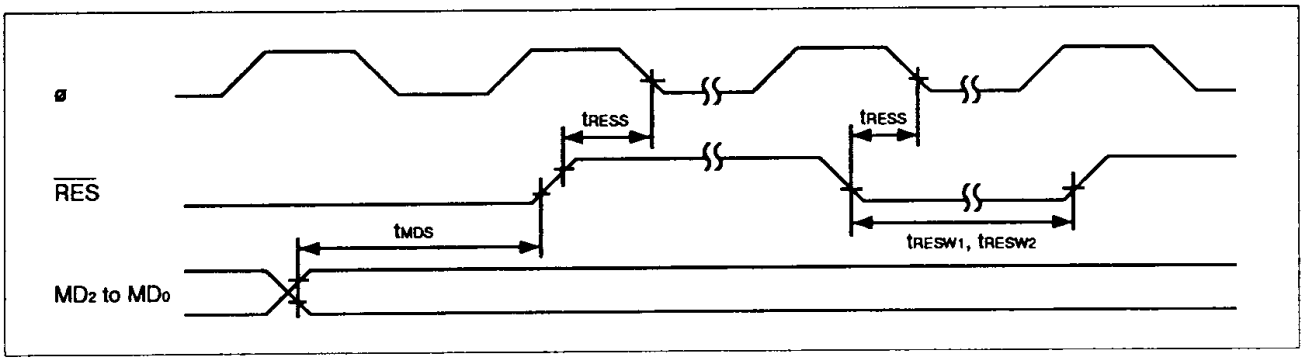

Figure 18-6 Reset Input Timing

2. Reset Output Timing

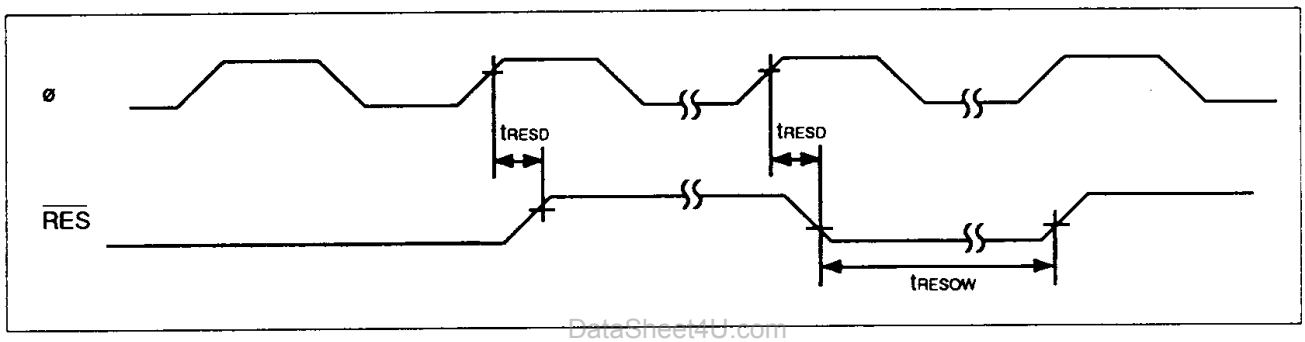

Figure 18-7 Reset Output Timing

3. Interrupt Input Timing

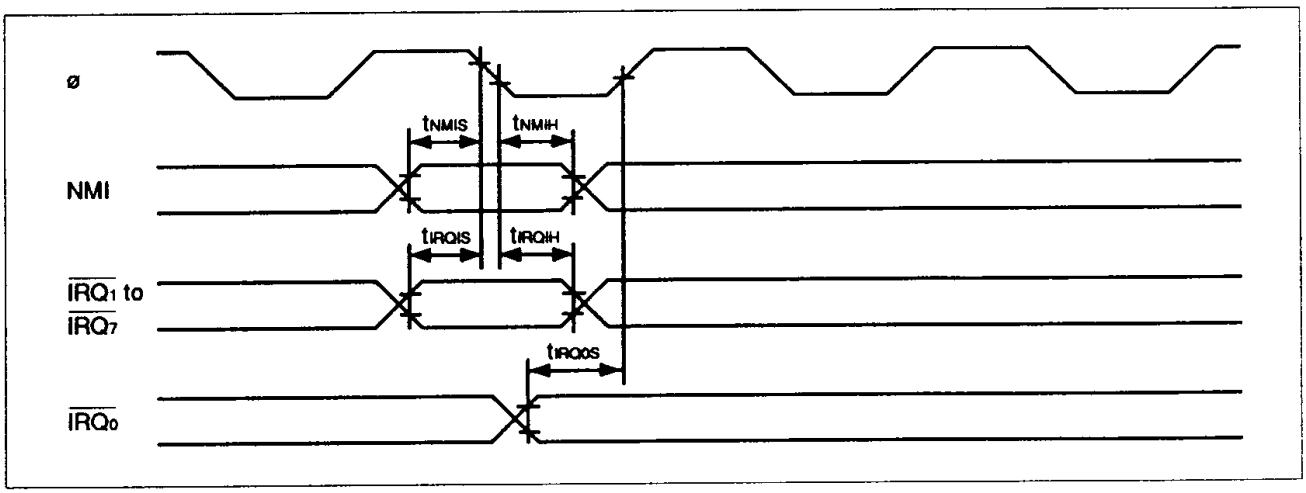

Figure 18-8 Interrupt Input Timing

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18.3.3 Clock Oscillator Stabilization Timing

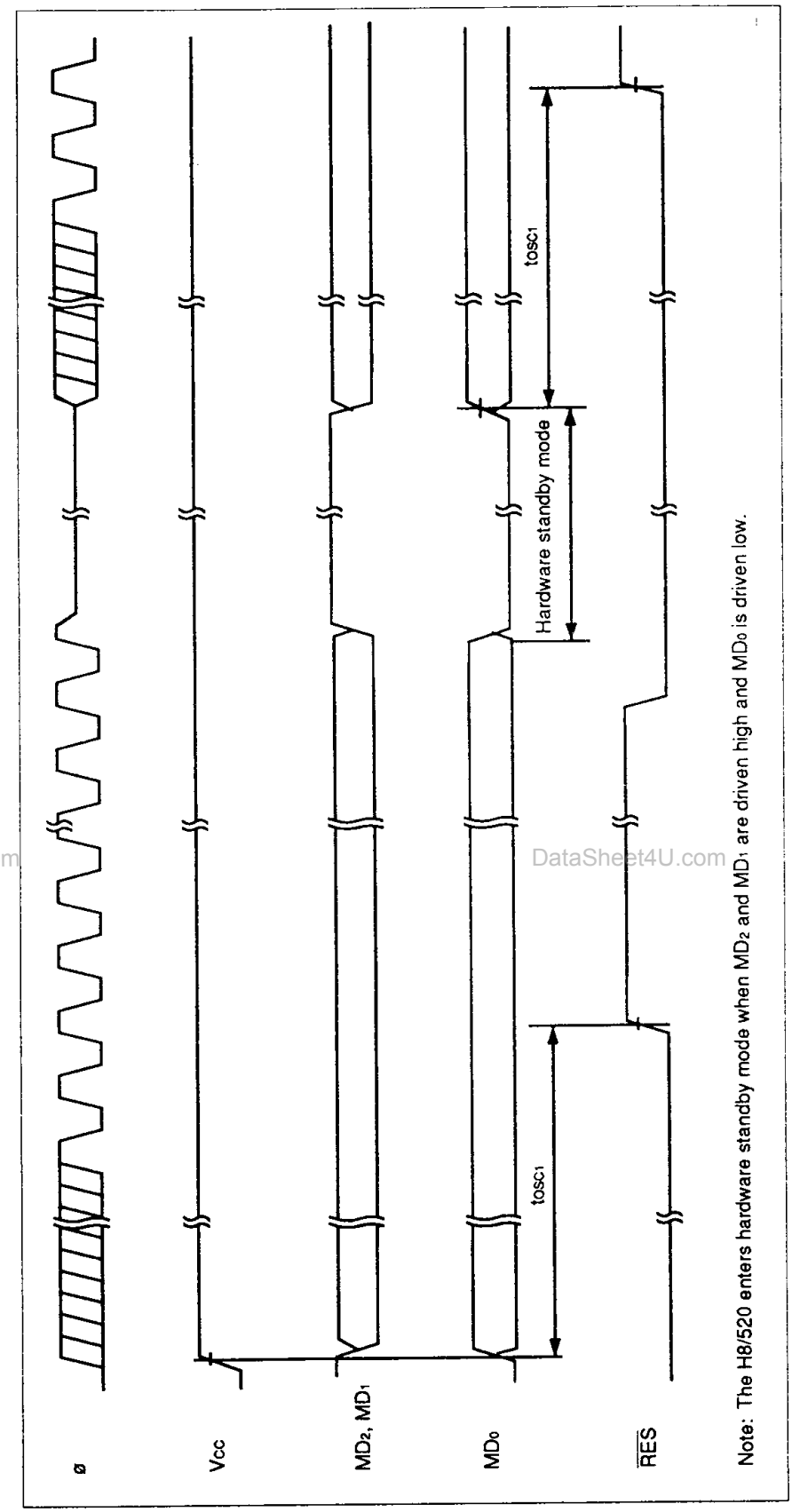

Figure 18-9 Clock Oscillator Stabilization

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18.3.4 I/O Port Timing

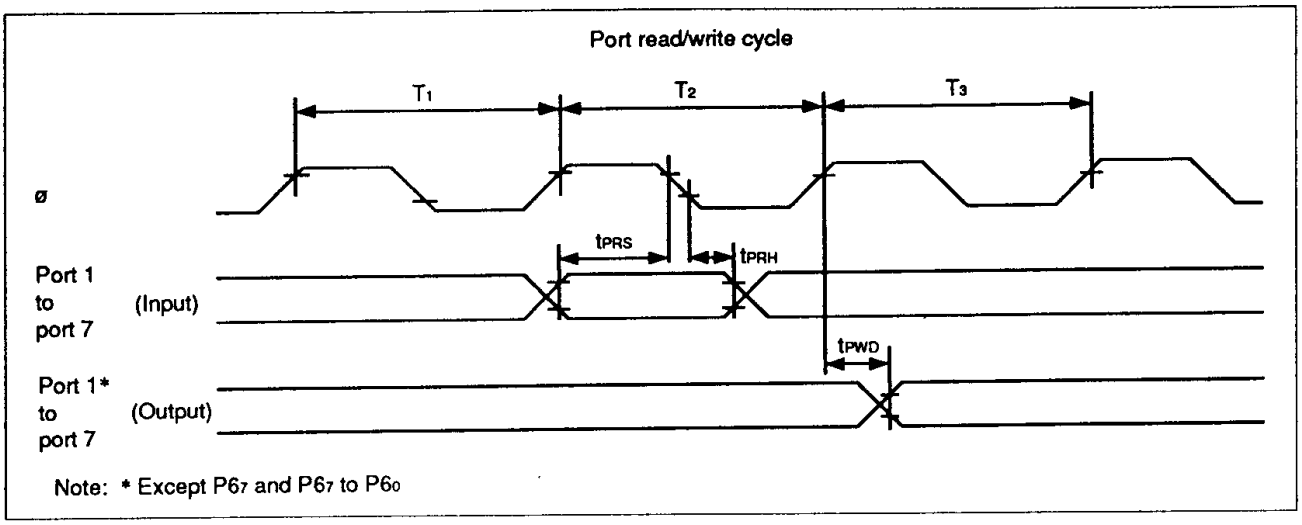

Figure 18-10 I/O Port Input/Output Timing

18.3.5 16-Bit Free-Running Timer Timing

1. Free-Running Timer Input/Output Timing

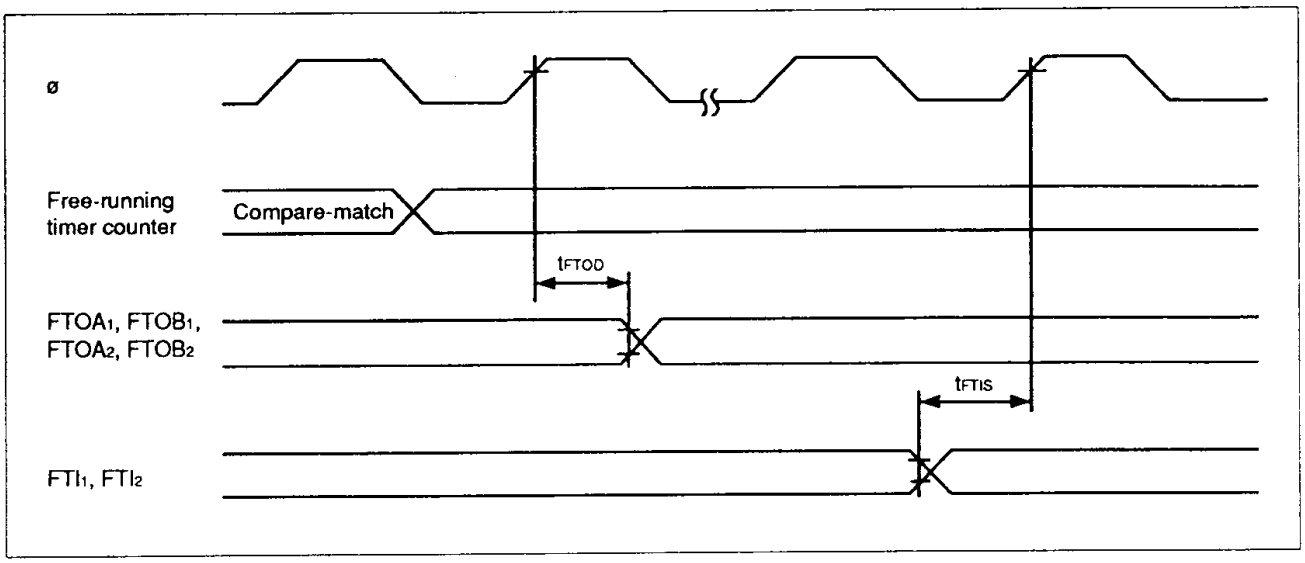

Figure 18-11 Free-Running Timer Input/Output Timing

2. External Clock Input Timing for Free-Running Timers

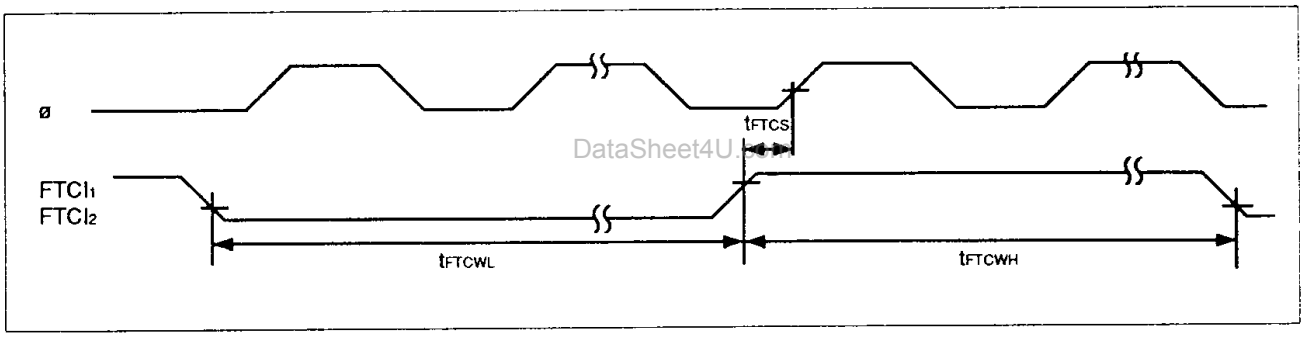

Figure 18-12 External Clock Input Timing for Free-Running Timers

18.3.6 8-Bit Timer Timing

1. 8-Bit Timer Output Timing

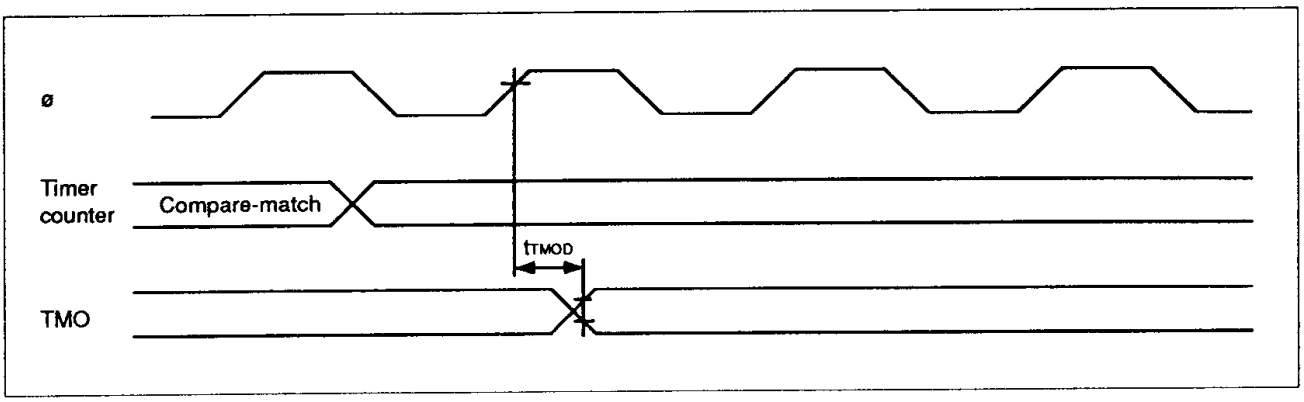

Figure 18-13 8-Bit Timer Output Timing

2. 8-Bit Timer Clock Input Timing

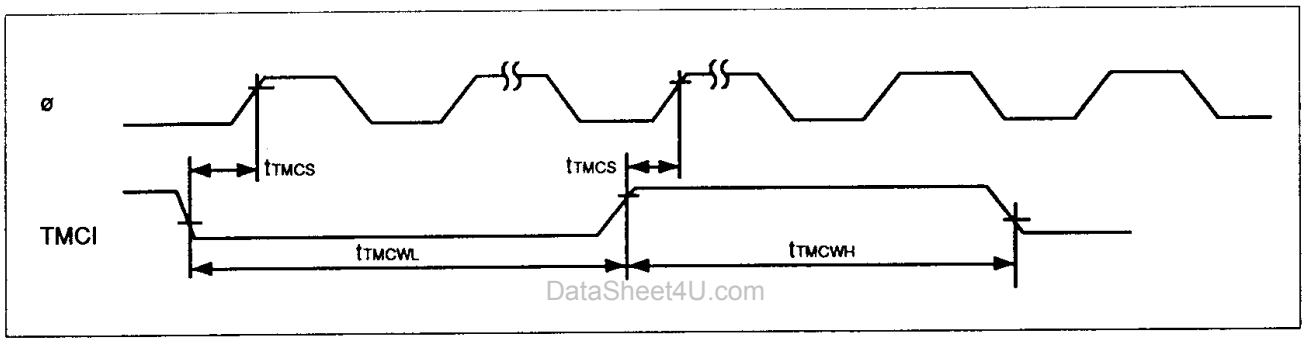

Figure 18-14 8-Bit Timer Clock Input Timing

3. 8-Bit Timer Reset Input Timing

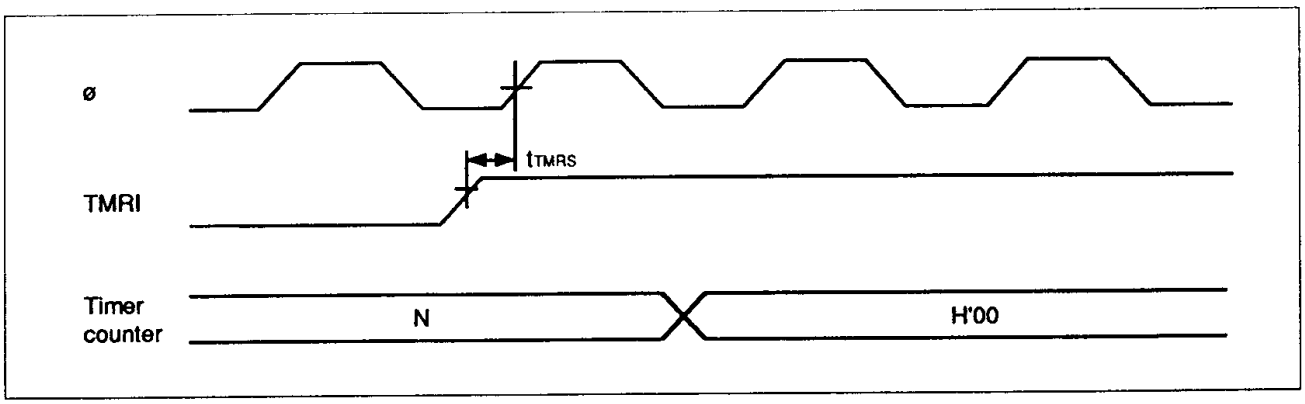

Figure 18-15 8-Bit Timer Reset Input Timing

18.3.7 Serial Communication Interface Timing

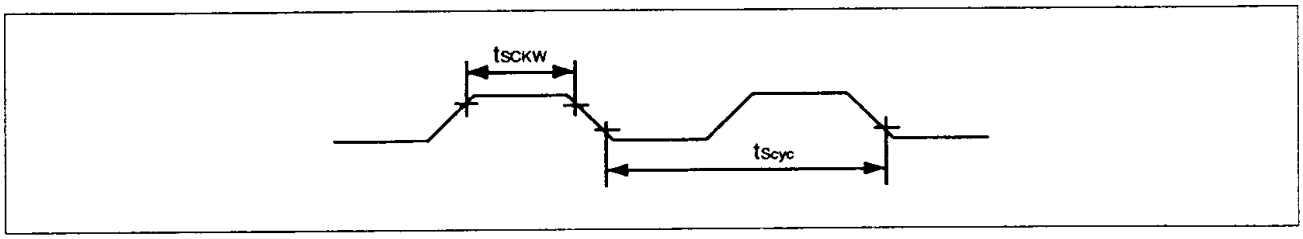

Figure 18-16 SCI Input Clock Timing

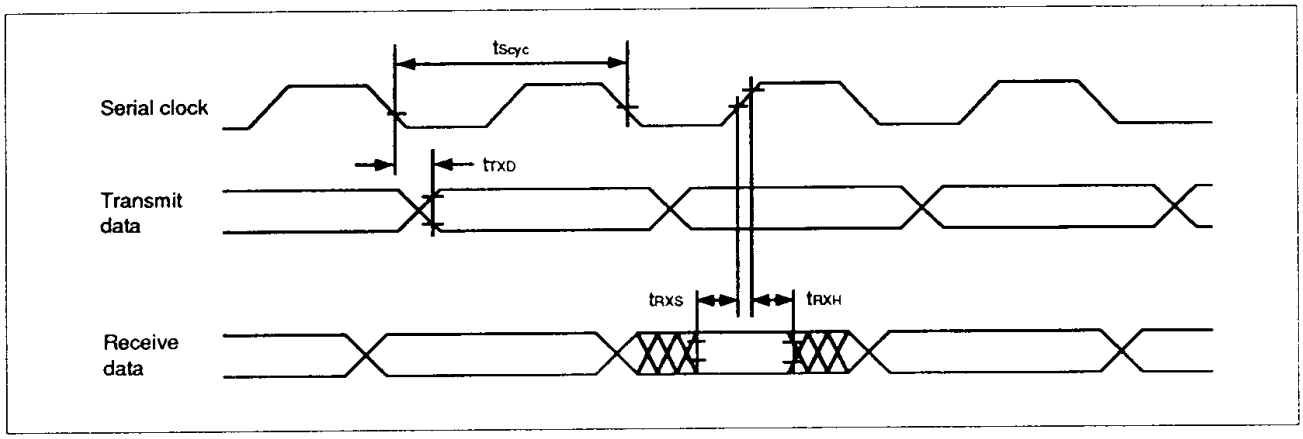

Figure 18-17 SCI Input/Output Timing (Synchronous Mode)

18.3.8 A/D External Trigger Input Timing

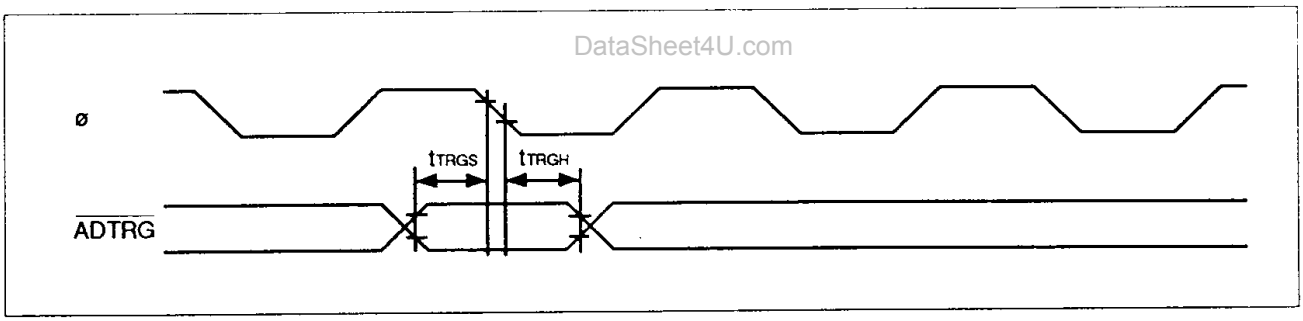

Figure 18-18 A/D External Trigger Input Timing

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Appendix F Package Dimensions

Figure F-1 shows the dimensions of the DC-64S package. Figure F-2 shows the dimensions of the DP-64S package. Figure F-3 shows the dimensions of the FP-64A package. Figure F-4 shows the dimensions of the CP-68 package.

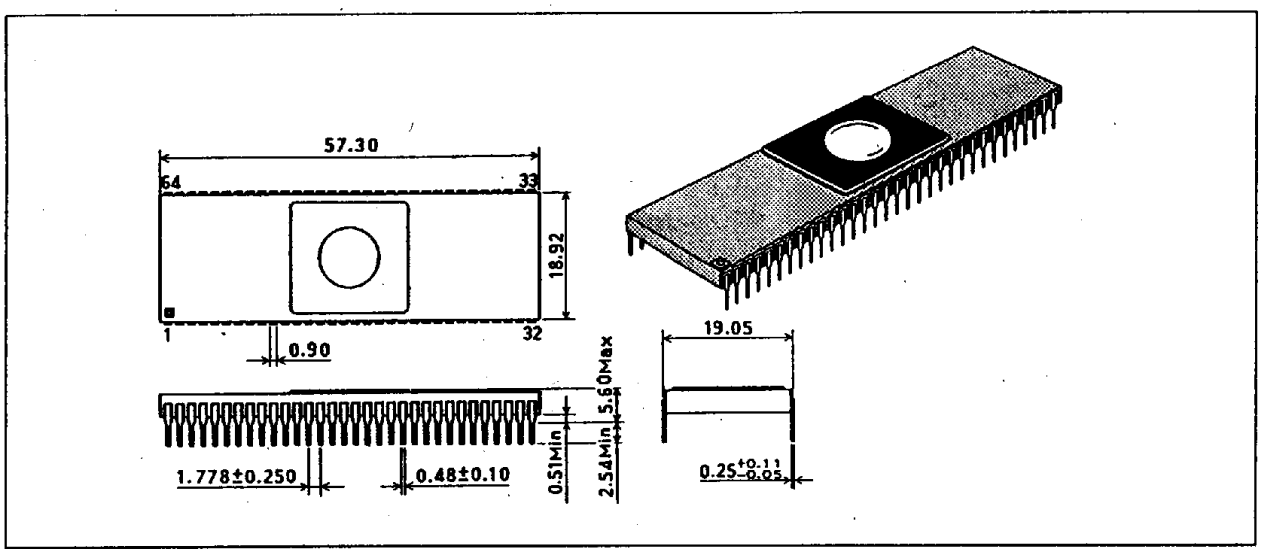

Figure F-1 Package Dimensions (DC-64S)

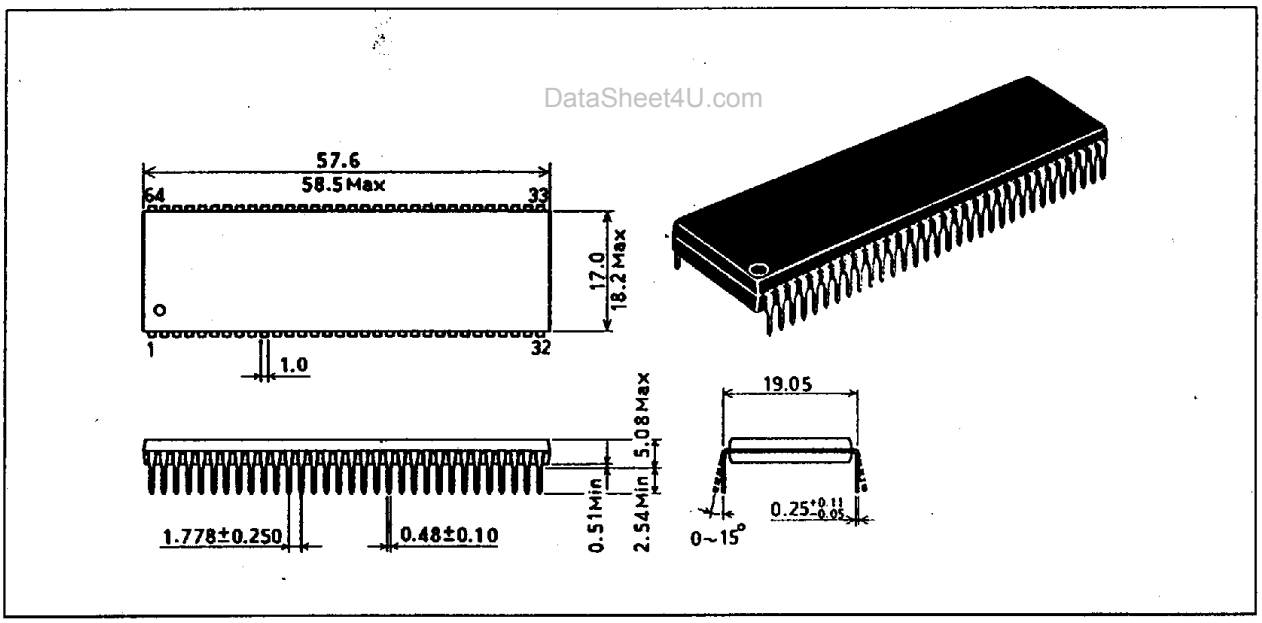

Figure F-2 Package Dimensions (DP-64S)

T-90-20

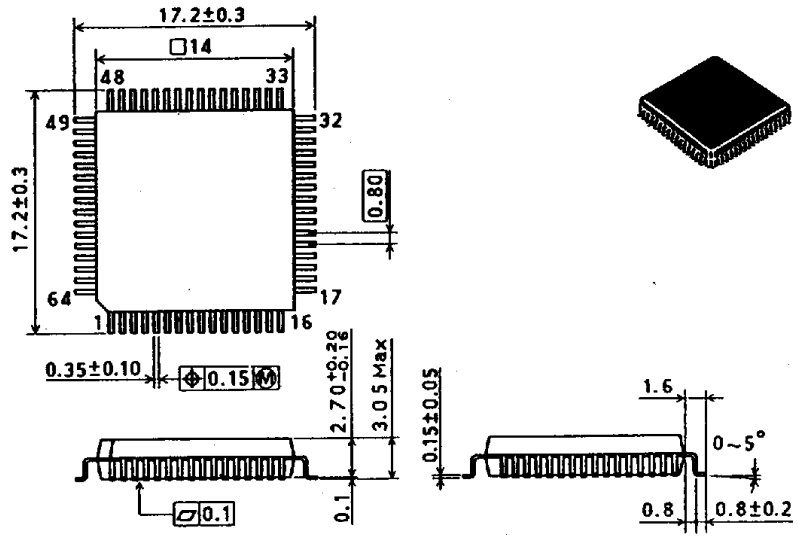

Figure F-3 Package Dimensions (FP-64A)

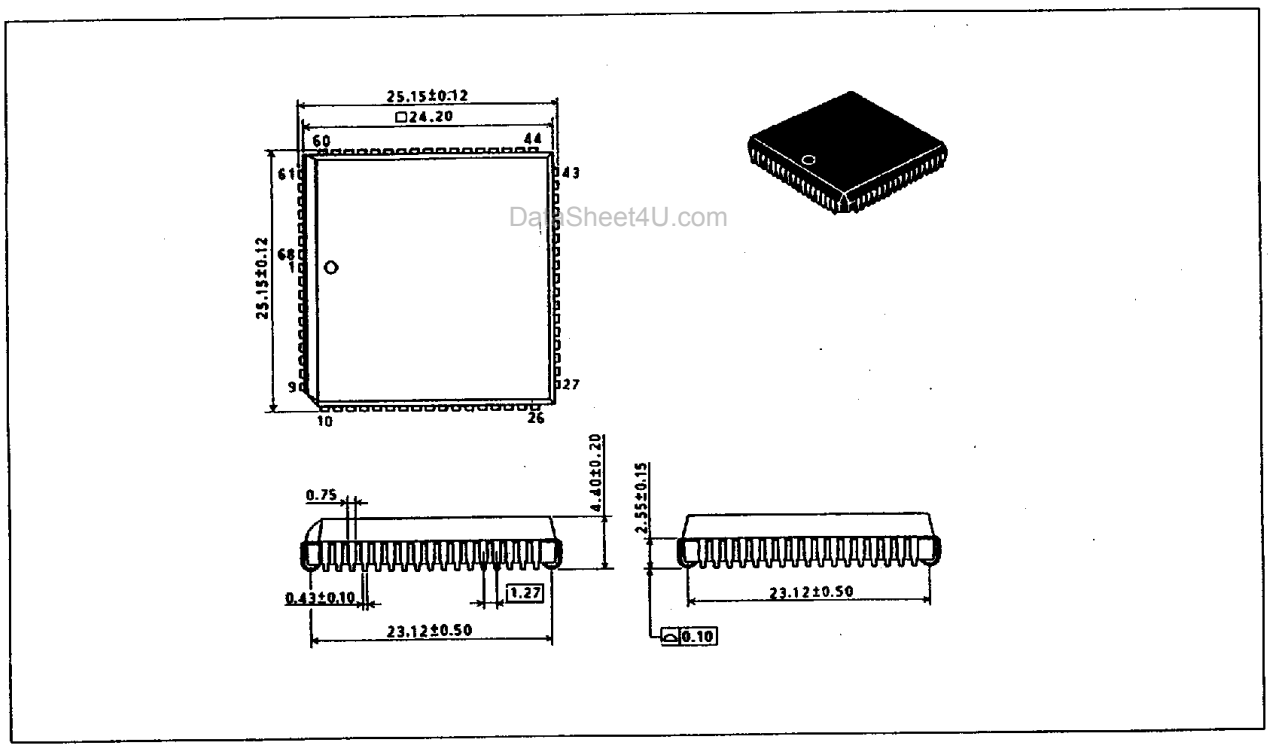

Figure F-4 Package Dimensions (CP-68)