HD66107T

(LCD Driver for High Voltage)

HITACHI

Description

The HD66107T is a multi-output, high duty ratio LCD driver used for large capacity dot matrix LCD panels. It consists of 160 LCD drive circuits with a display duty ratio up to 1/480: the seven HD66107Ts can drive a 640 × 480 dots LCD panel. Moreover, the LCD driver enables interfaces with various LCD controllers due to a built-in automatic generator of chip enable signals. Use of the HD66107T can help reduce the cost of an LCD-panel configuration, since it reduces the number of LCD drivers, compared with use of the HD61104 and HD61105.

Features

- Column and row driver
- 160 or 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit and 8-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby mode
- Recommended LCD controller LSIs: HD63645F, HD64645F, and HD64646FS (LCTC), HD66840/HD66841 (LVIC), HD66850 (CLINE)
- Power supply voltage
  - — Internal logic: +5 V ± 10%
  - — LCD drive circuit: 14.0 to 37.0 V
- Operation frequency: 8.0 MHz (max.)
- CMOS process
- 192-pin TCP

Ordering Information

Type No.	Number of Outputs	Outer Lead Pitch (µm)	Material of Tape*2	Note
HD66107T11	160	180	Kapton	
HD66107T24	160	180	Upilex	
HD66107T12	160	250	Kapton	
HD66107T00	160	280	Kapton	
HD66107T01	80	280	Kapton	12 perforated holes
HD66107T25	80	280	Kapton	8 perforated holes

Notes: 1. “Kapton” is a trademark of Dupont, Ltd.
“Upilex” is a trademark of Ube Industries, Ltd.
2. The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Description

Power Supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuits. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}: V_1 to V_4 supply power for driving an LCD (figure 1).

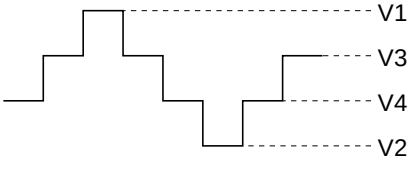
Control Signal

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

Table 1 Pin Function

Symbol	Pin No.	Pin Name	Input/Output
V_{CC}	167	V_{CC}	
GND	161, 186, 187	Ground	
V_{LCD}	166, 192	V_{LCD}	
V1L, R V2L, R V3L, R V4L, R	191, 165 188, 162 190, 164 189, 163	V1L, V1R V2L, V2R V3L, V3R V4L, V4R	
CL1	183	Clock 1	Input
CL2	184	Clock 2	Input
M	182	M	Input
D_0–D_7	174–181	DATA0–DATA7	Input
SHL	172	Shift left	Input
CH2	171	Channel 2	Input
BS	173	Bus select	Input
TEST	185	TEST	Input
Y1–Y160	1–160	Y1–Y160	Output
$\overline{E}$	169	Enable	Input
$\overline{CAR}$	168	Carry	Output
CH1	170	Channel	Input



V1, V2: Selected level
V3, V4: Nonselected level

Figure 1 Power Supply for Driving an LCD

M: M changes LCD drive outputs to AC.

D_0–D_7: D_0–D_7 input display data for the column driver (table 2).

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{E}$ connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}).

$\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66107Ts are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip devices are columns when CH1 = V_{CC}, and rows when CH1 = GND.

CH2: CH2 selects the number of output data bits. The number of output data bits is 160 when CH2 = GND, and 80 when CH2 = V_{CC}.

BS: BS selects the number of input data bits. When BS = V_{CC}, the chip latches 8-bits data. When BS = GND, the chip latches 4-bits data via D_0 to D_3. Fix D_4 through D_7 to GND.

TEST: Used for testing. Fixed to GND, otherwise.

Table 2 Relation between Display Data and LCD State

Display Data	LCD Output	LCD
1 (= high level)	V1L, R/V2L, R	On
0 (= low level)	Nonselected level	Off

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI Is Used as Row Driver)

SHL	Shift Direction of Shift Register					Scan Direction of Selected Line				
V_{CC}	E→	1→	2→	3→	4----------→160	Y1→	Y2→	Y3→	Y4	----------→Y160
GND	E→	160→	159→	158→	157----------→1	Y160→Y159→Y158→Y157				----------→Y1

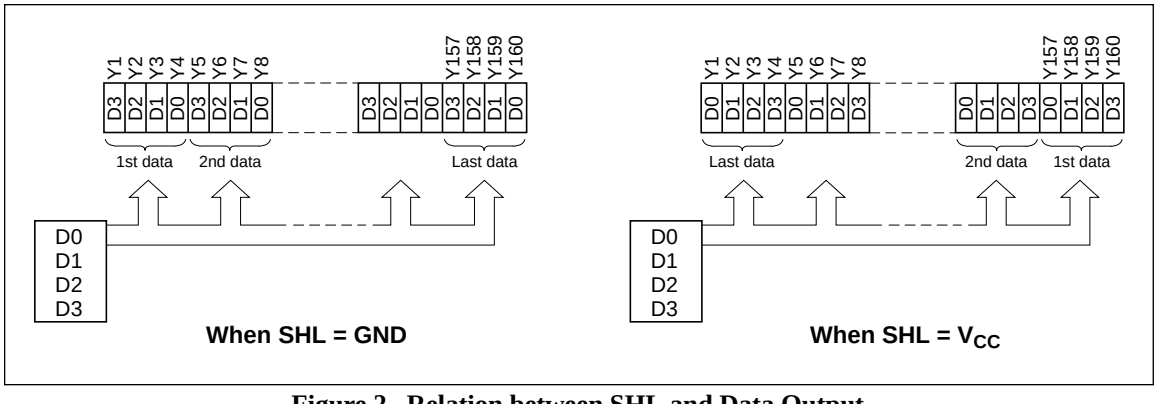


Figure 2 Relation between SHL and Data Output

LCD Drive Interface

Y1–Y160: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, V_4—according to the combination of M and display data (figure 3).

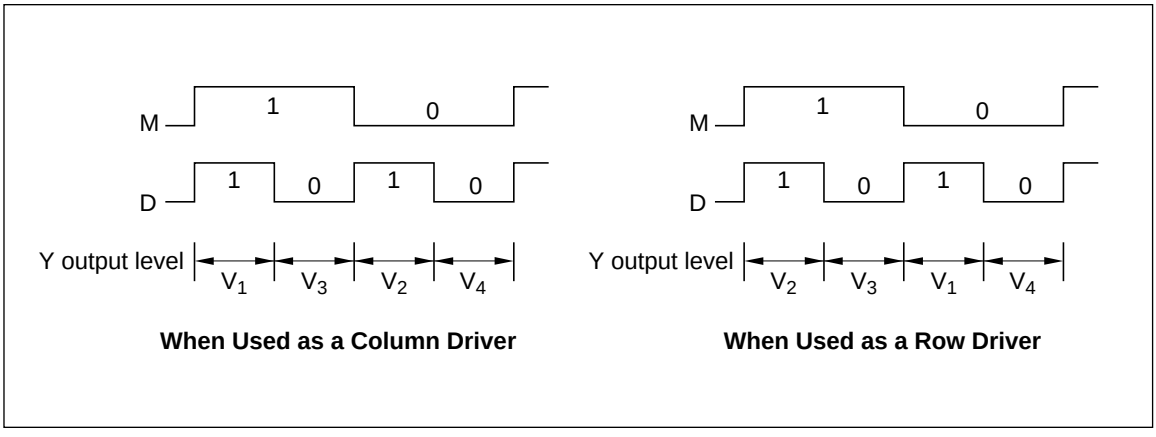
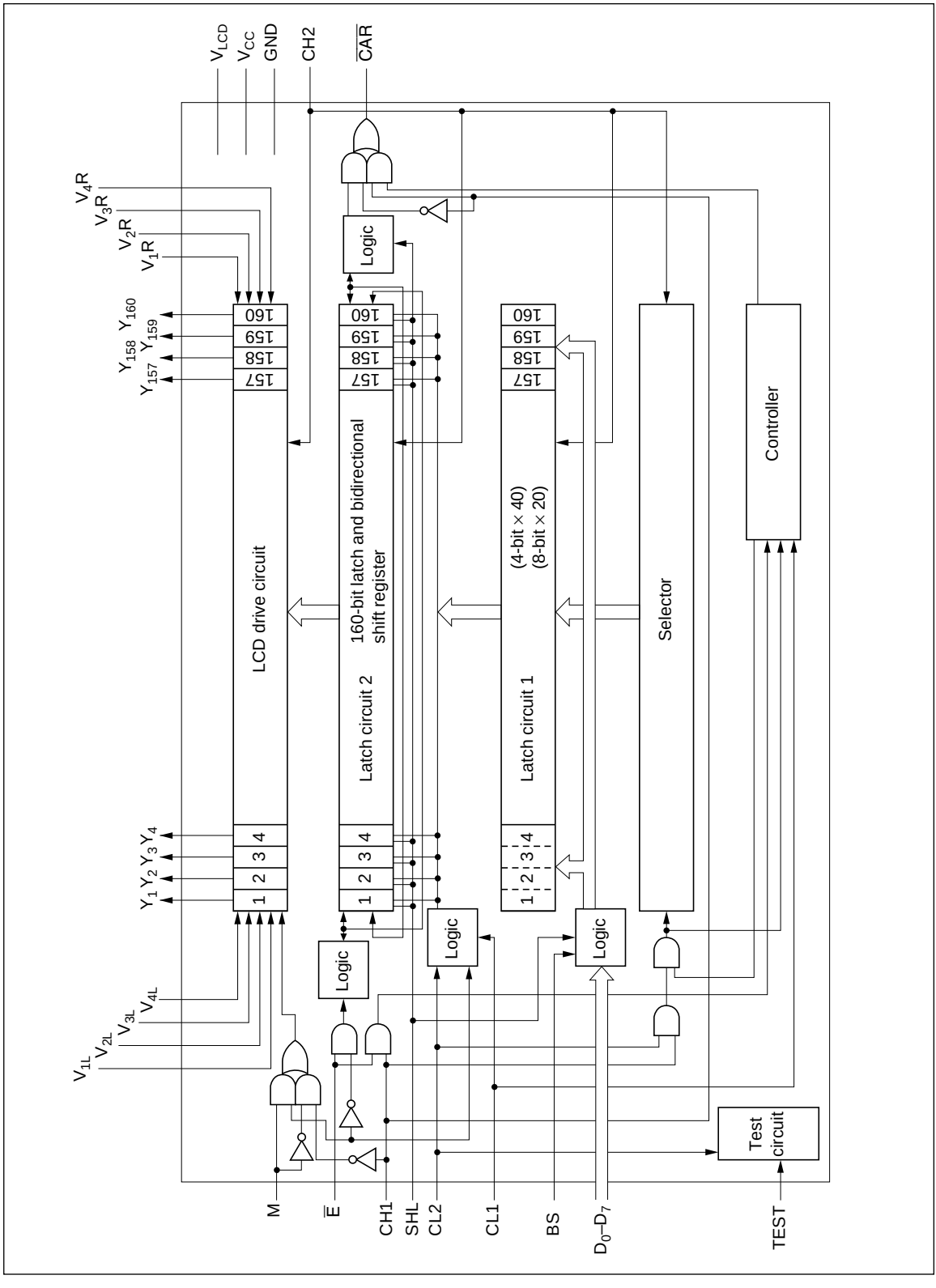


Figure 3 Selection of LCD Driver Output Level

Block Diagram



Function

LCD Drive Circuits

The LCD drive circuits generate four levels of voltages—V_1, V_2, V_3, and V_4—for driving an LCD. They select and transfer one of the four levels to the output circuit according to the combination of M and the data in the latch circuit 2.

Latch Circuit 2

Latch circuit 2 is used as a 160-bit latch circuit during column driving. Latch circuit 2 latches data input from latch circuit 1 at the falling edge of CL1 and outputs latched data to the drive circuits.

In the case of row driving, latch circuit 2 is used as a 160-bit bidirectional shift register. Data input from $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted in input order from bit 1 to bit 160 of the shift register. When SHL = GND, data is shifted from bit 160 to bit 1 of the register. Moreover, this latch circuit can be used as an 80-bit shift register. In this case, Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Latch Circuit 1

Latch circuit 1 consists of twenty 8-bit parallel data latch circuits. It latches data D_0 through D_7 at the falling edge of CL2 during column driving. The selector signals specify which 8-bit circuit latches data. Moreover, this circuit can be used as forty 4-bit parallel data latch circuits by switching BS, in which case the circuit latches data D_0 through D_3. Moreover, this latch circuit can be used as an 80-bit shift register. In this case Y_{41} through Y_{120} are enabled, while the other bits remain unchanged.

Selector

The selector consists of a 6-bit up and down counter and a decoder. During column driving it generates a latch signal for latch circuit 1, incrementing the counter at the falling edge of CL2.

Controller

This controller is enabled during column driving. It provides a power-down function which detects completion of data latch and stops LSI operations.

Moreover, the controller automatically generates a chip enable signal ($\overline{CAR}$) which starts next-stage data latching.

Test Circuit

The test circuit divides the external clock and generates test signals.

Fundamental Operations

Column Driving (1)

- CH2 = GND (160-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

The HD66107T starts data latch when $\overline{E}$ is at low level. In this case, 8-bit parallel data is latched at the falling edge of CL2. When 160-bit data latch is completed, the HD66107T automatically stops and enters standby mode and $\overline{CAR}$ is goes to low level. If $\overline{CAR}$ is connected with $\overline{E}$ of the next-stage LSI, this next-stage LSI is activated when $\overline{CAR}$ of the previous LSI goes low.

Data is output at the falling edge of CL1. When SHL = GND, data d_1 is output to pin Y_1 and d_{160} to Y_{160}. On the other hand, when SHL = V_{CC}, data d_{160} is output to pin Y_1 and d_1 to Y_{160}. The output level is selected from among V_1–V_4 according to the combination of display data and alternating signal M. See figure 4.

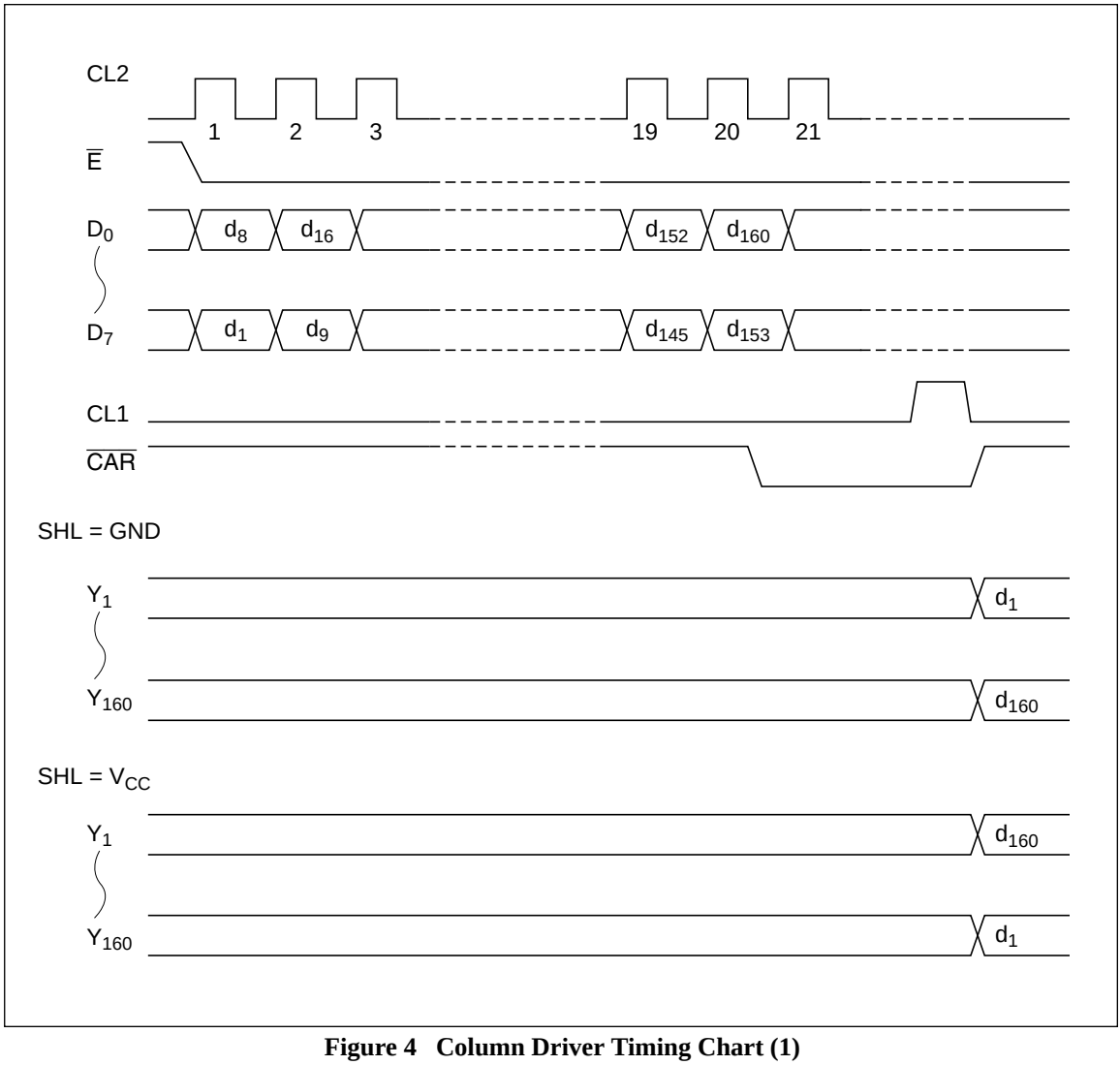


Figure 4 Column Driver Timing Chart (1)

Column Driving (2)

- CH2 = GND (160-bit data output mode)
- BS = GND (4-bit data latch mode)

4-bit display data (D_0–D_3) is latched at the falling edge of CL2. Other operations are performed in the same way as described in "Column Driving (1)". See figure 5.

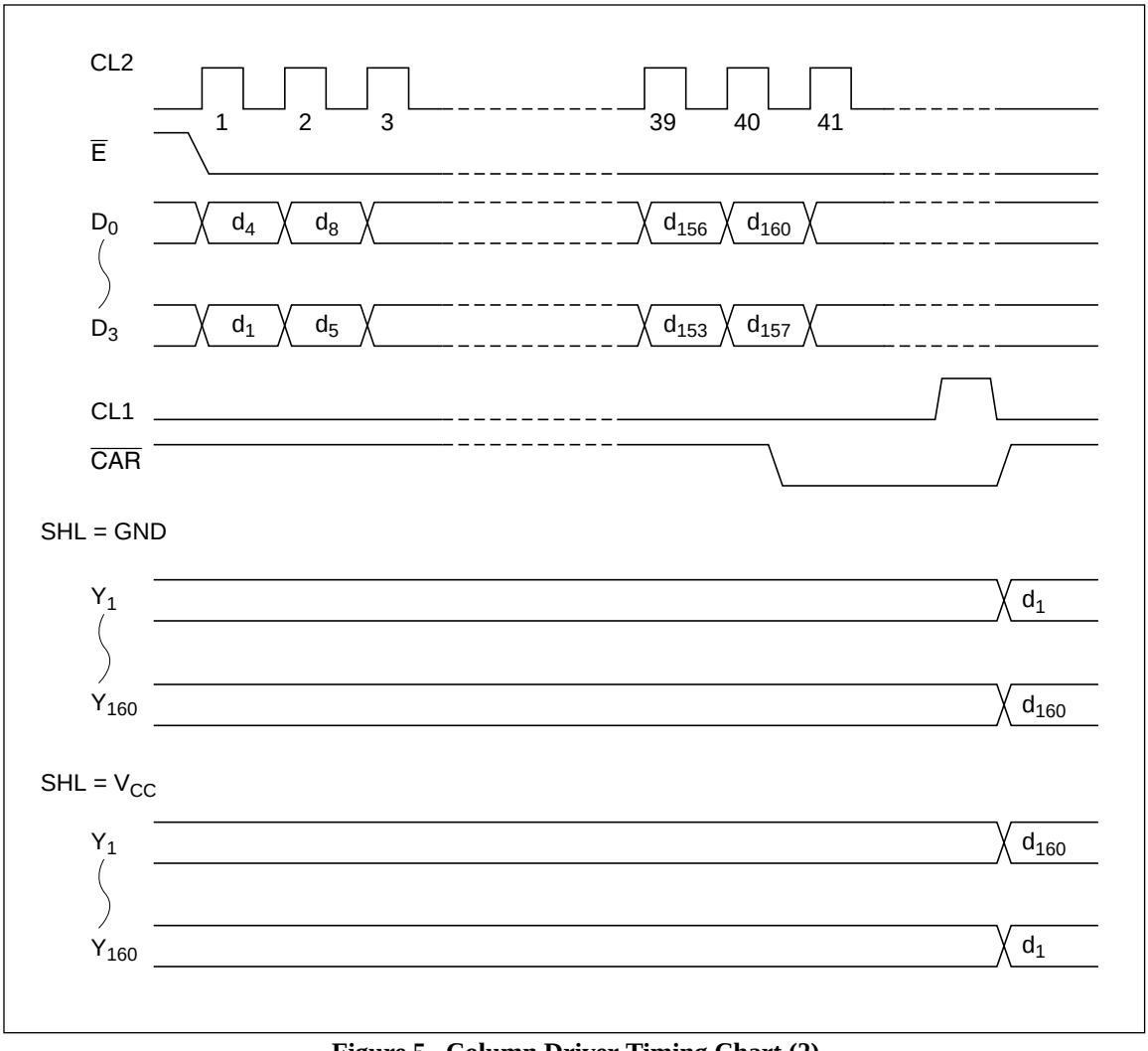


Figure 5 Column Driver Timing Chart (2)

Column Driving (3)

- CH2 = V_{CC} (80-bit data output mode)
- BS = V_{CC} (8-bit data latch mode)

When CH2 is high (V_{CC}), the HD66107T can be used as an 80-bit column driver. In this case, Y_{41} through Y_{120} are enabled, the states of Y_1 through Y_{40} and Y_{121} through Y_{160} remain unchanged.

When SHL = GND, data d_1 is output to pin Y_{41} and d_{80} is output to Y_{120}. Conversely, when SHL = V_{CC}, data d_{80} is output to Y_{41} and d_1 is output to Y_{120}. See figure 6.

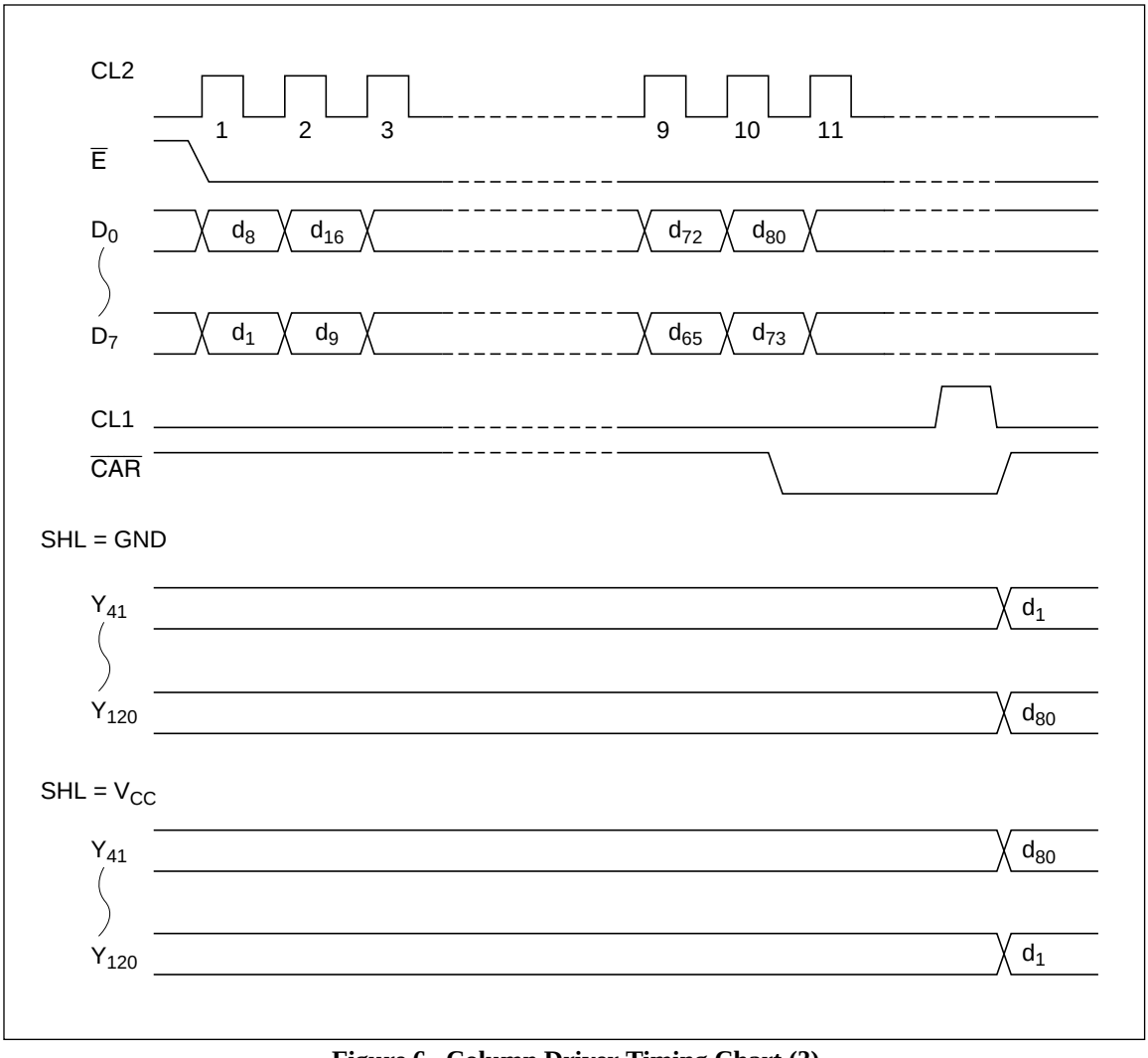


Figure 6 Column Driver Timing Chart (3)

Column Driving (4)

- CH2 = V_{CC} (80-bit data output mode)
- BS = GND (4-bit data latch mode)

When CH2 = V_{CC} and BS = GND, 4-bit parallel data is latched, while 80-bit data is output. The output of latched data is performed in described in "Column Driving (3)." See figure 7.

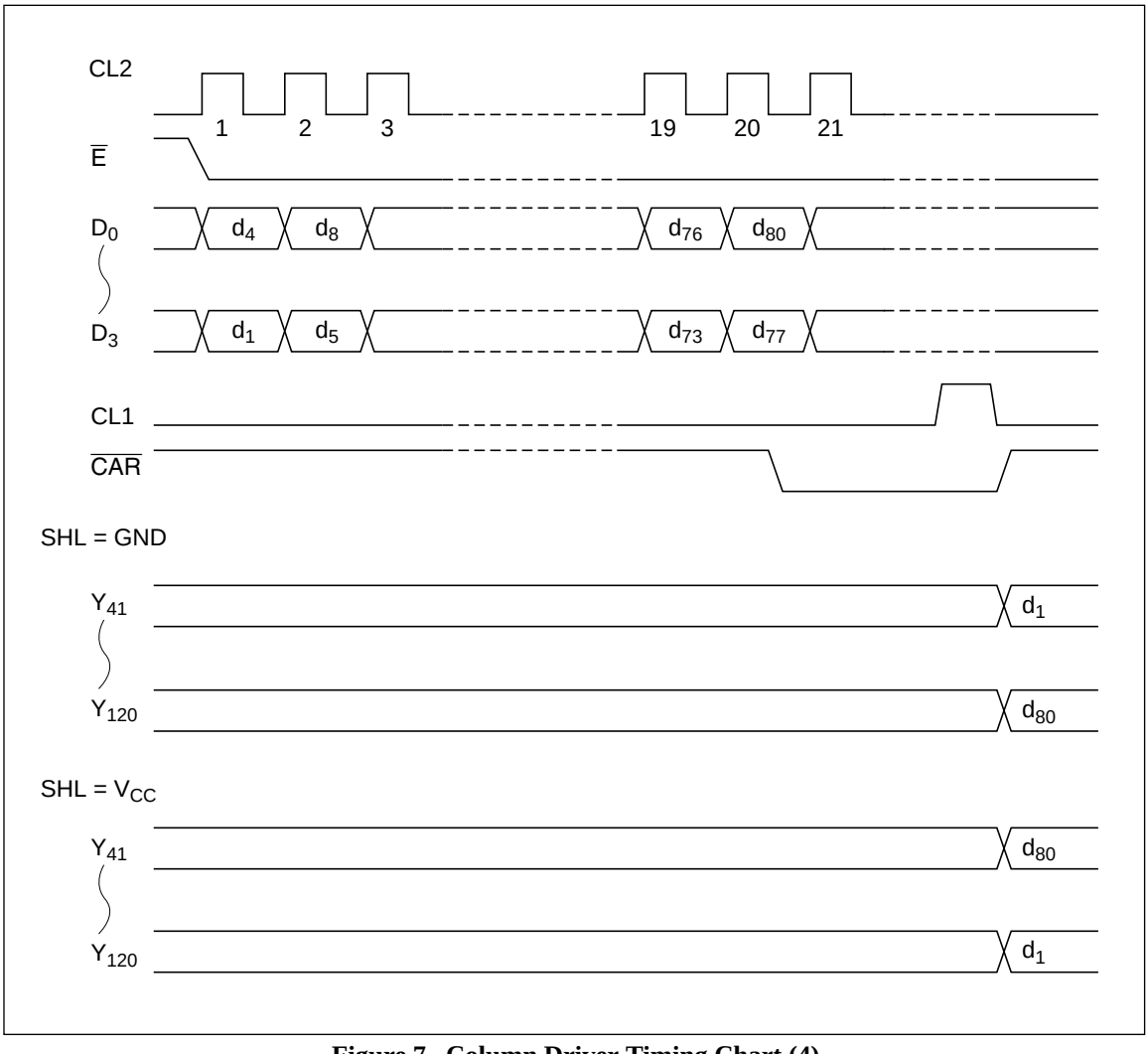


Figure 7 Column Driver Timing Chart (4)

Row Driving (1)

- CH2 = GND (160-bit data output mode)

The HD66107T shifts line scan data input through $\overline{E}$ at the falling edge of CL2.

When SHL = V_{CC}, 160-bit data is shifted from Y_1 to Y_{160}, whereas when SHL = GND, data is shifted from Y_{160} to Y_1. In both cases the HD66107T outputs the data delayed for 160 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next IC driver. See figure 8.

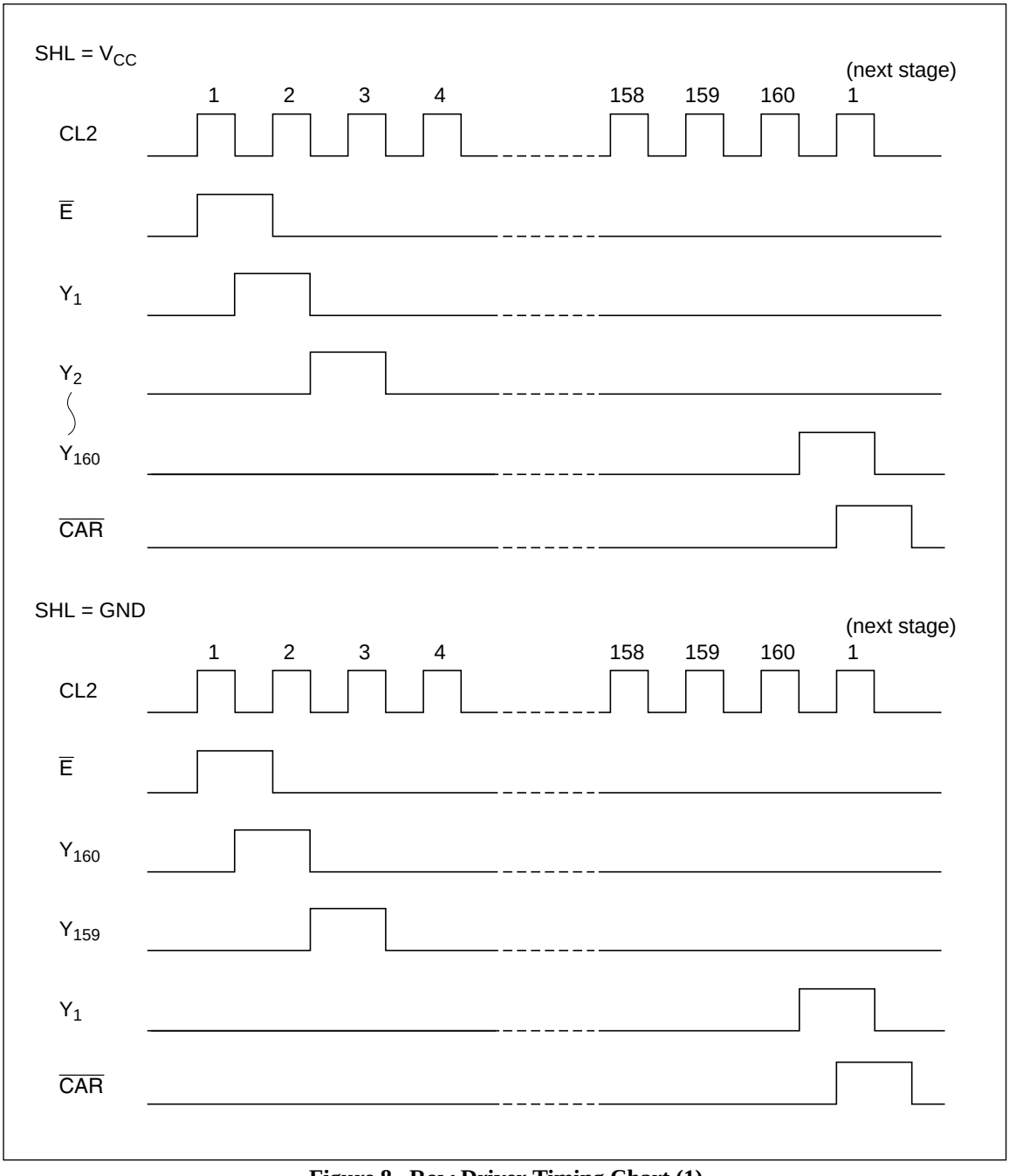


Figure 8 Row Driver Timing Chart (1)

Row Driving (2)

- CH2 = V_{CC} (80-bit data output mode)

When CH2 is high, the HD66107T can be used as an 80-bit row driver. In this case, Y_{41} to Y_{120} are enabled, while the other bits remain unchanged.

Line scan data input through $\overline{E}$ is shifted at the falling edge of CL2. When SHL = V_{CC}, data is shifted from Y_{41} to Y_{120}. Conversely, when SHL = GND, data is shifted from Y_{120} to Y_{41}. In both cases the HD66107T outputs the data delayed for 80 bits by the shift register through $\overline{CAR}$, becoming line scan data for the next LSI. See figure 9.

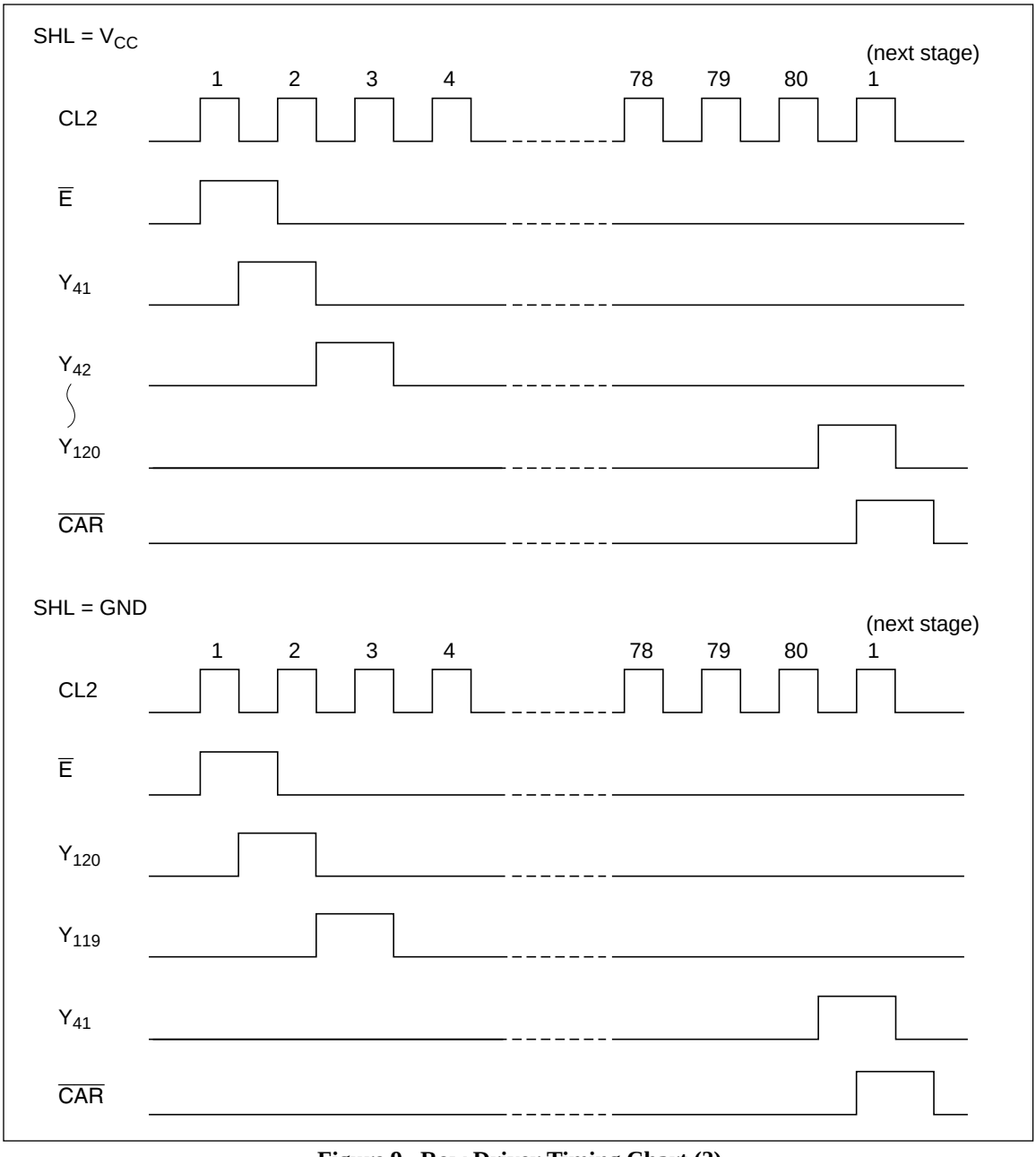
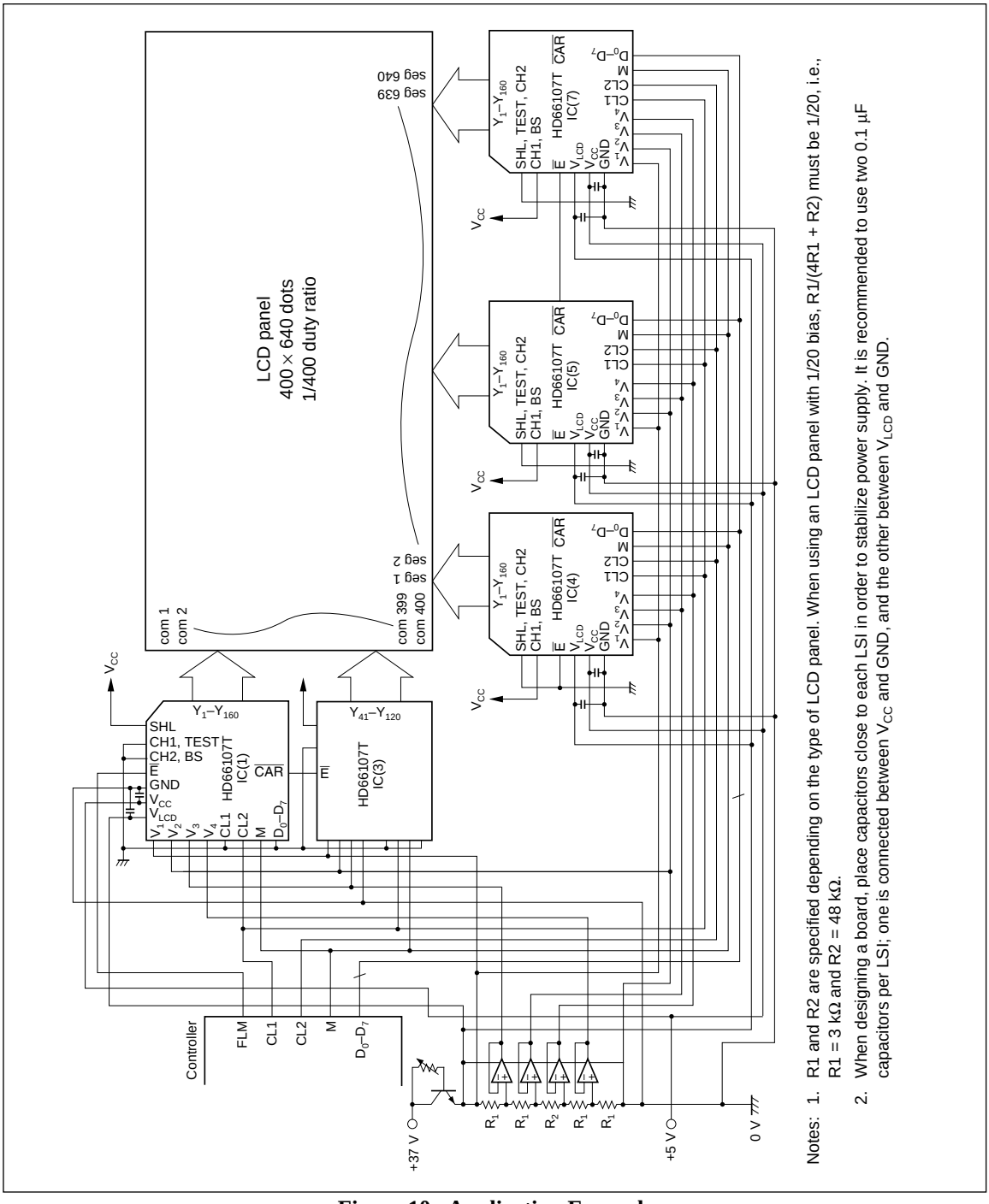


Figure 9 Row Driver Timing Chart (2)

Application

The following example shows a system configuration for driving a 640 × 400-dot LCD panel using the HD66107T.



Notes: 1. R1 and R2 are specified depending on the type of LCD panel. When using an LCD panel with 1/20 bias, R1/(4R1 + R2) must be 1/20, i.e., R1 = 3 kΩ and R2 = 48 kΩ.

2. When designing a board, place capacitors close to each LSI in order to stabilize power supply. It is recommended to use two 0.1 µF capacitors per LSI; one is connected between V_{CC} and GND, and the other between V_{LCD} and GND.

Figure 10 Application Example

Waveform Examples

Column Driving

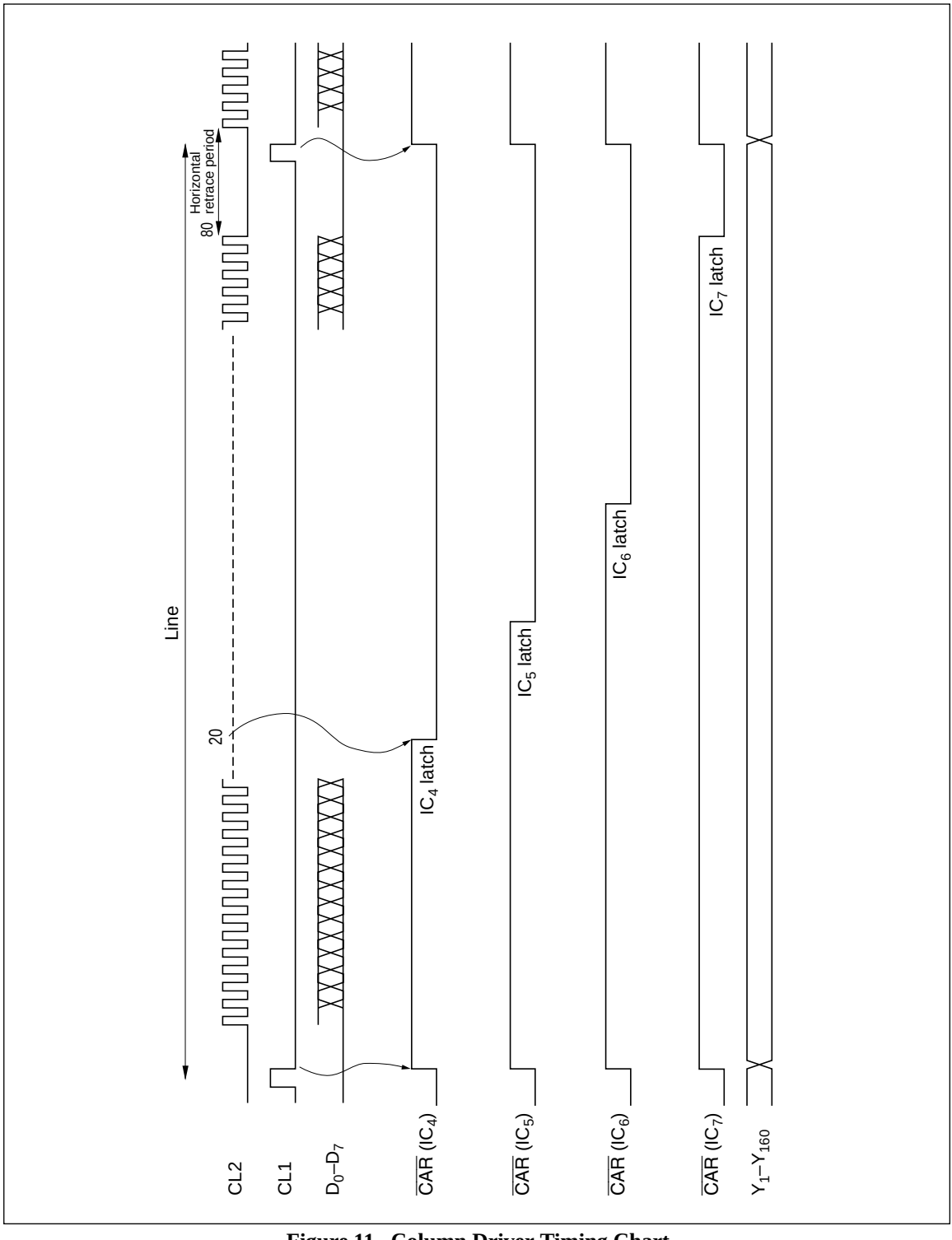


Figure 11 Column Driver Timing Chart

Row Driving

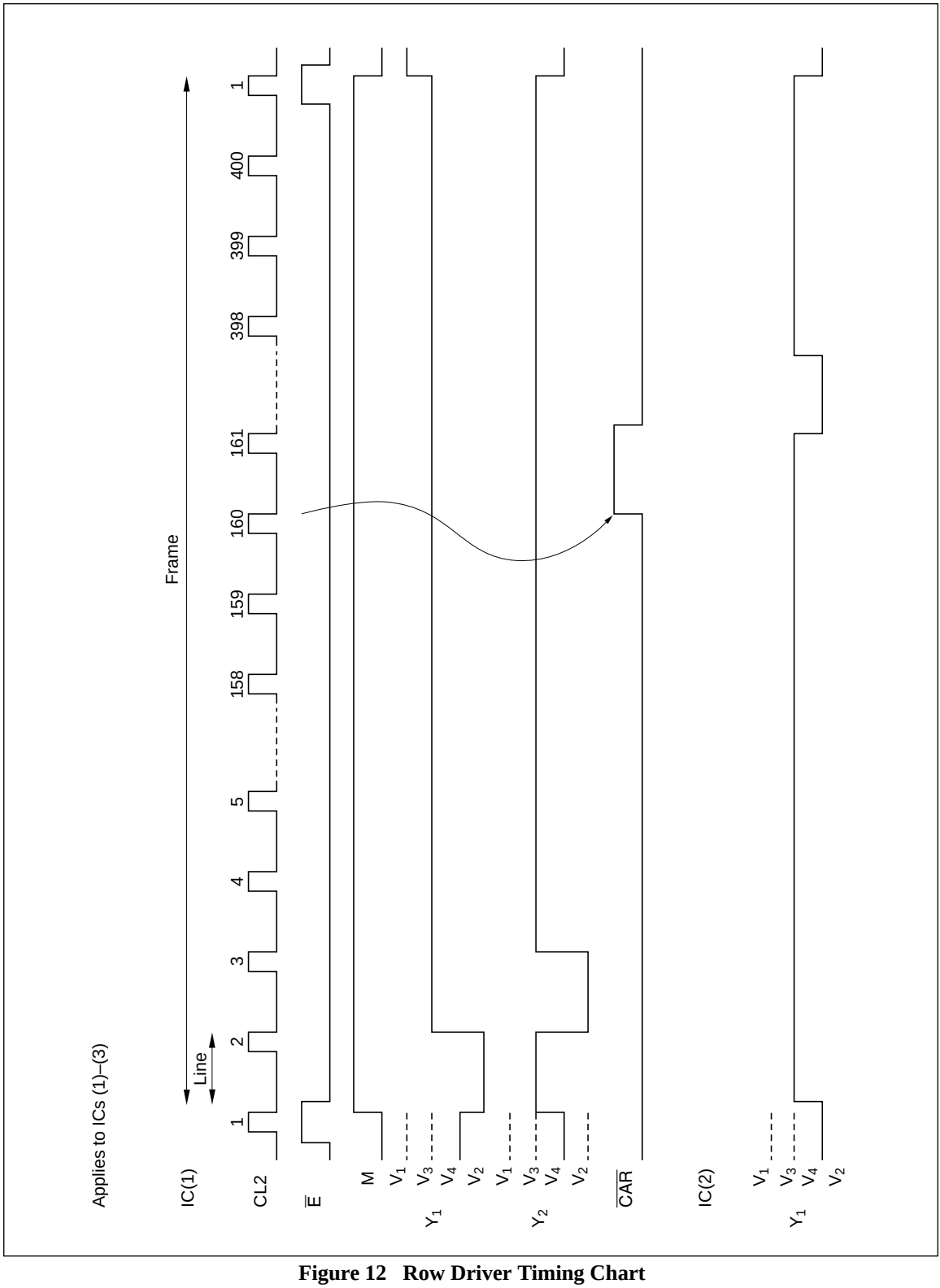


Figure 12 Row Driver Timing Chart

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	V_{LCD}	–0.3 to +38	V	1
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	–0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Reference point is GND (= 0 V).
2. Applies to input pins for logic circuit.
3. Applies to input pins for LCD drive circuits.
4. If the LSI is used beyond absolute maximum ratings, it may be permanently damaged. It should always be used within the above electrical characteristics to prevent malfunction or degradation of the LSI's reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ±10%, V_{LCD} = 14 to 37 V, Ta = –20 to 75°C)

Item	Symbol	Pin	Min	Max	Unit	Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL, BS, CH2, TEST, D_0–D_7, $\overline{E}$, CH1	$0.8 \times V_{CC}$	V_{CC}	V		
Input low voltage	V_{IL}		0	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}		—	0.4	V	I_{OL} = 0.4 mA	
Vi–Vj on resistance	R_{ON}	Y1–Y160, V1–V4	—	3.0	kΩ	I_{ON} = 150 µA	4
Input leak current (1)	I_{IL1}	CL1, CL2, M, SHL, BS, CH2, TEST, D_0–D_7, $\overline{E}$, CH1	–5.0	5.0	µA	V_{IN} = V_{CC} – GND	
Input leak current (2)	I_{IL2}	V1–V4	–100	100	µA	V_{IN} = V_{LCD} – GND	
Power dissipation (1)	I_{CC1}		—	5.0	mA	f_{CL2} = 8 MHz f_{CL1} = 28 kHz	1, 2
Power dissipation (2)	I_{LCD1}		—	2.0	mA		
Power dissipation (3)	I_{ST}		—	0.5	mA	In standby mode: f_{CL2} = 8 MHz, f_{CL1} = 28 kHz	1, 2
Power dissipation (4)	I_{CC2}		—	1.0	mA	f_{fCL1} = 28 kHz fm = 35 Hz	1, 3
Power dissipation (5)	I_{LCD2}		—	0.5	mA		

Notes: 1. Input and output current is excluded. When an input is at the intermediate level is CMOS, excessive current flows from the power supply though the input circuit. To avoid it, V_{IH} and V_{IL} must be fixed to V_{CC} and GND respectively.

2. Applies to column driving.

3. Applies to row driving.

4. Indicates the resistance between one pin from Y_1–Y_{160} and another pin from V_1–V_4 when load current is applied to the Y pin; defined under the following conditions.

   V_{LCD}–GND = 37 V
   V1, V3 = V_{LCD} – {2/20 (V_{LCD}–GND)}
   V2, V4 = V_{LCD} + {2/20 (V_{LCD}–GND)}

   This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltage should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 13).
   Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}–GND (figure 14).

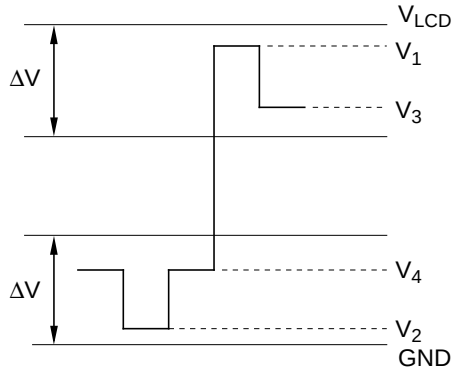


Figure 13 Driver's Output Waveform and Each Level of Voltage

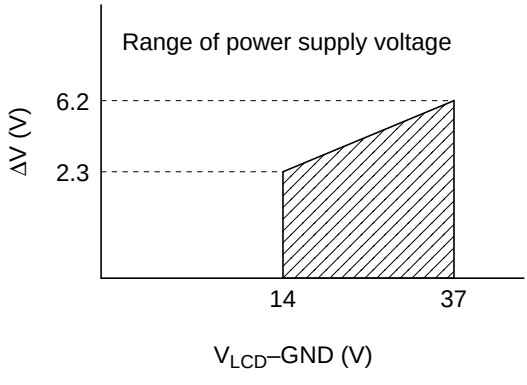


Figure 14 Power Supply Voltage V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 5 V ± 10%, V_{LCD} = 14 to 37 V, Ta = –20 to 75°C)

Column Driving

Item	Symbol	Pin Name	Min	Max	Unit	Note
Clock cycle time	t_{cyc}	CL2	125	—	ns	
Clock high-level width (1)	t_{CWH1}	CL2	30	—	ns	
Clock high-level width (2)	t_{CWH2}	CL1	60	—	ns	
Clock low-level width	t_{CWL}	CL2	30	—	ns	
Clock setup time	t_{SCL}	CL2	200	—	ns	
Clock hold time	t_{HCL}	CL2	200	—	ns	
Clock rising/falling time	t_{Ct}	CL1, CL2	—	30	ns	
Data setup time	t_{DSU}	D_0–D_7	30	—	ns	
Data hold time	t_{DH}	D_0–D_7	30	—	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	25	—	ns	
Output delay time (1)	t_{DCAR1}	$\overline{CAR}$	—	70	ns	1
Output delay time (2)	t_{DCAR2}	$\overline{CAR}$	—	200	ns	1
M phase difference	t_{CM}	M, CL1	—	300	ns	

Note: 1. Specified when connecting the load circuit shown in figure 15.

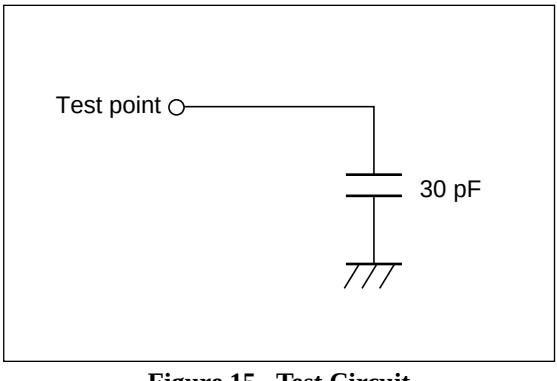


Figure 15 Test Circuit

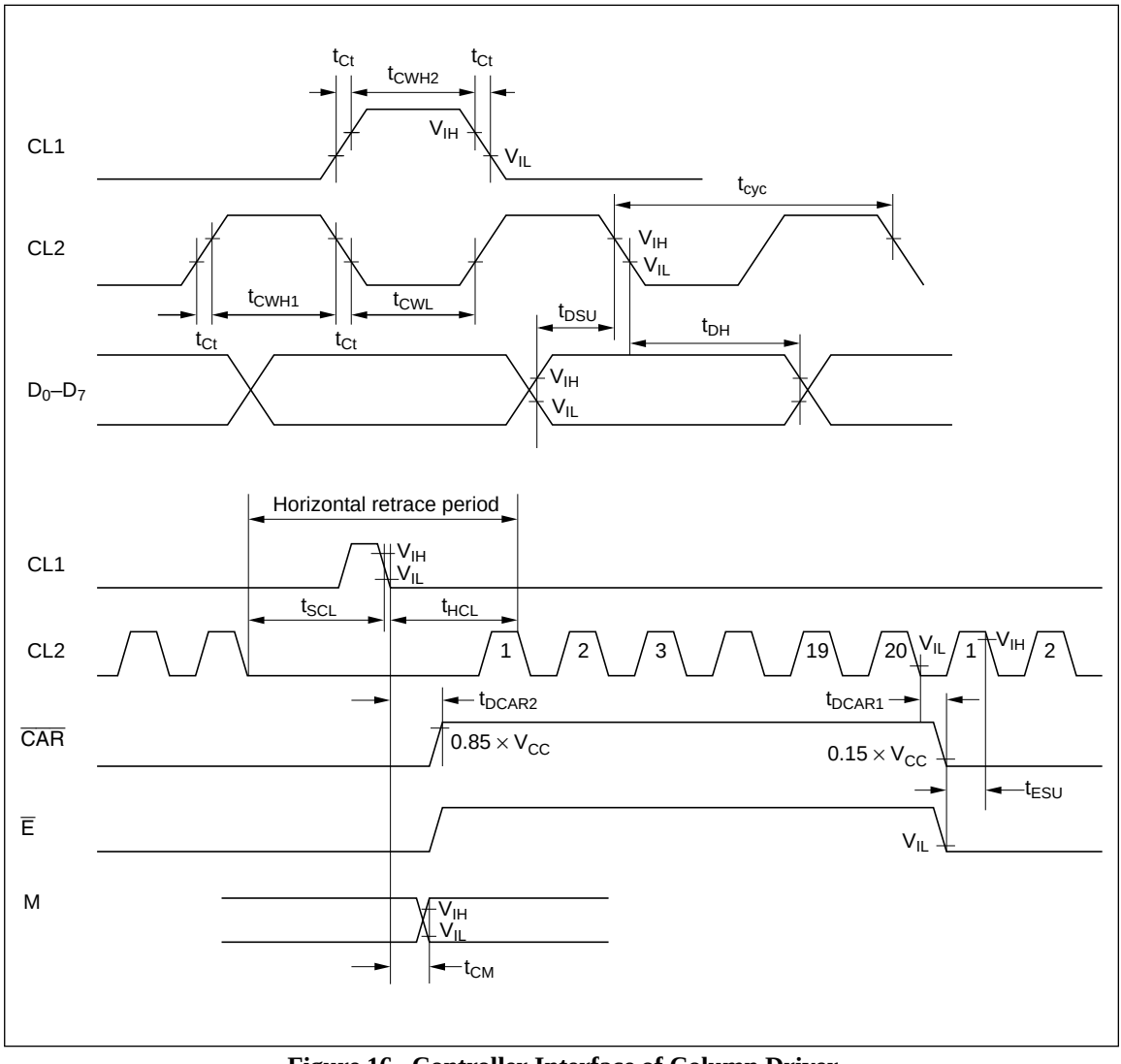


Figure 16 Controller Interface of Column Driver

Row Driving

Item	Symbol	Pin Name	Min	Max	Unit	Note
Clock low-level width	t_{WL1}	CL2	5	—	µs	
Clock high-level width	t_{WH1}	CL2	60	—	ns	
Data setup time	t_{DS2}	$\overline{E}$	100	—	ns	
Data hold time	t_{DH2}	$\overline{E}$	30	—	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	—	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	—	ns	1
Clock rising/falling time	t_{Ct}	CL2	—	30	ns	

Note: 1. Specified when connecting the load circuit shown in figure 15.

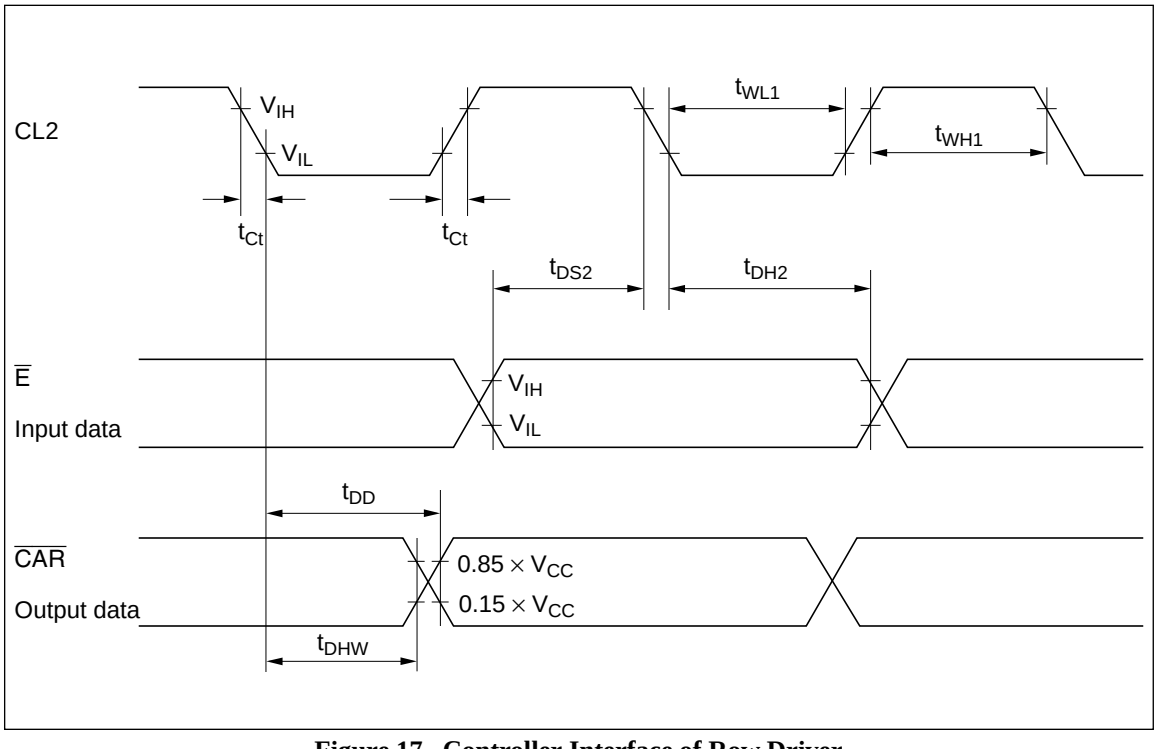


Figure 17 Controller Interface of Row Driver