

HD66113T

(120-Channel Common Driver Packaged
in a Slim Tape Carrier Package)

HITACHI

Description

The HD66113T is a common driver for large dot matrix liquid crystal graphics displays. It features 120 channels which can be divided into two groups of 60 channels by selecting data input/output pins. The driver is powered by about 3 V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66113T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

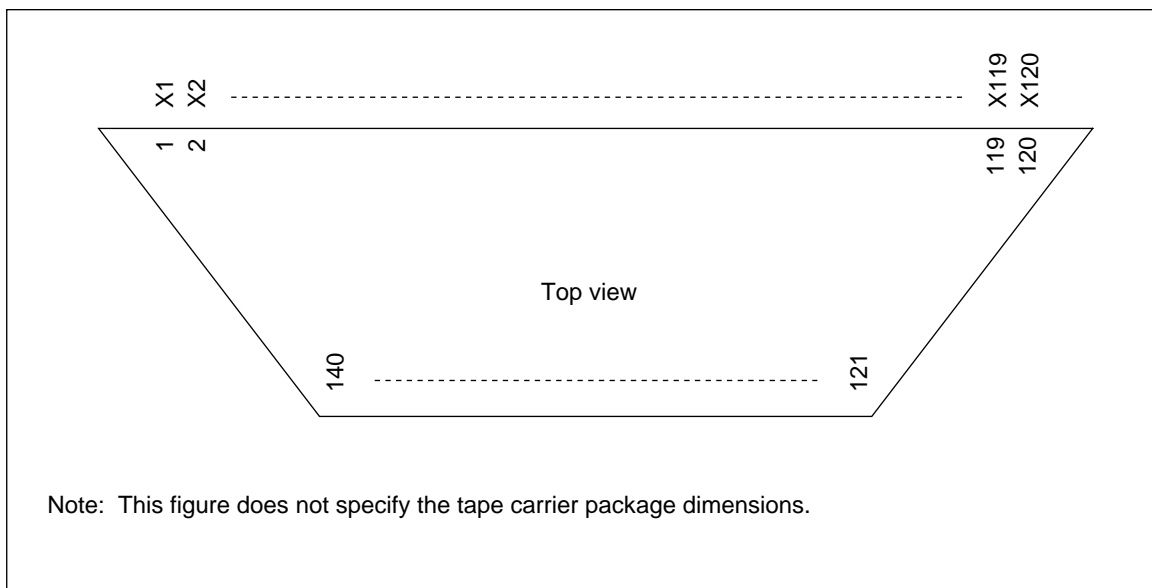
- Duty cycle: About 1/100 to 1/480
- 120 LCD drive circuits
- High LCD driving voltage: 14 V to 40 V
- Output division function (2 × 60-channel outputs)
- Display off function
- Operating voltage: 2.5 V to 5.5 V
- Slim-TCP
- Low output impedance: 0.7 k Ω (typ)

Ordering Information

Type No.	Outer Lead Pitch (μm)
HD66113TA0	190

Note: The details of TCP pattern are shown in "The Information of TCP."

Pin Arrangement



Pin Assignments

V _{LCD1}	V _{1L}	V _{6L}	V _{5L}	V _{2L}	GND	DIO1	M	DISPOFF	SHL	CH	DI	CL	DIO2	V _{CC}	V _{2R}	V _{5R}	V _{6R}	V _{1R}	V _{LCD2}
140	139	138	137	136	135	134	133	132	131	130	129	128	127	126	125	124	123	122	121

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Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
$V_{LCD1, 2}$	140, 121	V_{LCD}	—	Power supply
V_{CC}	126	V_{CC}	—	Power supply
GND	135	GND	—	Power supply
V_1L, V_1R	139, 122	V_1L, V_1R	Input	Power supply
V_2L, V_2R	136, 125	V_2L, V_2R	Input	Power supply
V_5L, V_5R	137, 124	V_5L, V_5R	Input	Power supply
V_6L, V_6R	138, 123	V_6L, V_6R	Input	Power supply
CL	128	Clock	Input	Control signal
M	133	M	Input	Control signal
CH	130	CH	Input	Control signal
SHL	131	Shift left	Input	Control signal
DIO1	134	Data	Input/output	Control signal
DIO2	127	Data	Input/output	Control signal
DI	129	Data	Input	Control signal
$\overline{\text{DISPOFF}}$	132	Display off	Input	Control signal
X1–X120	1–120	X1–X120	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_{LCD}, GND: Supply power to the LCD drive circuits (figure 1).

V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{6L}, V_{6R}: Supply different power levels to drive the LCD. V₁ and V₂ are selected levels, and V₅ and V₆ are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 60-output mode, CH = low: 120-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X61–X120 when CH and SHL are high, and to X60–X1 when SHL is low.

DISPOFF: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets the LCD drive outputs X1–X120 to the V₂ level. A high $\overline{\text{DISPOFF}}$ is normally used.

LCD Drive Outputs

X1–X120: Each X outputs one of four voltage levels V₁, V₂, V₅, or V₆, depending on the combination of the M signal and the data level (figure 3).

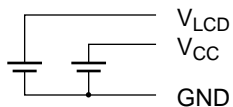


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 ••• → SR120 → DIO2
Low	Shift to left DIO2 → SR120 → SR119 ••• → SR1 → DIO1

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

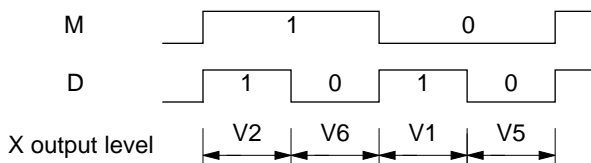
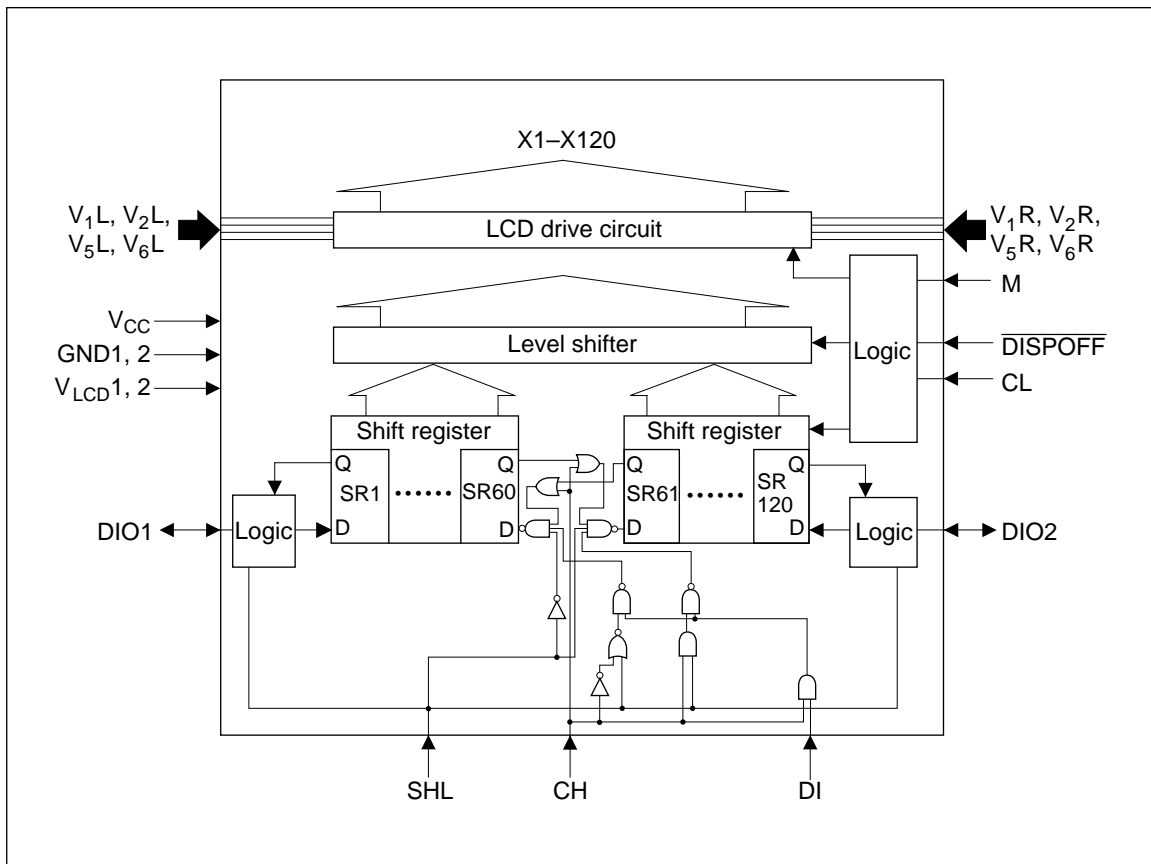


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 120-bit LCD drive circuit generates four voltage levels V_1 , V_2 , V_5 , and V_6 , which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 120-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	-0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	-0.3 to +42	V	1, 5
Input voltage 1	V_{T1}	-0.3 to $V_{CC} + 0.3$	V	1, 2
Input voltage 2	V_{T2}	-0.3 to $V_{LCD} + 0.3$	V	1, 3
Input voltage 3	V_{T3}	-0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	-20 to +75	°C	
Storage temperature	T_{stg}	-40 to +125	°C	

- Notes:
1. The reference point is GND (0 V).
 2. Applies to pins CL, M, SHL, DI, $\overline{DISPOFF}$, and CH.
 3. Applies to pins V_1 and V_6 .
 4. Applies to pins V_2 and V_5 .
 5. Power should be applied to V_{CC} -GND first, and then V_{LCD} -GND. It should be disconnected in the reverse order.
 6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics ($V_{CC} = 2.5\text{ V}$ to 5.5 V , $GND = 0\text{ V}$, and $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise stated)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	V_{OH}	2	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4\text{ mA}$	
Output low voltage	V_{OL}	2	—	—	0.4	V	$I_{OL} = 0.4\text{ mA}$	
V_i - X_j on resistance	R_{ON}	3	—	0.7	1.0	$k\Omega$	$I_{ON} = 150\ \mu\text{A}$	1
Input leakage current 1	I_{IL1}	1	-5	—	5	μA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	4	-25	—	25	μA	$V_{IN} = V_{LCD}$ to GND	
Current consumption 1	I_{GND}	—	—	—	0.5	mA	$f_{CL} = 36\text{ kHz}$ $f_M = 75\text{ kHz}$	2
Current consumption 2	I_{LCD}	—	—	—	1.0	mA		

Note: Pins: 1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{DISPOFF}}$
 2. DIO1, DIO2
 3. X1-X120, V
 4. V_1, V_2, V_5, V_6

- Notes: 1. Indicates the resistance between one of the pins X1–X120 and one of the voltage supply pins V_1 , V_2 , V_5 , or V_6 , when load current is applied to the X pin; defined under the following conditions:

$$V_{LCD-GND} = 40 \text{ V}$$

$$V_1, V_6 = V_{CC} - \{1/20 (V_{LCD-GND})\}$$

$$V_5, V_2 = GND + \{1/20 (V_{LCD-GND})\}$$

All voltages must be within ΔV , $V_{LCD} \geq V_1 \geq V_6 \geq V_{LCD} - 7.0 \text{ V}$, and $7.0 \text{ V} \geq V_5 \geq V_2 \geq GND$. Note that ΔV depends on the power supply voltage $V_{LCD-GND}$ (figure 5).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held at V_{CC} and GND, respectively.

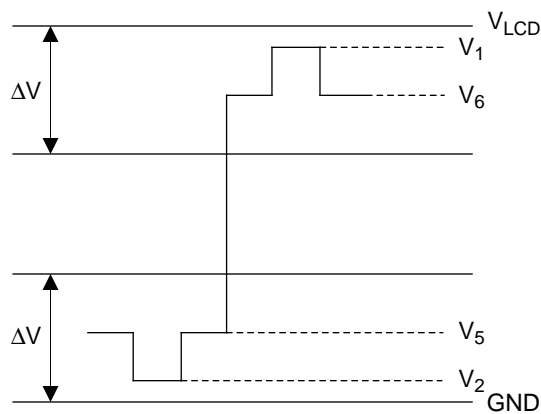


Figure 4 Relation between Driver Output Waveform and Voltage Levels

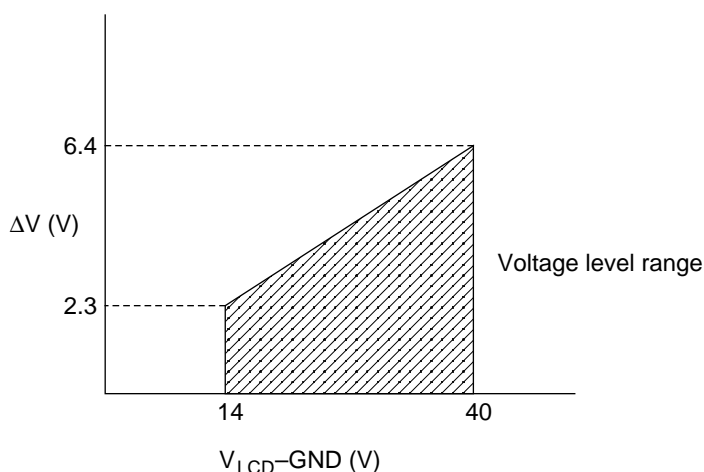


Figure 5 Relation between $V_{LCD-GND}$ and ΔV

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AC Characteristics ($V_{CC} = 2.5\text{ V}$ to 5.5 V , $GND = 0\text{ V}$, and $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	2
M phase difference	t_M	M, CL	-300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	μs	3
Output delay time 2	t_{pd2}	X (n), M	—	1.2	μs	3

AC Characteristics ($V_{CC} = 5.0\text{ V} \pm 10\%$, $GND = 0\text{ V}$, and $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	150	ns	2
M phase difference	t_M	M, CL	-300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	μs	3
Output delay time 2	t_{pd2}	X (n), M	—	0.7	μs	3

Notes: 1. $t_r, t_f < (t_{CYC} = t_{CWH} - t_{CWL})/2$ and $t_r, t_f \leq 30\text{ ns}$
2, 3 The load circuit shown in figure 6 is connected.

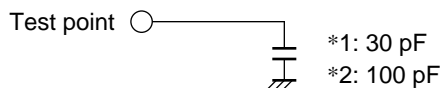


Figure 6 Load Circuit

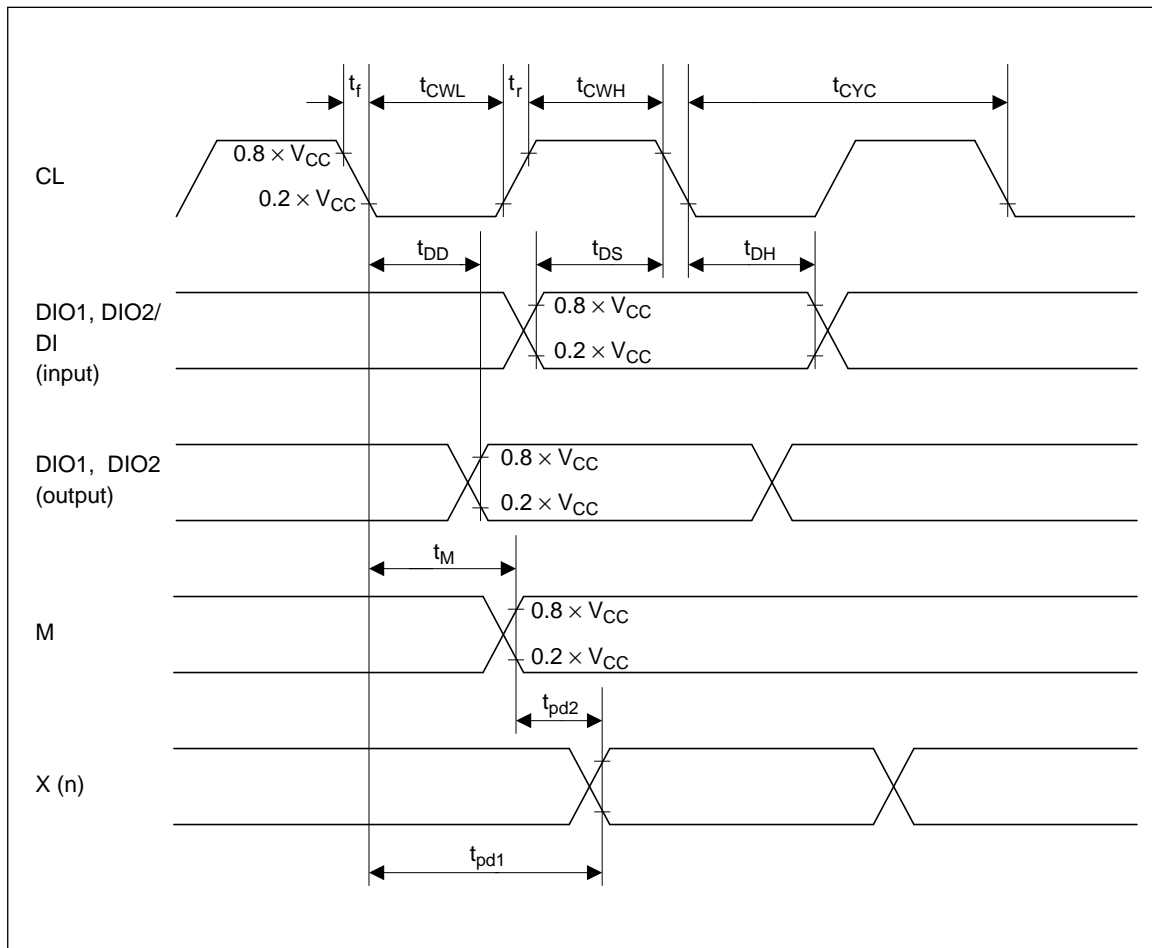
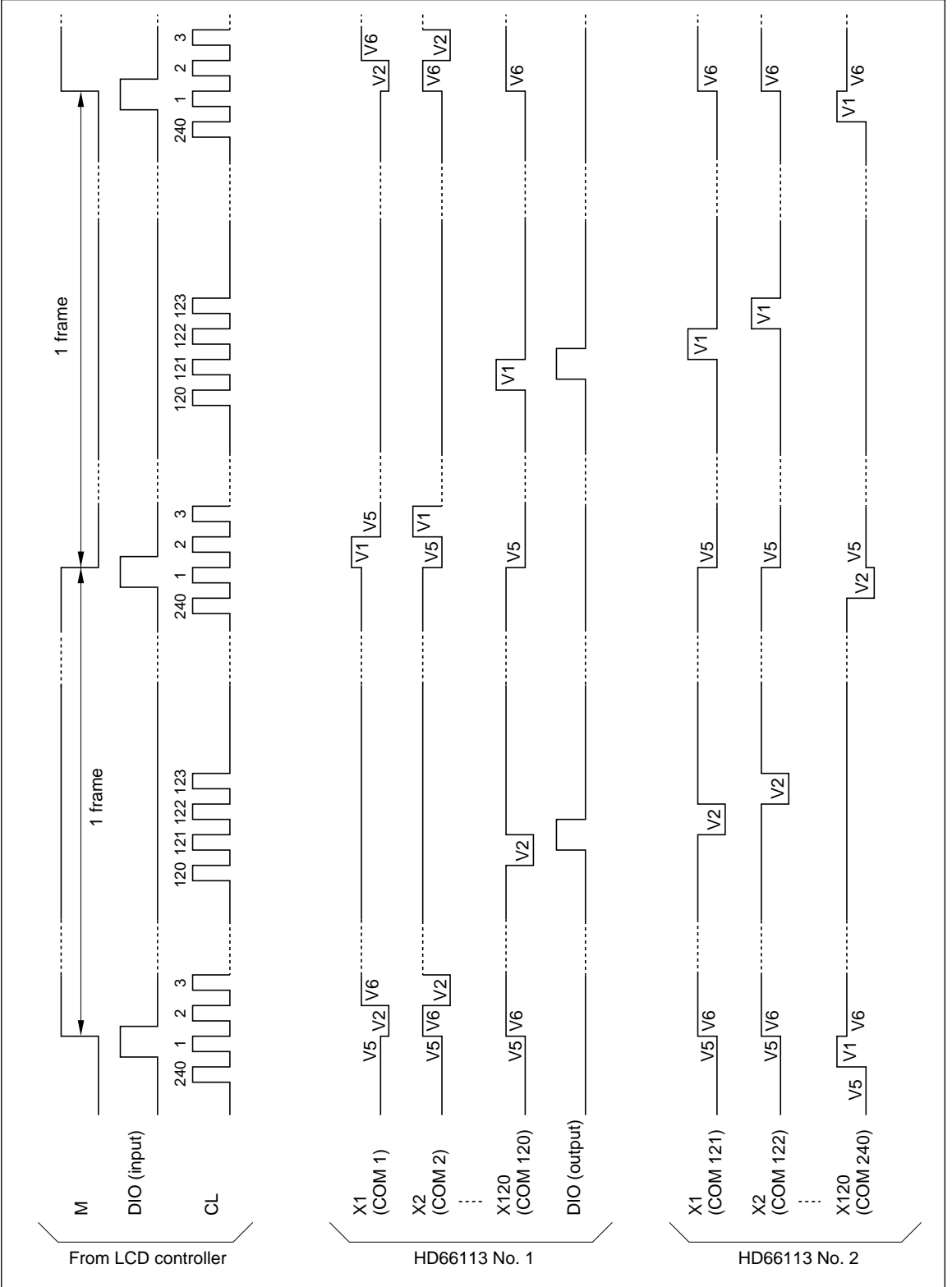


Figure 7 LCD Controller Interface Timing

Operation Timing (1/480 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66113Ts can be configured to drive a 600-line LCD panel with a 1/300 duty cycle. Figures 10 and 11 show examples of how HD66113Ts can be configured to drive a 240-line LCD panel with a 1/240 duty cycle.

The HD66113T's 120 channels can be divided into two groups of 60 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

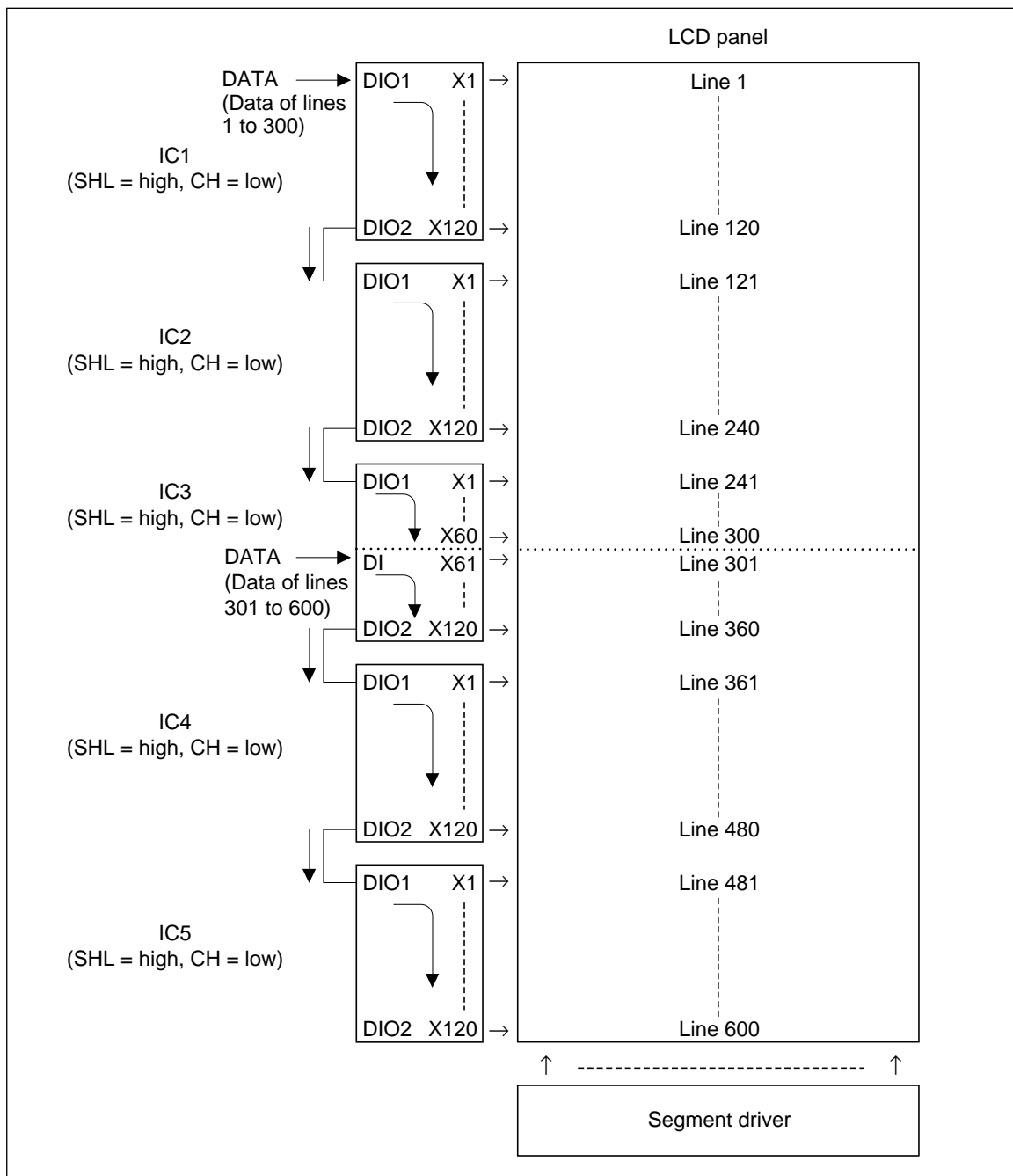


Figure 8 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (1)

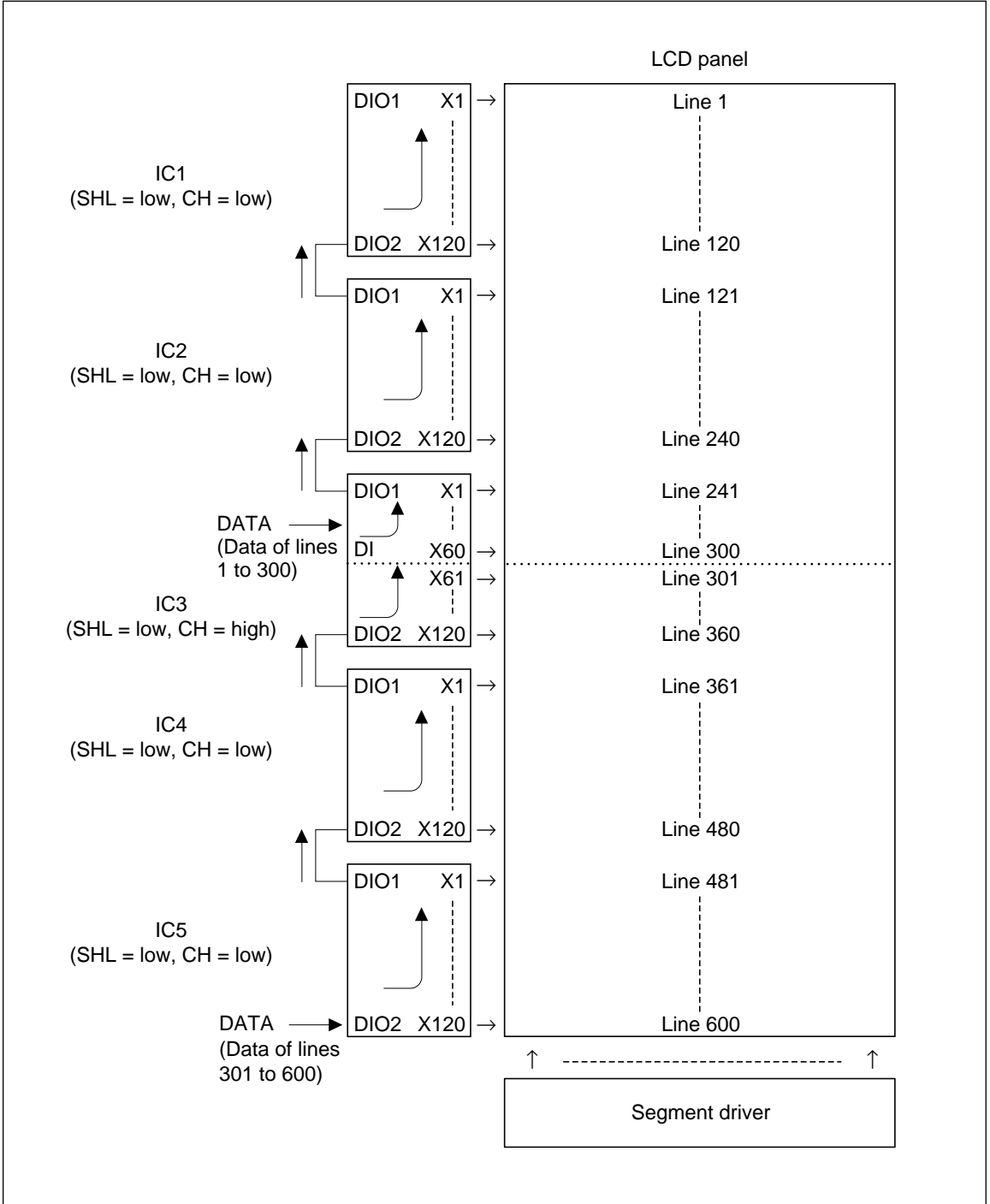


Figure 9 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (2)

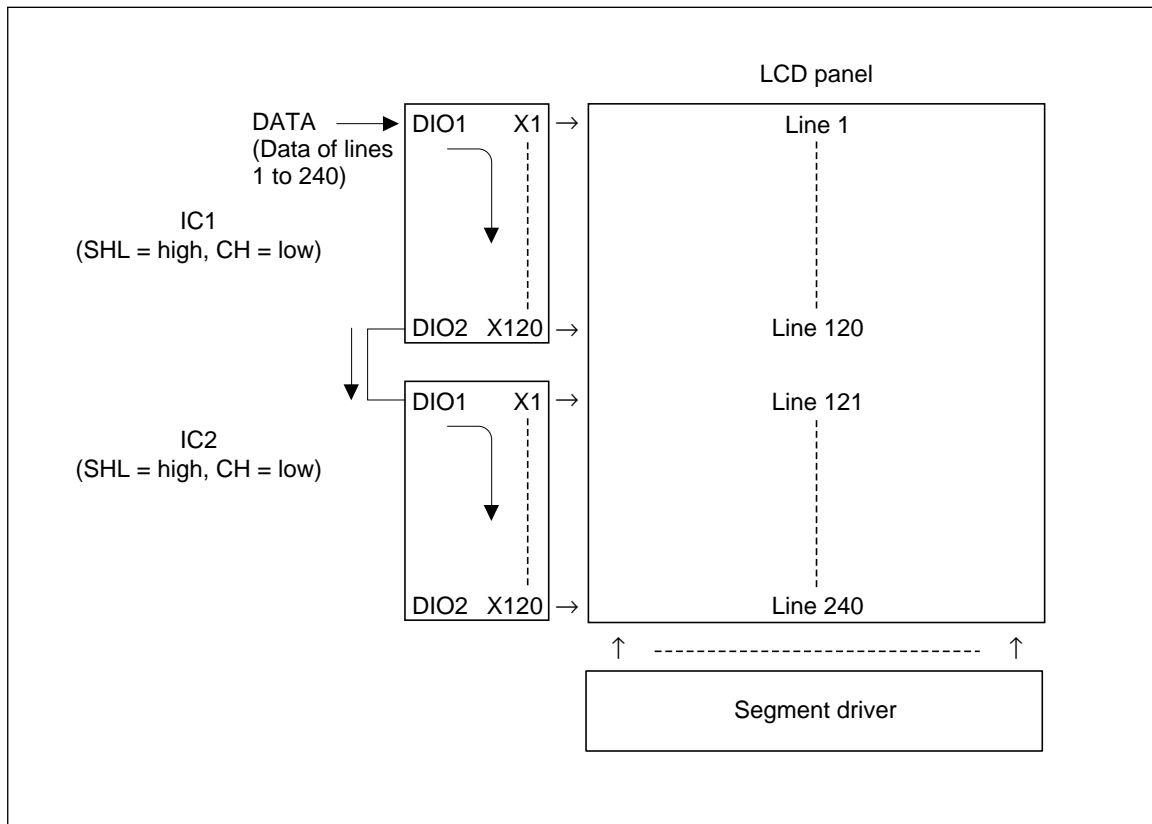


Figure 10 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (1)

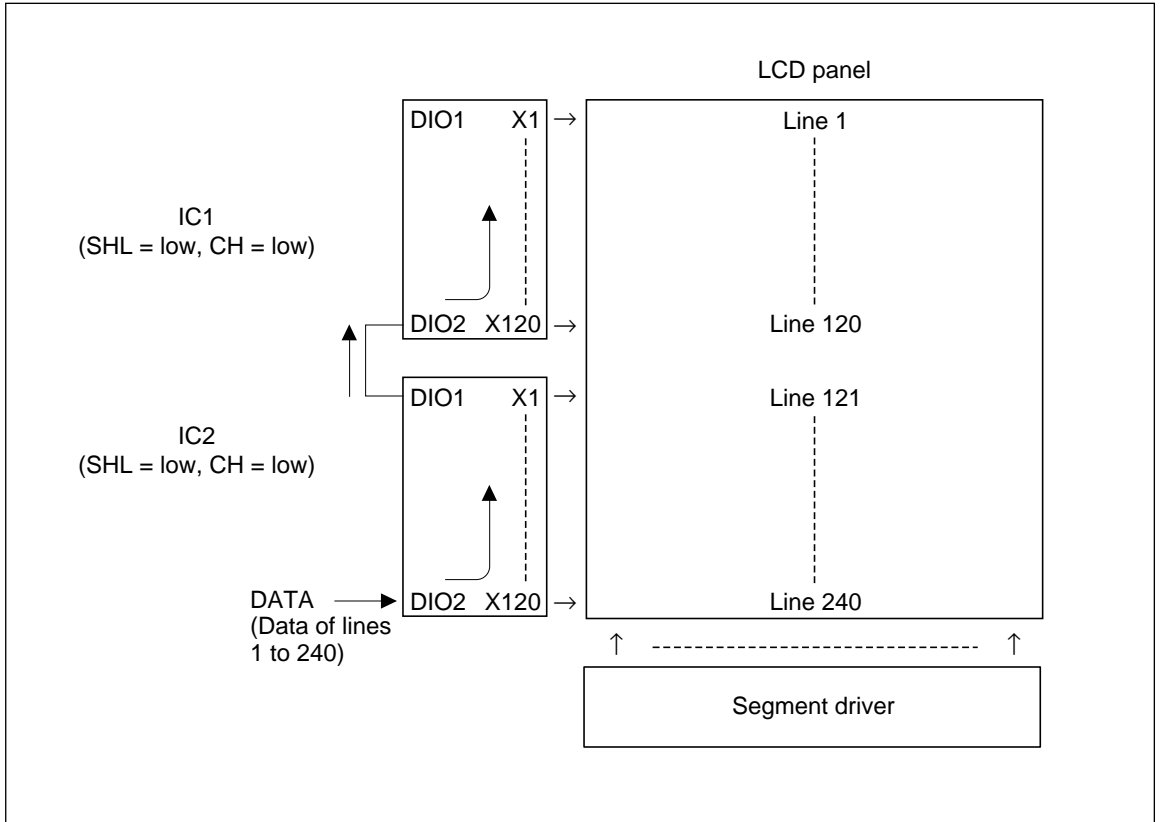


Figure 11 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (2)