

# HD66205

(Dot Matrix Liquid Crystal Graphic Display  
Common Driver with 80-Channel Outputs)

## HITACHI

### Description

The HD66205F/HD66205FL/HD66205TF/HD66205TFL/HD66205T/HD66205TL, the row LCD driver, features low output impedance and as many as 80 LCD outputs powered by 80 internal LCD drive circuits, and can drive a large liquid crystal graphic display. Because this device is fabricated by the CMOS process, it is suitable for battery-driven portable equipment, which fully utilizes the low power dissipation of liquid crystal elements. The HD66205 has a complete line-up: the HD66205F, a standard device powered by  $5\text{ V} \pm 10\%$ ; the HD66205FL, a 2.7 to 5.5 V, low power dissipation device; the HD66205TF and HD66205TFL, thin film package devices each powered by  $5\text{ V} \pm 10\%$  and 2.7 to 5.5 V; and the HD66205T, tape carrier package (TCP) devices powered by 2.7 to 5.5 V, respectively.

### Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - LCD drive: 10 to 28 V
- Display off function
- Internal 80-bit shift register
- Various LCD controller interfaces
  - LCTC series: HD63645, HD64645, HD64646
  - LVIC series: HD66840, HD66841
  - CLINE: HD66850

# HD66205

## Ordering Information 1 (Flat Package and Die Shipment)

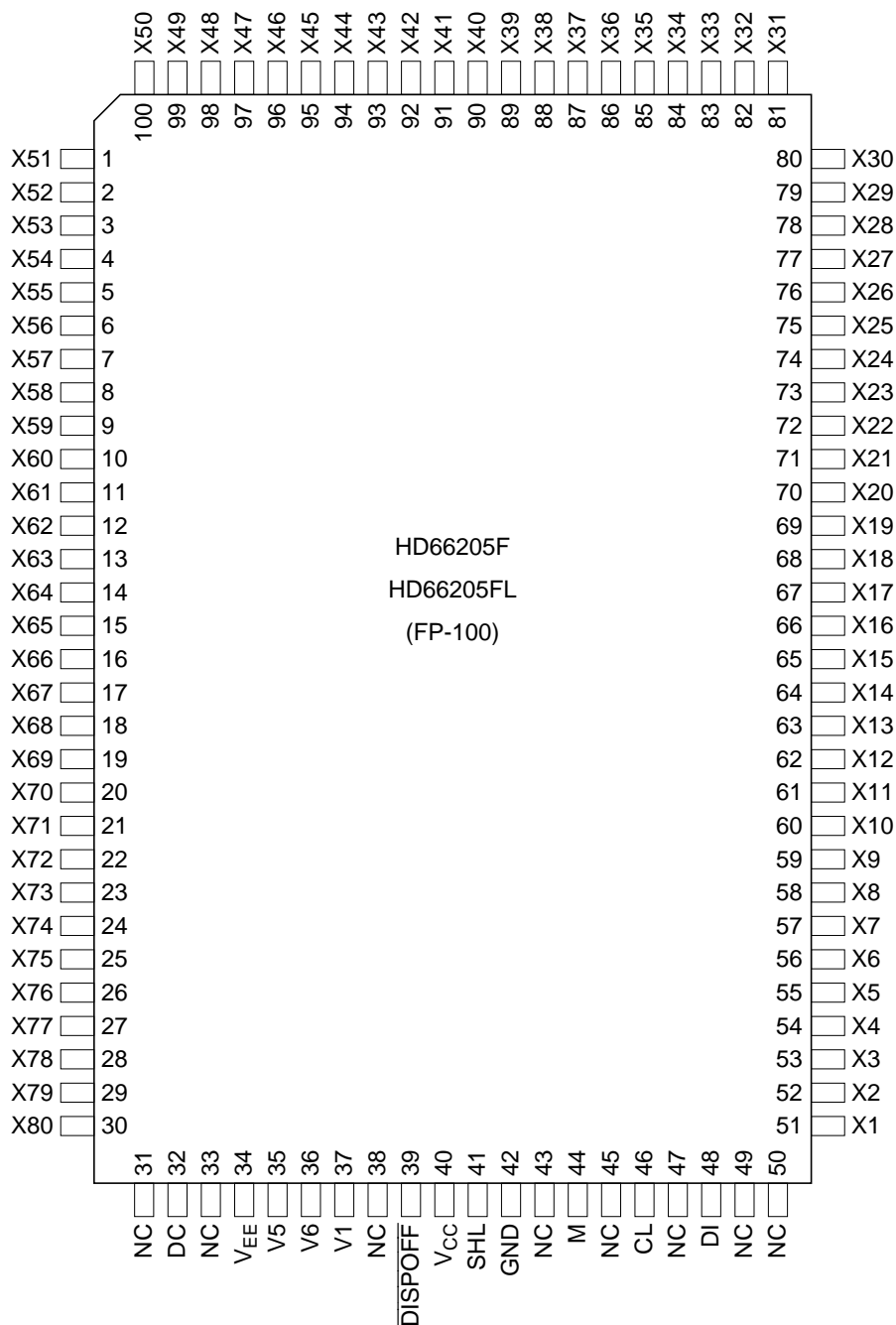
Type No.	Voltage Range	Package
HD66205F	5 V $\pm$ 10%	100-pin plastic QFP (FP-100)
HD66205FL	2.7 to 5.5 V	100-pin plastic QFP (FP-100)
HD66205TF	5 V $\pm$ 10%	100-pin thin plastic QFP (TFP-100)
HD66205TFL	2.7 to 5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66205	5 V $\pm$ 10%	Chip
HCD66205L	2.7 to 5.5 V	Chip

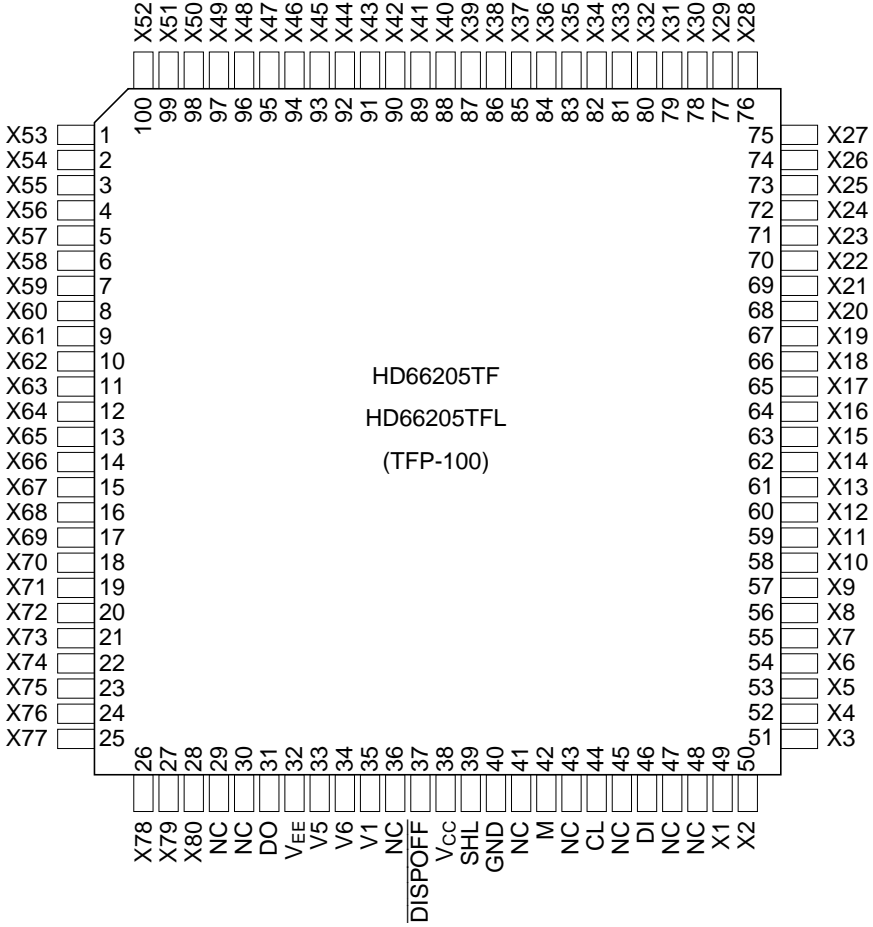
## Ordering Information 2 (Tape Carrier Package)

Type No.	Voltage Range	Outer Lead Pitch 1	Outer Lead Pitch 2	Device Length
HD66205TA1	2.7 to 5.5V	0.15mm	0.80mm	4 sprocket holes
HD66205TA2	2.7 to 5.5V	0.18mm	0.80mm	4 sprocket holes
HD66205TA3	2.7 to 5.5V	0.20mm	0.80mm	4 sprocket holes
HD66205TA6	2.7 to 5.5V	0.22mm	0.70mm	4 sprocket holes
HD66205TA7	2.7 to 5.5V	0.25mm	0.70mm	4 sprocket holes
HD66205TA9L	2.7 to 5.5V	0.22mm	0.70mm	3 sprocket holes

- Notes:
1. Outer lead pitch 1 is for LCD drive output pins, and outer lead pitch 2 for the other pins.
  2. Device length includes test pad areas.
  3. Spacing between two sprocket holes is 4.75mm.
  4. Tape film is Upirex (a trademark of Ube industries, Ltd.).
  5. 35-mm-wide tape is used.
  6. Leads are plated with Sn.
  7. The details of TCP pattern are shown in "The Information of TCP."

Pin Arrangement





(Top view)

## Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V <sub>CC</sub>	40/38	V <sub>CC</sub>	—	Power supply
GND	42/40	GND	—	Power supply
V <sub>EE</sub>	34/32	V <sub>EE</sub>	—	Power supply
V1	37/35	V1	Input	Power supply
V5	35/33	V5	Input	Power supply
V6	36/34	V6	Input	Power supply
CL	46/44	Clock	Input	Control signal
M	44/42	M	Input	Control signal
DI	48/46	Data in	Input	Control signal
DO	32/31	Data out	Output	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{\text{DISPOFF}}$	39/37	Display off	Input	Control signal
X <sub>1</sub> –X <sub>80</sub>	51–100, 1–30/ 1–28, 49–100	X1–X80	Output	LCD drive output
NC	31, 33, 38, 43, 45, 47, 49, 50/ 29, 30, 36, 41, 43, 45, 47, 48	No connection	—	—

## Pin Functions

### Power Supply

**V<sub>CC</sub>, V<sub>EE</sub>, GND:** V<sub>CC</sub>–GND supplies power to the internal logic circuits. V<sub>CC</sub>–V<sub>EE</sub> supplies power to the LCD drive circuits.

**V1, V5, V6:** Supply different levels of power to drive the LCD. V1 and V<sub>EE</sub> are selected levels, and V5 and V6 are non-selected levels. See figure 1.

### Control Signal

**CL:** Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts display data input via the DI pin.

**M:** Changes LCD drive outputs to AC.

**DI:** Inputs display data. DI of the first HD66205 must be connected to an LCD controller, and those of the other HD66205s must be connected to DI of the previous HD66205.

**DO:** Outputs display data. DO of the last HD66205 must be open, and those of the other HD66205s must be connected to DI of the next HD66205.

**SHL:** Selects the data shift direction for the shift register. See figure 2.

**DISPOFF:** A low  $\overline{\text{DISPOFF}}$  sets LCD drive outputs X1–X80 to V1 level.

### LCD Drive Output

**X1–X80:** Each X outputs one of the four voltage levels V1, V5, V6, or V<sub>EE</sub>, depending on a combination of the M signal and display data levels. See figure 3.

### Other

**NC:** Must be open.

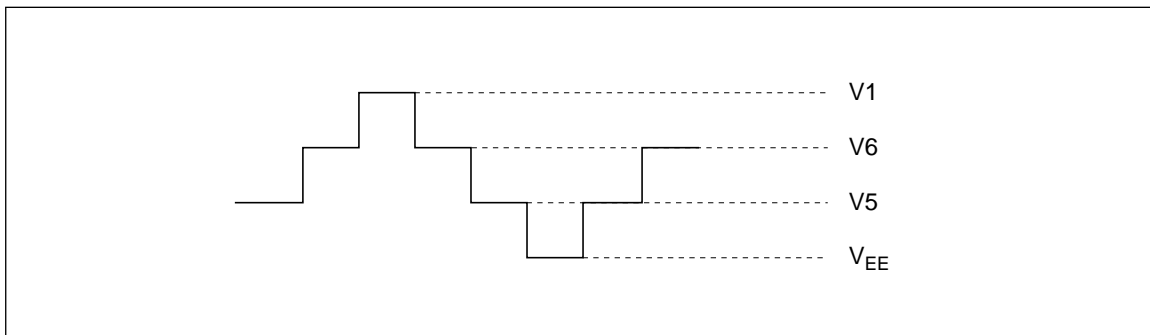
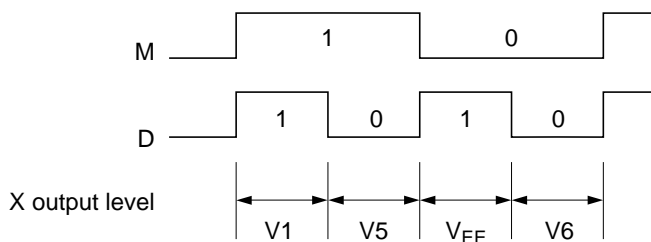


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

SHL level	Data shift direction	Common signal scan direction
Low	DI → SR1 → SR2 → SR80	X1 → X80
High	DI → SR80 → SR79 → SR1	X80 → X1

**Figure 2 Selection of Display Data Shift Direction**



**Figure 3 Selection of LCD Drive Output Level**

## Block Functions

### LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels  $V_1$ ,  $V_5$ ,  $V_6$ , and  $V_{EE}$ , for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the shift register.

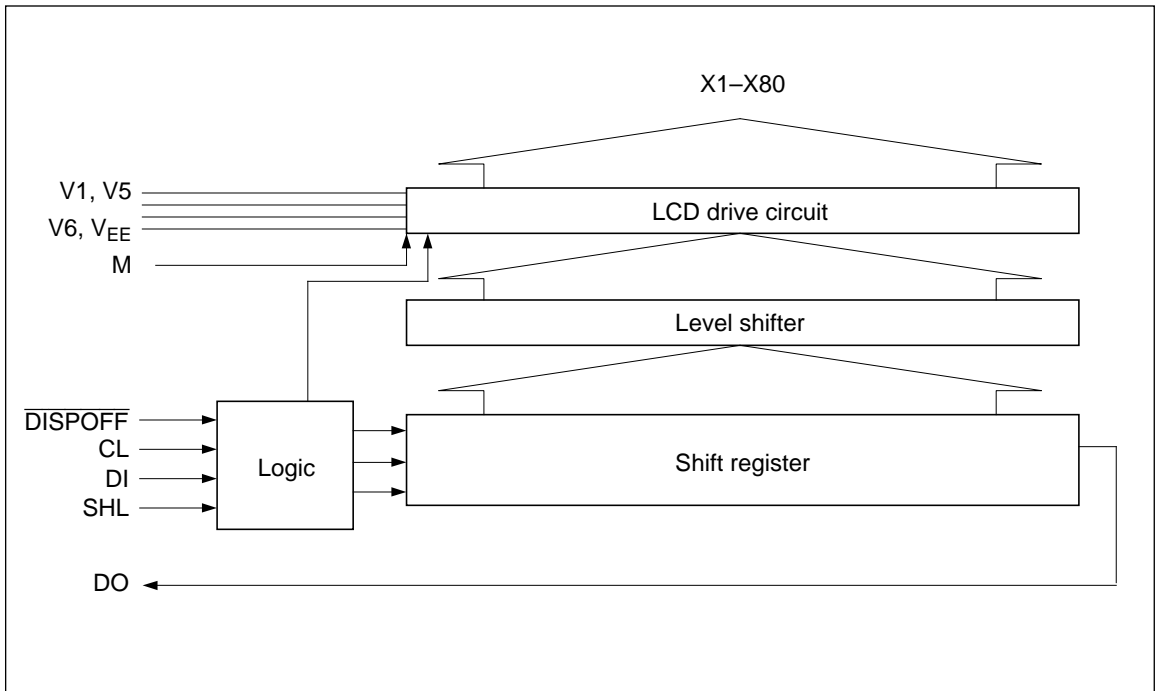
### Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

### Shift Register

The 80-bit shift register shifts data input via the DI pin by one bit, and the one bit of shifted-out data is output from the DO pin. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse.

## Block Diagram





Comparison of the HD66205 with the HD61105

Item	HD66205	HD61105
Display off function	Provided	Not provided
LCD drive voltage range	10 to 28 V	10 to 26 V
Shift clock phase selection function	Not provided	Provided (FCS pin)
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V5, V6 (V2 level is the same as V <sub>EE</sub> level)	V1, V2, V5, V6

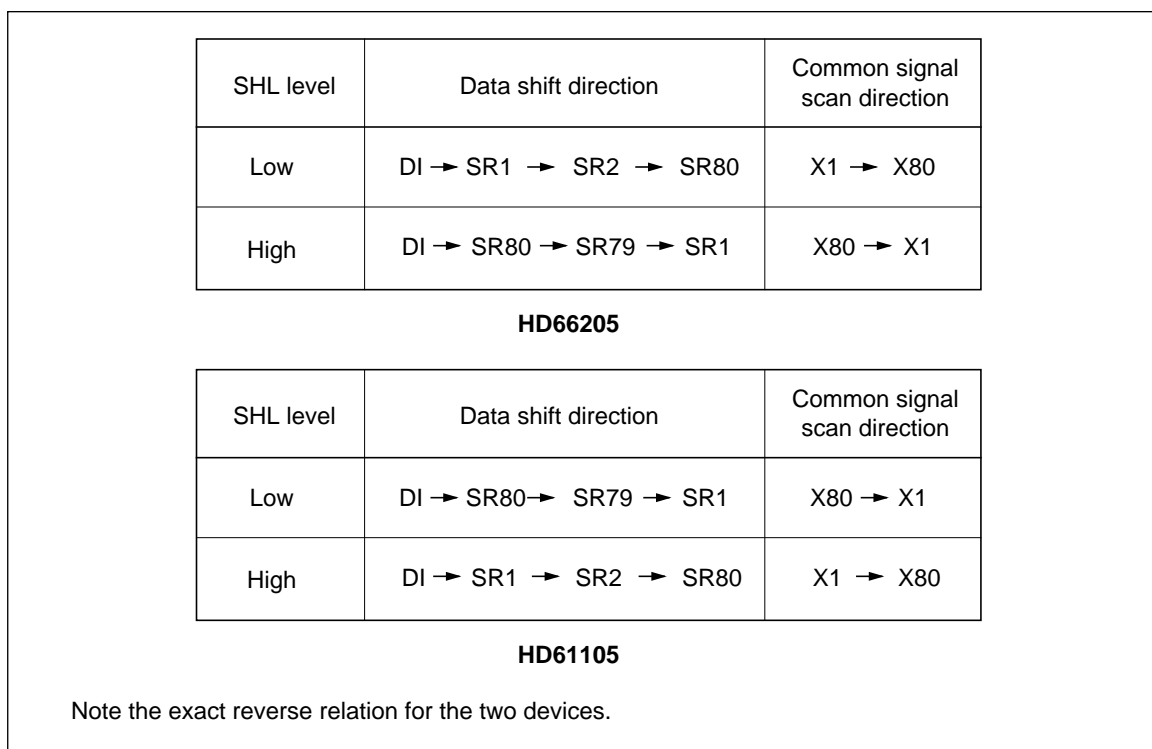


Figure 4 Relation between SHL and LCD Output Destinations for the HD66205 and HD61105

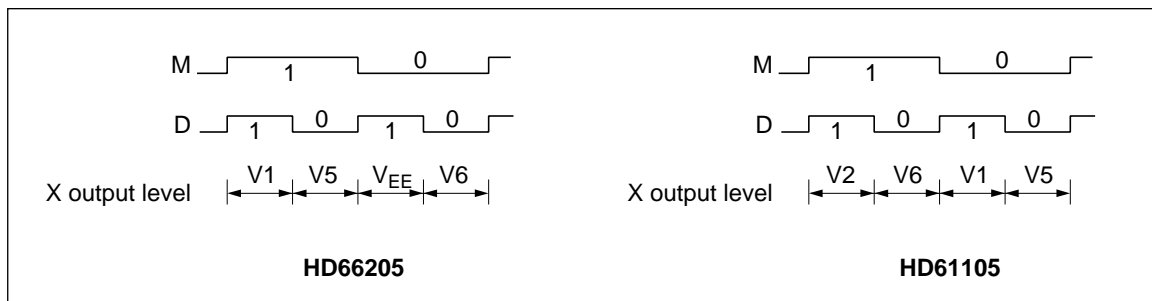


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66205 and HD61105

## Operation Timing

Figure 6 shows the operation timing for the Application Example.

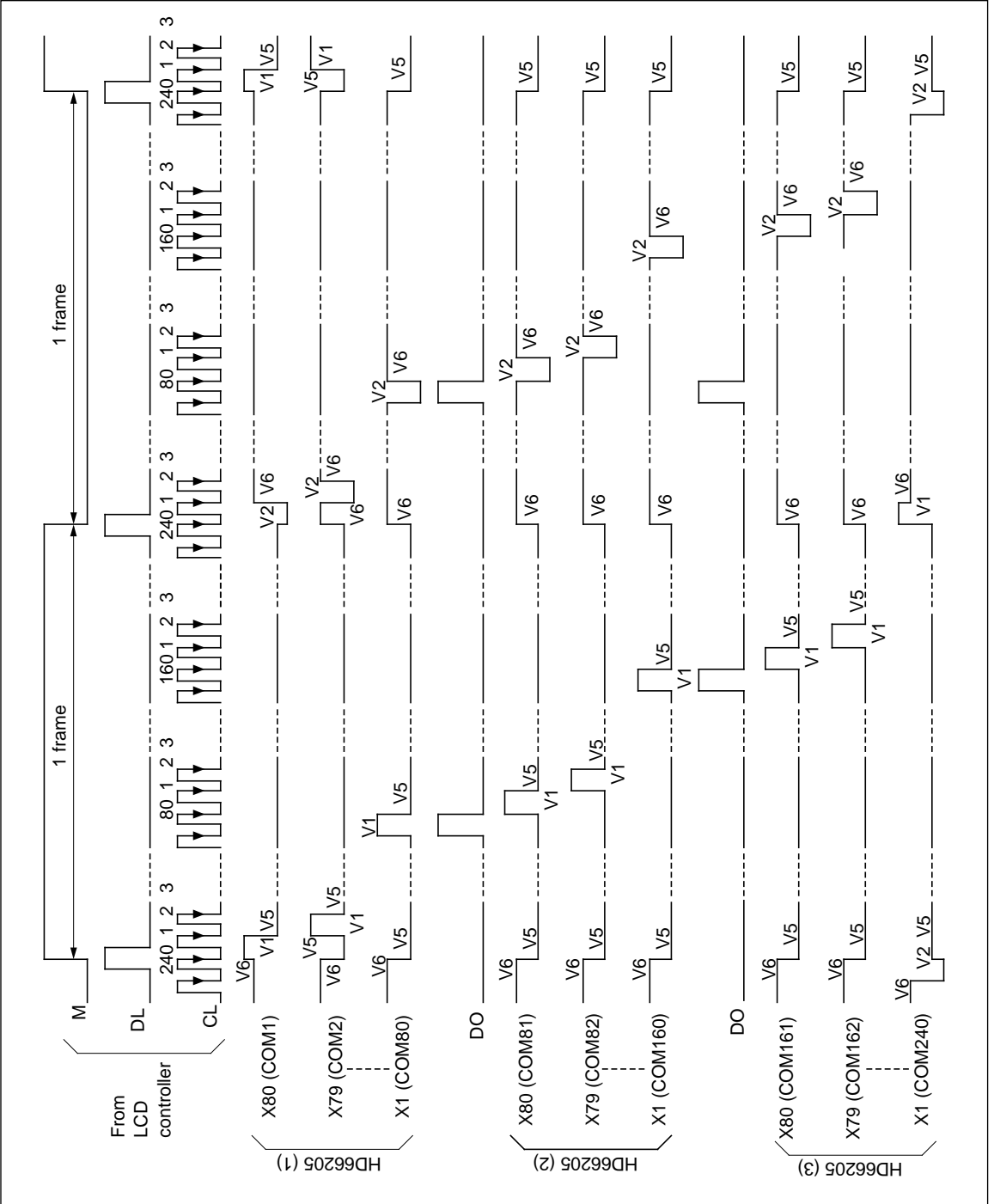
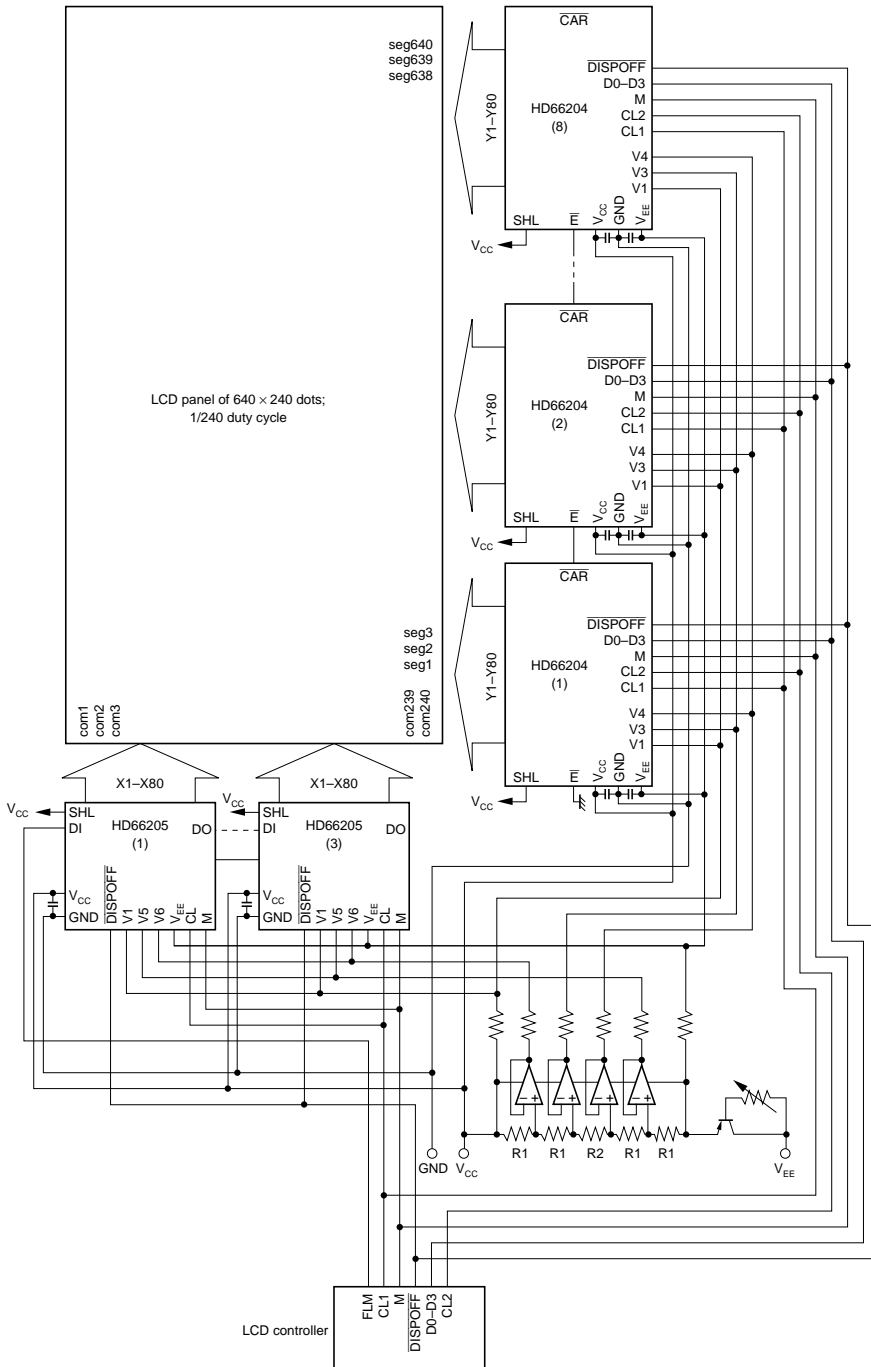


Figure 6 Relation between SHL and LCD Output Destinations

Application Example



- Notes:
1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is,  $R1/(4R1 + R2)$  should be 1/15.
  2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the V<sub>CC</sub> and GND pins, and the other between the V<sub>CC</sub> and V<sub>EE</sub> pins.

## Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	$V_{CC}$	-0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	$V_{EE}$	$V_{CC} - 30.0$ to $V_{CC} + 0.3$	V	
Input voltage 1	$V_{T1}$	-0.3 to $V_{CC} + 0.3$	V	1, 2
Input voltage 2	$V_{T2}$	$V_{EE} - 0.3$ to $V_{CC} + 0.3$	V	1, 3
Operating temperature	$T_{opr}$	-20 to +75	°C	
Storage temperature	$T_{stg}$	-55 to +125	°C	4

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL, M, SHL, DI, DISPOFF.

3. Applies to pins V1, V5, and V6.

4. -40 to +125°C for TCP devices.

5. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

## Electrical Characteristics

DC Characteristics for the HD66205F/HD66205TF ( $V_{CC} = 5\text{ V} \pm 10\%$ , GND = 0 V,  $V_{CC} - V_{EE} = 10$  to 28 V, and  $T_a = -20$  to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Condition	Notes
Input high voltage	$V_{IH}$	1	$0.7 \times V_{CC}$	—	$V_{CC}$	V		
Input low voltage	$V_{IL}$	1	0	—	$0.3 \times V_{CC}$	V		
Output high voltage	$V_{OH}$	2	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4\text{ mA}$	
Output low voltage	$V_{OL}$	2	—	—	0.4	V	$I_{OL} = 0.4\text{ mA}$	
$V_i$ - $Y_j$ on resistance	$R_{ON}$	3	—	—	2.0	k $\Omega$	$I_{ON} = 100\text{ }\mu\text{A}$	1
Input leakage current 1	$I_{IL1}$	1	-1.0	—	1.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	$I_{IL2}$	4	-25	—	25	$\mu\text{A}$	$V_{IN} = V_{CC}$ to $V_{EE}$	
Current consumption 1	$I_{GND}$	—	—	—	100	$\mu\text{A}$	$f_{CL} = 20\text{ kHz}$ $V_{CC} - V_{EE} = 28\text{ V}$	2
Current consumption 2	$I_{EE}$	—	—	150	500	$\mu\text{A}$	Same as above	2

Pins and notes on next page.

**DC Characteristics for the HD66205FL/HD66205TFL/HD66205T** ( $V_{CC} = 2.7$  to  $5.5$  V,  $GND = 0$  V,  $V_{CC} - V_{EE} = 10$  to  $28$  V, and  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Condition	Notes
Input high voltage	$V_{IH}$	1	$0.7 \times V_{CC}$	$V_{CC}$	V		
Input low voltage	$V_{IL}$	1	0	$0.3 \times V_{CC}$	V		
Output high voltage	$V_{OH}$	2	$V_{CC} - 0.4$	—	V	$I_{OH} = -0.4$ mA	
Output low voltage	$V_{OL}$	2	—	0.4	V	$I_{OL} = 0.4$ mA	
Vi–Yj on resistance	$R_{ON}$	3	—	2.0	k $\Omega$	$I_{ON} = 100$ $\mu$ A	1
Input leakage current 1	$I_{IL1}$	1	-1.0	1.0	$\mu$ A	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	$I_{IL2}$	4	-25	25	$\mu$ A	$V_{IN} = V_{CC}$ to $V_{EE}$	
Current consumption 1	$I_{GND}$	—	—	100	$\mu$ A	$f_{CL} = 16.8$ kHz $f_M = 35$ Hz $V_{CC} = 3.0$ V $V_{CC} - V_{EE} = 28$ V	2
Current consumption 2	$I_{EE}$	—	—	250	$\mu$ A	Same as above	2

Pins: 1. CL, M, SHL, DI,  $\overline{DISPOFF}$   
 2. DO  
 3. X1–X80, V1, V5, V6  
 4. V1, V5, V6

- Notes: 1. Indicates the resistance between one pin from X1–X80 and another pin from V1, V5, V6, and  $V_{EE}$ , when load current is applied to the X pin; defined under the following conditions.  
 $V_{CC} - V_{EE} = 28$  V  
 $V1, V6 = V_{CC} - \{1/10(V_{CC} - V_{EE})\}$   
 $V5 = V_{EE} + \{1/10(V_{CC} - V_{EE})\}$   
 V1 and V6 should be near  $V_{CC}$  level, and V5 should be near  $V_{EE}$  level (figure 7). All voltage must be within  $\Delta V$ .  $\Delta V$  is the range within which  $R_{ON}$ , the LCD drive circuits' output impedance, is stable. Note that  $\Delta V$  depends on power supply voltage  $V_{CC} - V_{EE}$  (figure 8).
2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this,  $V_{IH}$  and  $V_{IL}$  must be held to  $V_{CC}$  and GND levels, respectively.
3. Applies to standby mode.

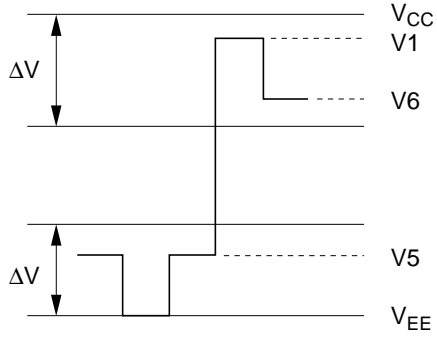


Figure 7 Relation between Driver Output Waveform and Level Voltages

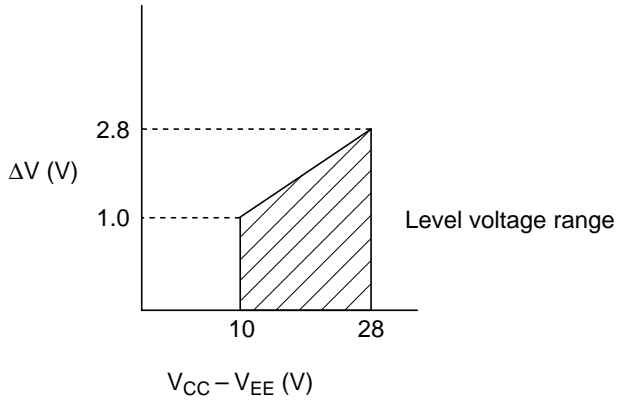


Figure 8 Relation between  $V_{CC} - V_{EE}$  and  $\Delta V$

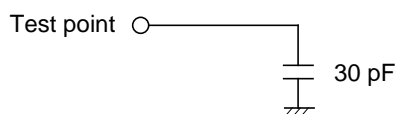
**AC Characteristics for the HD66205F/HD66205TF** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , and  $T_a = -20\text{ to }+75^\circ\text{C}$ , unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Note
Clock cycle time	$t_{CYC}$	CL	10	—	$\mu\text{s}$	
Clock high-level width	$t_{CWH}$	CL	50	—	ns	
Clock low-level width	$t_{CWL}$	CL	1.0	—	$\mu\text{s}$	
Clock rise time	$t_r$	CL	—	30	ns	
Clock fall time	$t_f$	CL	—	30	ns	
Data setup time	$t_{DS}$	DI, CL	100	—	ns	
Data hold time	$t_{DH}$	DI, CL	100	—	ns	
Data output delay time	$t_{DD}$	DO, CL	—	3.0	$\mu\text{s}$	1
Data output hold time	$t_{DHW}$	DO, CL	100	—	ns	
Disp off ( $\overline{\text{DISPOFF}}$ ) rise time	$t_{r2}$	$\overline{\text{DISPOFF}}$	—	200	ns	
Disp off ( $\overline{\text{DISPOFF}}$ ) fall time	$t_{f2}$	$\overline{\text{DISPOFF}}$	—	200	ns	

**AC Characteristics for the HD66205FL/HD66205TFL/HD66205T** ( $V_{CC} = 2.7\text{ to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ , and  $T_a = -20\text{ to }+75^\circ\text{C}$ , unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Note
Clock cycle time	$t_{CYC}$	CL	10	—	$\mu\text{s}$	
Clock high-level width	$t_{CWH}$	CL	80	—	ns	
Clock low-level width	$t_{CWL}$	CL	1.0	—	$\mu\text{s}$	
Clock rise time	$t_r$	CL	—	30	ns	
Clock fall time	$t_f$	CL	—	30	ns	
Data setup time	$t_{DS}$	DI, CL	100	—	ns	
Data hold time	$t_{DH}$	DI, CL	100	—	ns	
Data output delay time	$t_{DD}$	DO, CL	—	7.0	$\mu\text{s}$	1
Data output hold time	$t_{DHW}$	DO, CL	100	—	ns	
Disp off ( $\overline{\text{DISPOFF}}$ ) rise time	$t_{r2}$	$\overline{\text{DISPOFF}}$	—	200	ns	
Disp off ( $\overline{\text{DISPOFF}}$ ) fall time	$t_{f2}$	$\overline{\text{DISPOFF}}$	—	200	ns	

Note: 1. The load circuit shown in figure 9 is connected.



**Figure 9 Load Circuit**

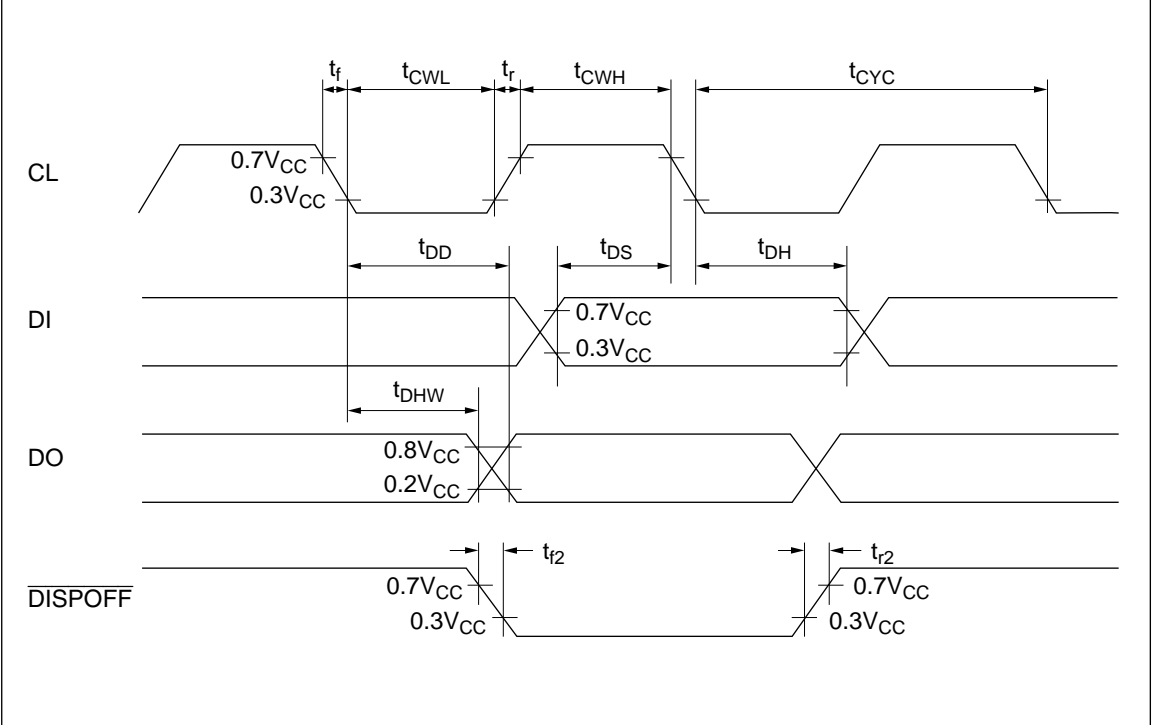


Figure 10 LCD Controller Interface Timing