HD66300T

(Horizontal Driver for TFT-Type LCD Color TV)

HITACHI

Description

The HD66300T is a horizontal driver used for TFT-type (Thin Film Transistor) LCD color TVs. Specifically, it drives the drain bus signals of a TFT-type LCD panel.

The HD66300T receives as input three video signals R, G, B, and their inverted signals $\overline{R}$, $\overline{G}$ and $\overline{B}$. Internal sample and hold circuitry then samples and holds these signals before outputting them via voltage followers to drive an TFT-type LCD panel.

The HD66300T can drive LCD panels from 480 × 240 pixels middle-resolution up to 720 × 480 pixels high-resolution. It has 120 LCD drive outputs and enables design of a compact LCD TV due to TCP (Tape Carrier Package) technology.

Features

- LCD drive outputs: 120
- Internal sample and hold circuits: 480 (4 circuits per output)
- Support of single-rate sequential drive mode and double-rate sequential drive mode
- Support of various types of color filter arrangements through an internal color sequence controller
- Vertical pixels: 240 (middle-resolution) or 480 (high-resolution)
- Horizontal pixels: 480 to 720
- Support of monodirectional connection mode and interleaved connection mode through a bidirectional shift register
- Dynamic range: 15 V_{PP}
- Power supply: +5 V and –15 V
- CMOS process

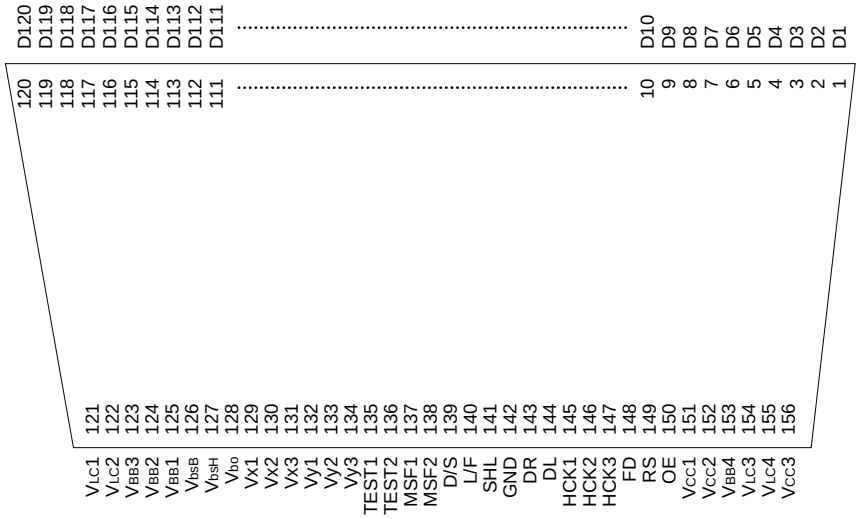
Ordering Information

Type No.	Package
HD66300T00	156-pin TCP

Note: The details of TCP pattern are shown in "The Information of TCP."

Hitachi semiconductor

Pin Arrangement



(Top view)

Note : This boes not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Connected to	Functions (Refer to)
D1 to D120	120	O	LCD panel	1
HCK1, HCK2, HCK3	3	I	Controller	2
DL, DR	2	I/O	Controller or next HD66300T	3
FD	1	I	Controller	4
RS	1	I	GND	5
OE	1	I	Controller	6
SHL	1	I	V_{CC} or GND	7
D/S	1	I	V_{CC} or GND	8
L/F	1	I	V_{CC} or GND	9
MSF1, MSF2	2	I	V_{CC} or GND	10
TEST1, TEST2	2	I	GND	11
Vx1, Vx2, Vx3, Vy1, Vy2, Vy3	6	I	Inverter	12
V_{bo}	1	I	Power source	13
V_{bsB}, V_{bsH}	2	I	Power source	14
$V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$	4	—	Power source	15
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$	3	—	Power source	16
GND	1	—	Power source	17
$V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$	4	—	Power source	18

Pin Functions

1. D1 to D120: These pins output LCD drive signals.

2. HCK1, HCK2, HCK3: These pins input three-phase clock pulses, which determine the signal sampling timing for sample and hold circuits.

3. DL, DR: These pins input or output data into or from the internal bidirectional shift register. The state of pin SHL determines whether these pins input or output data.

SHL	DL	DR
V_{CC}	Output	Input
GND	Input	Output

4. FD: This pin inputs the field determination signal, which allows the sample and hold circuitry and the shift matrix circuit to operate synchronously with TV signals, at its rising and falling edge.

FD = high: First field
FD = low: Second field

When a non-interlace signal is applied, it must be inverted every field.

When an interlace signal is applied in double-rate sequential drive mode with per-line inversion (mode 1, 2, 3), the signal must be set high in both fields. The signal must be set low, however, in each field's horizontal retrace period.

5. RS: This pin inputs a test signal and should be connected to pin GND.

6. OE: This pin inputs the signal which controls the controller of the shift matrix circuit; it changes the selection of a sample and hold circuit and the shift matrix (combination of color data), at its rising edge. It also switches the bias current of the output buffer, as shown in the following table.

OE	Bias Current of Output Buffer
High	Large current (determined by VbsB)
Low	Small current (determined by VbsH)

7. SHL: This pin selects the shift direction of the shift register.

SHL	Shift Direction
High	DL ← DR
Low	DL → DR

8. D/S: This pin selects the LCD drive mode.

D/S	Mode
High	Double-rate sequential drive mode
Low	Single-rate sequential drive mode

9. L/F: This pin selects the inversion mode of LCD drive signals.

L/F	Mode
High	Per-line inversion mode
Low	Per-field inversion mode

10. MSF1, MSF2: These pins select the function of the shift matrix circuit; they should be set according to both the type of color filter arrangement on a TFT-type LCD panel and the drive mode.

Filter Arrangement	Drive Mode	MSF1	MSF2
Diagonal mosaic pattern	Single-rate	GND	V_{CC}/GND*
	Double-rate	GND	V_{CC}/GND*
Vertical stripe pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	V_{CC}
Unicolor triangular pattern	Single-rate	V_{CC}	V_{CC}
	Double-rate	V_{CC}	GND
Bicolor triangular pattern	Single-rate	V_{CC}	GND
	Double-rate	V_{CC}	GND

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

Note: * Refer to table 2 and timing charts of each mode.

11. TEST1, TEST2: These pins input test signals and should be connected to pin GND.

12. Vx1, Vx2, Vx3, Vy1, Vy2, Vy3: Video signals are applied to these pins; positive video signals are connected to pins Vxi and negative video signals to pins Vyi.

13. V_{bo}: Bias voltage is applied to this pin for the differential amplifier in the sample and hold circuitry.

14. V_{bsB}, V_{bsH}: Bias voltage is applied to this pin for the two power sources of the output buffer.

VbsB: The voltage for driving a capacitive load
VbsH: The voltage for holding the output voltage

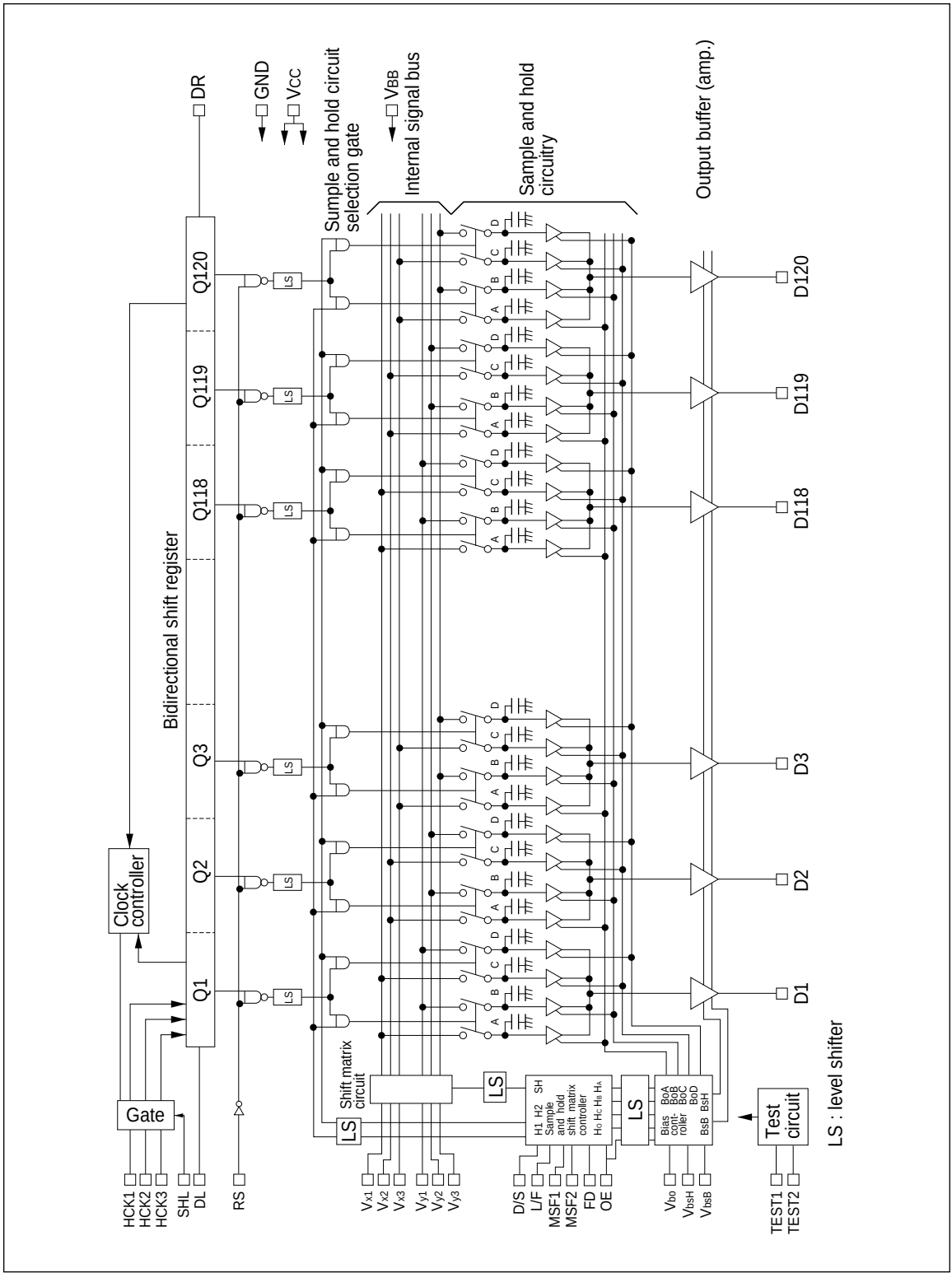
15. $V_{LC}1$, $V_{LC}2$, $V_{LC}3$, $V_{LC}4$: +5 V LCD drive voltage is applied to these pins.

16. $V_{CC}1$, $V_{CC}2$, $V_{CC}3$: +5 V is applied to these pins for the logic and the analog units.

17. GND: 0 V is applied to this pin for the logic unit.

18. $V_{BB}1$, $V_{BB}2$, $V_{BB}3$, $V_{BB}4$: –15 V is applied to these pins for the LCD drive unit.

Internal Block Diagram



Block Functions

Shift Register: The shift register generates the sampling timing for video signals. It is driven by three-phase clocks HCK1, HCK2, and HCK3, whose phases are different from each other by 120°; each clock determines the sampling timing for one color signal so that three clocks support the three color signals R, G, and B. The shift direction of this register can be changed.

Level Shifter: The level shifter changes 5-V signals into 20-V signals.

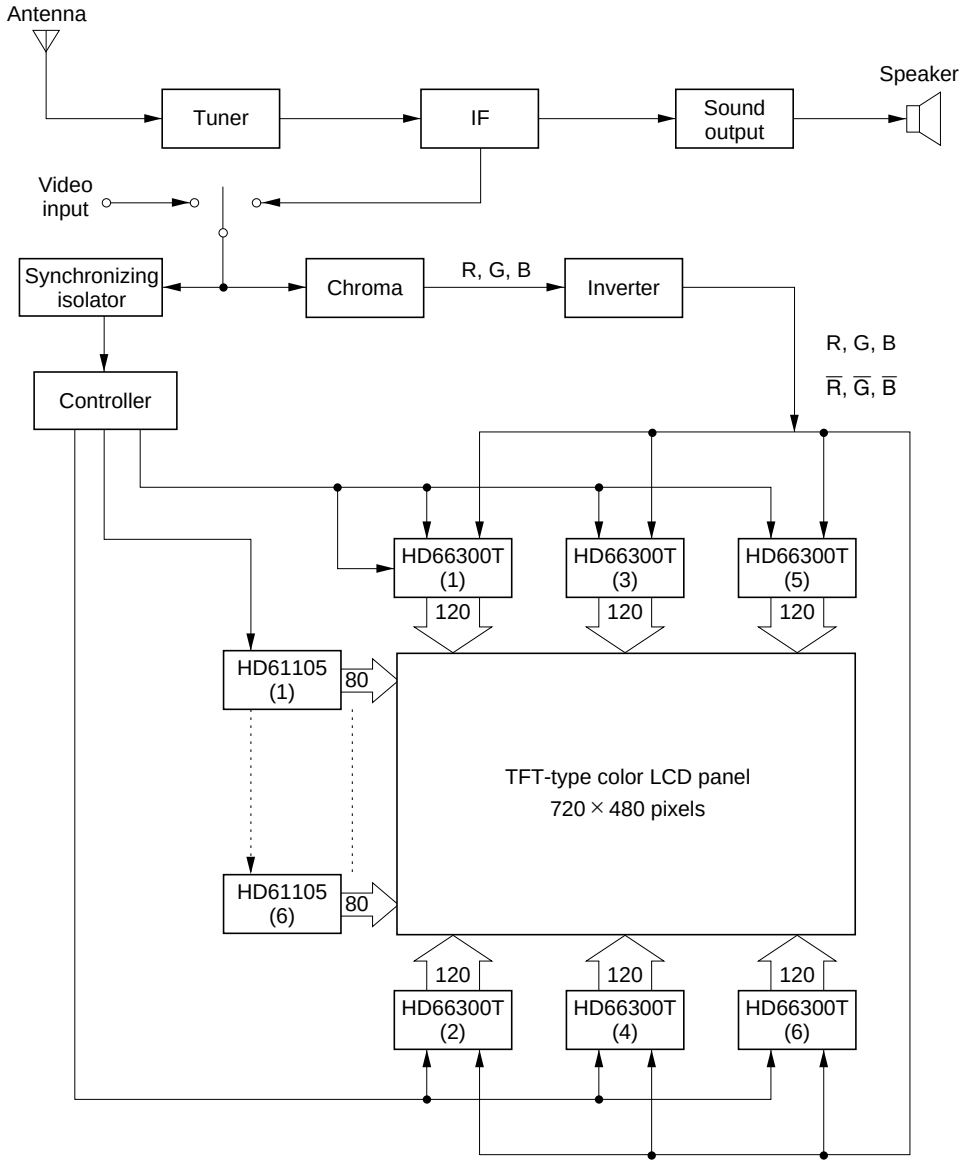
Sample and Hold Circuitry: In double-rate sequential drive mode, two sample and hold circuits are selected to sample video signals during one horizontal scanning period out of the four circuits attached to one LCD drive signal. One of the two selected circuits is read out in the first half of the following horizontal scanning period, and the other selected circuit is read out in the second half. While the two circuits are being read out, the other two circuits sample signals and are alternately read out in the same procedure mentioned above.

In single-rate sequential drive mode, one sample and hold circuit samples a signal during one horizontal scanning period, and is read out in the following horizontal scanning period. While it is being read out, one circuit out of the other three samples a signal.

Shift Matrix Circuit: The shift matrix circuit, a color sequence controller, changes over the sampled video signal every horizontal scanning period.

Output Buffer: The output buffer consists of a source follower circuit and can change the through-rate of an output signal by changing the external bias voltage.

System Block Configuration Example



Example of HD66300T Connection to LCD Panel

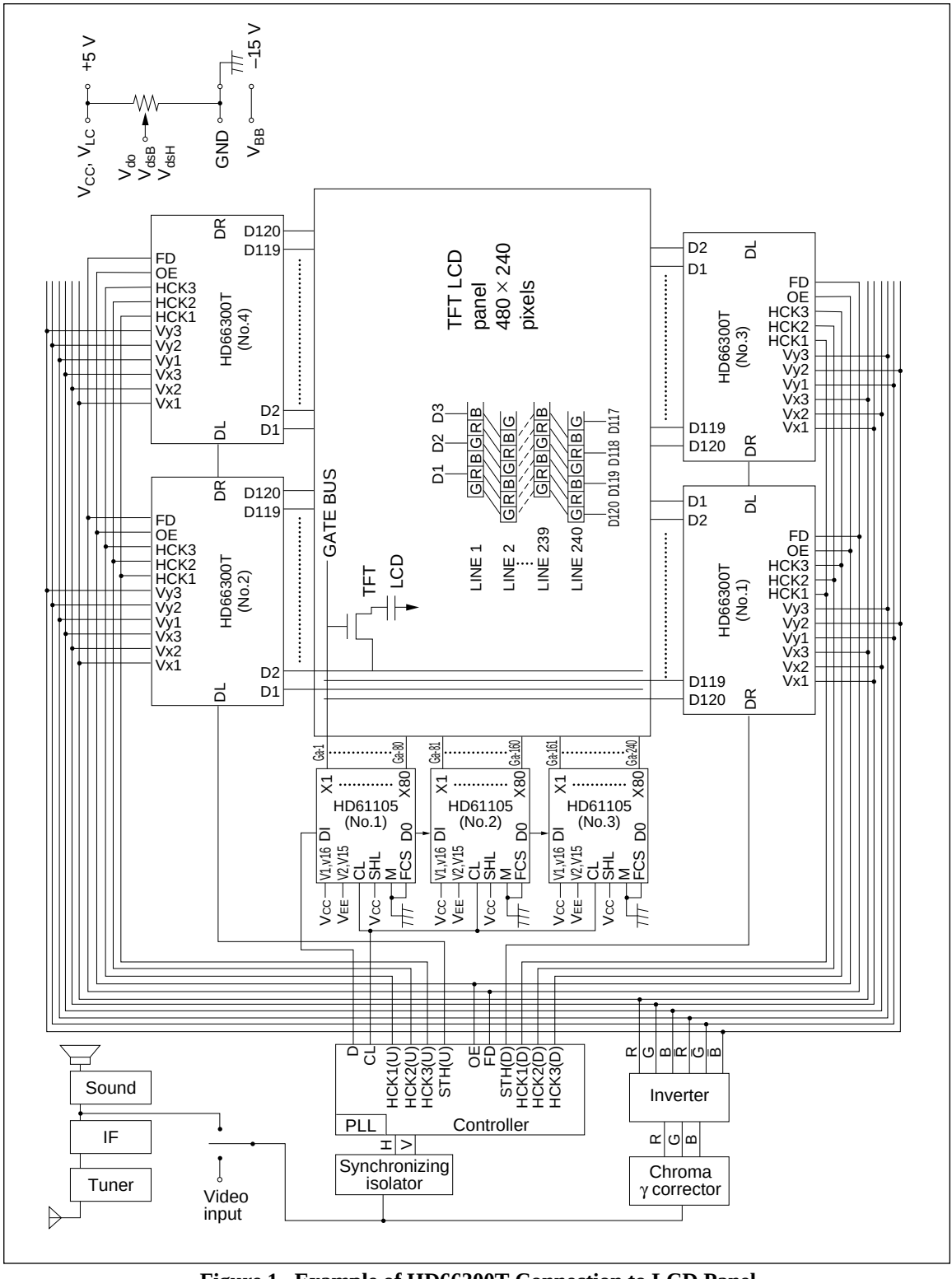
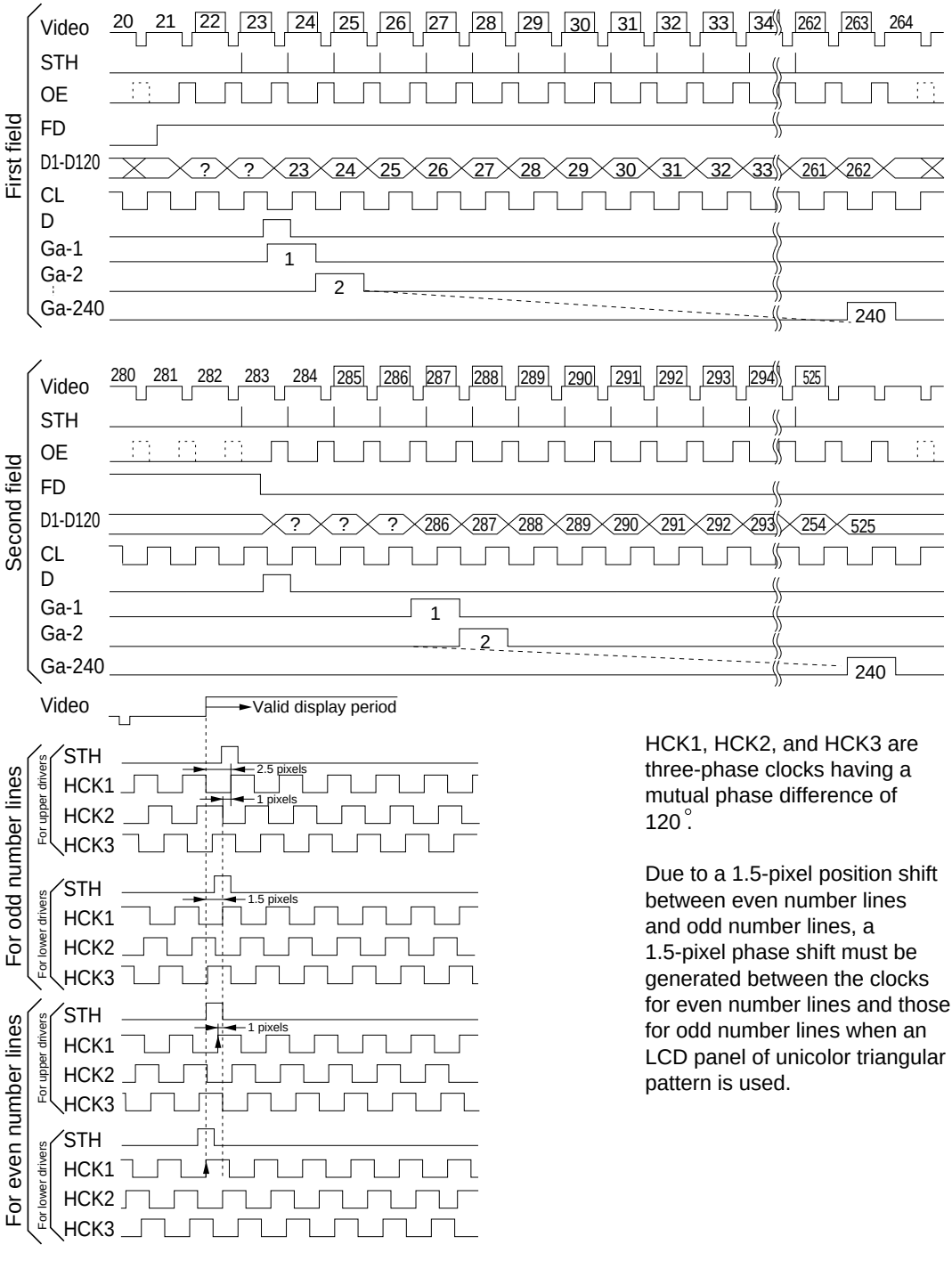


Figure 1 Example of HD66300T Connection to LCD Panel



HCK1, HCK2, and HCK3 are three-phase clocks having a mutual phase difference of 120°.

Due to a 1.5-pixel position shift between even number lines and odd number lines, a 1.5-pixel phase shift must be generated between the clocks for even number lines and those for odd number lines when an LCD panel of unicolor triangular pattern is used.

Figure 2 Timing Chart

Functional Description

Screen Size

Number of horizontal pixels:

- 120, 240, 360, 600, and 720 in monodirectional connection mode
- 240, 480, and 720 in bidirectional connection mode

Number of vertical pixels:

- 240 in single-rate sequential drive mode
- 480 in double-rate sequential drive mode

Single-Rate Sequential Drive Mode and Double-Rate Sequential Drive Mode

Single-Rate Sequential Drive Mode: A typical TV signal* has 525 scanning lines, 480 of which are part of the valid display period. In interlace scanning mode, 480 scanning lines are equally divided into a first field and a second field.

In single-rate sequential drive mode, a 240-pixel-high LCD panel is used. 240 scanning lines of the first and second fields of the TV signal are respectively assigned to the 240 lines of the LCD panel.

One line of an LCD panel is driven every horizontal scanning period in this mode.

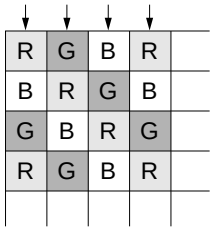
Double-Rate Sequential Drive Mode: To obtain a high-resolution display, a 480-pixel-high LCD panel is used. If 480 scanning lines are respectively assigned to the 480 lines of the LCD panel, the LCD alternating frequency becomes 15 Hz, which causes flickering and degrades display quality. To avoid this problem, the following method is employed. In the first field, the first scanning line is assigned to the first and second lines of the LCD panel, the second scanning line is assigned to the third and fourth lines, and so on. In the second field, the first scanning line is assigned to the second and third lines, the second scanning line is assigned to the fourth and fifth lines, and so on.

Two lines of an LCD panel are driven every horizontal scanning period in this mode.

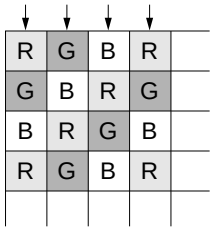
Note: * Refer to the index for the further information of NTSC TV system signals and LCD.

Supportable Types of Color Filter Arrangements

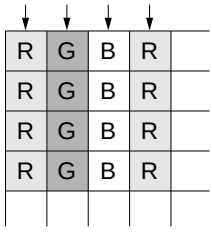
The order and timing for the HD66300T to output color signals depend on the color filter arrangement on a TFT-type LCD panel. The HD66300T can support TFT-type LCD panels having the following color filter arrangements by specifying the operation of the internal color sequence controller and by changing the external signals to be supplied.



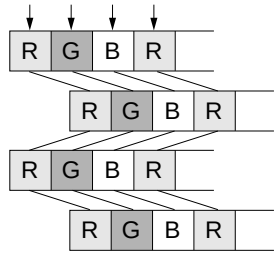
(a) Diagonal from top-left to bottom-right mosaic pattern



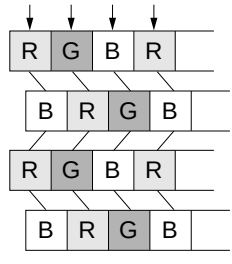
(b) Diagonal from top-left to bottom-left mosaic pattern



(c) Vertical stripe pattern



(d) Unicolor triangular pattern



(e) Bicolor triangular pattern

Figure 3 Supportable Types of Color Filter Arrangements

Mode Setting Pins

Mode setting pins MSF1, MSF2, and D/S must be set according to both the type of color filter arrangement on the TFT-type LCD panel and the drive mode (single-rate sequential drive mode or double-rate sequential drive mode). These pins activate the internal color sequence controller, which changes the sequence of color video signals corresponding to each sample and hold circuit and allows the LSI to output color data in the right order for the LCD panel being used.

Per-Field Inversion and Per-Line Inversion

The inversion mode of LCD drive signals can be selected by pin L/F.

Per-Field Inversion (Available with L/F = Low)

In a certain field, all LCD drive signals have one polarity and in the following field, they all have the inverted polarity.

Per-Line Inversion (Available with L/F = High)

In a certain field, all LCD drive signals have positive polarity in odd number lines and negative polarity in even number lines, while in the following field, the situation is reversed, that is, negative polarity in odd number lines and positive polarity in even number lines.

Table 1 Mode Setting Pins

Filter Arrangement	Drive Mode	D/S	MSF1	MSF2	Referential Timing Charts
Diagonal mosaic pattern	Single-rate	GND	GND	V_{CC}, GND	MODES 15, 16, 18, and 19
	Double-rate	V_{CC}	GND	V_{CC}, GND	MODES 1, 2, 5, 6, 8, 9, 12, and 13
Vertical stripe pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	V_{CC}	MODES 3, 7, 10, and 14
Unicolor triangular pattern	Single-rate	GND	V_{CC}	V_{CC}	MODES 17 and 20
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11
Bicolor triangular pattern	Single-rate	GND	V_{CC}	GND	MODE 17
	Double-rate	V_{CC}	V_{CC}	GND	MODES 4 and 11

Single-rate: Single-rate sequential drive mode
Double-rate: Double-rate sequential drive mode

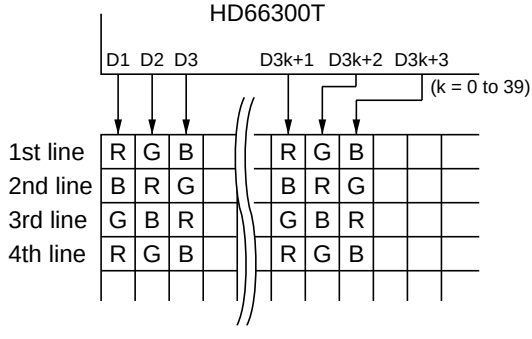
Interface

Video Signals Connection

Video signals must be connected to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3; in principle, positive video signals R, G, and B signals must be input to pins Vx1, Vx2, and Vx3, and negative video signals $\overline{R}$, $\overline{G}$, and $\overline{B}$ to pins Vy1, Vy2, and Vy3. For actual connection between an LCD panel and the LCD drive signal output pins, refer to the following example.

In the Case of Diagonal from Top-Left to Bottom-Right Mosaic Pattern

This example describes the case in which an LCD panel having a diagonal from top-left to bottom-right mosaic pattern is driven in double-rate sequential drive mode and monodirectional connection mode.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → B → G → R →
D2 (= D3k + 2)	G → R → B → G →
D3 (= D3k + 3)	B → G → R → B →

The Signal Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	Vx1 → Vx3 → Vx2 → Vx1 →
D2 (= D3k + 2)	Vx2 → Vx1 → Vx3 → Vx2 →
D3 (= D3k + 3)	Vx3 → Vx2 → Vx1 → Vx3 →

(Refer to MODE 5)

The Connection of Signals

Signal	Color
Vx1	R
Vx2	G
Vx3	B
Vy1	$\overline{R}$
Vy2	$\overline{G}$
Vy3	$\overline{B}$

In the Case of Diagonal from Top-Right to Bottom-Left Mosaic Pattern, Vertical Stripe Pattern

The same procedure for video signal connection applies to the case in which a TFT-type LCD panel having a diagonal from top-right to bottom-left mosaic pattern or a vertical stripe pattern is used, as well as to the cases where a panel of any pattern is used through the bidirectional connection mode.

Triangular Pattern, Single-Rate Sequential Drive Mode

The following procedures are required when a panel of unicolor or bicolor triangular pattern is used:

1. Unicolor Triangular Pattern, Single-Rate Sequential Drive Mode

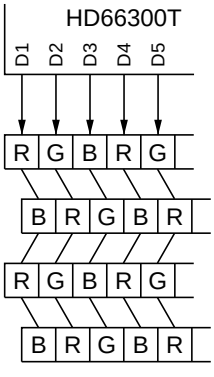
   The clock phase must be changed every line because of the 1.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)

   The connection of signals here is the same as that described above.

2. Bicolor Triangular Pattern, Single-Rate Sequential Drive Mode

   The clock phase must be changed every line because of the 0.5-pixel phase shift between even number lines and odd number lines. (Refer to the explanation of sampling clocks.)

   The connection of video signals in the second field must be changed from that in the first field. See the following tables.



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → B → R → B →
D2 (= D3k + 2)	G → R → G → R →
D3 (= D3k + 3)	B → G → B → G →

The Signal Sequence for Each Output Pin

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to Mode 17)

The Connection of Signal in Each Field

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	2nd Field	1st Field	2nd Field
Vx1	R	$\overline{B}$	R	B
Vx2	G	$\overline{R}$	G	R
Vx3	B	$\overline{G}$	B	G
Vy1	B	$\overline{R}$	$\overline{B}$	$\overline{R}$
Vy2	R	$\overline{G}$	$\overline{R}$	$\overline{G}$
Vy3	G	$\overline{B}$	$\overline{G}$	$\overline{B}$

Triangular Pattern, Double-Rate Sequential Drive Mode

Changing the phase of the sampling clocks is sufficient when the panel is driven in single-rate sequential drive mode. However, when the panel is driven in double-rate sequential drive mode, the above countermeasure does not work, since the display data for two lines is sampled at one time here. Consequently, delaying the input video signal for a time period corresponding to the shift between pixels is required.

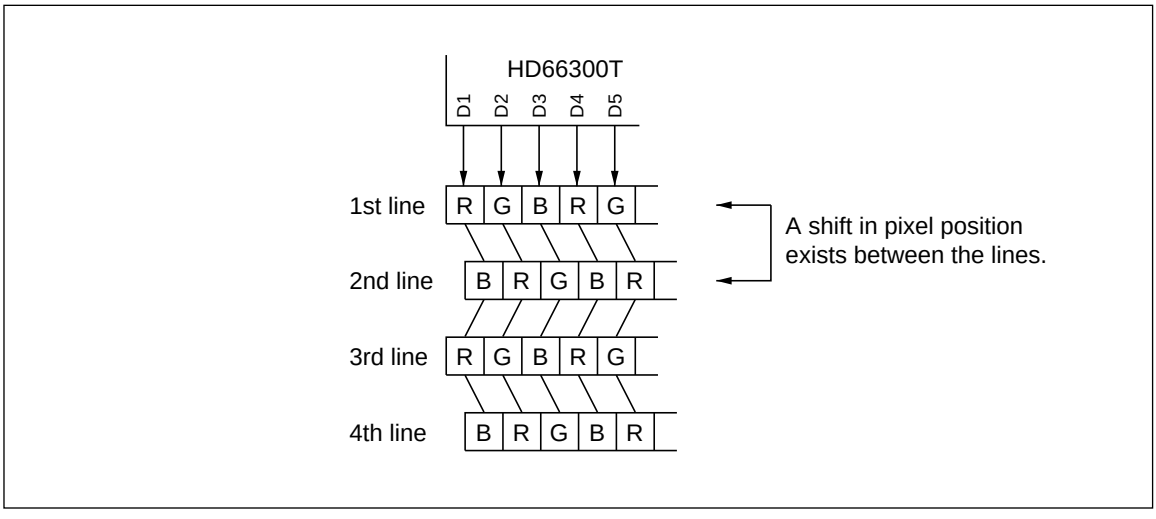


Figure 4 Pixel Position Shift (Triangular Pattern, Double-Rate Sequential Drive Mode)

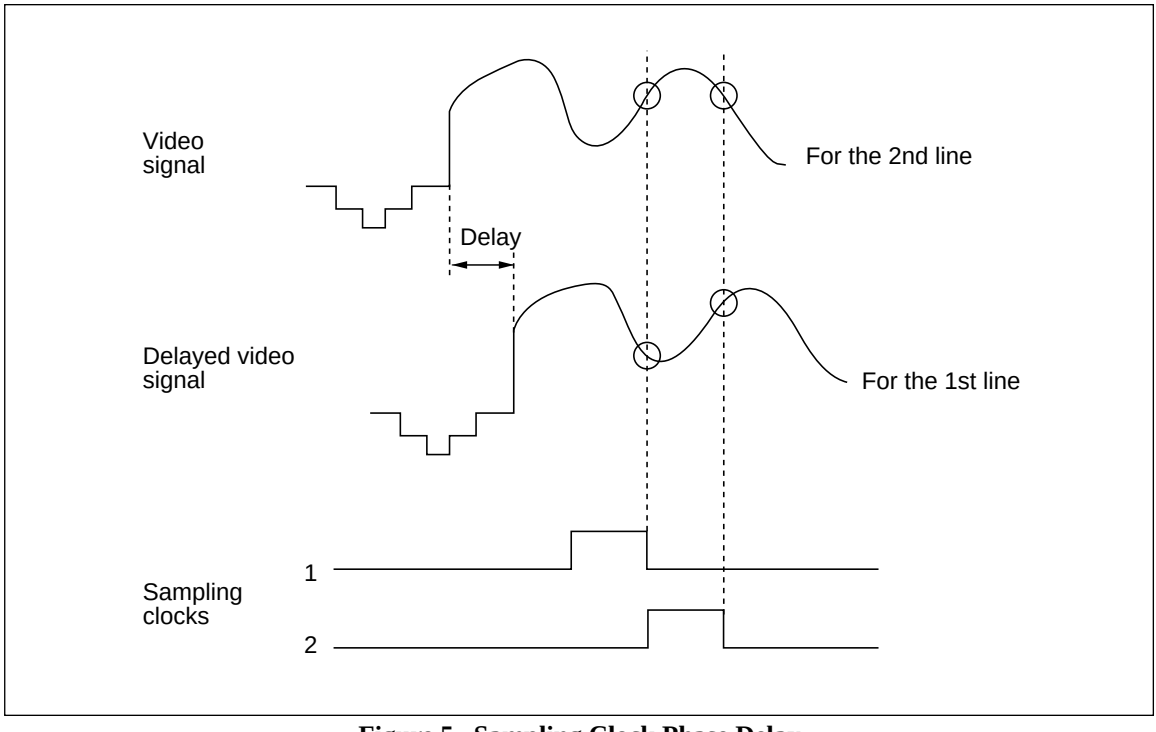
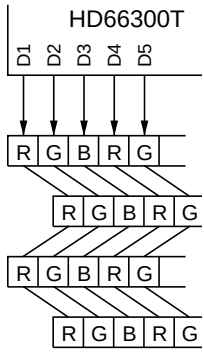


Figure 5 Sampling Clock Phase Delay

1. Unicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R → R → R → R →
D2 (= D3k + 2)	G → G → G → G →
D3 (= D3k + 3)	B → B → B → B →

The Signal Sequence for Each Output Pin (In Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In Non-Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

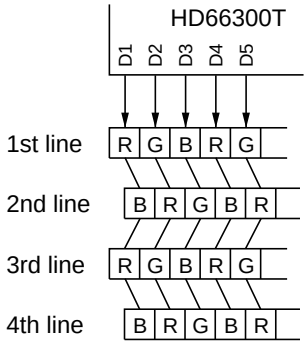
The Connection of Signals in Each Field (In Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	$\overline{R}$	Delayed R	R
Vx2	Delayed G	$\overline{G}$	Delayed G	G
Vx3	Delayed B	$\overline{B}$	Delayed B	B
Vy1	R	Delayed $\overline{R}$	$\overline{R}$	Delayed $\overline{R}$
Vy2	G	Delayed $\overline{G}$	$\overline{G}$	Delayed $\overline{G}$
Vy3	B	Delayed $\overline{B}$	$\overline{B}$	Delayed $\overline{B}$

The Connection of Signals in Each Field (In Non-Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	R	$\overline{R}$	$\overline{R}$	R
Vy2	G	$\overline{G}$	$\overline{G}$	G
Vy3	B	$\overline{B}$	$\overline{B}$	B

2. Bicolor Triangular Pattern, Double-Rate Sequential Drive Mode



The Color Sequence for Each Output Pin

Output Pin	Color Sequence
D1 (= D3k + 1)	R →R →R →R →
D2 (= D3k + 2)	G→R →G →R →
D3 (= D3k + 3)	B →G →B →G →

The Signal Sequence for Each Output Pin (In Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vy1 → Vx1 → Vy1 → Vx1 →
	D2 (= D3k + 2)	Vy2 → Vx2 → Vy2 → Vx2 →
	D3 (= D3k + 3)	Vy3 → Vx3 → Vy3 → Vx3 →

(Refer to MODE 4)

The Signal Sequence for Each Output Pin (In Non-Interlace Mode)

	Output Pin	Signal Sequence
1st field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →
2nd field	D1 (= D3k + 1)	Vx1 → Vy1 → Vx1 → Vy1 →
	D2 (= D3k + 2)	Vx2 → Vy2 → Vx2 → Vy2 →
	D3 (= D3k + 3)	Vx3 → Vy3 → Vx3 → Vy3 →

(Refer to MODE 11)

The Connection of Signals in Each Field (in Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	$\overline{B}$	Delayed R	B
Vx2	Delayed G	$\overline{R}$	Delayed G	R
Vx3	Delayed B	$\overline{G}$	Delayed B	G
Vy1	B	Delayed $\overline{R}$	$\overline{B}$	Delayed $\overline{R}$
Vy2	R	Delayed $\overline{G}$	$\overline{R}$	Delayed $\overline{G}$
Vy3	G	Delayed $\overline{B}$	$\overline{G}$	Delayed $\overline{B}$

The Connection of Signals in Each Field (in Non-Interlace Mode)

	Per-Field Inversion Mode (L/F = Low)		Per-Line Inversion Mode (L/F = High)	
	1st Field	**2nd Field**	**1st Field**	**2nd Field**
Vx1	Delayed R	Delayed $\overline{R}$	Delayed R	Delayed $\overline{R}$
Vx2	Delayed G	Delayed $\overline{G}$	Delayed G	Delayed $\overline{G}$
Vx3	Delayed B	Delayed $\overline{B}$	Delayed B	Delayed $\overline{B}$
Vy1	B	$\overline{B}$	$\overline{B}$	B
Vy2	R	$\overline{R}$	$\overline{R}$	R
Vy3	G	$\overline{G}$	$\overline{G}$	G

Connection to LCD Panels

There are two modes of connecting HD66300T chips to an LCD panel:

1) monodirectional connection mode
2) bidirectional connection mode

In the former mode, the HD66300Ts are set on either the upper side or lower side of the panel, while in the latter mode, the HD66300Ts are set on both sides and the upper drivers and the lower drivers are alternately connected to each pixel-column.

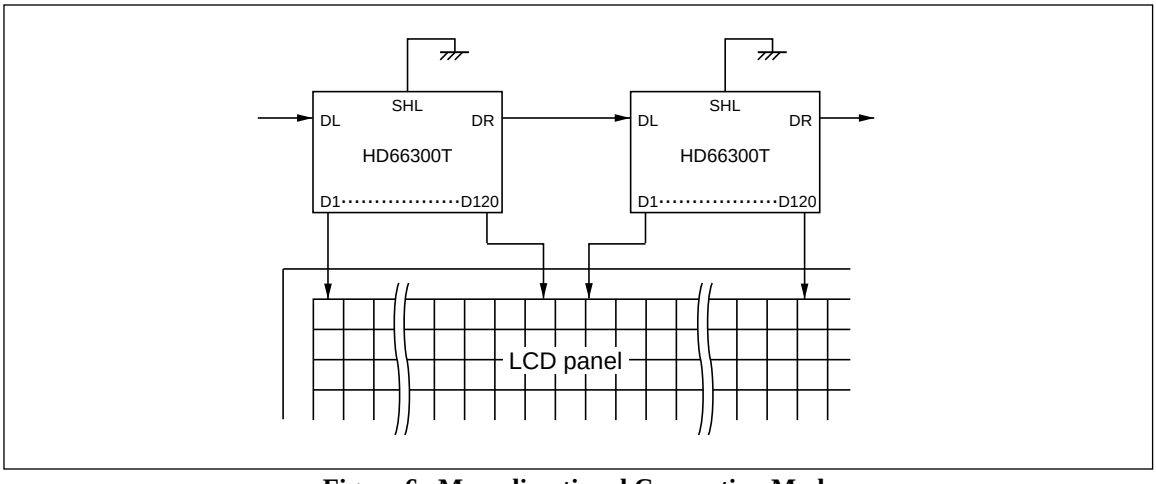


Figure 6 Monodirectional Connection Mode

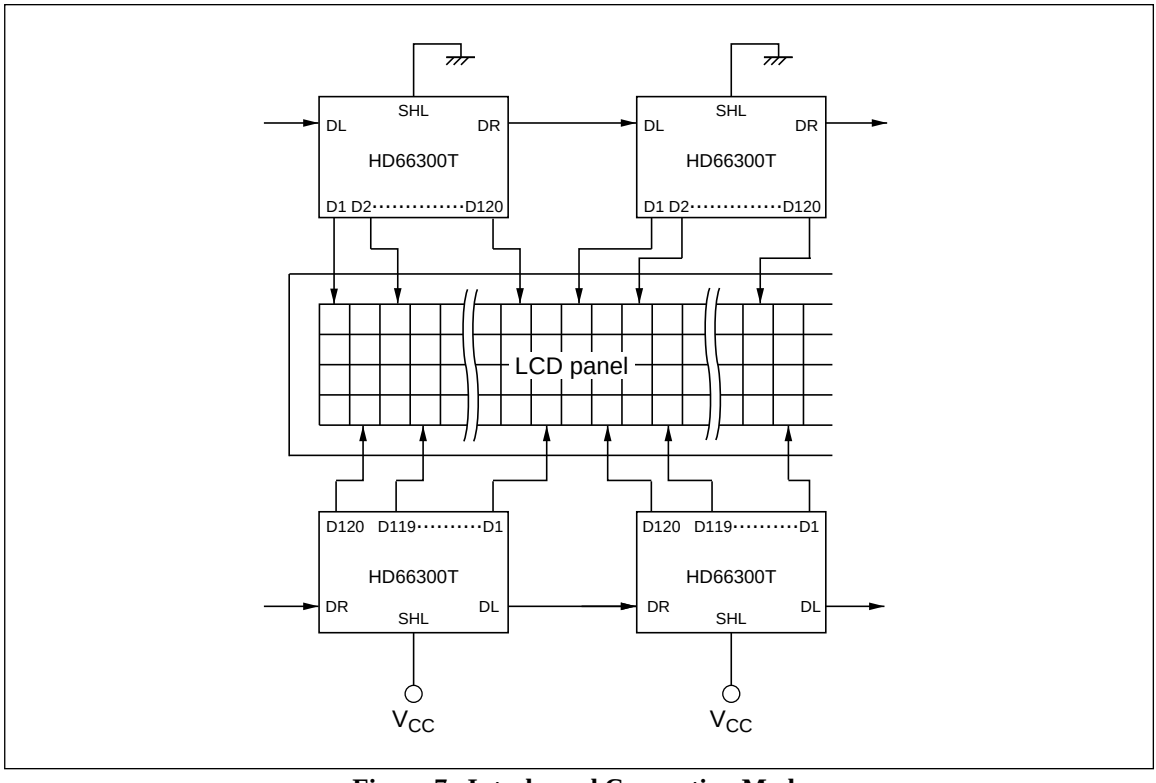


Figure 7 Interleaved Connection Mode

Internal Operation

The HD66300T has four sample and hold circuits for each outputs as shown in the block diagram, and its internal bidirectional shift register controls which circuits to sample data.

It has three-phase shift clocks with mutual phase difference of 120° to drive the shift register, which enables driving an LCD panel with mosaic pattern and triangular pattern.

The operation of sample and hold circuits and sampling operation are described below followed by the description of the relationship between three-phase shift clock phases and frequencies.

After the above description, determination of bias voltage is described; bias voltage controls driving characteristics of a differential amplifier and output buffer of the sample and hold circuits.

Finally, the OE and FD signals are described; they determine the operation of the sample and hold shift matrix circuit. Timing charts for each mode follow the description.

Sample and Hold Circuitry

Operation of Sample and Hold Circuitry

The HD66300T has four sample and hold circuits A, B, C, and D per LCD drive signal output. Sample and hold circuit pair A and B is supplied with the same sampling clock pulses as circuit pair C and D. One of the signals output by these circuits is connected to an output driver.

These sample and hold circuits repeat sampling and outputting of signals alternately to drive an TFT-type LCD panel.

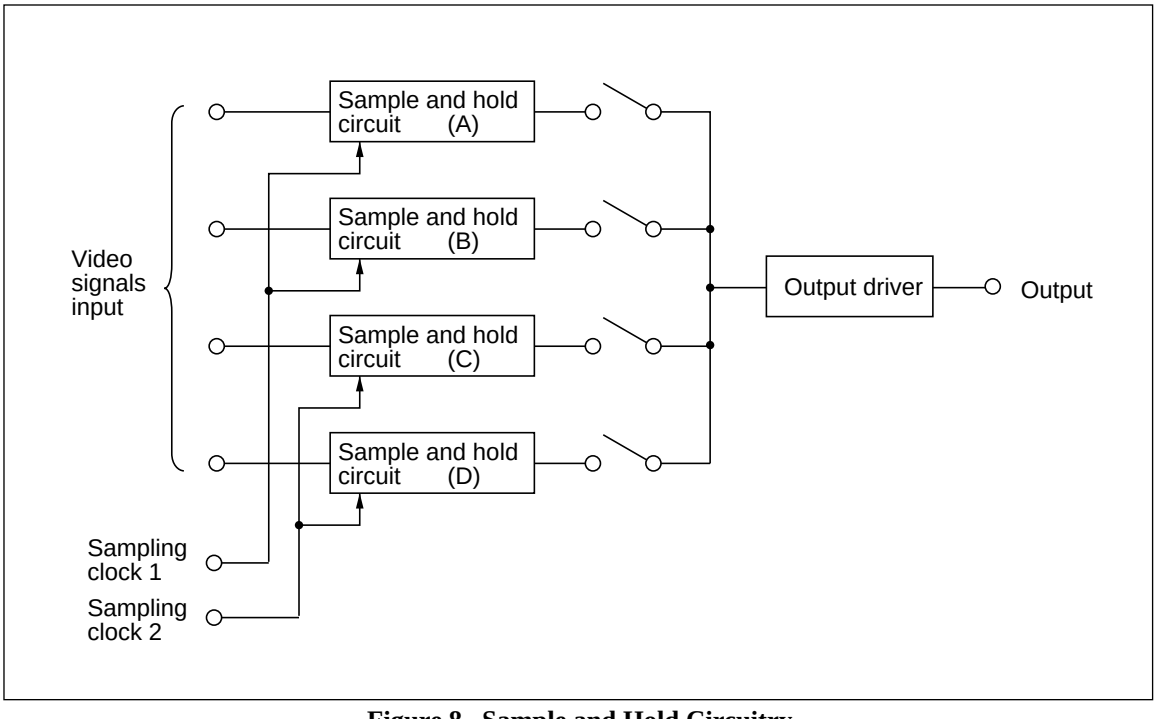


Figure 8 Sample and Hold Circuitry

In single-rate sequential drive mode, sample and hold circuits A and D are alternately used; circuits B and C perform sampling operation, but are not used since they are not connected to the output driver.

In single-rate sequential drive mode, one sample and hold circuit samples the signal during one horizontal scanning period, and outputs it as an LCD drive signal in the following horizontal scanning period.

In double-rate sequential drive mode, all sample and hold circuits A, B, C, and D are alternately used.

In double-rate sequential drive mode, two sample and hold circuits sample two signals during one horizontal scanning period, and output one of them as an LCD drive signal in the first half of the following horizontal scanning period, and output the other signal in the second half.

The following shows the timing charts of sampling and outputting operation.

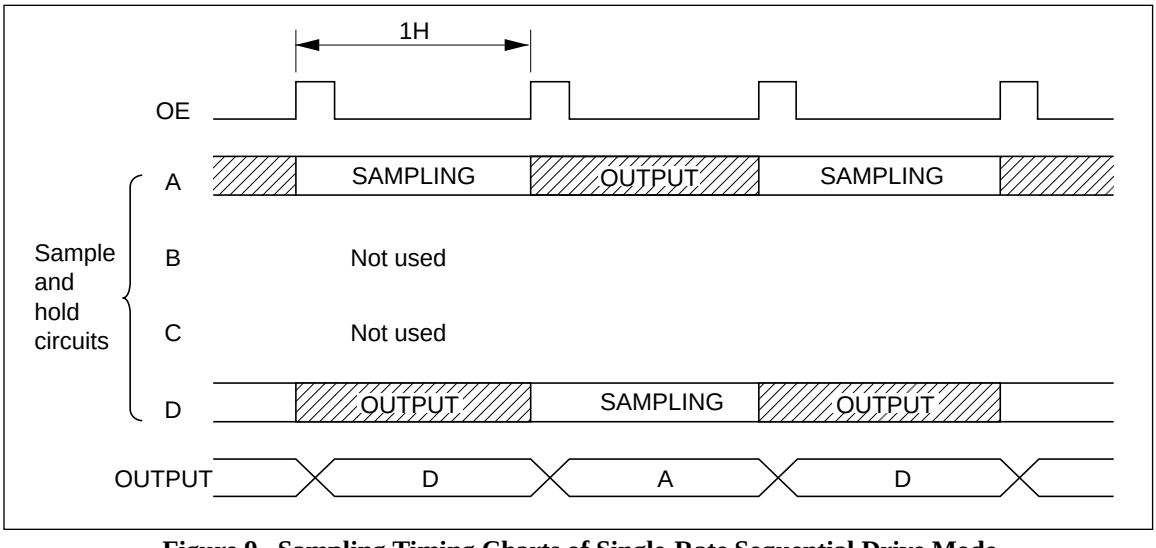


Figure 9 Sampling Timing Charts of Single-Rate Sequential Drive Mode

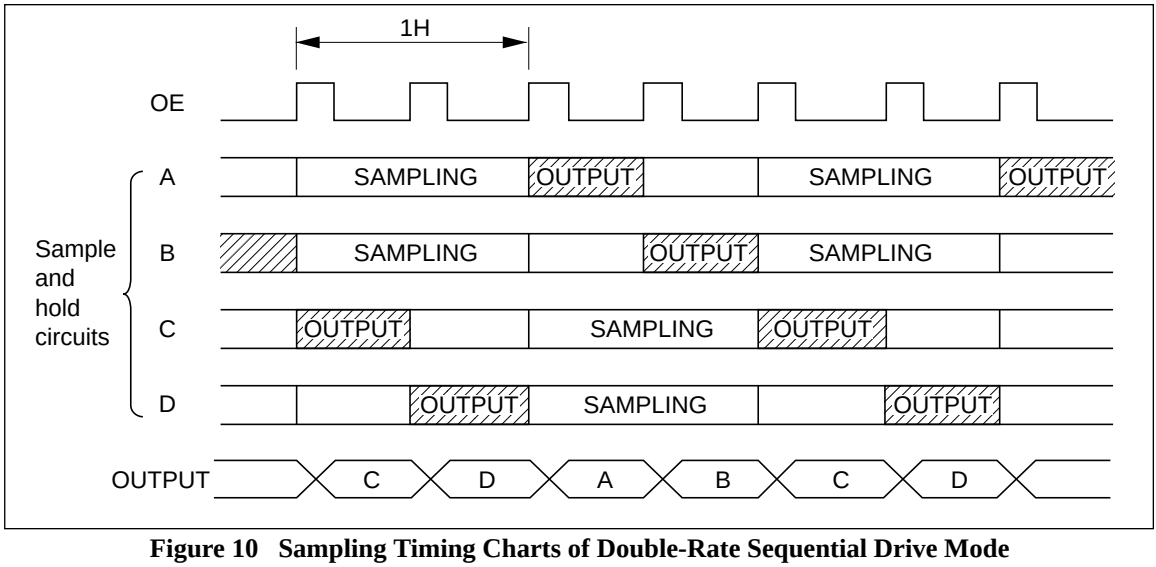


Figure 10 Sampling Timing Charts of Double-Rate Sequential Drive Mode

Sampling Operation

The HD66300T has a bidirectional shift register composed of 120 bits and each bit of the shift register generates the sampling pulses to control the sampling operation of the four sample and hold circuits connected to each LCD drive signal output pin. When a bit of the shift register is 1, the corresponding sample and hold circuits are in the sampling state; when it is 0, the corresponding sample and hold circuits are in the hold state. Consequently, shifting a 1 into the shift register activates in turn the sample and hold circuits corresponding to each LCD drive signal output pin.

Figure 11 is a shift register sketch illustrating the relationship between the shift register and the shift clocks HCK1, HCK2, and HCK3. Note that the order of sampling pulse generation depends on the state of pin SHL. D1 corresponds to DL and D120 to DR.

Figure 12 is a timing chart of sampling pulses generated by the shift register.

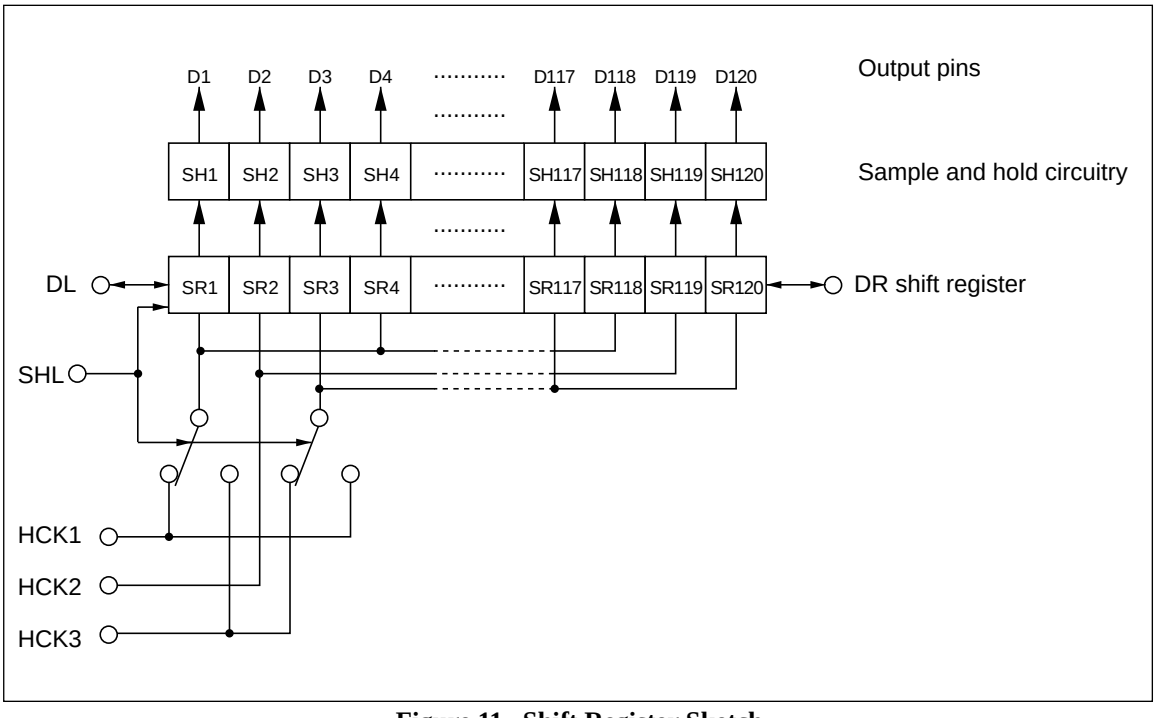
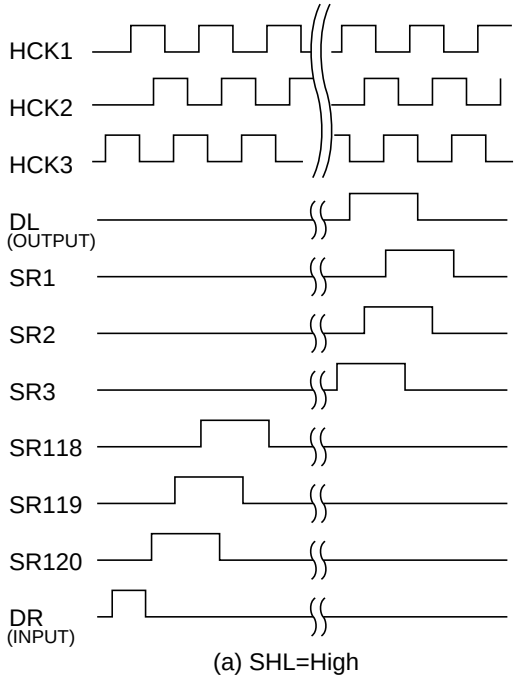
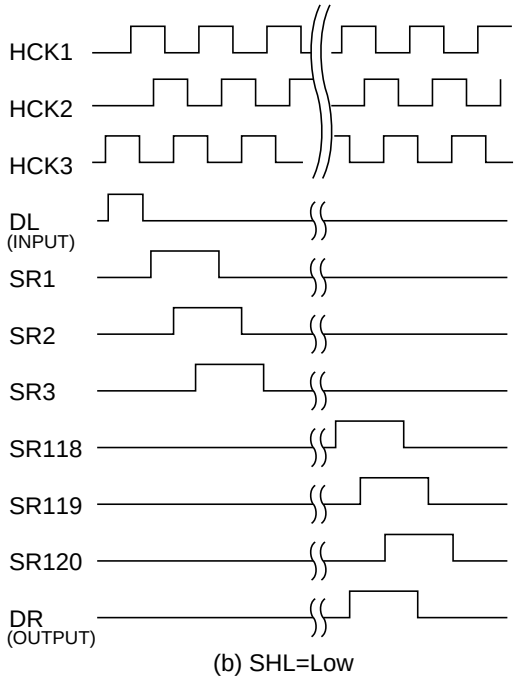


Figure 11 Shift Register Sketch



(a) SHL=High



(b) SHL=Low

Figure 12 Sampling Pulse Timing Chart

Three-Phase Shift Clocks

Three-Phase Shift Clocks and Sample Start Signal: Shift clocks HCK1, HCK2, and HCK3, which are operation clocks for the shift register, must be three-phase clocks with 50-percent duty. The HCK2 clock must be generated 120° after the HCK1 clock, and the HCK3 clock 240° after the HCK1 clock. Sampling operation starts when 1 is input from pin DL or DR at a rising edge of the HCK1 clock pulse.

In monodirectional connection mode, all the HD66300T chips must be supplied with the same three-phase shift clock pulses. In interleaved connection mode, the frequency of the three-phase shift clocks must be half of that in monodirectional connection mode, and the phase shift between the upper drivers clocks and the lower drivers clocks must be one pixel.

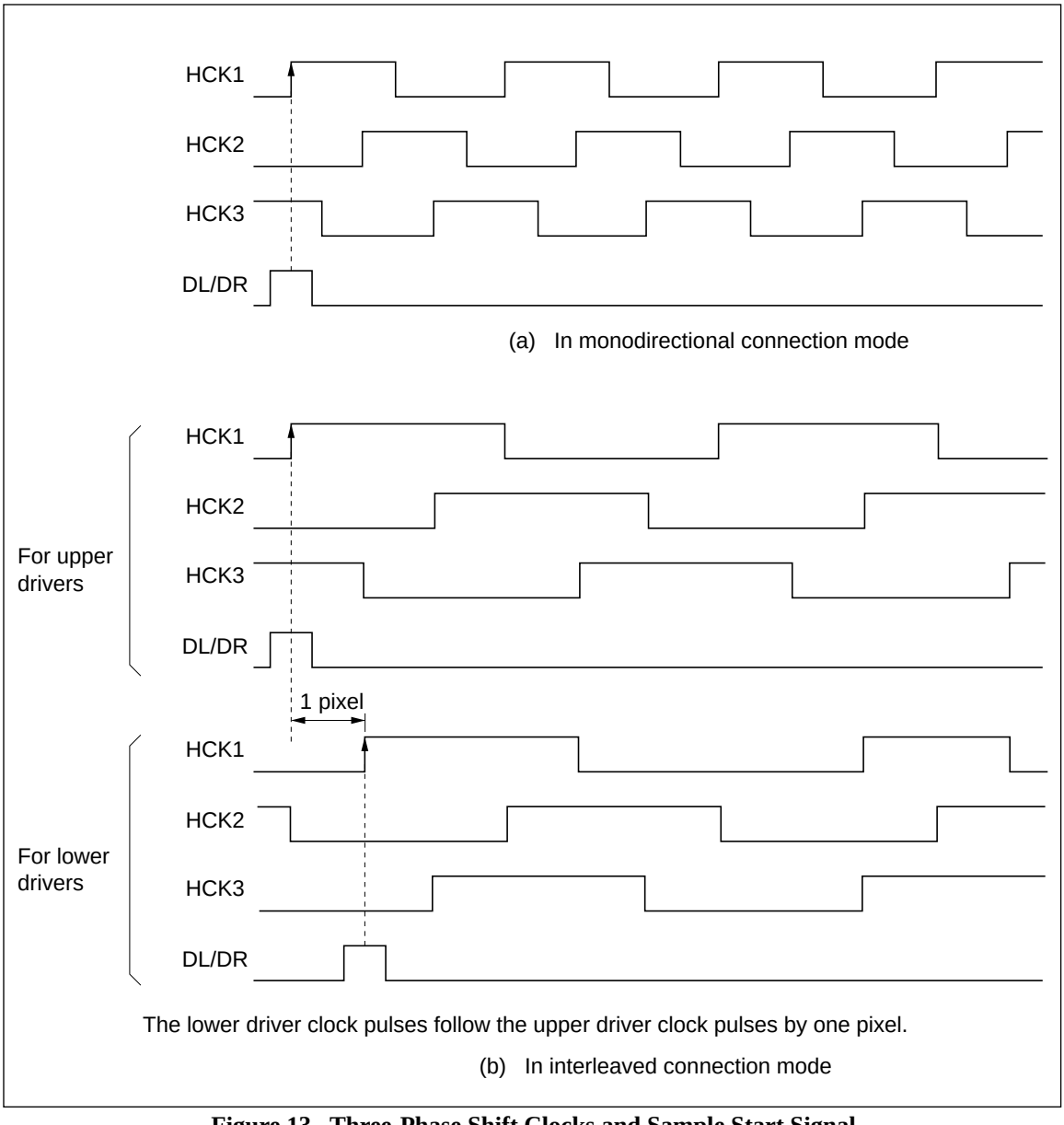


Figure 13 Three-Phase Shift Clocks and Sample Start Signal

Some position shift exists between the pixels of even number lines and those of odd number lines for LCD panels having triangular patterns. This requires generating a phase shift between the three-phase clocks for even number lines and those for odd number lines. The required phase shift is 1.5 pixels for LCD panels having a unicolor triangular pattern, while it is 0.5 pixels for those having a bicolor triangular pattern.

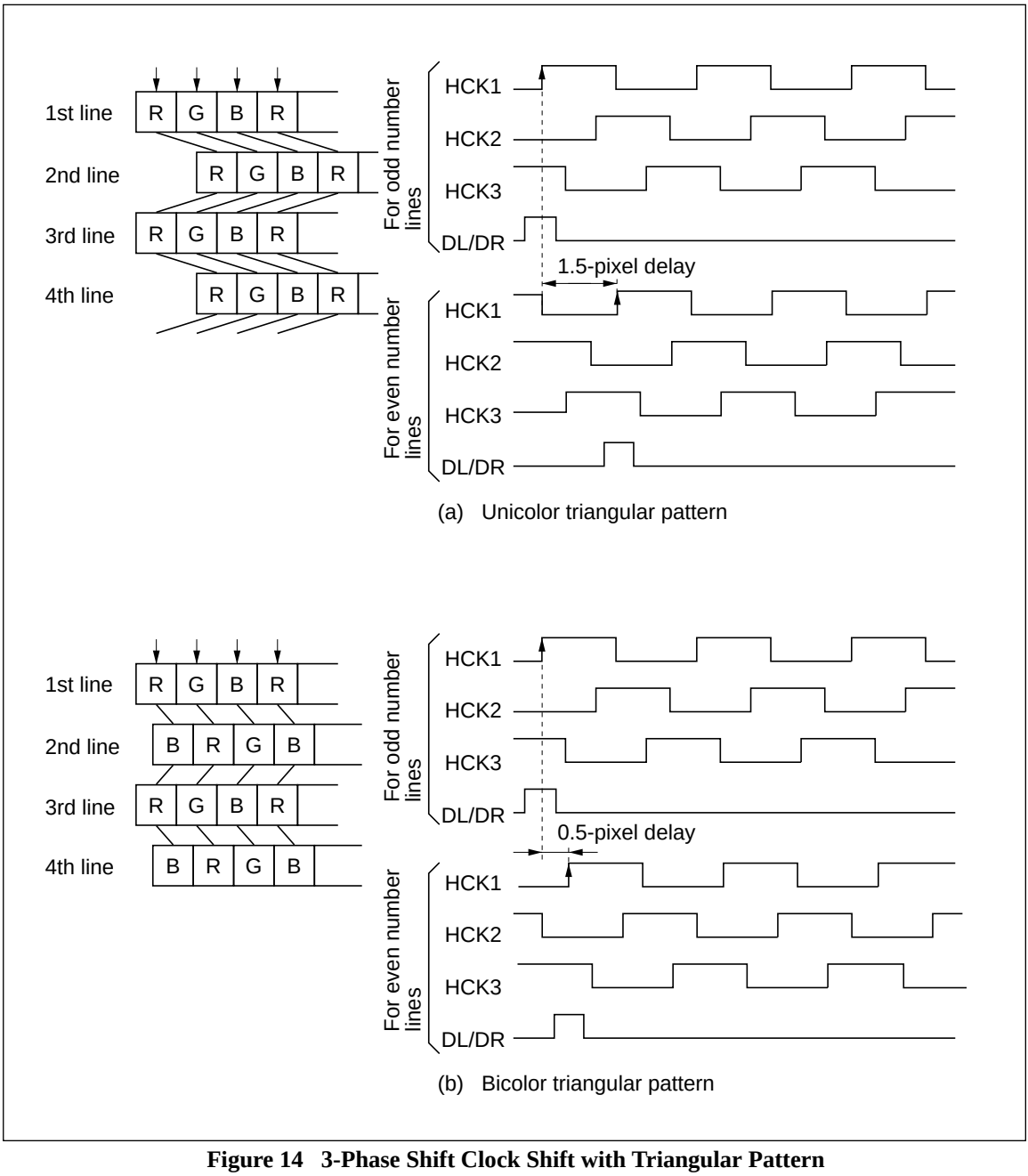


Figure 14 3-Phase Shift Clock Shift with Triangular Pattern

How to Generate Three-Phase Shift Clocks: Three-phase shift clocks can be generated by dividing the base clock, which is generated from a horizontal synchronizing clock, through the use of a frequency multiplier such as a PLL circuit.

The number of horizontal pixels of the LCD panel and the valid display ratio determines the base clock frequency f.

If the number of horizontal pixels is 480 and the valid display ratio is 95% in the NTSC system, the base clock frequency f is about 9.59 MHz according to the following equation.

$$\begin{aligned} f &= (1/\text{valid display period}) \times (\text{no. of horizontal pixels/valid display ratio}) \\ &= 480/(52.7\ \mu\text{sec} \times 0.95) \\ &= 9.59\ (\text{MHz}) \end{aligned}$$

The three-phase clocks can be generated by dividing f by 3 (in the monodirectional connection mode) or 6 (in the bidirectional connection mode).

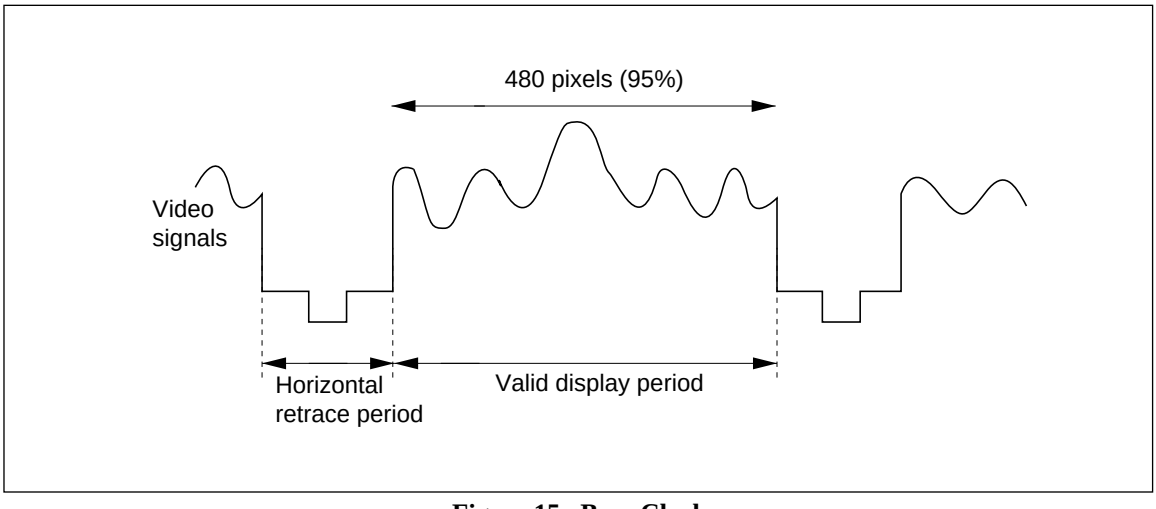


Figure 15 Base Clock

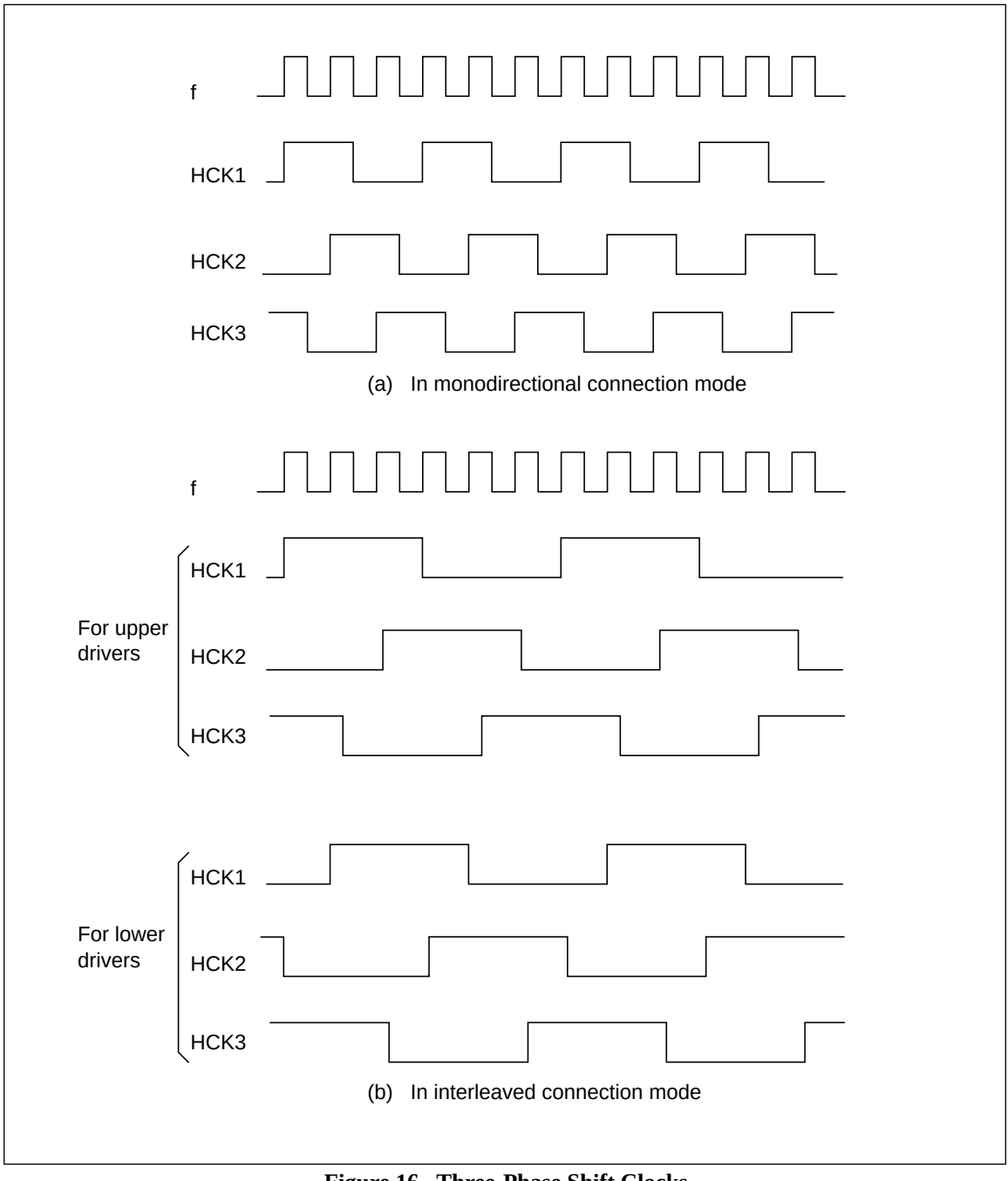


Figure 16 Three-Phase Shift Clocks

Bias Voltage

Voltages V_{bsB} , V_{bsH}, and V_{bo} control the drive capability of the output buffer and differential amplifier. Here the LSI must be used in the range of

$$V_{CC} - 4.0\ V \le V_{bsB}\ ,\ V_{bsH}\ ,\ V_{bo} \le V_{CC} - 2.0\ V$$

V_{bsB} controls the drive current capability of the output buffer when OE is high (IV_{sB}) and V_{bsH} controls the leakage correction current of when OE is low (IV_{sH}). Figure 17 and figure 18 show the relationship between IV_{sB} and V_{bsB} and the relationship between IV_{sH} and V_{bsH}, respectively.

V_{bsB} and V_{bsH} should be to an appropriate level for the electrical characteristics of the LCD panel used.

The rise time (t_{DDR}) and the fall time (t_{DDF}) of the output buffer depend on the input level of V_{bsB}.

Figure 19 shows the relationship between t_{DDR}, t_{DDF} and V_{bsB}.

V_{bo} controls the bias current of the differential amplifier (IV_{bo}).

Figure 20 shows the relationship between the rise and fall times (t_{DDR}, t_{DDF}) of the output buffer and V_{bo}.

V_{bo} should be adjusted to an appropriate level for the electrical characteristics of the LCD panel used.

The increase of total current consumption is 120 times larger than that of IV_{bsB}, IV_{bsH} and IV_{bo}, because figure 17, 18 and 21 each shows the case of one output and HD66300T has 120 outputs.

Figure 17, 18, 19, 20 and 21 are just for reference and do not guarantee the characteristics.

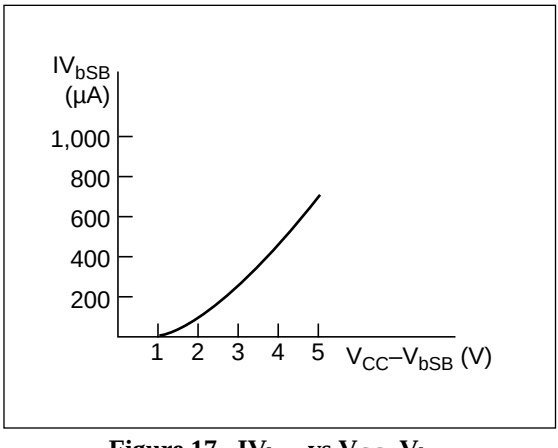


Figure 17 IV_{bsB} vs V_{CC}–V_{bsB}

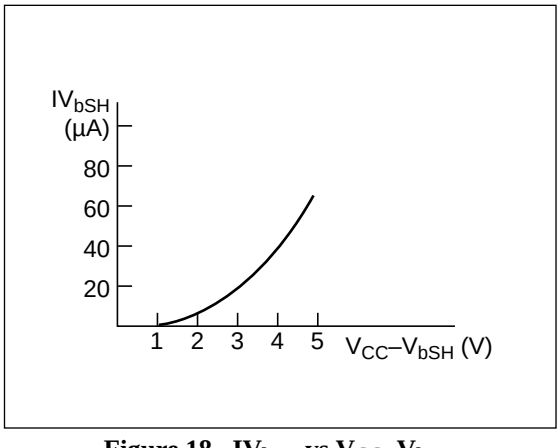


Figure 18 IV_{bsH} vs V_{CC}–V_{bsH}

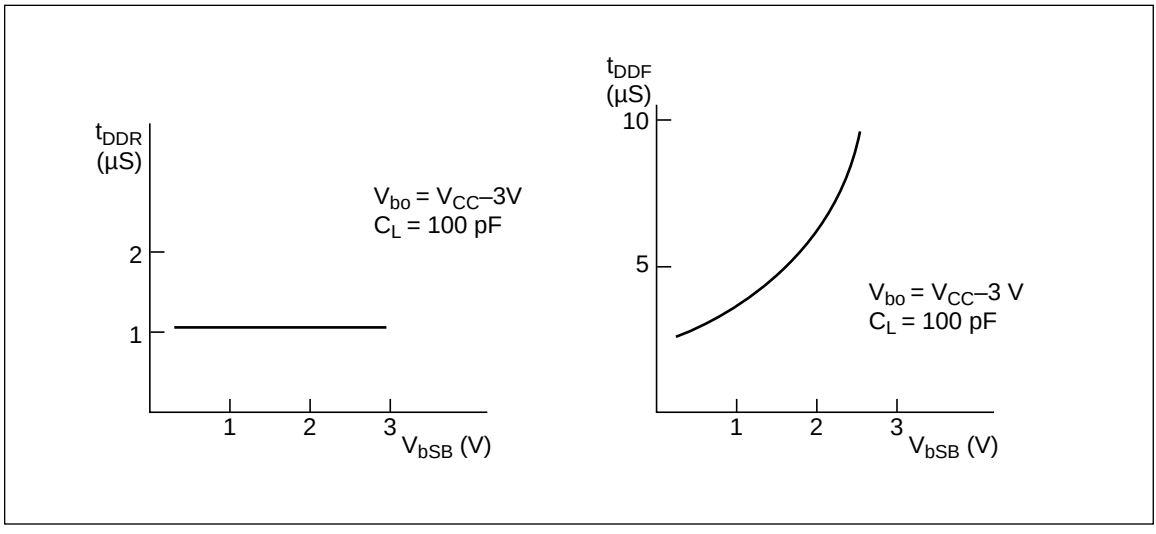


Figure 19 t_{DDR}, t_{DDF} vs V_{bsB}

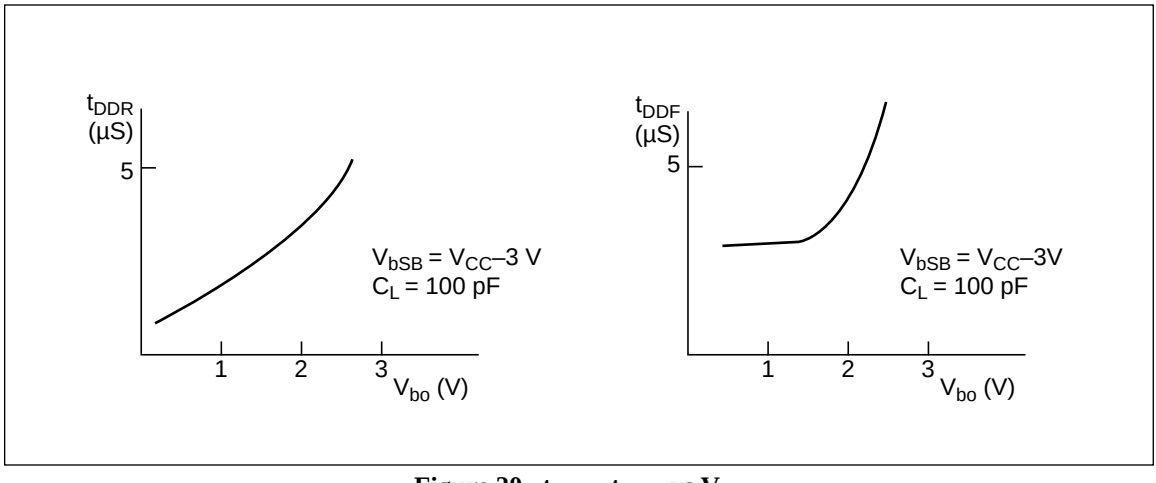


Figure 20 t_{DDR}, t_{DDF} vs V_{bo}

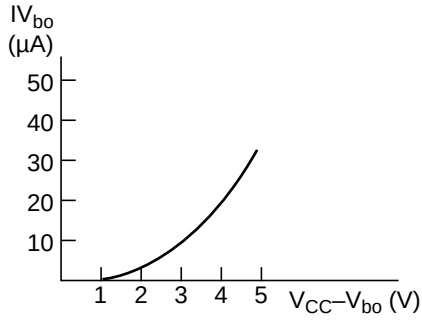


Figure 21 IV_{bo} vs V_{CC}–V_{bo}

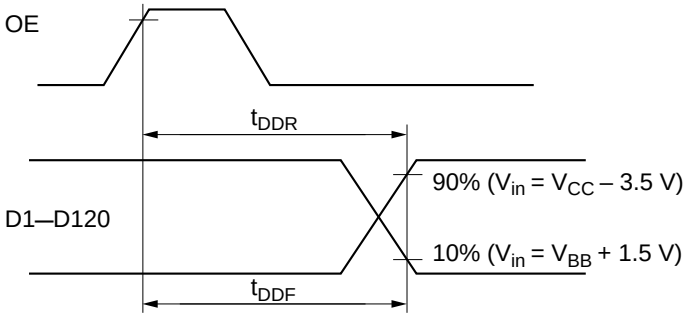


Figure 22 Definition of t_{DDR} and t_{DDF}

OE Signal

The OE signal has the following functions:

Clock for Internal Circuits: Controls the sample and hold circuitry and the controller of the shift matrix circuit, and switches the output signal at the OE signal rising edge.

Switching of Drive Capability of the Output Buffer: Determines the current drive capability of the output buffer;

OE = high: Drives with large current (300 µA, typ)
OE = low: Drives with small current (20 µA, typ)

This function allows the output buffer to operate with large current during the transition of an output signal, thus shortening its falling time. At the same time it allows the output buffer to operate with small current while an output signal is stable, lowering current consumption.

The drive current is controlled by bias voltages V_{bsB} (large current) and V_{bsH} (small current).

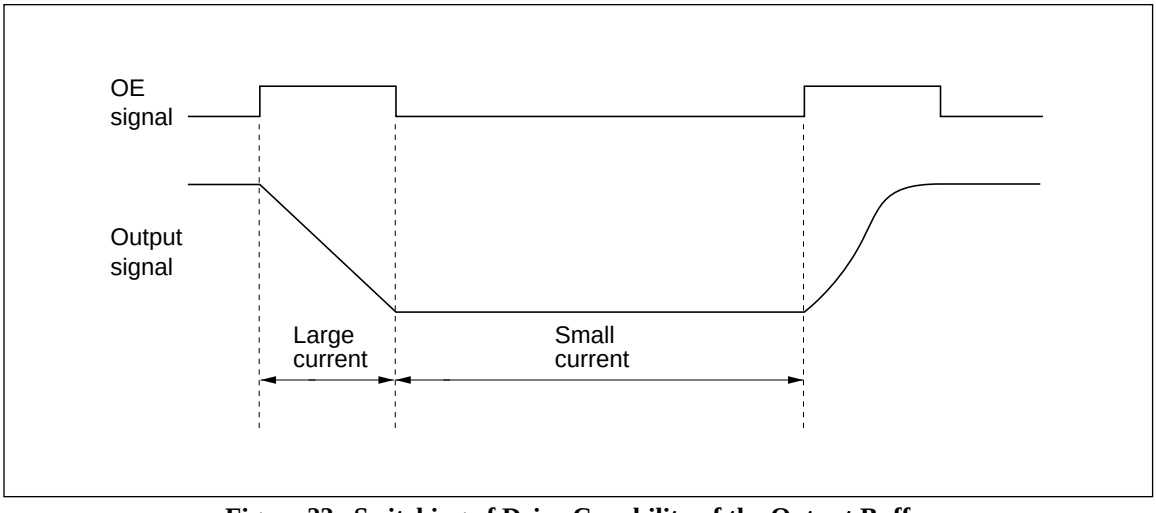


Figure 23 Switching of Drive Capability of the Output Buffer

FD Signal

The FD signal is the field determination signal; a field is determined by the state of this signal at the rising edge of the OE signal. This signal synchronizes the internal controllers with TV signals.

The order of outputting signals is determined at the fourth rising edge of the OE signal after the rising or falling edge of the FD signal in double-rate sequential drive mode, while it is determined at the third rising edge in single-rate sequential drive mode; herein after, as long as the FD signal is not changed, signals will be output in the determined order at most every 12 pulses of the OE signal in double-rate sequential drive mode, while at most every 6 pulses in single-rate sequential drive mode.

The FD signal should usually be high in the first field and low in the second field. In some modes, however, it should be high in both fields, but low for at least one-pulse time period of the OE signal during the horizontal scanning period.

The order of outputting signals and the timing of inputting the FD signal vary depending on the mode. For more details, refer to the appropriate timing charts.

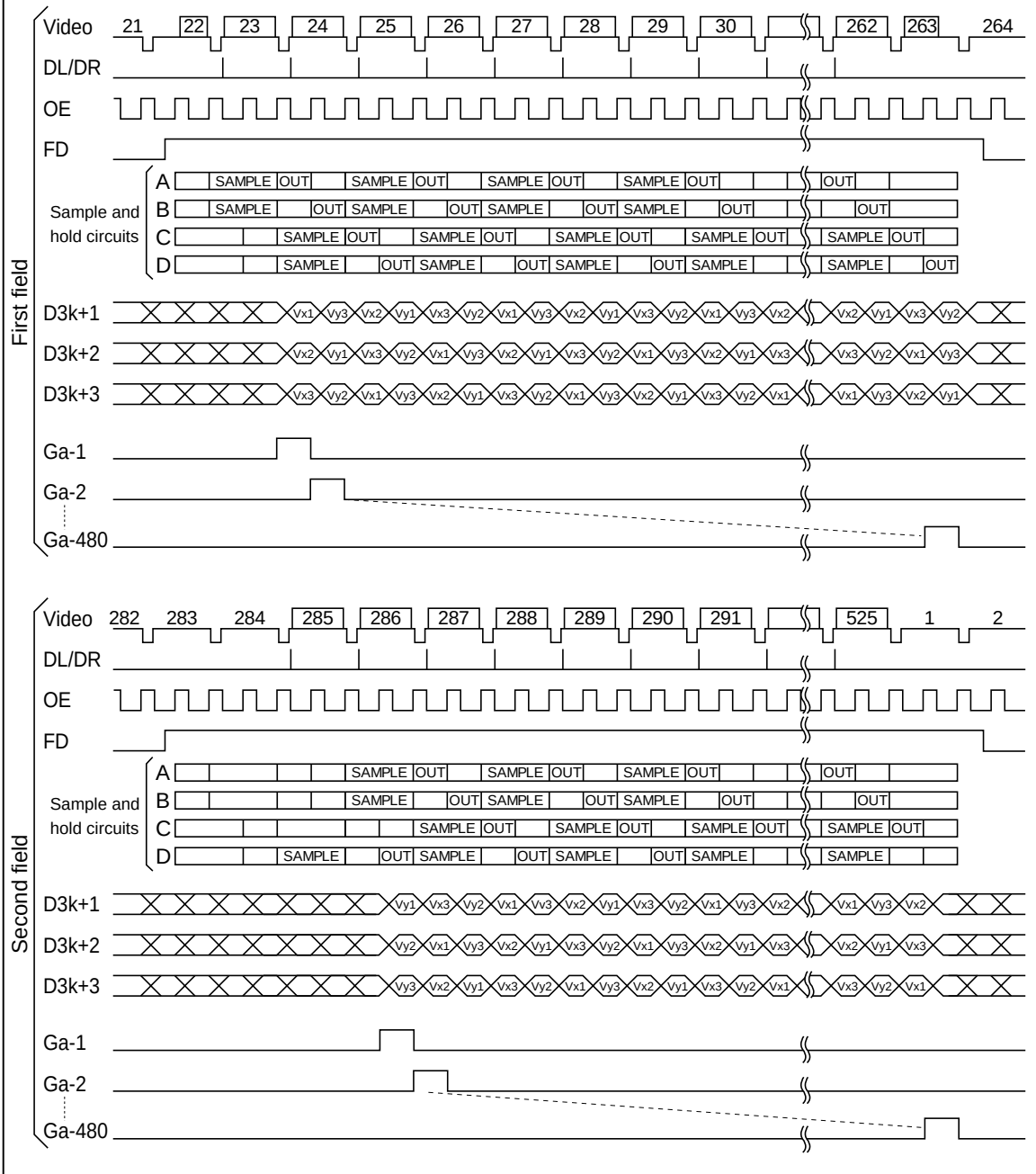
Timing Charts for Each Mode

Table 2 Reference Timing Charts for Each Mode

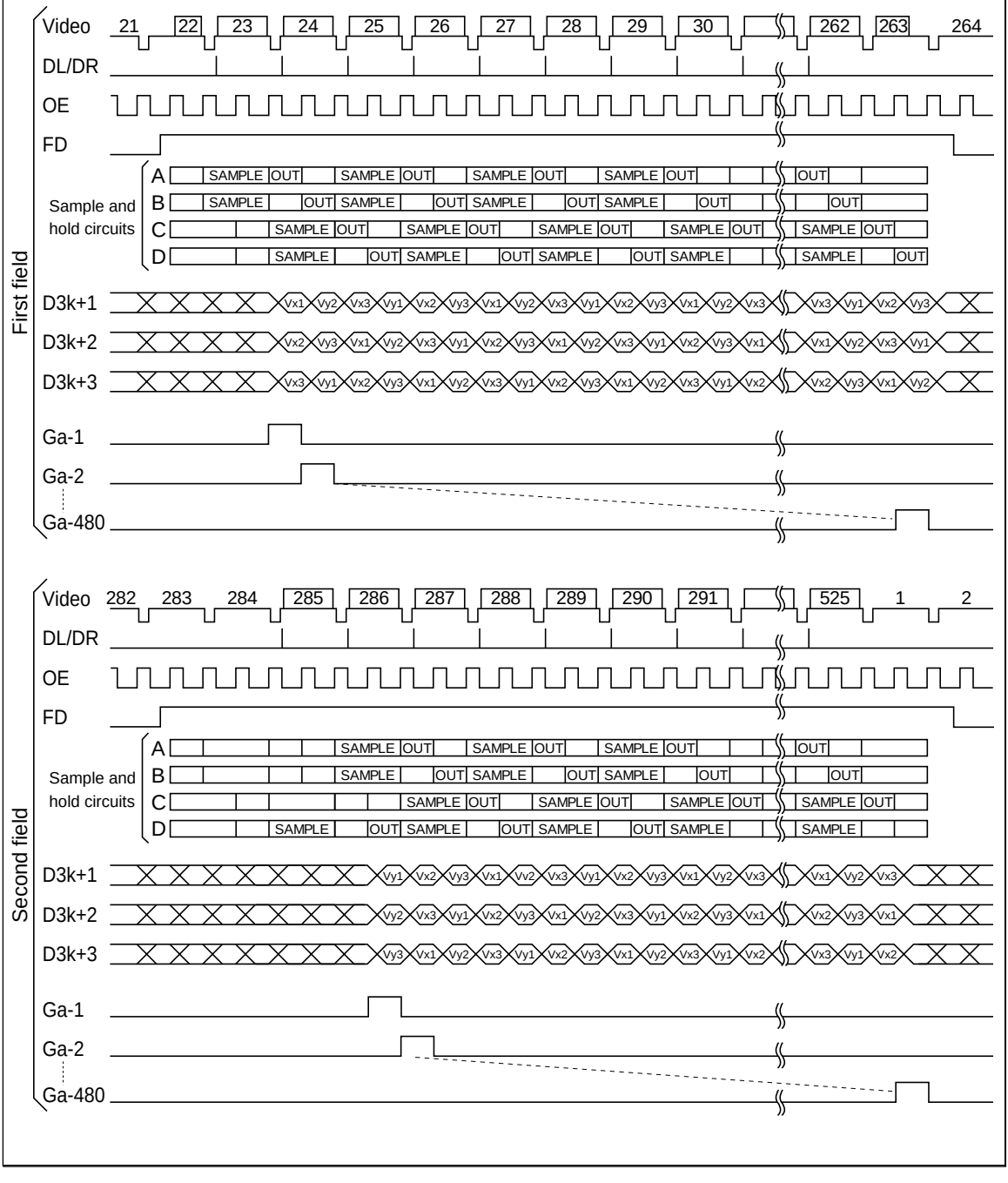
Filter Arrangement			Single (D/S = Low)		Double (D/S = High)			
					Interlace		Non-Interlace	
			Per-Line	Per-Field	Per-Line	Per-Field	Per-Line	Per-Field
Mosaic	Top-left to bottom-right	Inter-leaved	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
		Mono-directional	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
	Top-right to bottom-left	Inter-leaved	MODE 16	MODE 19	MODE 1	MODE 5	MODE 8	MODE 12
		Mono-directional	MODE 15	MODE 18	MODE 2	MODE 6	MODE 9	MODE 13
Vertical stripe			MODE 17	MODE 20	MODE 3	MODE 7	MODE 10	MODE 14
Unicolor triangular			MODE 17	MODE 20	MODE 4	MODE 4	MODE 11	MODE 11
Bicolor triangular			MODE 17	MODE 17	MODE 4	MODE 4	MODE 11	MODE 11

Single: Single-rate sequential drive mode
Double: Double-rate sequential drive mode
Per-Line: Per-line inversion mode
Per-Field: Per-field inversion mode
Interleaved: Interleaved connection mode
Monodirectional: Monodirectional connection mode

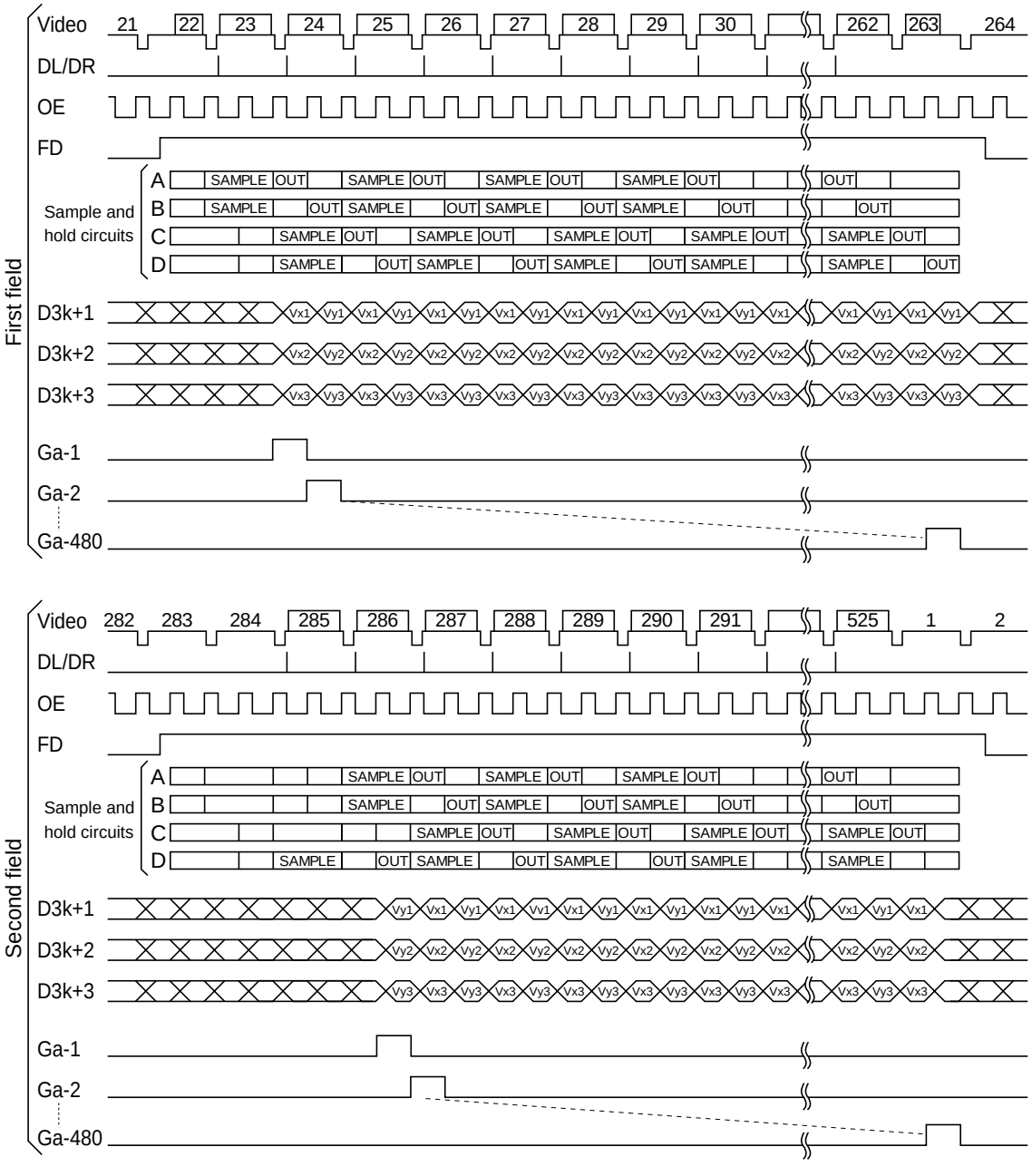
MODE 1	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



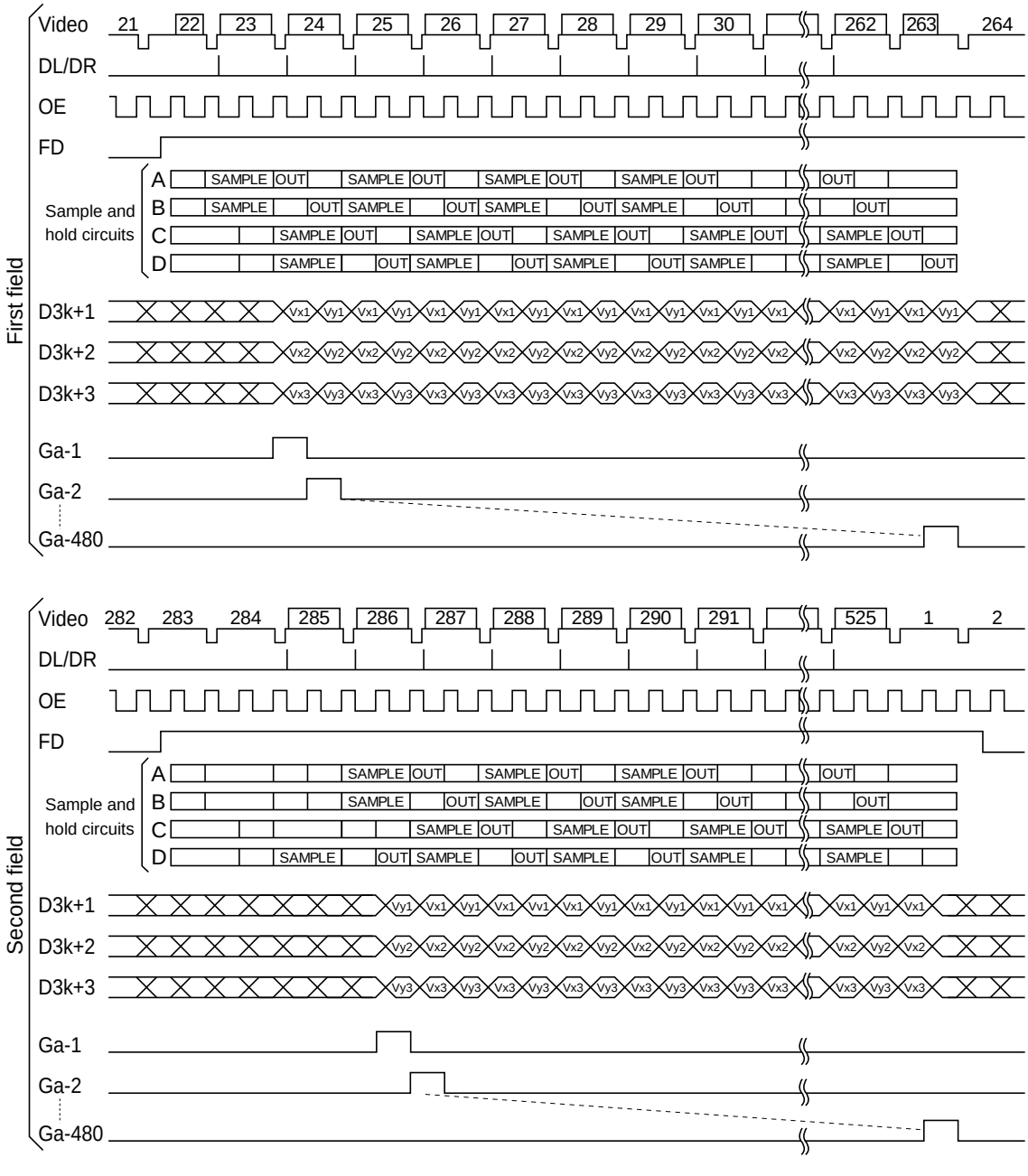
MODE 2	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	GND



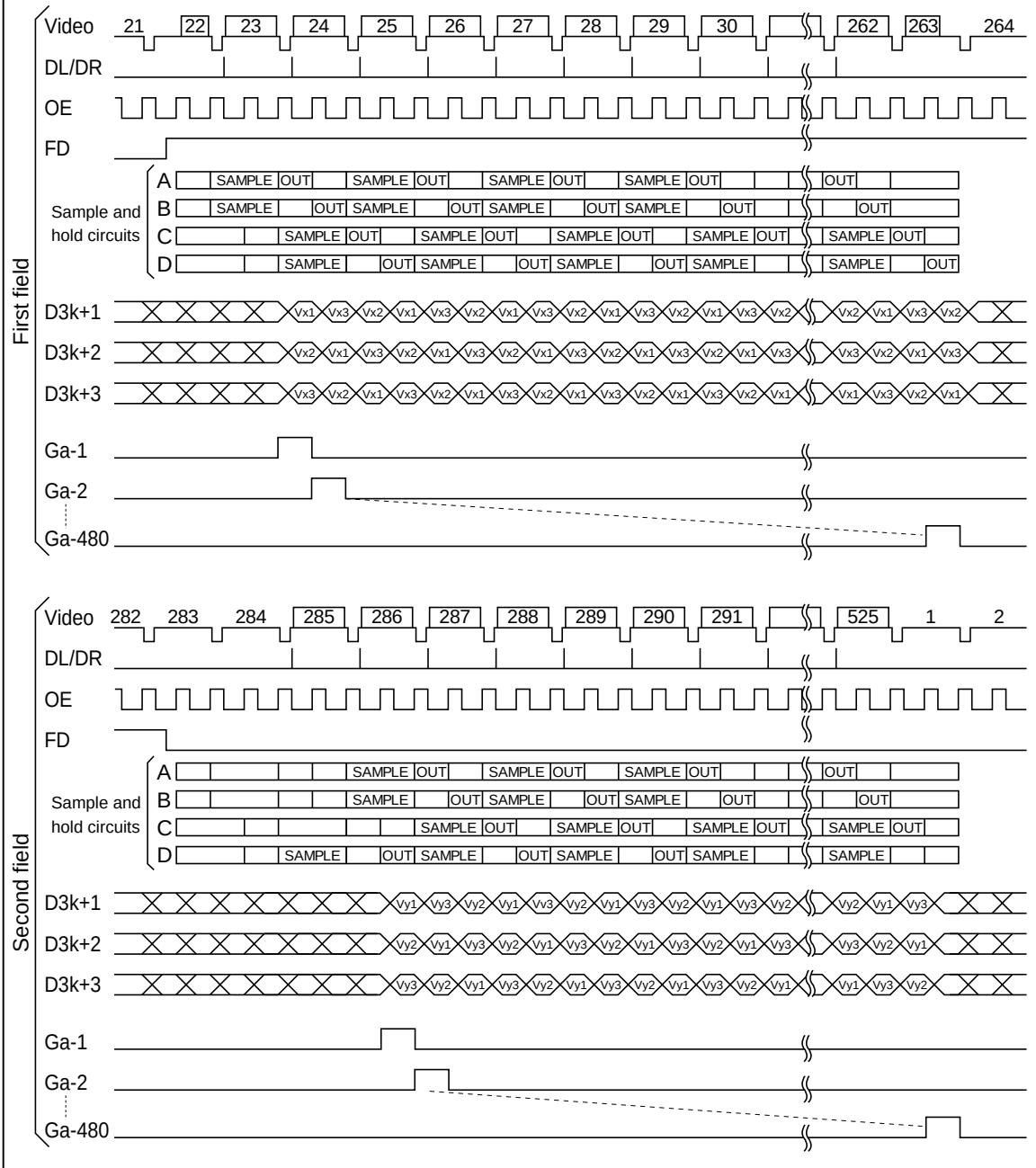
MODE 3	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



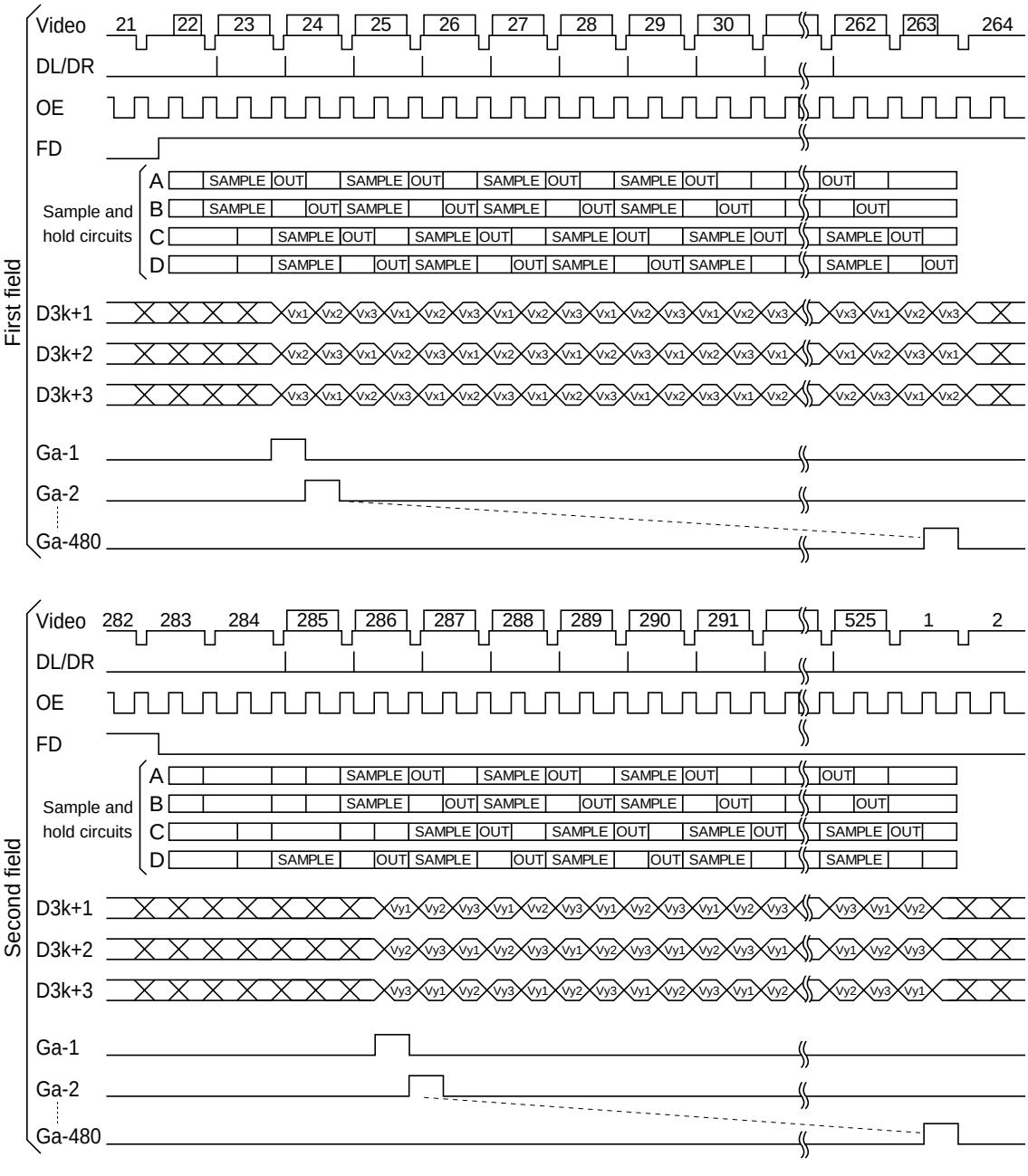
MODE 4	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



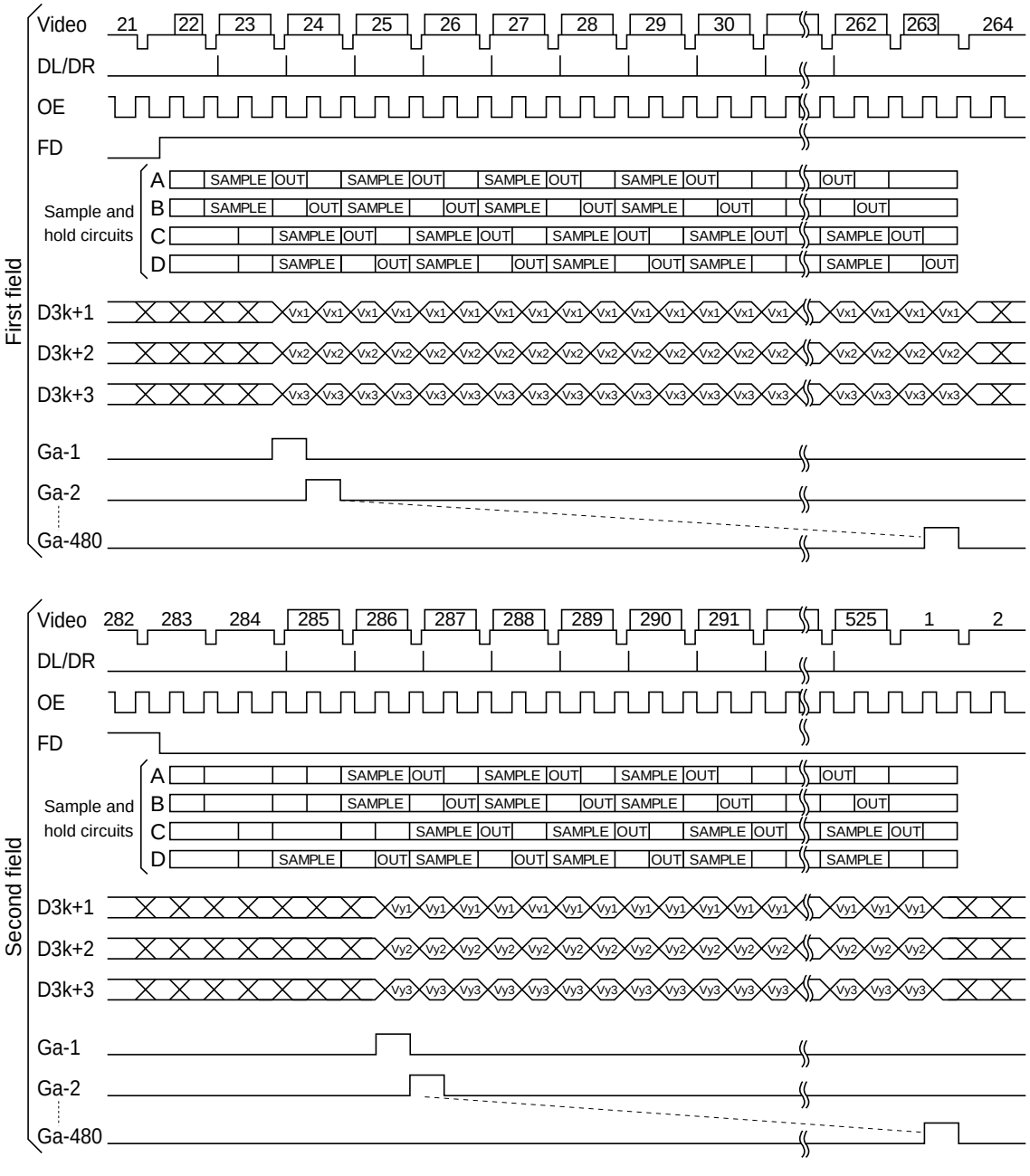
MODE 5	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}



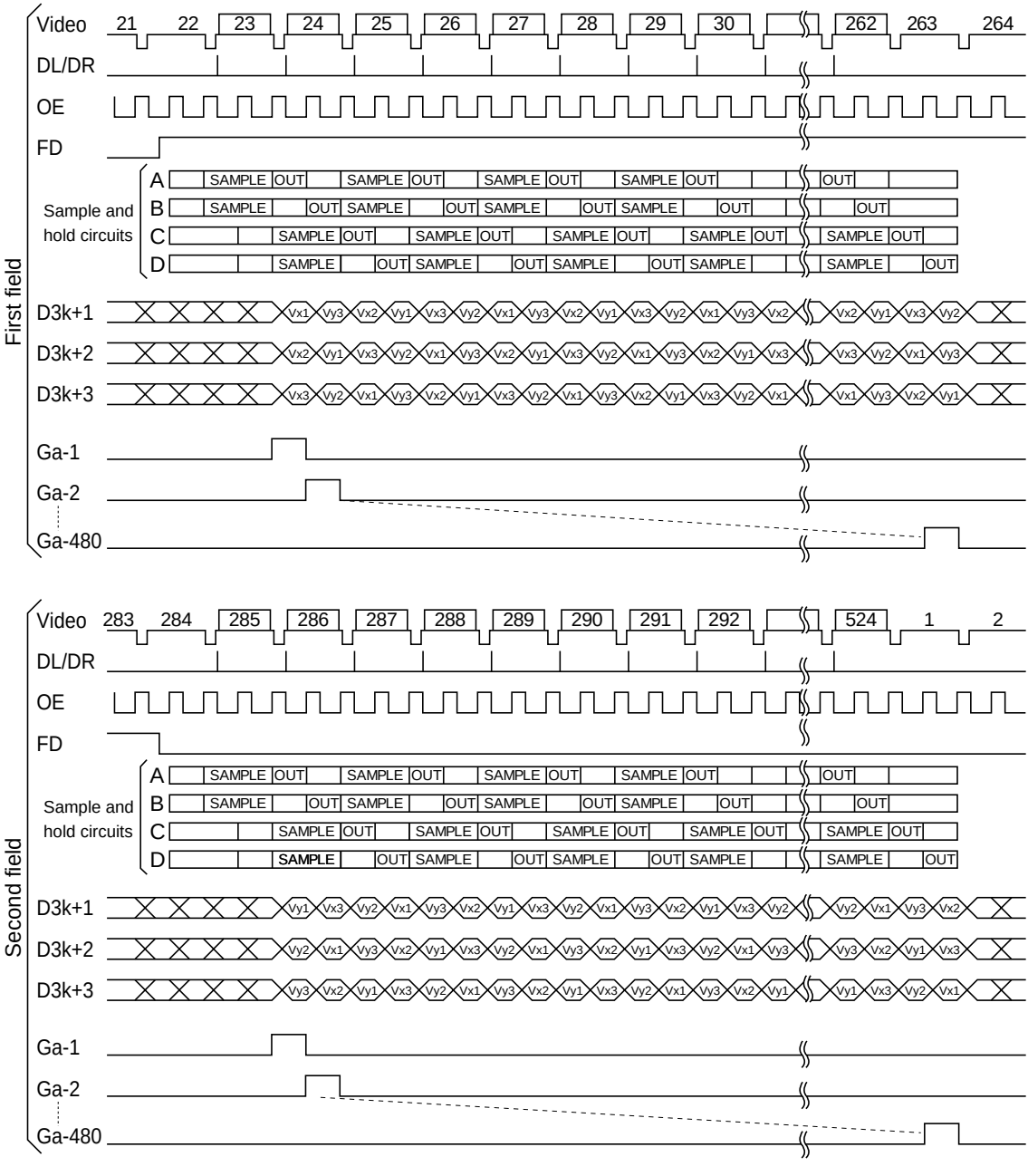
MODE 6	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



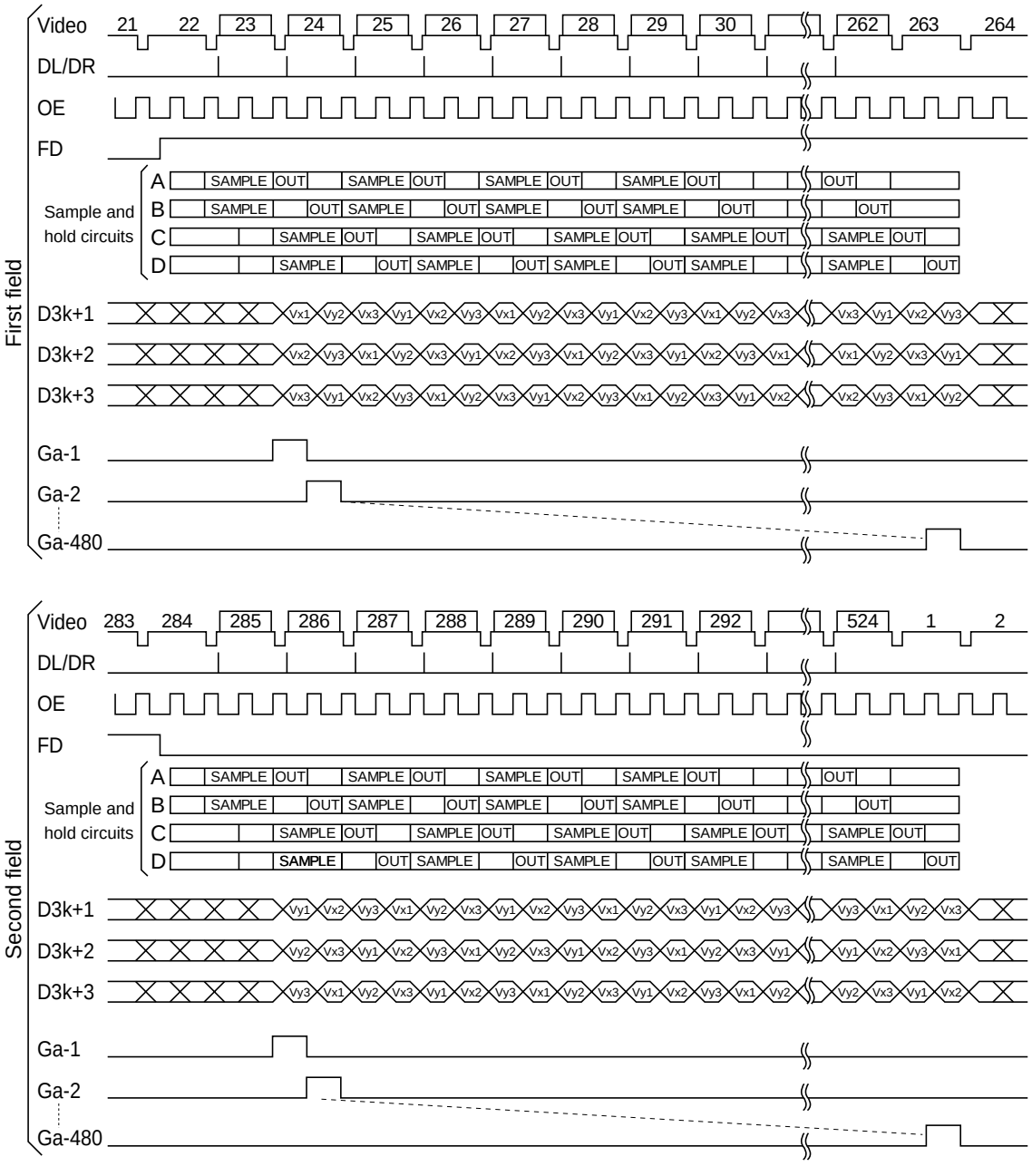
MODE 7	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



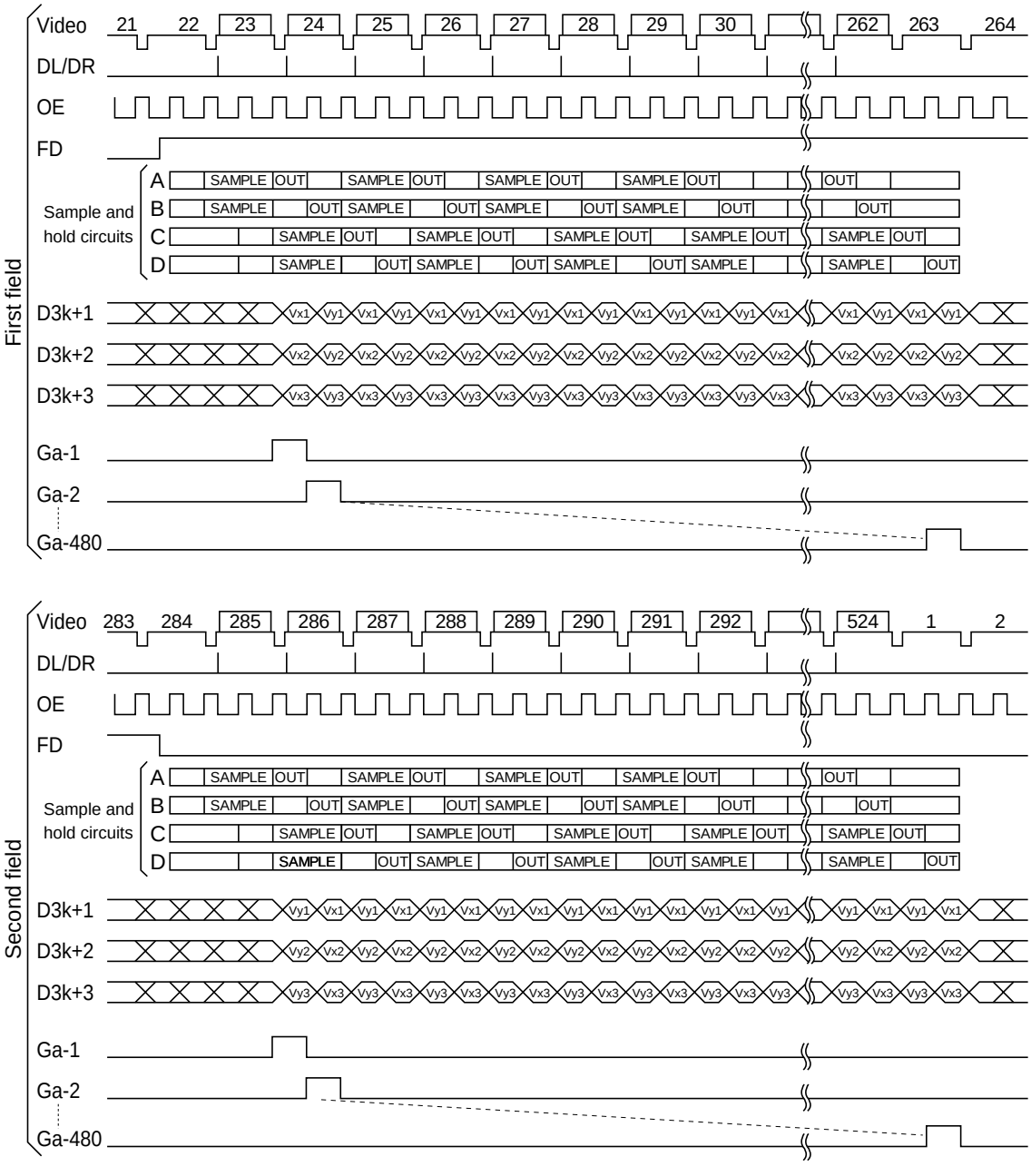
MODE 8	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



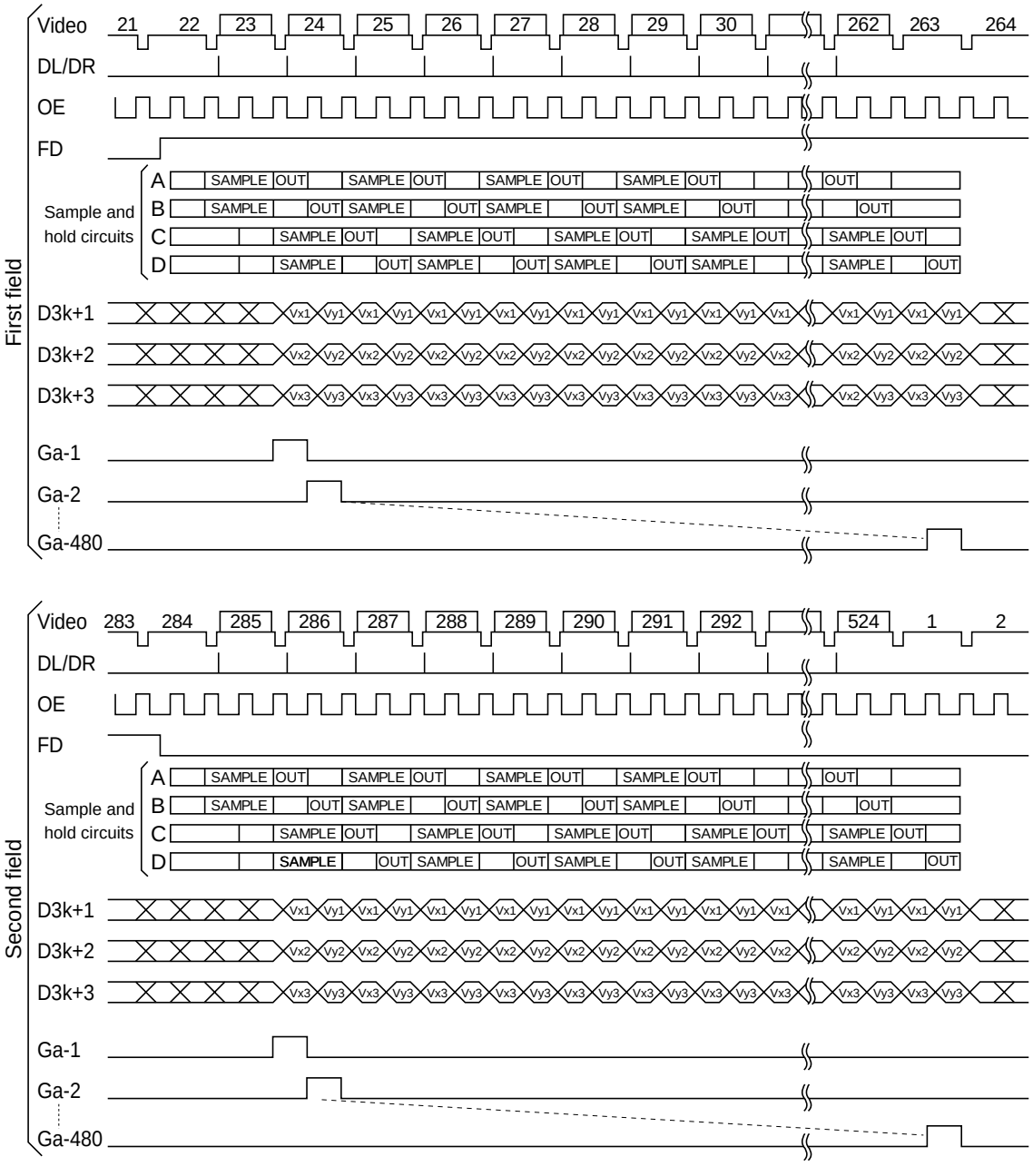
MODE 9	
D/S	V_{CC}
L/F	V_{CC}
MSF1	GND
MSF2	GND



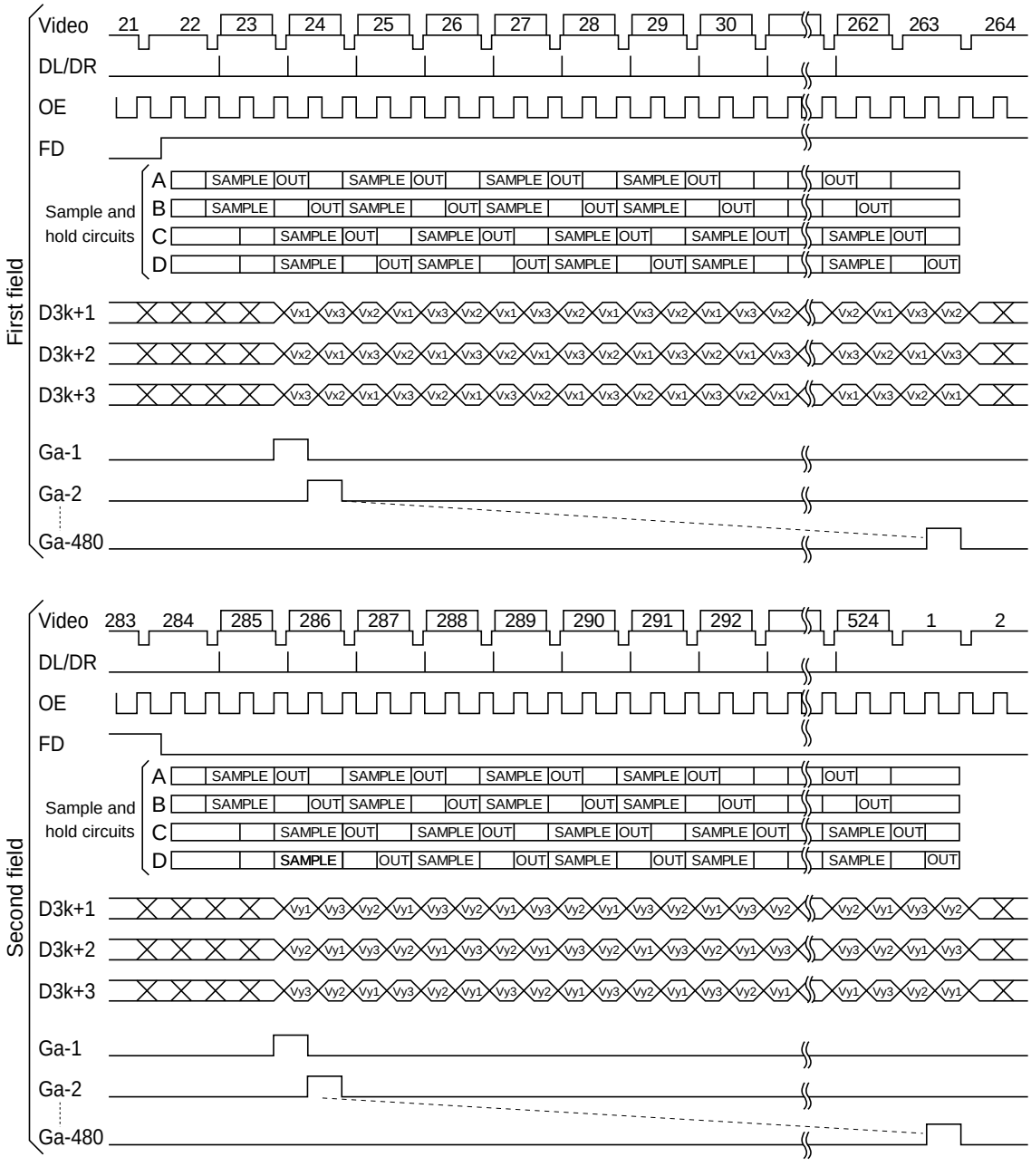
MODE 10	
D/S	V_{CC}
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



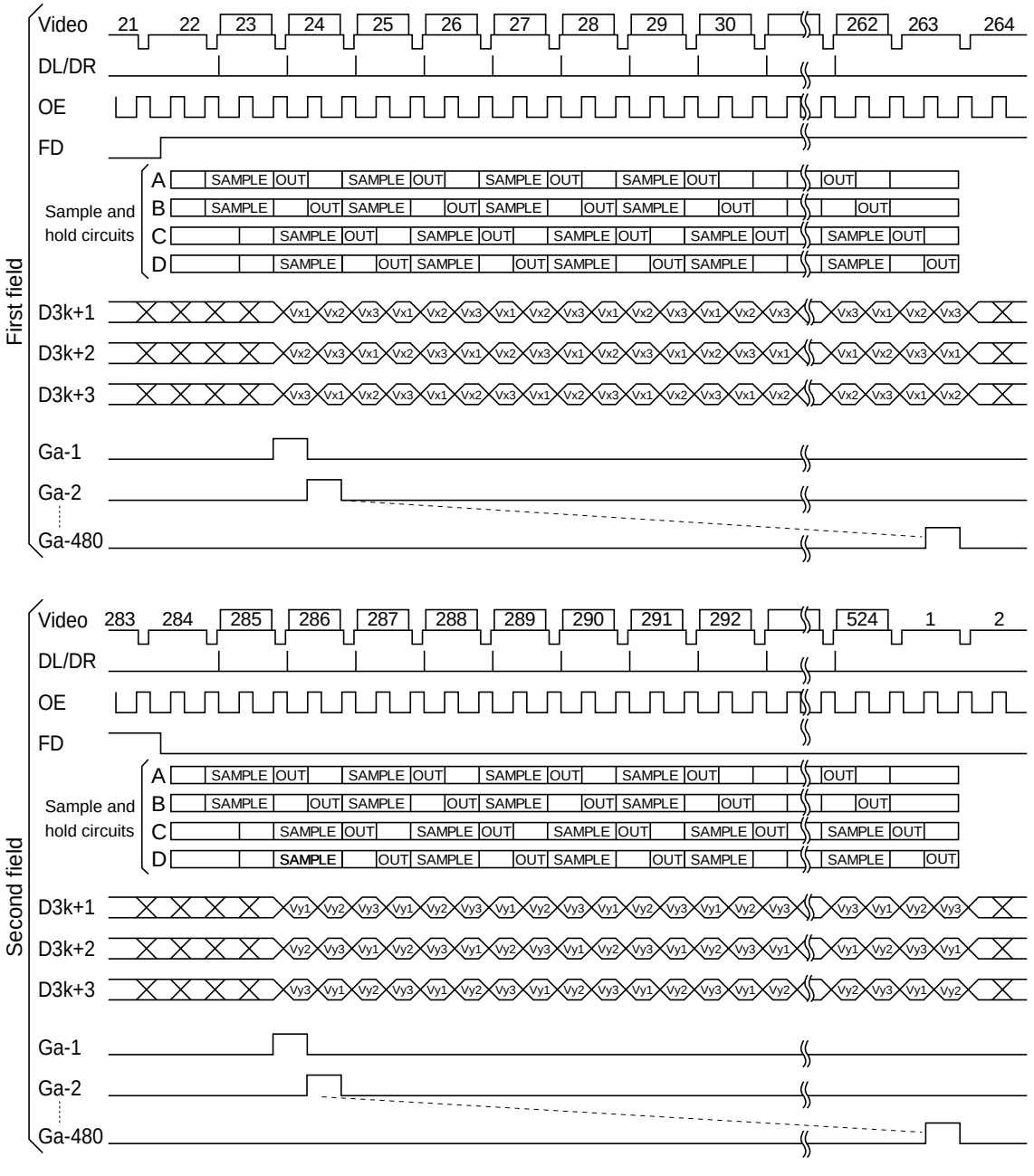
MODE 11	
D/S	V_{CC}
L/F	V_{CC}/GND
MSF1	V_{CC}
MSF2	GND



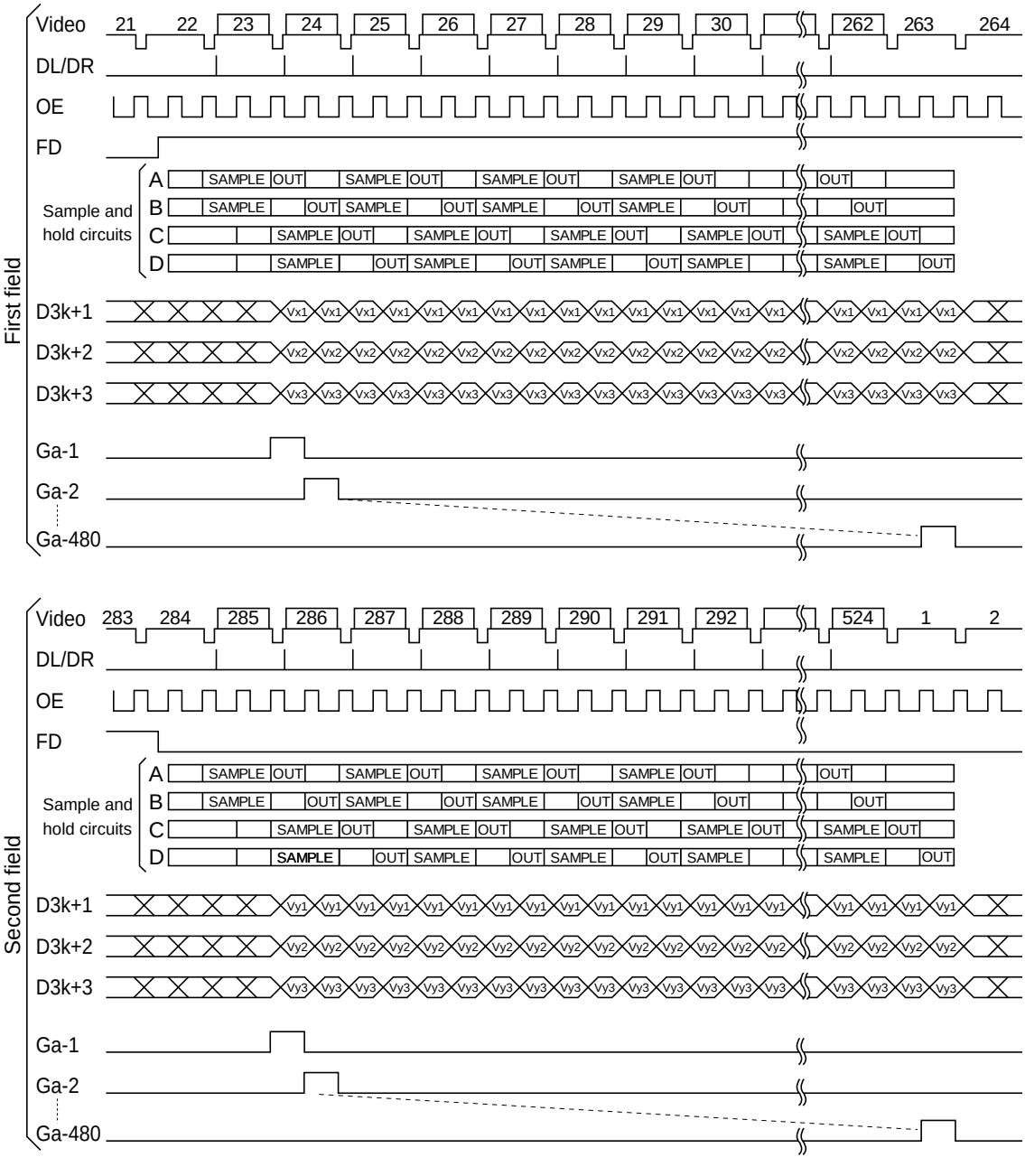
MODE 12	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	V_{CC}



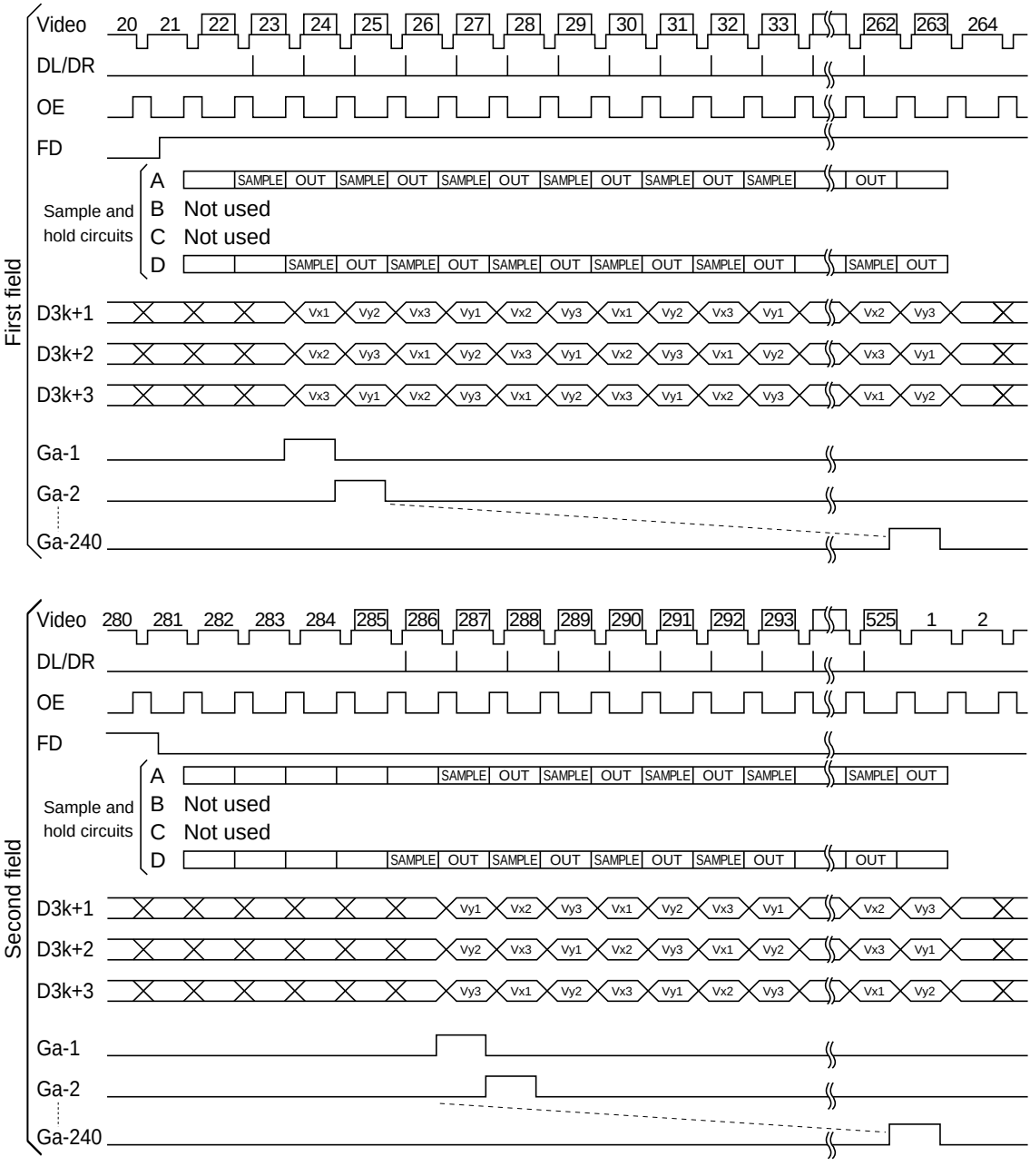
MODE 13	
D/S	V_{CC}
L/F	GND
MSF1	GND
MSF2	GND



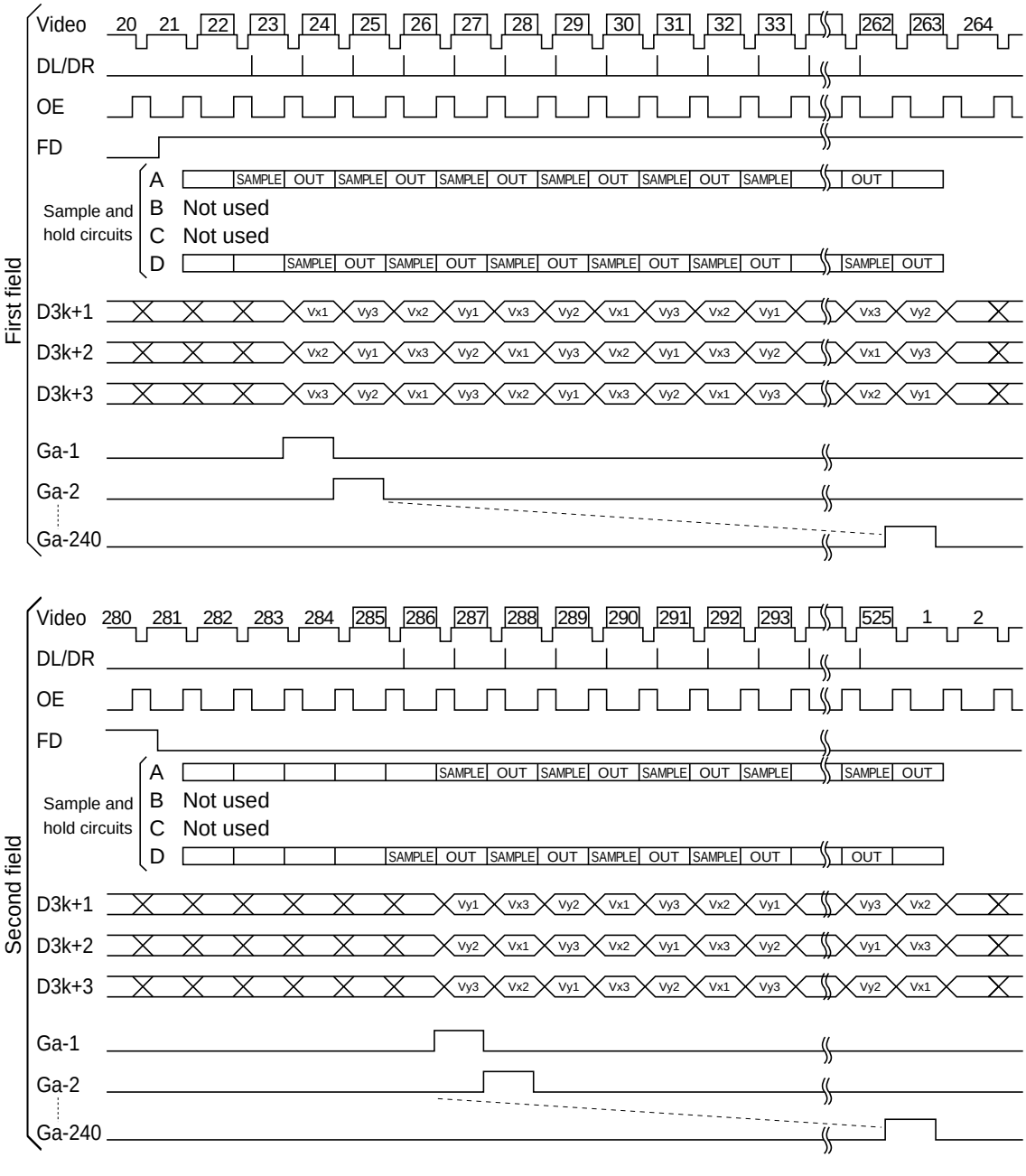
MODE 14	
D/S	V_{CC}
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



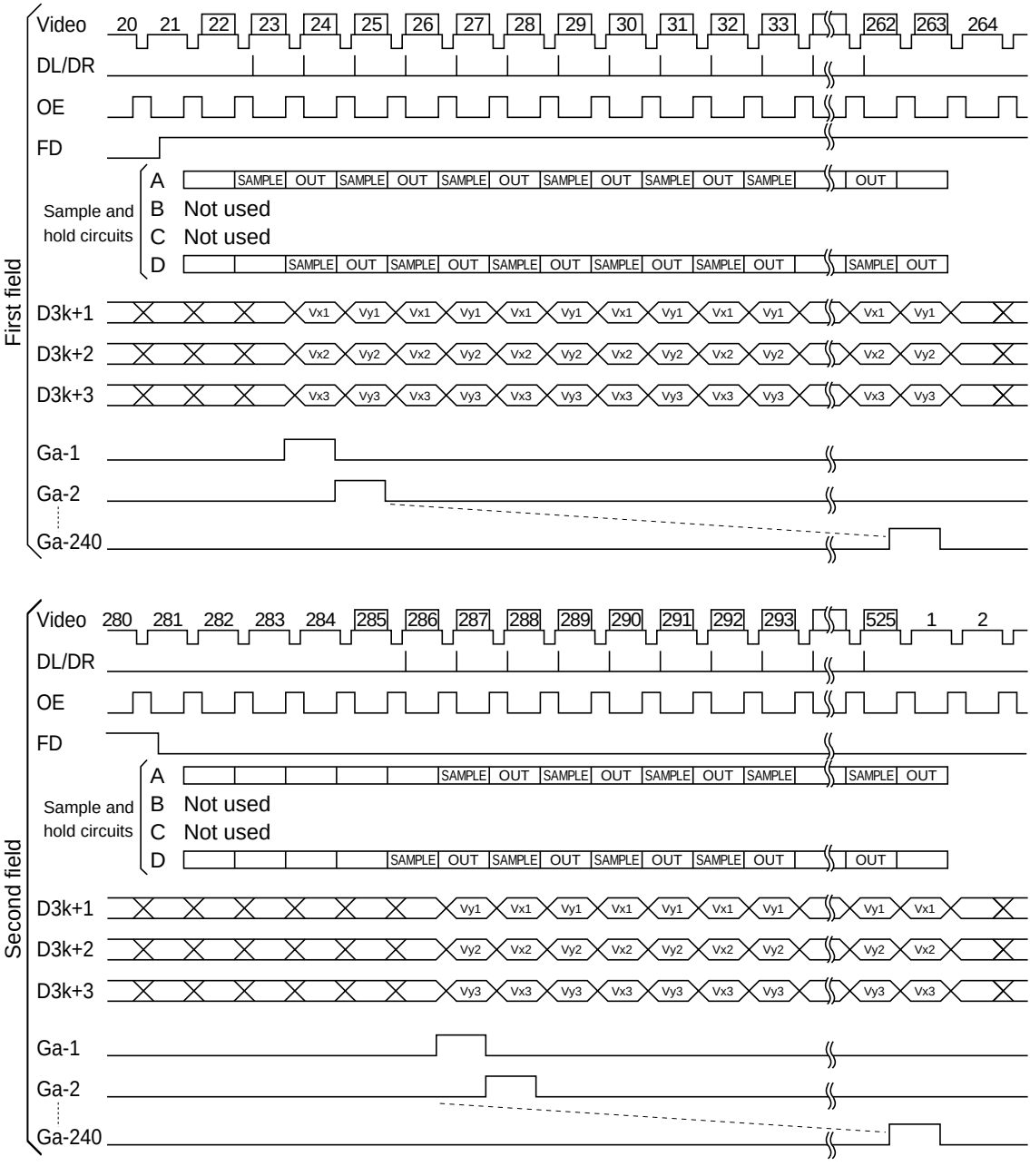
MODE 15	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	V_{CC}



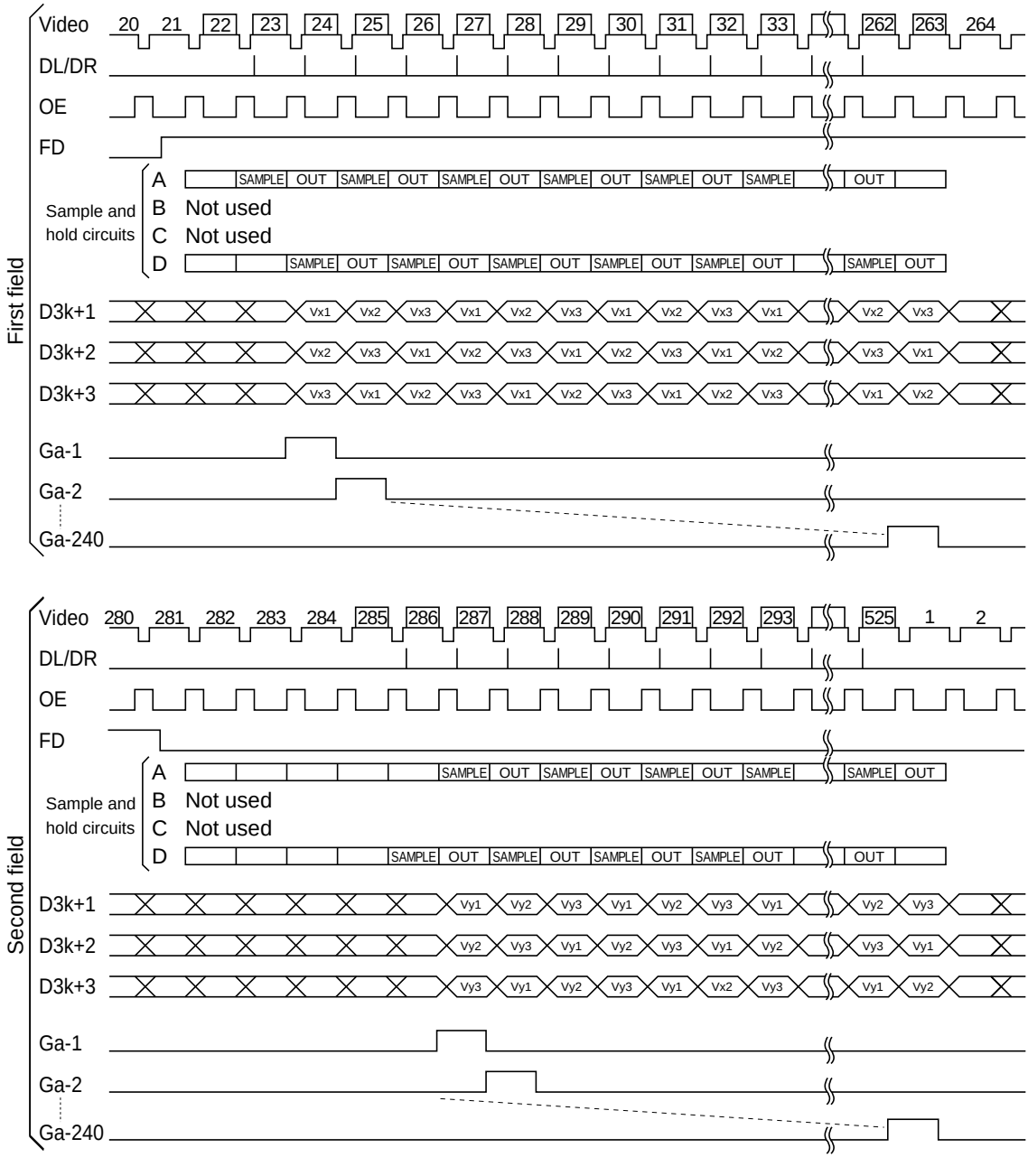
MODE 16	
D/S	GND
L/F	V_{CC}
MSF1	GND
MSF2	GND



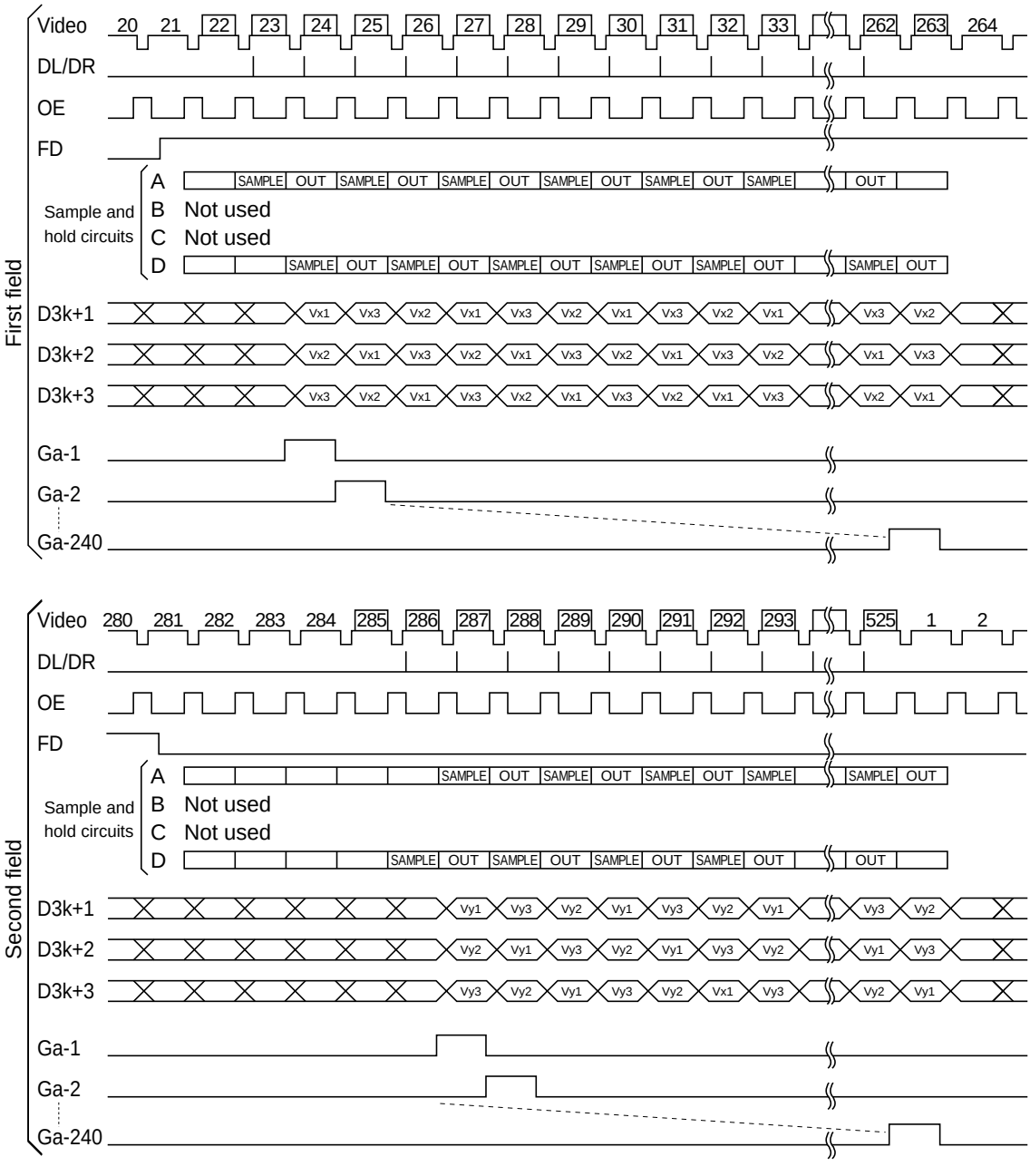
MODE 17	
D/S	GND
L/F	V_{CC}
MSF1	V_{CC}
MSF2	V_{CC}



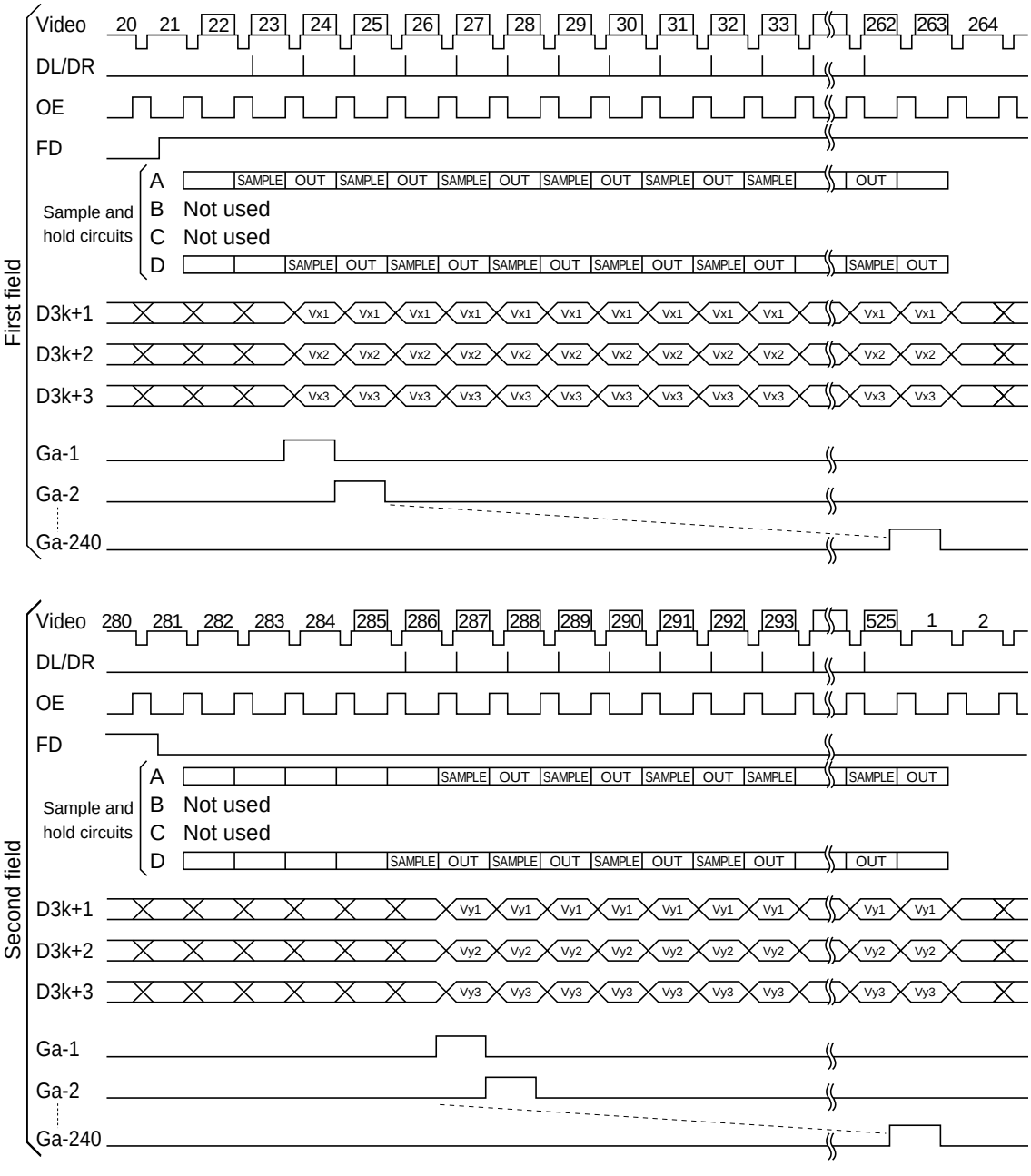
MODE 18	
D/S	GND
L/F	GND
MSF1	GND
MSF2	V_{CC}



MODE 19	
D/S	GND
L/F	GND
MSF1	GND
MSF2	GND



MODE 20	
D/S	GND
L/F	GND
MSF1	V_{CC}
MSF2	V_{CC}



NTSC System TV Signals and LCD

A TV screen display, which is updated 30 times per second, is called a “frame” and is composed of 525 scanning lines. One frame contains two fields; scanning lines 1 to 262.5 scan the display in the first field, and scanning lines 262.5 to 525 scan the display in the second field to fill the gaps which are left unscanned in the first field. This scanning mode is called an “interlace scan.”

The time period in which one scanning line scans the display is called a “horizontal scanning period” and is about 63.5 µs. Within the horizontal scanning period, the time period that display operation is actually performed is called the “valid display period.” The other period is called the “horizontal retrace period.”

There are two modes for displaying a TV screen image on an LCD panel. In the first mode, each scanning line in the two fields is assigned to one line of the LCD panel; thus, each of the 240 lines of the panel are driven by the positive signal in the first field and by the negative signal in the second field. Here, 30-Hz alternating frequency is available, but the number of vertical pixels is limited to 240.

(Single-rate sequential drive mode)

In the second mode, every other line of the LCD panel can be driven by the first field and the remaining lines can be driven likewise by the second field. In this case, if one pixel of the LCD panel is considered, it is recognized that the pixel is driven by signals with opposite polarity every frame. This lowers the alternating frequency to 15 MHz, which is only half of the frame frequency. Driving LCD elements with signals of such low alternating frequency causes flickering and degrades display quality. To raise the alternating frequency to 30 MHz, a method can be employed in which LCD elements are driven once every field instead of once every frame.

Specifically, in the first field, the first and second lines of the LCD panel are driven respectively during the first half and second half of the complete horizontal scanning period. The same rule is repeated for the following lines. In the second field, on the other hand, the combination of two lines is different. The first line is driven during the second half of the horizontal scanning period, and then the second and third lines are driven respectively during the first and second half of the following horizontal scanning period. The same rule is repeated for the following lines.

Employing this method enables the implementation of 480 vertical pixels.

(Double-rate sequential drive mode)

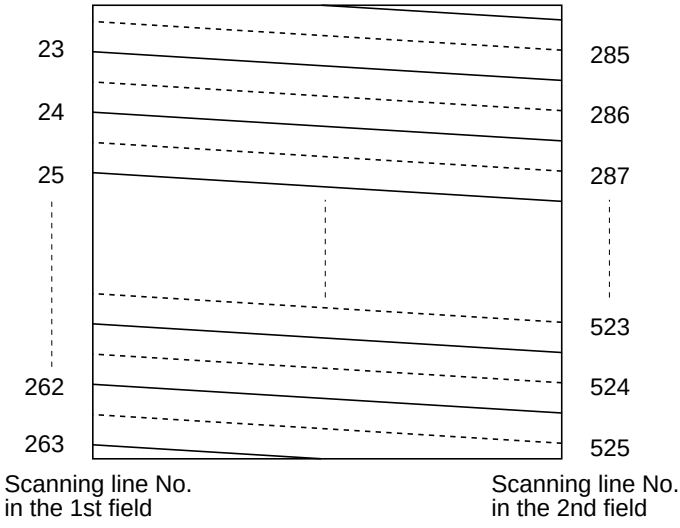


Figure 24 Example of NTSC System TV Signals Scanning

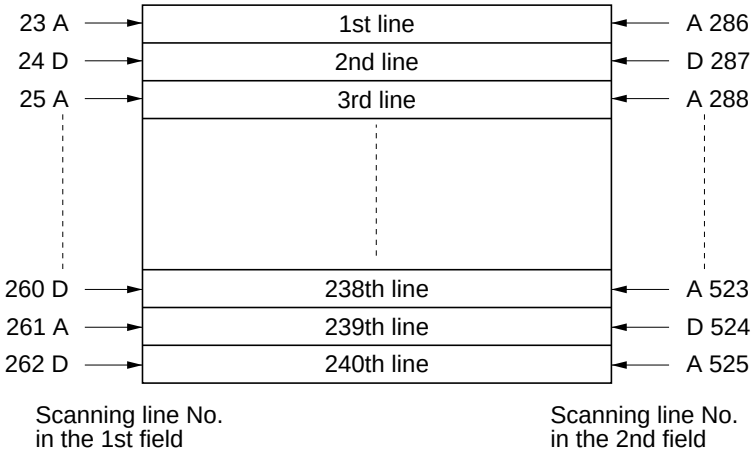


Figure 25 Middle-Resolution Display by Single-Rate Sequential Drive Mode

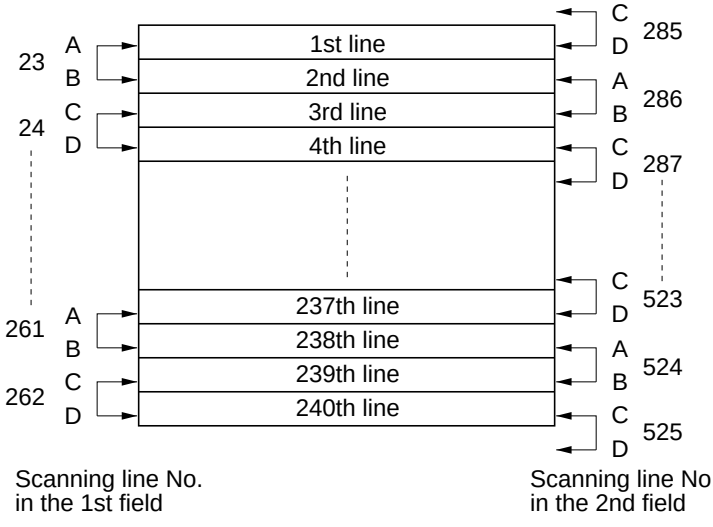


Figure 26 High-Resolution Display by Double-Rate Sequential Drive Mode

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Remarks	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V		
Power supply for analog unit	V_{BB}	V_{CC}– 23 to V_{CC} + 0.3	V		
Input voltage for logic unit	V_{TC}	–0.3 to V_{CC} + 0.3	V		3
Input voltage for analog unit	V_{TB}	V_{BB}– 0.3 to V_{CC} + 0.3	V		4
Operating temperature	T_{opr}	–20 to +75	°C	Applies to logic circuit	
		–10 to +60	°C	Applies to analog circuit	
Storage temperature	T_{stg}	–40 to +125	°C		
LCD level voltage	V_{LCD}	V_{BB} to V_{CC} + 0.3	V		

Notes: 1. Value referred to GND = 0 V.

2. If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
4. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.

Electrical Characteristics

DC Characteristics ($V_{LCD} = V_{CC} = 5$ V ±10%, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to +75 ˚C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions			Notes
Input high-level voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V				3
Input low-level voltage	V_{IL}	GND	—	0.3V_{CC}	V				
Output high-level voltage	V_{OH}	V_{CC} – 0.4	—	—	V	$-I_{OH}$ = 0.3 mA			4
Output low-level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 0.3 mA			
Input leakage current (1)	I_{LI1}	–10	—	+10	µA	V_I = 0 V, V_{CC}			1
Input leakage current (2)	I_{LI2}	–10	—	+10	µA	$V_I = V_{BB}$, V_{CC}			2
Output current (1)	I_{OUT}	—	—	–150	µA	$V_{CC} - V_{BB}$ = 20 V Apply V_{in} to Vx and Vy. $V_{in} = (V_{CC} - V_{BB})/2$ $V_{bo} = V_{CC} - 3$ V $V_{bsH} = V_{CC} - 3$ V $V_{bsB} = V_{CC} - 3$ V	Dk = V_{in} – 0.5 V	OE = V_{CC}	5
		—	—	–10	µA			OE = GND	
Output current (2)	I_{IN}	+150	—	—	µA		DK = V_{in} + 0.5 V	OE = V_{CC}	
		+10	—	—	µA			OE = GND	
Current consumption	I_{GND}	—	—	3.0	mA	f_{ck} = 2.5 MHz, $V_{bo} = V_{CC} - 3$ V $V_{bsH} = V_{CC} - 3$ V, $V_{bsB} = V_{CC} - 3$ V OE = 33 kHz, FD = 30 Hz OE duty = 7/32			6
	I_{BB}	—	15	30	mA				
Bias voltage	V_b	V_{CC} – 4.0	V_{CC} – 3.0	—	V	$V_{bo} = V_{bsH} = V_{bsB}$, C_L = 100 pF, t_{DDR} < 6.3 µs			
Dynamic range	V_{DY}	V_{BB} + 1.5	—	V_{CC} – 3.5	V	$V_{CC} - V_{BB}$ = 20 V, T_a = –10 to +60°C –0.5 V < V_{off} < +0.5 V $V_{bo} = V_{bsH} = V_{bsB} = V_{CC} - 3$ V			5, 7, 9

Item	Symbol	Min	Typ	Max	Unit	Test Conditions		Notes
Offset voltage	$V_{off\ (L)}$	–5 – 180	—	–5 + 180	mV	$V_{CC} - V_{BB}$ = 20 V Ta = –10 to + 60°C f_{ck} = 2.5 MHz $V_{bo} = V_{bsH} = V_{bsB}$ $= V_{CC} - 3$ V	V_{in} = –11 V	5, 8, 9
	$V_{off\ (H)}$	+55 – 180	—	+55 + 180	mV		V_{in} = –1 V	

Notes:
1. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, TEST2, V_{bo}, V_{bsH}, and V_{bsB}.
2. Applies to pins Vx1, Vx2, Vx3, Vy1, Vy2, and Vy3.
3. Applies to pins HCK1, HCK2, HCK3, DL, DR, FD, RS, OE, SHL, D/S, L/F, MSF1, MSF2, TEST1, and TEST2.
4. Applies to pins DL and DR.
5. Applies to pins D1 to D120.
6. The shift register is constantly shifting one 1.
   Mode setting: L/F = V_{CC}, D/S = V_{CC}, MSF1 = GND, MSF2 = V_{CC}
   (The other input pins must be V_{CC} or GND level.)
7. The operations are the same as those when offset voltage is measured.
8. Definition of “offset voltage” is shown figure 27.
9. These characteristics are defined within the temperature which is shown in the test condition.

AC Characteristics ($V_{LCD} = V_{CC} = 5\ V \pm 10\%$, GND = 0 V, $V_{CC} - V_{BB} = 16$ to 20 V, $T_a = -20$ to +75°C)

Item	Symbol	Min	Max	Unit	Test Condition	Notes
Three-phase clock period	t_{CKCK}	210	1000	ns		
Three-phase clock pulse width	t_{CWH} t_{CWL}	100	—	ns		
Interval between three-phase clock falling edge and rising edge	t_{fr1} t_{fr2} t_{fr3}	30	—	ns		1
Interval between three-phase clock rising edge and falling edge	t_{rf}	20	—	ns		2
Clock rise and fall times	t_{ct}	—	30	ns		
DL, DR input setup time	t_{su}	50	—	ns		
DL, DR input hold time	t_{HLI}	20	—	ns		
DL, DR output delay time	t_{pd}	—	90	ns	C_L = 15 pF	
DL, DR output hold time	t_{HLO}	5	—	ns		
OE input period	t_{CYCO}	30	80	µs		
OE input high-level pulse width	t_{OWH}	3	15	µs		
OE rise and fall times	t_{or} t_{of}	—	30	ns		
FD input setup time	t_{FS}	100	—	ns		
FD input hold time	t_{FH}	100	—	ns		

Notes: 1. Necessary for preventing the three-phase shift register from racing.

2. t_{rf} must satisfy the DR and DL input hold time (t_{HLI}) of the next horizontal driver. ($t_{rf} + t_{HLO} > t_{HLI}$)

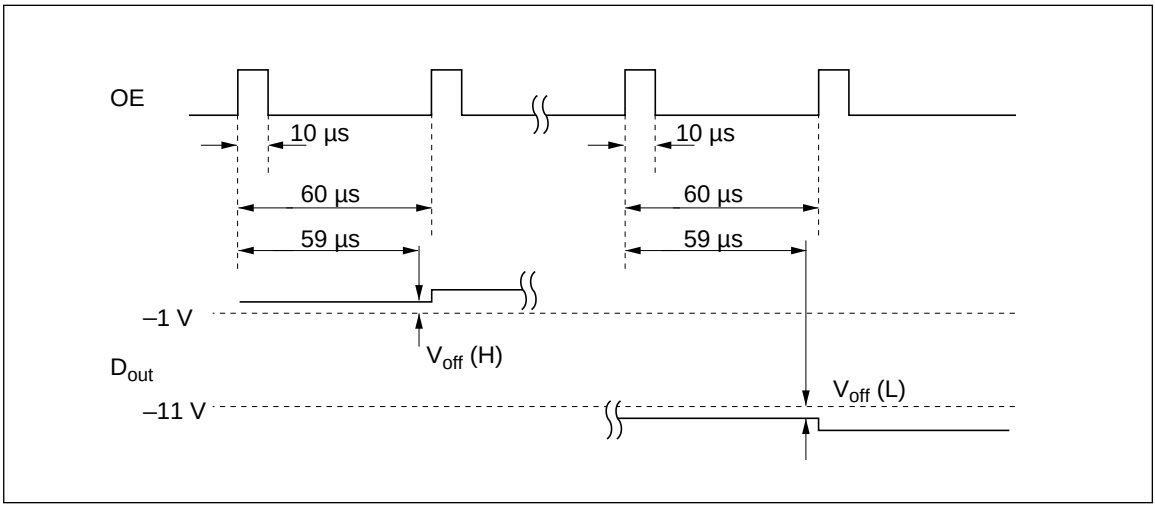


Figure 27 Offset Voltage

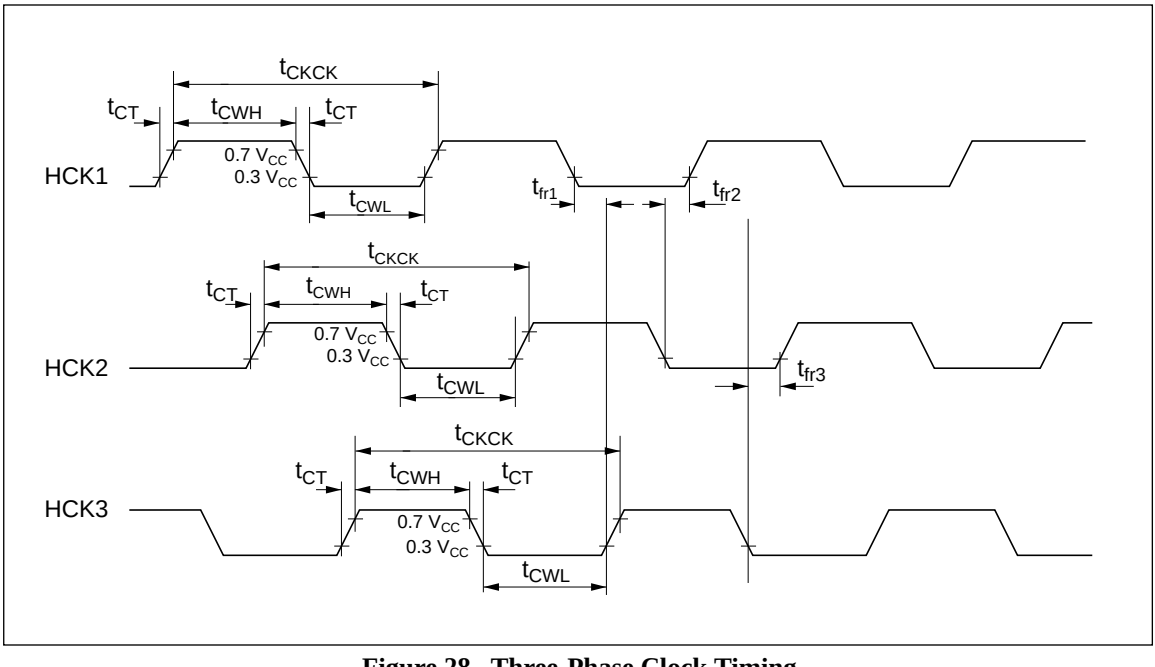


Figure 28 Three-Phase Clock Timing

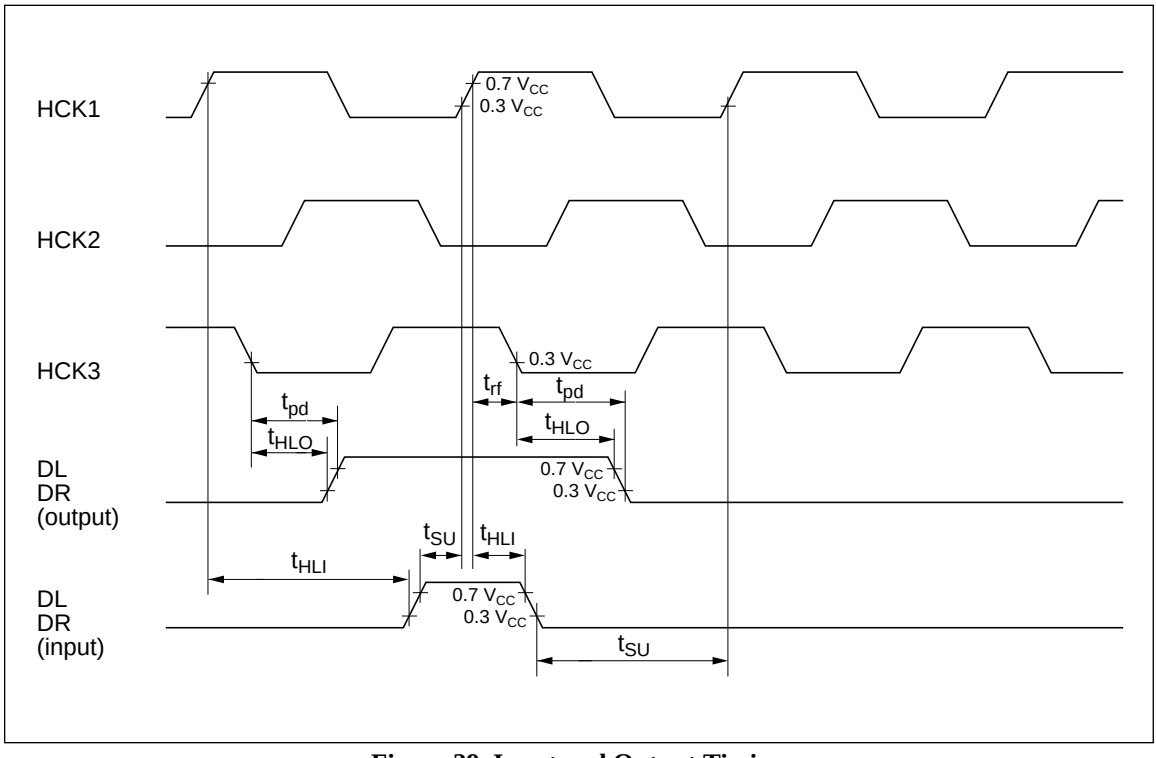


Figure 29 Input and Output Timing

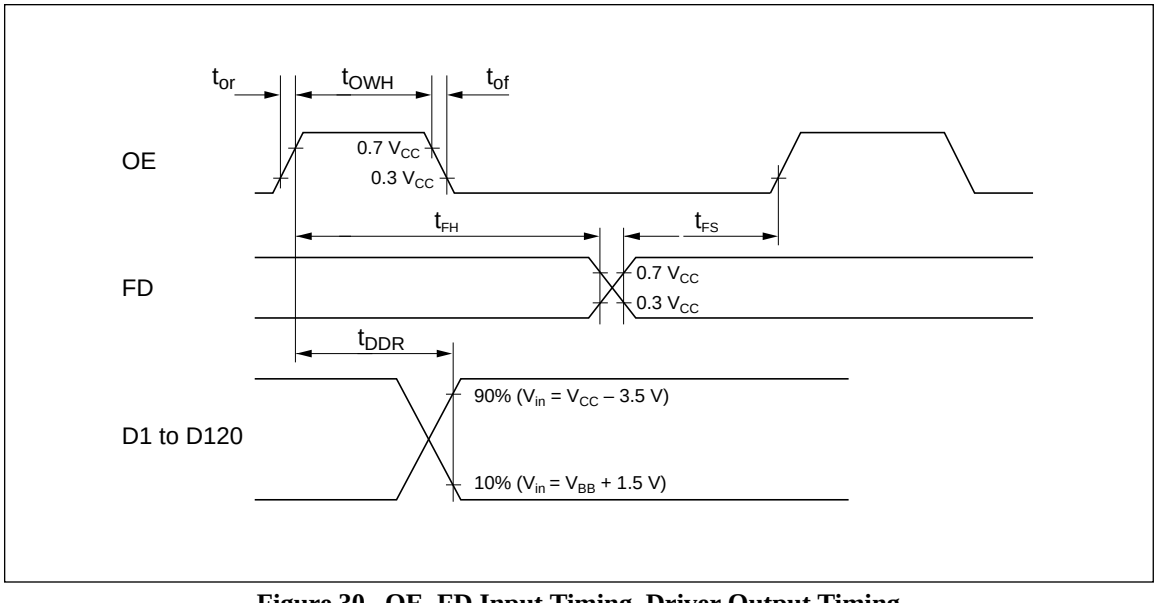


Figure 30 OE, FD Input Timing, Driver Output Timing