HD66310T

TFT-Type LCD Driver for VDT

HITACHI

Description

The HD66310T is a drain bus driver for TFT-type (thin film transistor) LCDs. It receives 3-bit digital data for one dot, selects a level from eight voltage levels, and outputs the level to an LCD.

The HD66310T can drive an LCD panel with an RGBW filter to display a maximum of 4096 colors.

Features

- Full color display: a maximum of 4096 colors
  RGB color filter: 512 colors, 8 gray scales
  RGBW color filter: 4096 colors, 8 gray scales
- High-speed operation
  Number of input data bits: 3 bits × 4
  Maximum operation clock frequency:
  — 12 MHz (HD66310T00)
  — 15 MHz (HD66310T0015)
  Maximum pixels: 480 × 640 dots
- 160 internal driver circuits
- Bidirectional shift
- Internal chip enable signal generator
- Stand-by function
- LCD driving voltage: 15 V to 23 V
- CMOS process

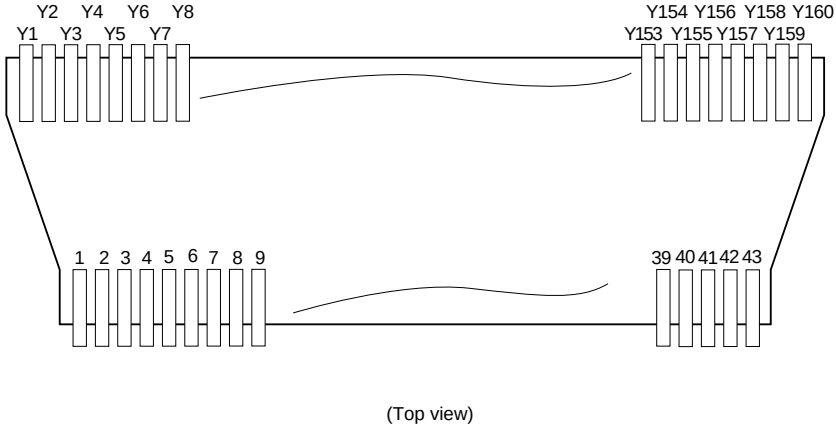
Ordering Information

Type No.	Max. Operating Clock Frequency	Power Supply for Logic Unit	Operating Temperature	Package
HD66310T00	12 MHz	5 V ± 10%	–20 to +75°C	203-pin TCP
HD66310T0015	15 MHz	5 V ± 5%	–20 to +65°C	

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Arrangement



(Top view)

1	V0L	22	DMY1
2	V1L	23	D20
3	V2L	24	D21
4	V3L	25	D22
5	V4L	26	D23
6	V5L	27	DMY2
7	V6L	28	CL1
8	V7L	29	CL2
9	V_{CC1}	30	BS
10	V_{CC2}	31	SHL
11	EIO1	32	EIO2
12	$\overline{RVS}$	33	TEST
13	D00	34	GND
14	D01	35	V_{EE}
15	D02	36	V7R
16	D03	37	V6R
17	DMY0	38	V5R
18	D10	39	V4R
19	D11	40	V3R
20	D12	41	V2R
21	D13	42	V1R
		43	V0R

Note: This does not apply to TCP dimensions.

Pin Description

Pin List

Pin Name	Number of Pins	Input/Output	Functions (Refer to)
$V_{CC}1$, $V_{CC}2$	2	Power supply	1.
GND	1	Power supply	
V_{EE}	1	Power supply	
V0L–V7L, V0R–V7R	16	Power supply	2.
CL1	1	Input	3.
CL2	1	Input	4.
D00, D10, D20, to D03, D13, D23	12	Input	5.
$\overline{RVS}$	1	Input	6.
SHL	1	Input	7.
EIO1, EIO2	2	Input/output	8.
TEST, BS	2	Input	9.
Y1–Y160	160	Output	10.
DMY0–DMY2	3	—	11.

Pin Functions

1. $V_{CC}1$, $V_{CC}2$, GND, V_{EE}: These pins are used for the power supply.

V_{CC}–GND: Power supply of low voltage
V_{CC}–V_{EE}: Power supply of high voltage

2. V0L–V7L, V0R–V7R: 8-level LCD driving voltage is applied to these pins. One of the eight levels is selected according to the value of the 3-bit input display data. The L and R pins of the same voltage level are connected in the driver.

3. CL1: Inputs clock pulses, which determine the output timing of the LCD driving voltage. The output changes at the CL1 rising edge.

4. CL2: Inputs clock pulses, which determine the input timing of display data. The driver samples data at the CL2 falling edge.

Table 1 Voltage Level Selection According to Display Data Value

Display Data			Voltage Level	
D2j	D1j	D0j	$\overline{RVS}$ = 1	$\overline{RVS}$ = 0
0	0	0	V0	V7
0	0	1	V1	V6
0	1	0	V2	V5
0	1	1	V3	V4
1	0	0	V4	V3
1	0	1	V5	V2
1	1	0	V6	V1
1	1	1	V7	V0

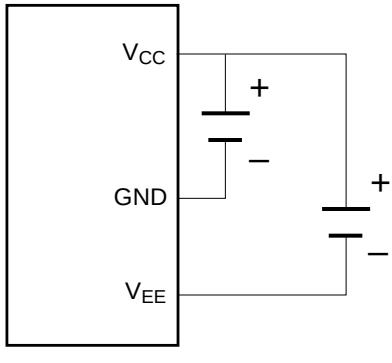


Figure 1 Power Supply for the Device

5. D00–D03, D10–D13, D20–D23: Input display data. See table 1 for the voltage level selection by the display data.

6. $\overline{\text{RVS}}$: Determines if logical I/O display data is reversed. Display data is reversed when $\overline{\text{RVS}}$ is low.

7. SHL: Selects the shift direction of display data.

8. EIO1, EIO2: Inputs/outputs chip enable signals. The SHL signal selects which pin is for input or output. When the chip enable input signal is low, data input starts. When display data corresponding to 160 outputs are input, the chip enable output signal changes from high to low.

9. TEST, BS: Used for test purposes only. Connect to a low level for normal operation.

10. Y1–Y160: Output LCD driving signals.

11. DMY0–DMY2: Reserved pins that should be left open.

Table 2 Input/Output Selection for EIO1 and EIO2

SHL	EIO1	EIO2
GND	Input	Output
V_{CC}	Output	Input

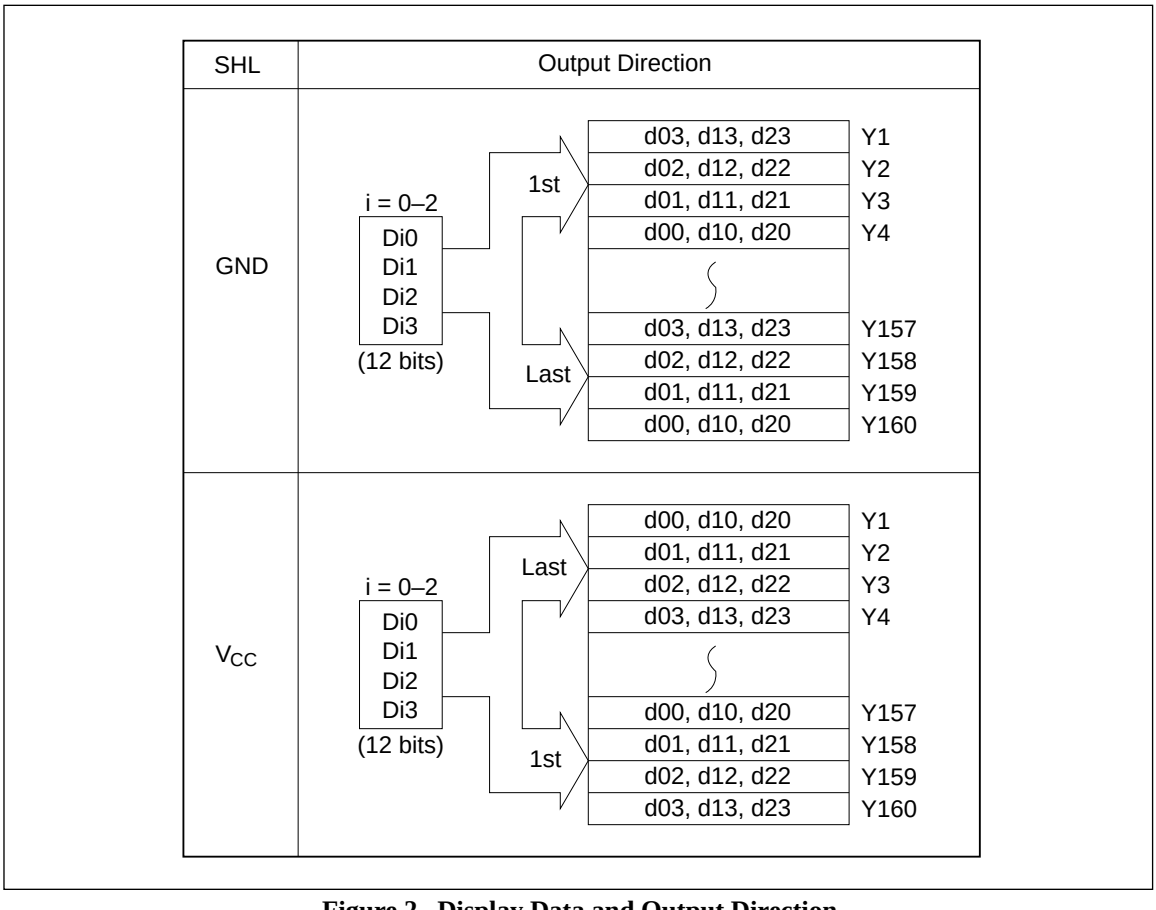
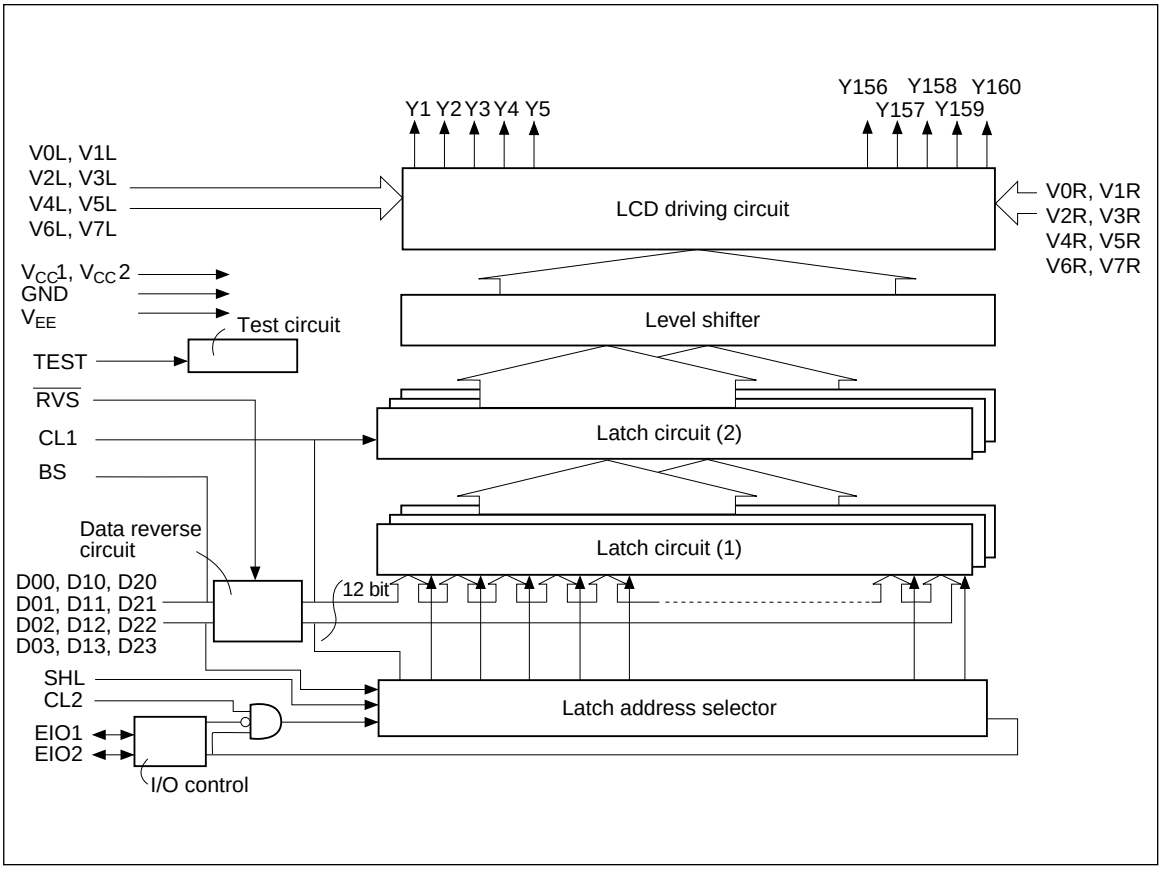


Figure 2 Display Data and Output Direction

Internal Block Diagram



Block Functions

Latch Address Selector: Contains a 6-bit up/down counter and a decoder, and sends the latch signals to latch circuit (1) at the CL2 falling edge.

Data Reverse Circuit: Reverses the input display data when $\overline{RVS}$ = 0, and does not reverse data when $\overline{RVS}$ = 1.

Latch Circuit (1): Consists of three planes of 160-bit latch circuit. Each bit of 3-bit data is separately latched in its corresponding plane depending on its significance. Each plane is divided into forty 4-bit blocks, and all four bits are latched into the block at once, as specified by the latch signal from the address selector. In total, the 3-plane circuit latches 12 bits of data at one time.

Latch Circuit (2): Consists of three planes of 160-bit latch circuit, which latches the data from latch circuit (1) at the timing determined by CL1, and holds the data for one line scanning period.

Level Shifter: Raises the driving voltage of 5 V to the appropriate LCD driving voltage.

LCD Driving Circuit: Outputs an 8-level LCD driving voltage. This circuit receives 3-bit data for one dot from latch circuit (2) and selects one level from eight voltage levels.

Test Circuit: Generates test signals.

System Configuration

A block configuration of the TFT-type color display system using the HD66310T is shown in figure 3.

The HD66310T receives 3-bit data for one pixel and selects one of the eight LCD driving voltage levels to send to the LCD. The LCD driving output circuit, which is produced by the CMOS structure, can use any LCD driving voltage level from V_{CC} to V_{EE}. When the LCD panel uses an RGB color filter (the Triad arrangement), 512 (8^3) colors can be displayed. When using an RGBW color filter (the Quad arrangement), 4096 (8^4) colors can be displayed.

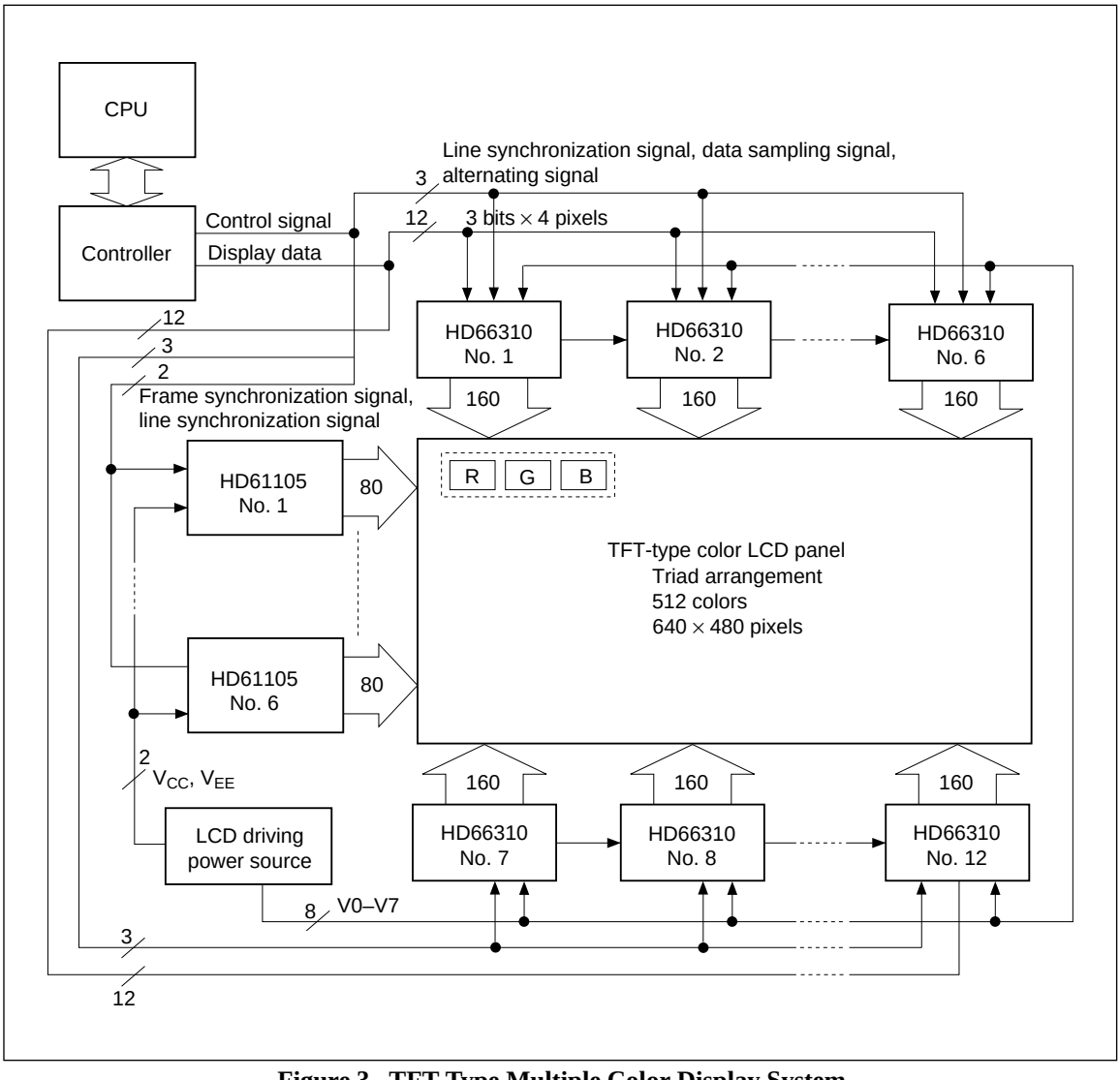


Figure 3 TFT-Type Multiple Color Display System

Internal Operation

8-Level Output

The HD66310 internal circuit unit for one data output is shown in figure 4. The circuit receives 3-bit data (D0j, D1j, D2j) and selects one of eight voltage levels (V0–V7) to output to the LCD.

The transfer gates of the output circuit are produced by the CMOS structure. Therefore, any voltage level between V_{CC} to V_{EE} can be applied to lines V0 to V7.

The HD66310 has 160 of the above circuits.

Operation Timing

The HD66310 operation timing is shown in figure 5.

When the SHL signal is at the GND level, data input is started by a low EIO1 (data input enable) signal. At the CL2 falling edge, 12 bits of data, which are for four outputs (3 bits for gray scales × 4 outputs), are input together. When the data input corresponding to 160 outputs are completed, the HD66310 automatically enters the stand-by mode, and the EIO2 signal changes to low.

The LCD driving output changes at the CL1 rising edge. The voltage level selected by data d1 is output from pin Y1, and the level selected by d160 is output from Y160. See table 1 for the voltage level selection by the input data.

When the SHL signal is at the V_{CC} level, data input is started by a low EIO2 signal. When the data input for 160 outputs are completed, the EIO1 signal changes to low. The voltage level selected by data d1 is output from pin Y160, and the level selected by d160 is output from Y1.

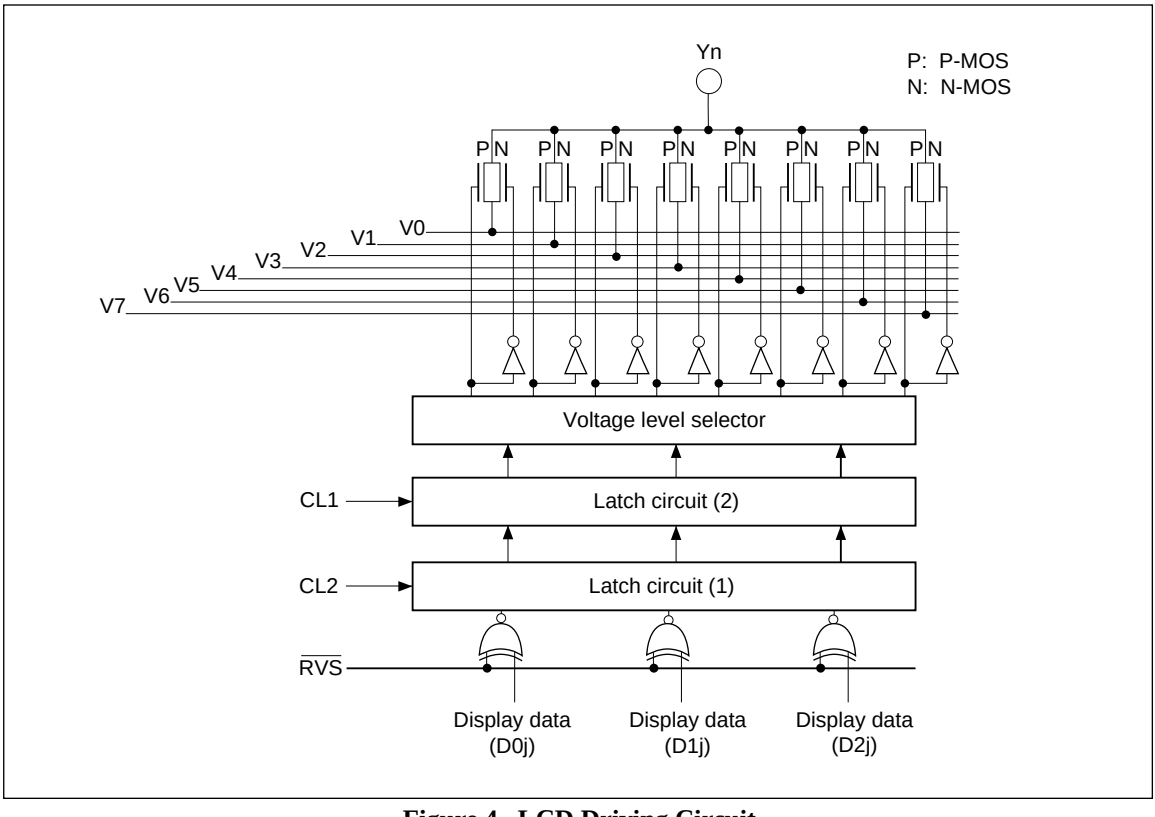


Figure 4 LCD Driving Circuit

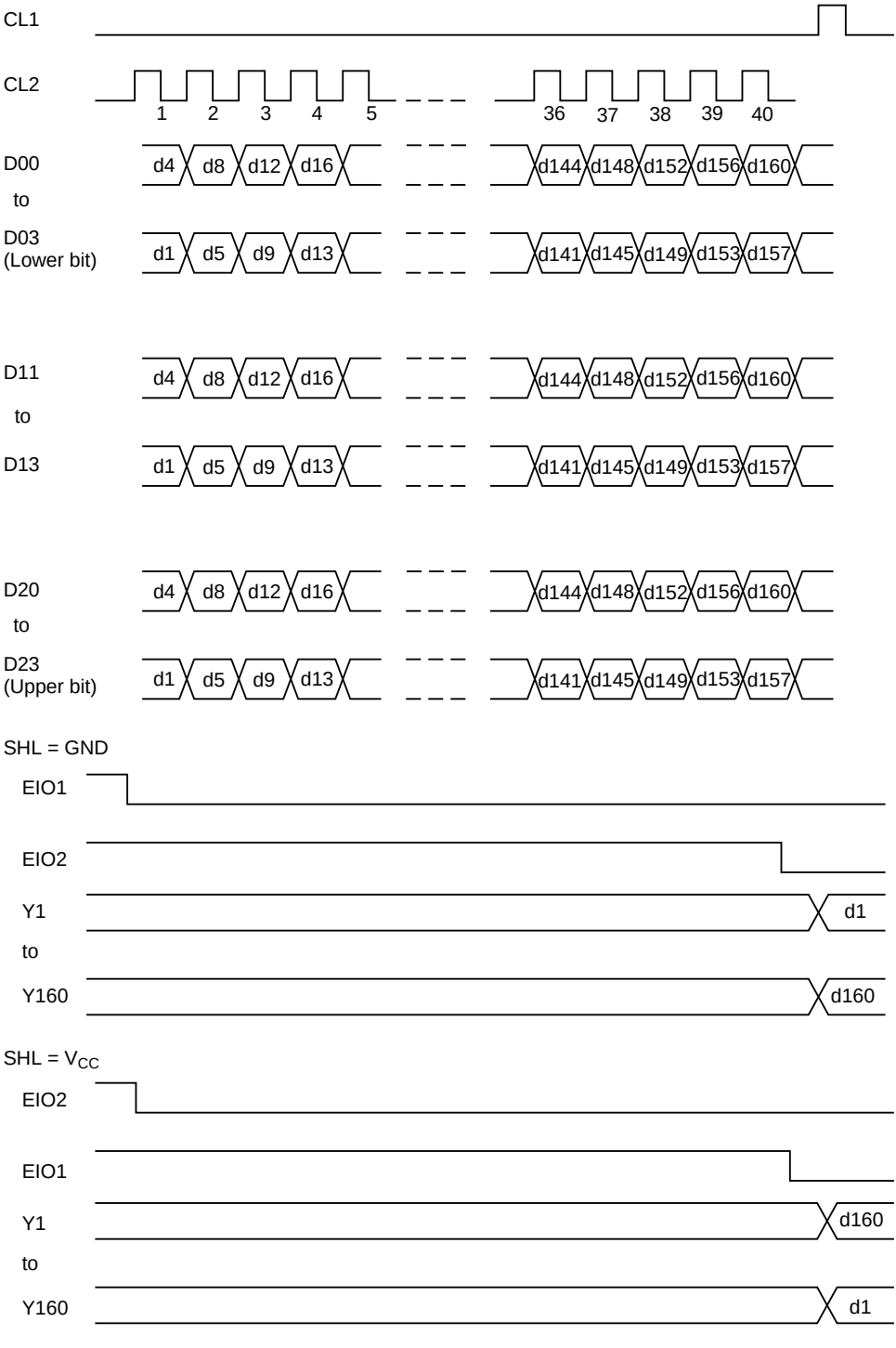


Figure 5 Basic Operation Timing Chart

Cascade Connection

When the SHL signal is at the GND level, the HD66310 begins to input data when the EIO1 signal goes low. When the data input is completed, the EIO2 signal changes to low. By connecting the EIO2 pin of the first HD66310 to the EIO1 pin of the next HD66310, the low EIO2 signal activates the next HD66310. Figure 6 shows a connection example.

When the SHL signal is at the VCC level, the EIO2 pin of the first HD66310 is connected to GND, and the EIO1 pin is connected to the next HD66310 EIO2 pin.

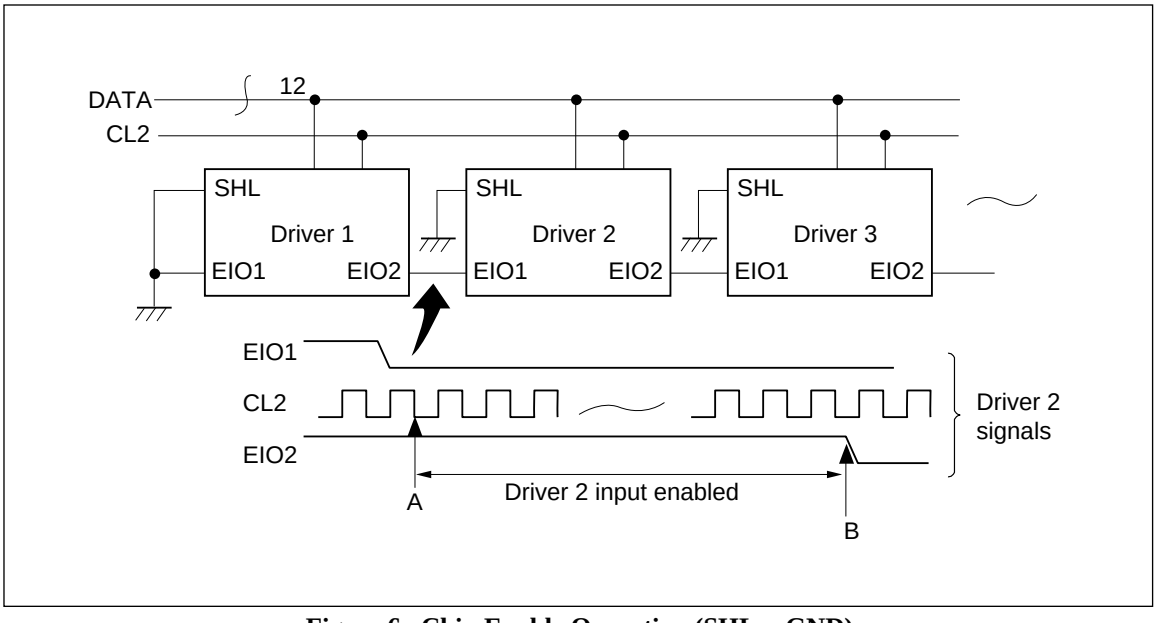


Figure 6 Chip Enable Operation (SHL = GND)

LCD Driving Power Supply Circuitry

Multiple-Level Driving Voltage Method

AC voltage must be applied to the LCD, since DC voltage deteriorates the LCD. To display eight gray scales, 16 voltage levels, shown in figure 7, must be applied.

Although the HD66310 has eight LCD driving voltage input levels, it can output 16 driving voltage levels using the level selector shown in figure 8, since the transfer gates of the output circuit are produced by the CMOS structure.

External Power Supply Circuitry

Figures 8 and 9 show the external power supply circuit when displaying 512 colors in the Triad arrangement, and figure 10 shows the circuit for displaying 64 colors in the Triad arrangement. Table 3 shows the specifications of the LCD panel and the HD66310 pins for each power supply circuit.

The circuit shown in figure 8 is the basic one used when displaying 512 colors in the Triad arrangement. However, the HD66310 can dispense with the level selector, as shown in figure 9, using the internal $\overline{RVS}$ (output reverse) pin. See table 1 for detailed $\overline{RVS}$ functions.

When displaying 64 colors in the Triad arrangement, the $\overline{RVS}$ pin functions as the alternating signal input pin, as shown in figure 10.

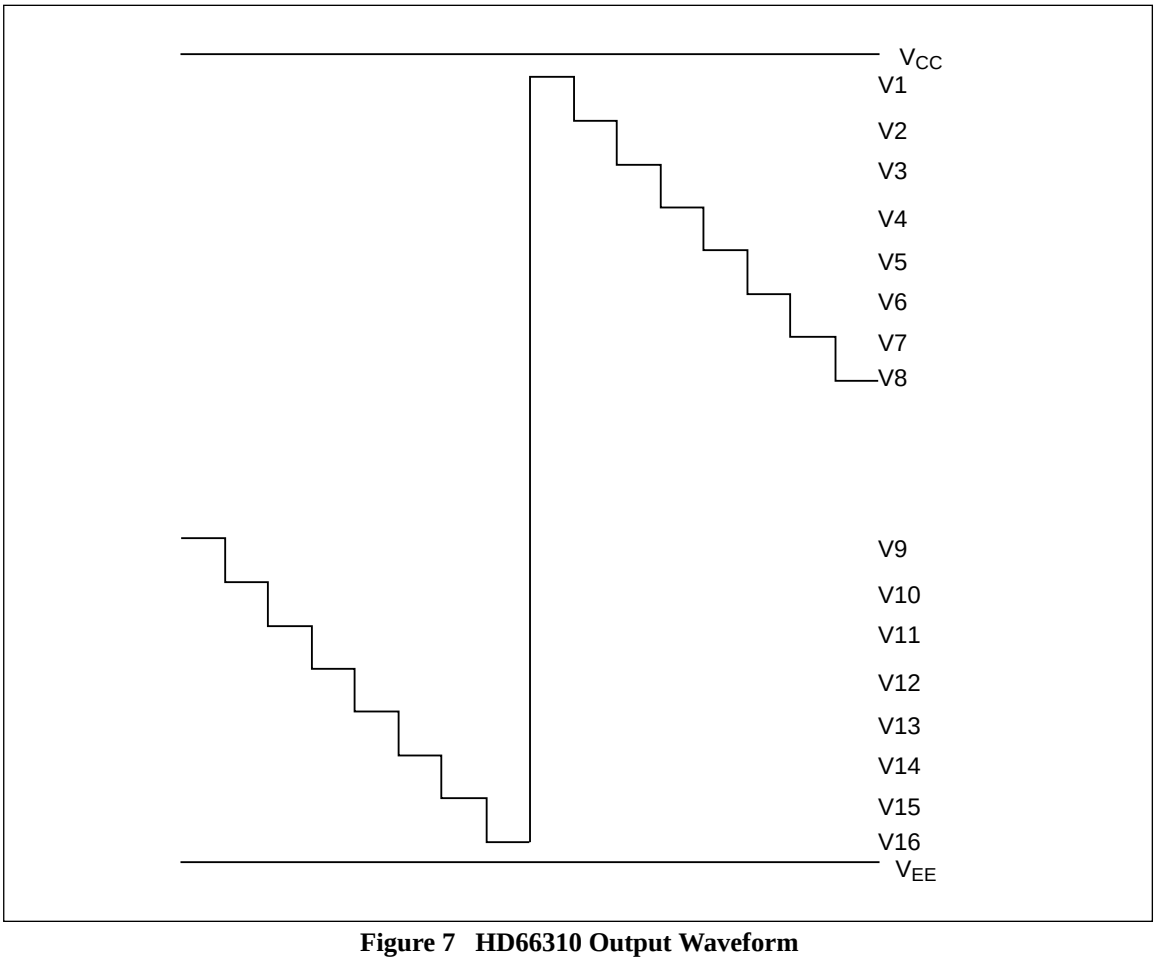


Figure 7 HD66310 Output Waveform

Table 3 Color Display and Pin Specifications

Output Level	Panel Spec.	Display Data Di2	Di1	Di0	$\overline{RVS}$ pin	Power Supply (Refer to)
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	1	Fig. 8
8 × 2 (AC)	Quad: 4096 colors Triad: 512 colors	1/0 (upper bit)	1/0	1/0 (lower bit)	Alternating signal	Fig. 9
4 × 2 (AC)	Quad: 256 colors Triad: 64 colors	1	1/0 (upper bit)	1/0 (lower bit)	Alternating signal	Fig. 10

1: V_{CC} level voltage
0: GND level voltage

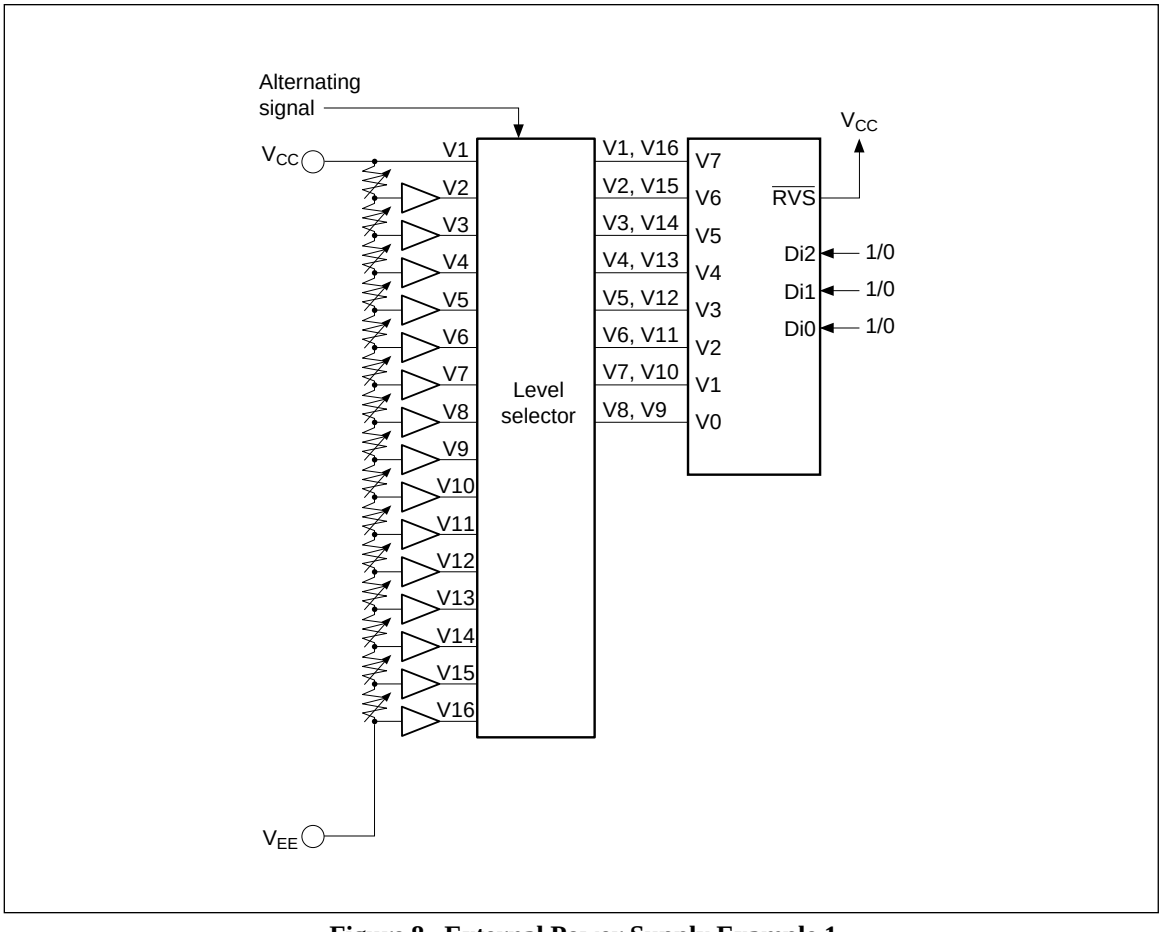


Figure 8 External Power Supply Example 1

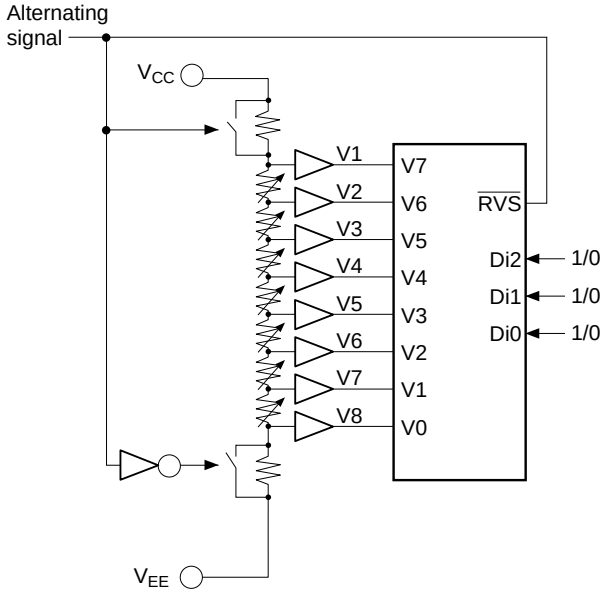


Figure 9 External Power Supply Example 2

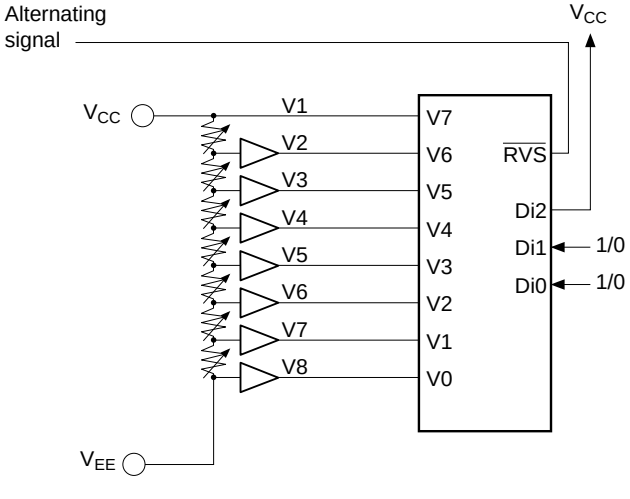


Figure 10 External Power Supply Example 3

Design for Timing

When using the RVS pins to simplify the power source, as shown in figures 9 and 10, it is recommended to add a vertical retrace period, (a scanning period in which no scan electrode is selected) at the end of a frame scanning period, as shown in figure 12, for the following two reasons.

- As shown in figure 4, the data reverse circuit is before the latch circuit (1). The LCD driving output is reversed one CL1 period after a transition of the $\overline{RVS}$ signal, as shown in figure 11. However, the power supply lines immediately reverses polarity after a transition of the $\overline{RVS}$ signal, as shown in figures 9 and 10. Therefore, the HD66310 outputs invalid data during the last CL1 of a frame period.
- In the power supply circuits shown in figures 9 and 10, voltage temporarily becomes unstable just after the $\overline{RVS}$ transition, causing the LCD display to become jumbled.

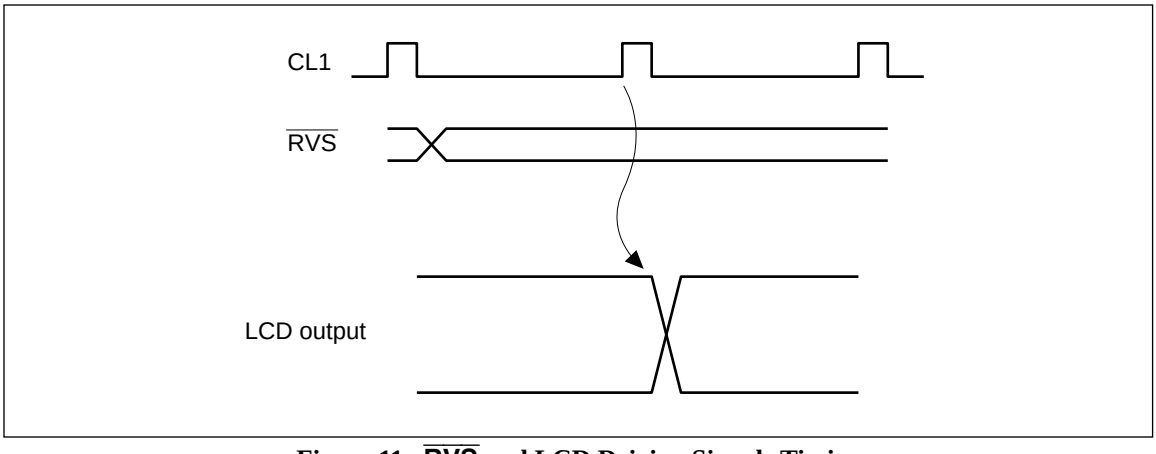


Figure 11 $\overline{RVS}$ and LCD Driving Signals Timing

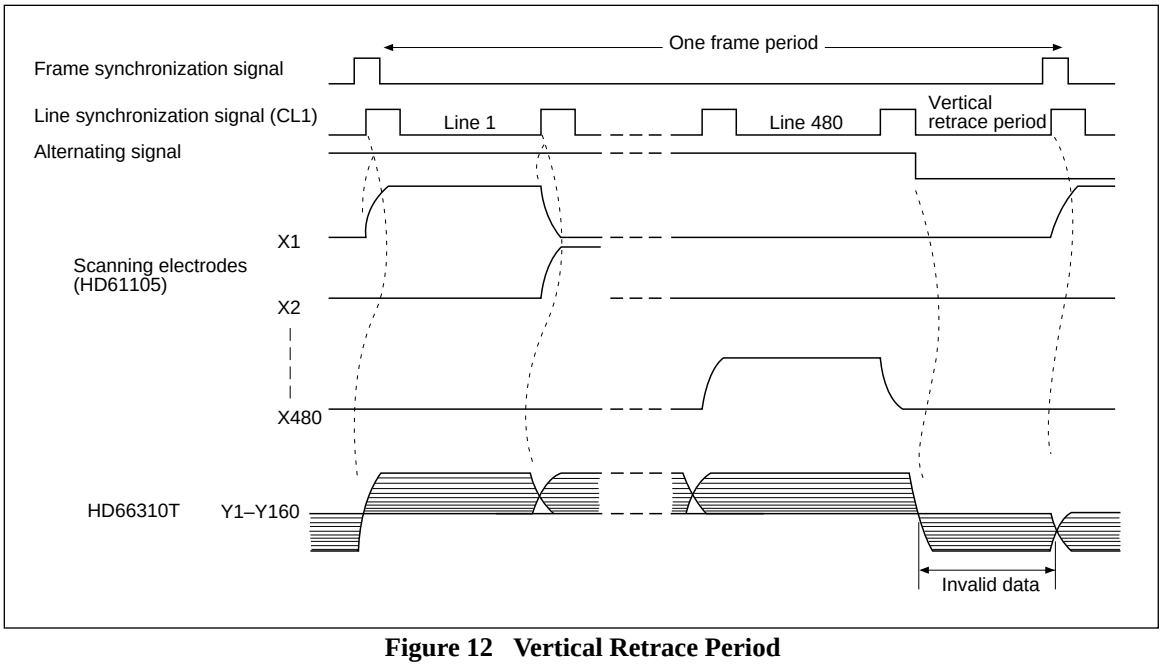


Figure 12 Vertical Retrace Period

Application

Figure 13 shows an HD66310T application for a 480 × 640-dot, 512-color LCD panel. Figure 14 shows the operation timing chart for the system.

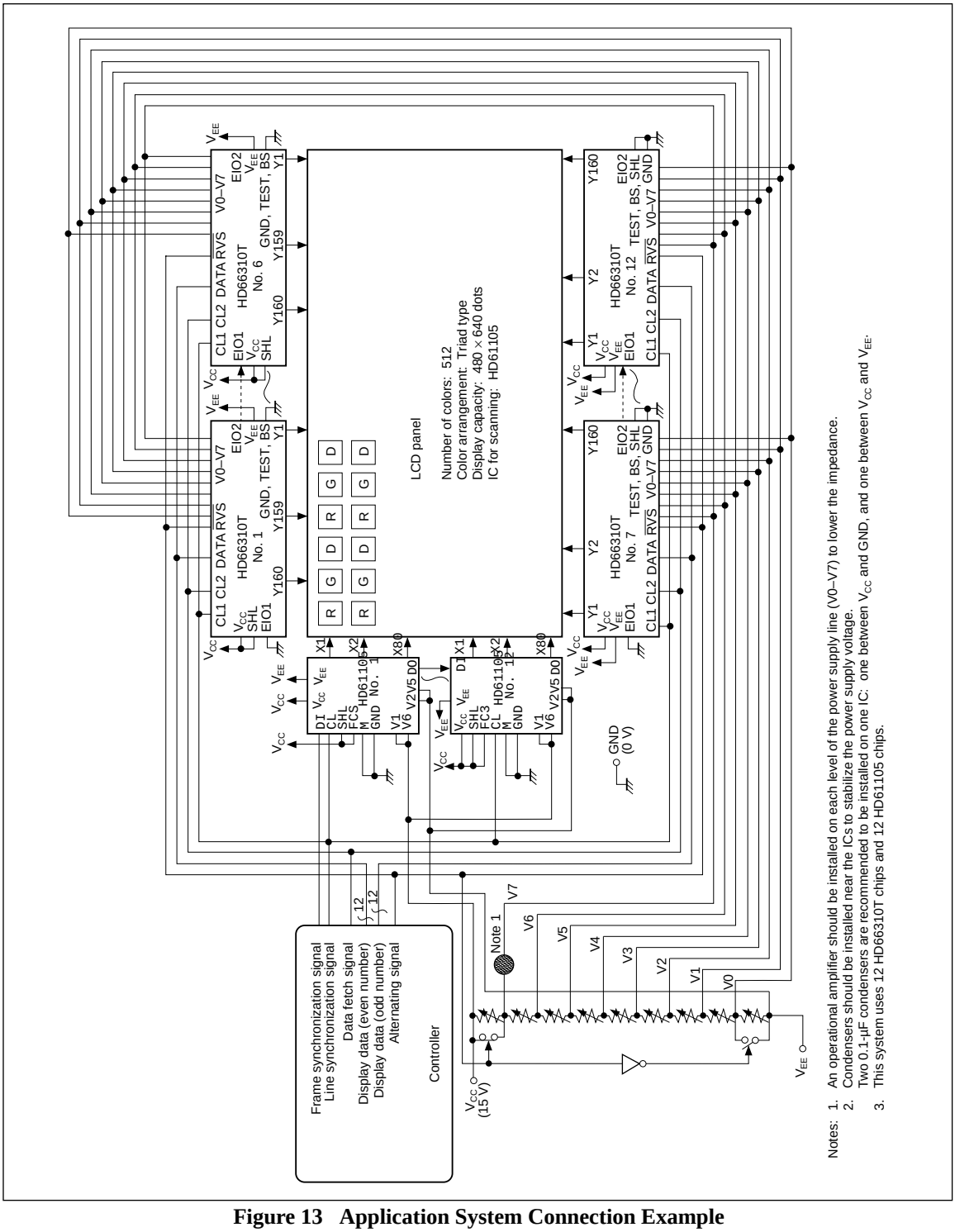


Figure 13 Application System Connection Example

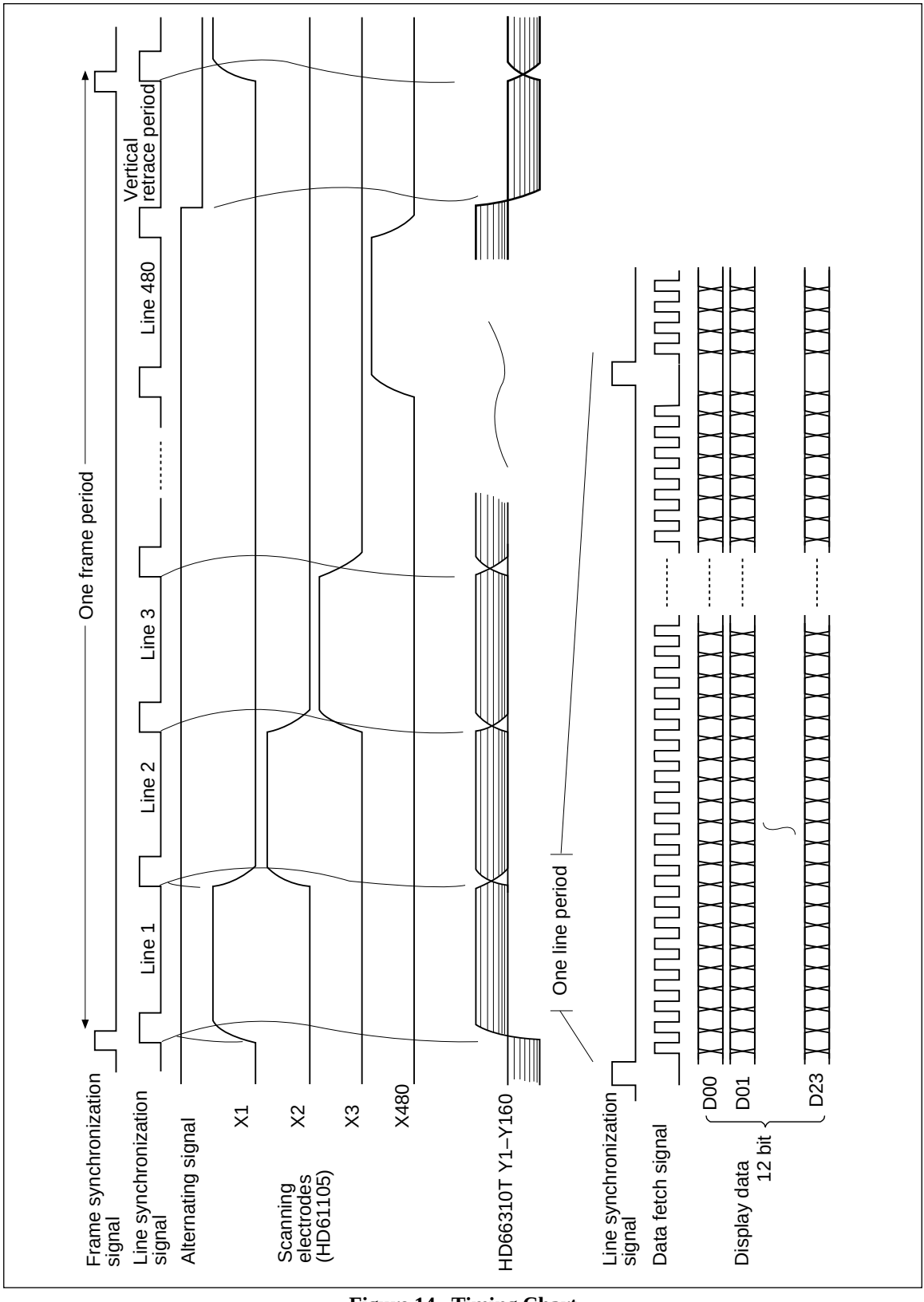


Figure 14 Timing Chart

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Power supply for logic unit	V_{CC}	–0.3 to +7.0	V	2
Power supply for LCD driving unit	V_{EE}	V_{CC} – 25 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)	V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
Operating temperature	T_{opr}	–20 to +75 (HD66310T00) –20 to +65 (HD66310T0015)	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes: 1. Exceeding the absolute maximum ratings could result in permanent damage to the LSI. The recommended operating conditions are within the electrical characteristic limits listed on the following pages. Exceeding these limits may cause malfunctions and affect reliability.

2. Values are in reference to GND = 0 V.

3. Applies to input pins SHL, CL1, CL2, BS, $\overline{RVS}$, TEST, and D00–D23. Also applies to input/output pins EIO1 and EIO2 when these pins function as input pins.

Electrical Characteristics

DC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, $V_{CC} - V_{EE}$ = 15 to 23 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
LCD driving power supply voltage	$V_{CC} - V_{EE}$	15		23	V		1
Input high-level voltage (1)	V_{IH1}	$0.8 \times V_{CC}$		V_{CC}	V		2
Input low-level voltage (1)	V_{IL1}	0		$0.2 \times V_{CC}$	V		2
Input high-level voltage (2)	V_{IH2}	$0.75 \times V_{CC}$		V_{CC}	V		3
Input low-level voltage (2)	V_{IL2}	0		$0.25 \times V_{CC}$	V		3
Output high-level voltage	V_{OH}	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	4
Output low-level voltage	V_{OL}			0.4	V	I_{OL} = 0.4 mA	4
Input leakage current (1)	I_{L1}	–5.0		+5.0	µA	$V_{IN} = V_{CC}$ to GND	5
Input leakage current (2)	I_{L2}	–10		+10	µA	$V_{IN} = V_{CC}$ to GND	6
Input leakage current (3)	I_{L3}	–100		+100	µA	$V_{IN} = V_{CC}$ to V_{EE}	7
LCD driver on resistance	RON			2.5	kΩ	$V_{CC} - V_{EE}$ = 20 V	8
Current consumption (1)	$-I_{P1}$			25 30	mA mA	Data fetch 12 MHz Data fetch 15 MHz	9, 11, 12
Current consumption (2)	$-I_{P2}$			2 2.5	mA mA	Stand-by 12 MHz Stand-by 15 MHz	9, 11, 12
Current consumption (3)	$-I_{P3}$			3 3.7	mA mA	12 MHz 15 MHz	10, 11, 12

Notes:
1. Voltage between V_{CC} and V_{EE}.
2. Applies to CL1, CL2, SHL, Dij, $\overline{RVS}$, TEST, and BS.
3. Applies to EIO1 (input) and EIO2 (input).
4. Applies to EIO1 (output) and EIO2 (output).
5. Applies to CL1, CL2, SHL, $\overline{RVS}$, Dij, TEST, and BS.
6. Applies to EIO1 (input) and EIO2 (input).
7. Applies to V0L to V7L and V0R to V7R.
8. Applies to Y1 to Y160.
9. Current between V_{CC} and GND under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.
10. Current between V_{CC} and V_{EE} under the conditions of $V_{IH} = V_{CC}$, V_{IL} = 0 V, and no load on the output pins.

11. f_{CL2} and f_{CL1} are 15 MHz, 37.5 kHz respectively in 15 MHz version.
12. f_{CL2} and f_{CL1} are 12 MHz, 30 kHz respectively in 12 MHz version.

AC Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, T_a = –20 to +75°C in 12 MHz version)
(V_{CC} = +5 V ±5%, GND = 0 V, T_a = –20 to +65°C in 15 MHz version)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Clock period	t_{CYC}	83 (66)			ns		1
Clock high-level pulse width	t_{CWH}	30 (23)			ns		1
Clock low-level pulse width	t_{CWL}	30 (23)			ns		1
Clock rise time	t_R			10 (10)	ns		2
Clock fall time	t_F			10 (10)	ns		2
Clock setup time	t_{SU}	100 (100)			ns		2
Clock hold time	t_H	100 (100)			ns		2
Data setup time	t_{DSU}	20 (10)			ns		3
Data hold time	t_{DH}	30 (25)			ns		3
Enable input setup time	t_{ESU}	20 (10)			ns		4
Enable output delay time	t_{ED}			53 (46)	ns	See figure 16 for test load	4
CL1 high-level pulse width	t_{WH}	100 (100)			ns		5
$\overline{RVS}$ setup time	t_{RSU}	50 (50)			ns		6
$\overline{RVS}$ hold time	t_{RH}	50 (50)			ns		6

Data in ( ) is the characteristics in 15 MHz version.

Notes: 1. Applies to CL2.
2. Applies to CL1 and CL2.
3. Applies to Dij and CL2.
4. Applies to EIO1, EIO2, and CL2.
5. Applies to CL1.
6. Applies to $\overline{RVS}$ and CL2.

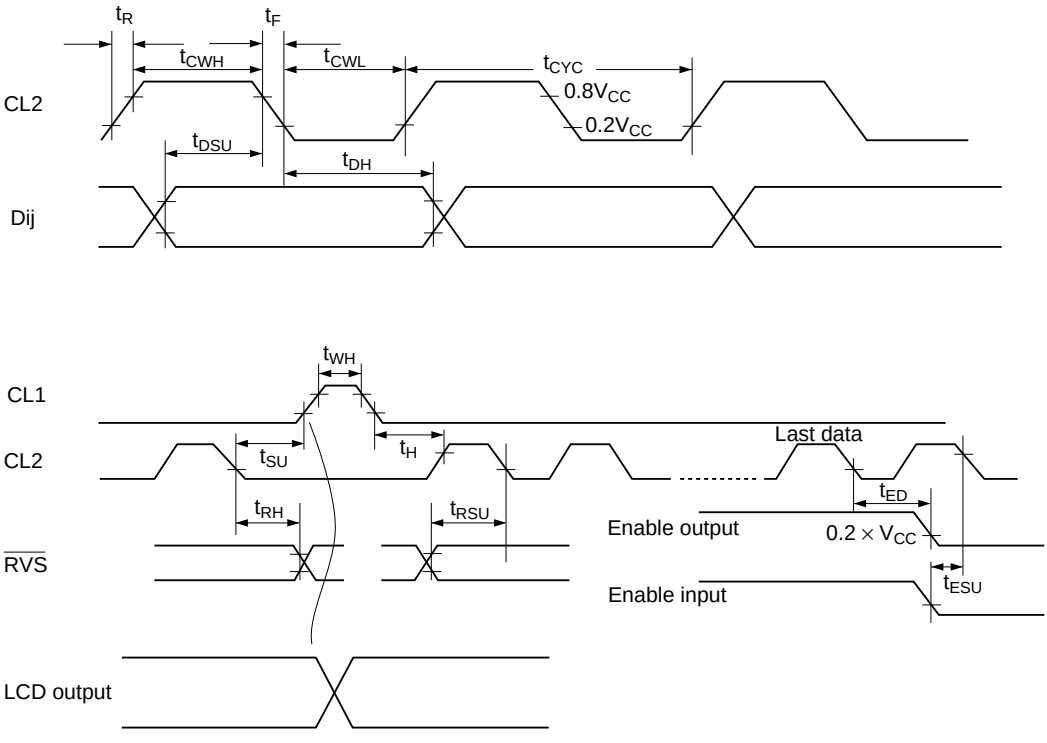


Figure 15 Timing Chart

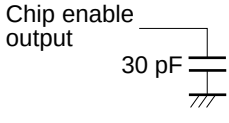


Figure 16 Test Load