HD66330T (TFT Driver)

64-Level Gray Scale Driver for TFT Liquid Crystal Display

HITACHI

Description

The HD66330T, a signal driver LSI, drives an active matrix LCD panel having TFTs (thin film transistor) in the picture element (pixel) area. The LSI receives 6-bit digital display data per dot and outputs corresponding gray scale voltage. This LSI easily achieves multicoloring of a VGA-sized color TFT LCD and is suitable for applications such as multimedia.

Features

- Multicolor display
  The HD66330T receives 6-bit digital display data per dot, and selects and outputs an LCD drive voltage among 64-level gray scale voltages. When R, G, and B color filters are added to the LCD panel, a maximum of 260,000 colors can be displayed.
- High-speed operation
  Operating clock: 35 MHz maximum
  Amount of input data: 3 dots × 6 bits (gray scale data)
- Applicable systems
  PC (640 × 480/400 dots) systems
- Internal 192-bit drive function
- Internal standby function
- Internal chip-enable signal generation circuit
- Supply voltage: 4.5 V to 5.5 V
- Bidirectional shift

Ordering Information

Type No.	Outer Lead Pitch (µm)	Package
HD66330TA0	160	236-pin TCP

Note: The details of TCP pattern are shown in “The Information of TCP.”

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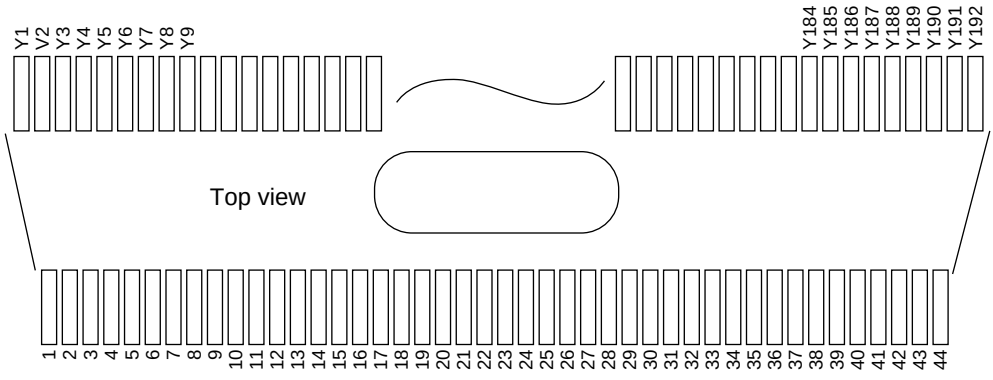
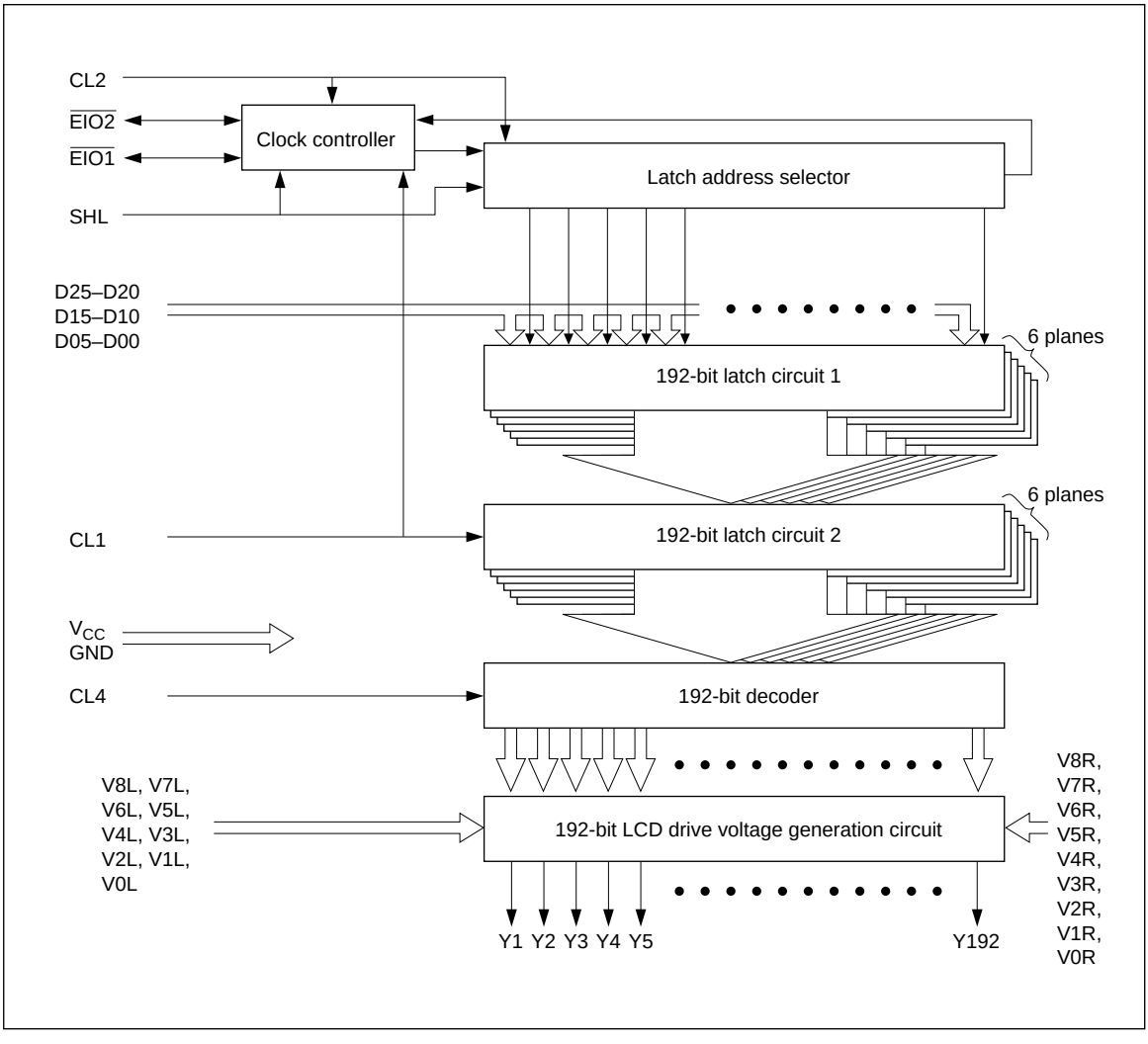
Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

1	V8L	11	D01	21	SHL	31	D21	41	V5R
2	V7L	12	D02	22	GND	32	D22	42	V6R
3	V6L	13	D03	23	$\overline{\text{EIO2}}$	33	D23	43	V7R
4	V5L	14	D04	24	E10	34	D24	44	V8R
5	V4L	15	D05	25	D11	35	D25		
6	V3L	16	$\overline{\text{EIO1}}$	26	D12	36	V0R		
7	V2L	17	CL4	27	D13	37	V1R		
8	V1L	18	CL2	28	D14	38	V2R		
9	V0L	19	CL1	29	D15	39	V3R		
10	D00	20	V_{CC}	30	D20	40	V4R		

Internal Block Diagram



Block Functions

Clock Controller: Generates chip enable signals ($\overline{EIO2}$ and $\overline{EIO1}$) and controls the internal timing signals.

Latch Address Selector: Generates latch signals, which sequentially trigger latch operation of input display data.

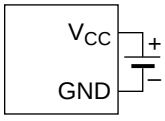
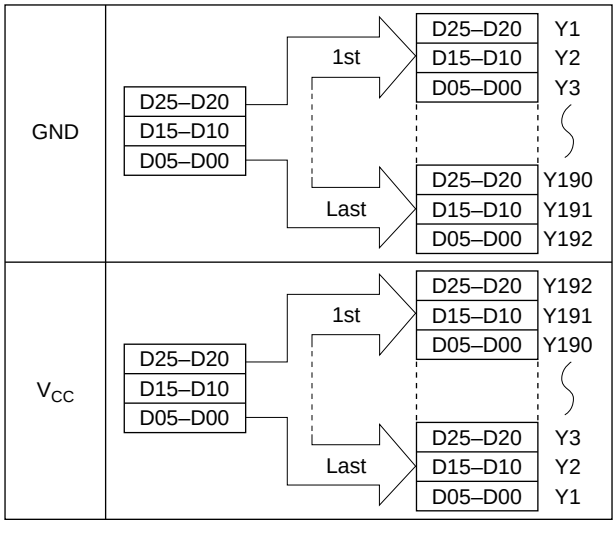
Latch Circuit 1: Latches 3-pixel × 6-bit sequentially input display data; composed of 192 × 6 bits.

Latch Circuit 2: Latches 192 × 6-bit data latched in latch circuit 1 synchronously with the CL1 signal.

Decoder: Generates a decode signal per pixel for the LCD drive voltage generation circuit using an upper 3-bit decoder and a lower 3-bit decoder.

LCD Drive Voltage Generation Circuit: Generates LCD drive voltages from LCD drive power supply voltages according to the decode signals generated by the decoder.

Pin Functions

Signal Name	Numbers	I/O	Functions
V_{CC}	1	Power supply	 V_{CC}–GND: Supplies power to the LSI.
GND	1	Power supply	
V8L–V0L, V8R–V0R	18	Power supply	Supplies power to the LCD drive voltage generation circuit. The same voltage must be applied to corresponding L- and R-power pins within a range of V_{CC} to GND.
CL1	1	Input	Inputs display data latch pulses for latch circuit 2. At the rising edge of each CL1 pulse, latch circuit 2 latches display data input from latch circuit 1 and outputs LCD drive voltages corresponding to the latched data.
CL2	1	Input	Inputs display data latch pulses for latch circuit 1. At the falling edge of each CL2 pulse, latch circuit 1 latches display data input via D25–D00 and outputs the latched data to latch circuit 2.
D25–D20, D15–D10, D05–D00	18	Input	Inputs 6-bit (gray scale data) × 3-pixel display data.
SHL	1	Input	Selects the shift direction of the display data. 
CL4	1	Input	Controls the 2-phase function. A high level period of this signal specifies the first phase period that performs high output current operation, and a low level specifies the second phase period that outputs the voltage corresponding to the display data.

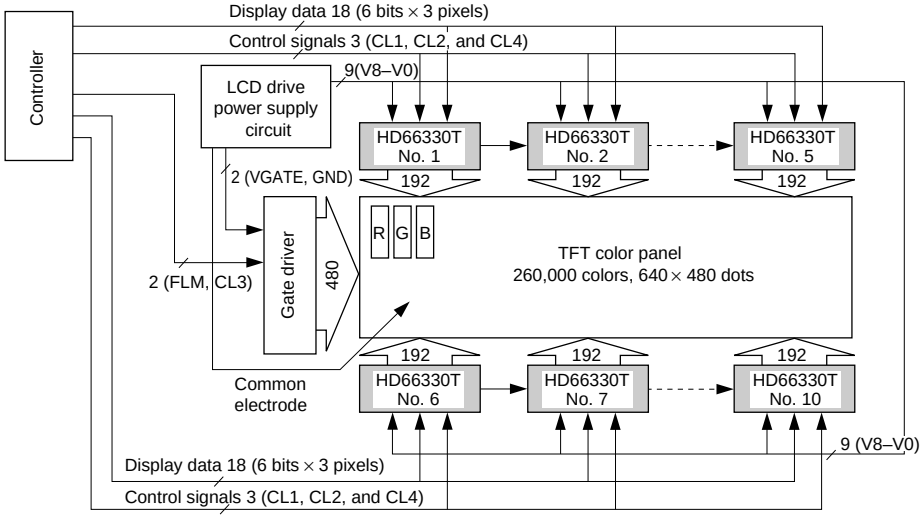
Signal Name	Numbers	I/O	Functions
$\overline{EIO1}$, $\overline{EIO2}$	2	Input/output	Provides chip-enable signals. Input or output depends on the SHL signal, as shown below. At any one time, the signal being used for input must go low to enable the LSI to latch display data, and the signal being used for output will be driven low after 192 pixels of display data have been read.
Y1–Y192	192	Output	Outputs LCD drive voltages.

SHL Level	$\overline{EIO1}$	$\overline{EIO2}$
GND	Input	Output
V_{CC}	Output	Input

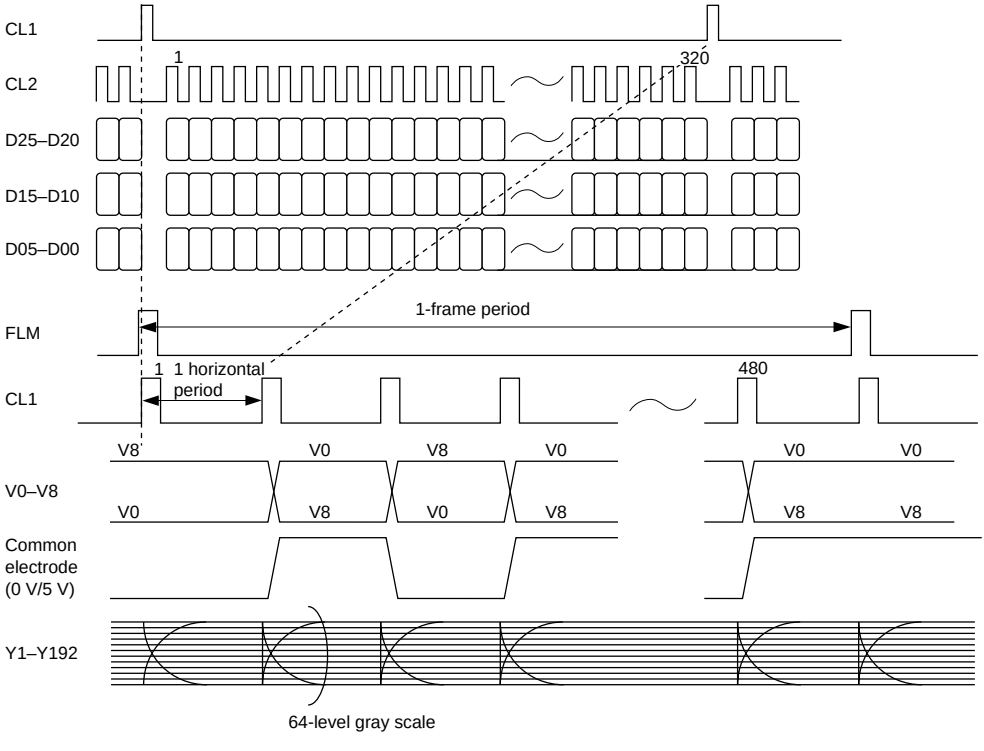
System Overview

The following shows a block diagram of a TFT color LCD system configured with multiple HD66330Ts. The HD66330Ts latch 6-bit data per dot, and selects and outputs one level among 64 internally generated LCD drive voltage levels. When the pixels are structured using R, G, and B color filters, a maximum of 260,000 colors can be displayed.

System block diagram

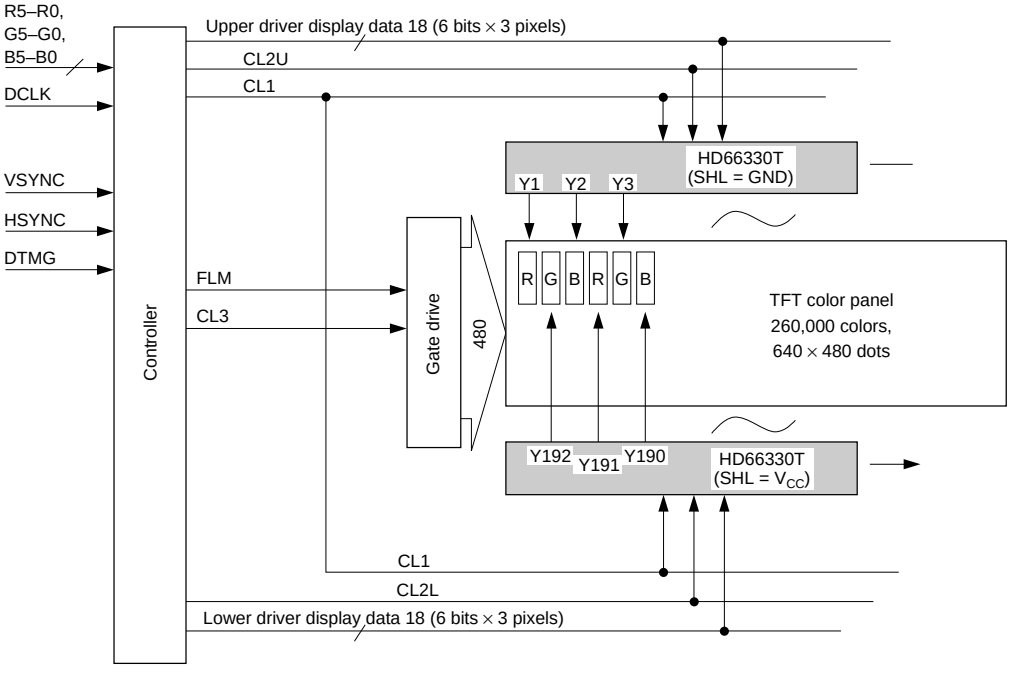


Timing chart (example of the common-voltage AC-drive method)

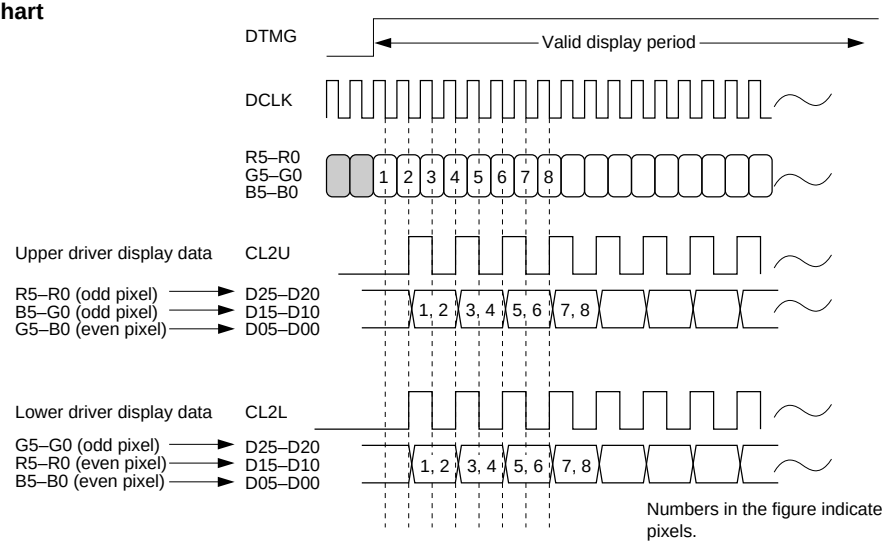


Timing Chart for Display Data

The following figures show the display data timing and hardware configuration for the TFT color LCD system configured with HD66330Ts. Since color panels usually have a narrow connection pitch with driver LSIs, the HD66330Ts should be located above (upper drivers) and below (lower drivers) the panel and alternately connected to the panel pins. In such a configuration, the RGB data and the system dot clock (DCLK) should be divided between the upper and lower drivers. Here, DCLK should be divided into two by the controller.

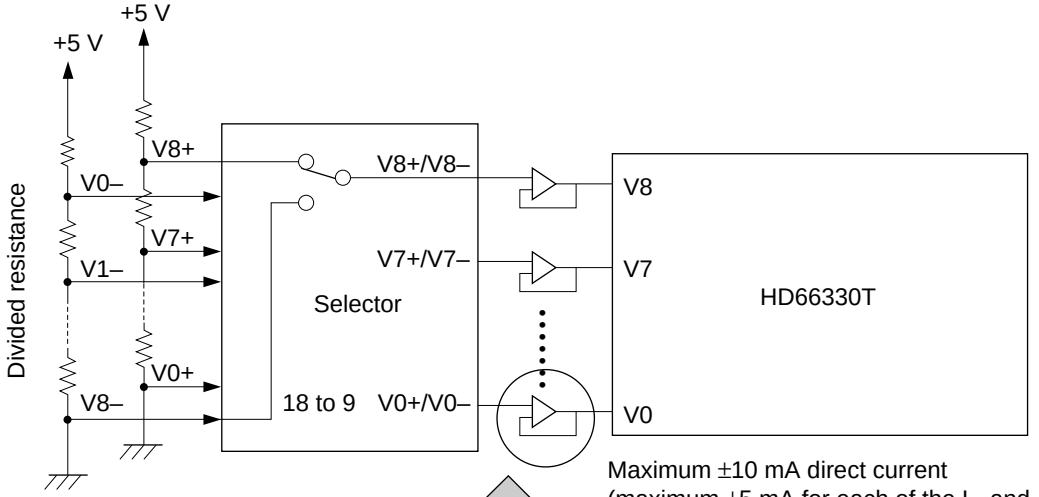


Timing chart



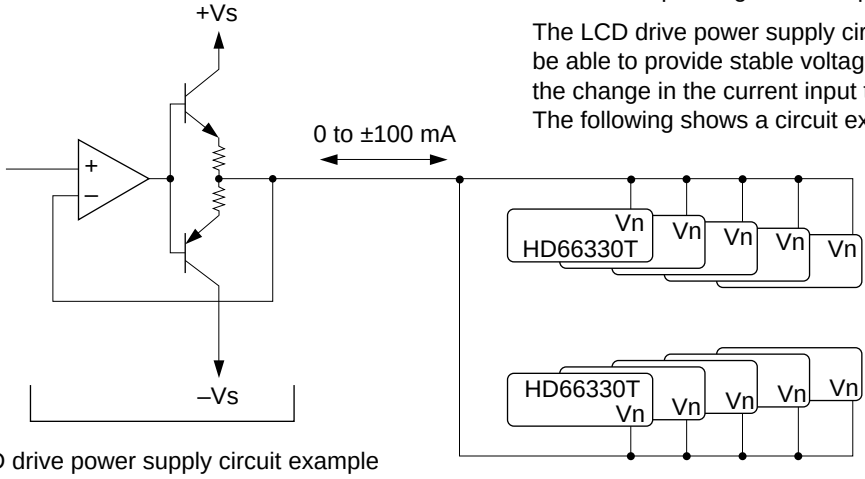
Power Supply Circuit Example

The figures below show an example of a circuit used to generate LCD drive power supply voltages V0 to V8. In this example, 18 levels of voltage are generated by divided resistance to alternate the current for the LCD panel, and either positive or negative voltages are selected and supplied to the HD66330T. To stabilize voltage, an operational amplifier should be connected to each selector output.



Maximum ±10 mA direct current (maximum ±5 mA for each of the L- and R-pins) flows in the LCD drive power supply voltage pins V0 to V8 of one HD66330T. When 10 ICs are used, the current amounts to ±100 mA maximum. The direct current changes within 0 to ±100 mA depending on the display data.

The LCD drive power supply circuit must be able to provide stable voltage despite the change in the current input to the IC. The following shows a circuit example:



LCD drive power supply circuit example
(per one voltage level)

Power Supply Voltage Examples

Voltage levels to be input to LCD drive power supply pins V0 to V8 should be determined according to panel specifications such as voltage intensity characteristics. The table below lists voltage level examples for reference:

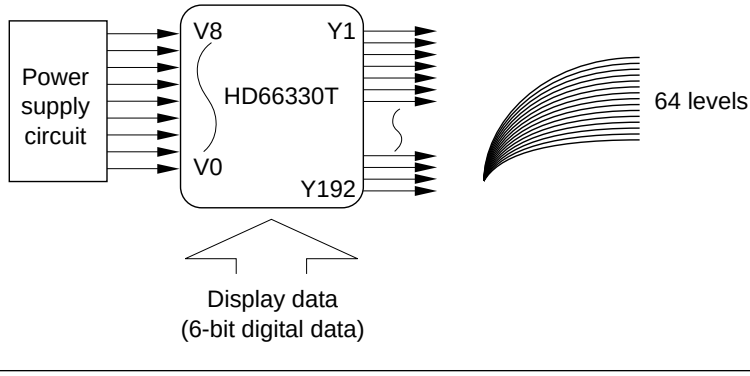
	V0	V1	V2	V3	V4	V5	V6	V7	V8	Counter Electrode
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0	0
	5.0	4.0	3.5	3.0	2.5	2.0	1.5	1.0	0	5.0

Relationship between Display Data and Output Voltage

The HD66330T outputs 64-level gray scale voltage generated by 9 levels of LCD drive power supply voltage and 6-bit digital data. The figure below shows the relationship among the input voltages from the LCD drive power supply circuit, digital codes, and output voltages.

Display Data						Output Voltage	
Di5	Di4	Di3	Di2	Di1	Di0	1st Phase	2nd Phase
0	0	0	0	0	0	V1	V0 + 1/8 × (V1–V0)
0	0	0	0	0	1	V1	V0 + 2/8 × (V1–V0)
0	0	0	0	1	0	V1	V0 + 3/8 × (V1–V0)
0	0	0	0	1	1	V1	V0 + 4/8 × (V1–V0)
0	0	0	1	0	0	V1	V0 + 5/8 × (V1–V0)
0	0	0	1	0	1	V1	V0 + 6/8 × (V1–V0)
0	0	0	1	1	0	V1	V0 + 7/8 × (V1–V0)
0	0	0	1	1	1	V1	V1
0	0	1	0	0	0	V2	V1 + 1/8 × (V2–V1)
0	0	1	0	0	1	V2	V1 + 2/8 × (V2–V1)
0	0	1	0	1	0	V2	V1 + 3/8 × (V2–V1)
0	0	1	0	1	1	V2	V1 + 4/8 × (V2–V1)
0	0	1	1	0	0	V2	V1 + 5/8 × (V2–V1)
0	0	1	1	0	1	V2	V1 + 6/8 × (V2–V1)
0	0	1	1	1	0	V2	V1 + 7/8 × (V2–V1)
0	0	1	1	1	1	V2	V2
0	1	0	0	0	0	V3	V2 + 1/8 × (V3–V2)
0	1	0	0	0	1	V3	V2 + 2/8 × (V3–V2)
0	1	0	0	1	0	V3	V2 + 3/8 × (V3–V2)
0	1	0	0	1	1	V3	V2 + 4/8 × (V3–V2)
0	1	0	1	0	0	V3	V2 + 5/8 × (V3–V2)
0	1	0	1	0	1	V3	V2 + 6/8 × (V3–V2)
0	1	0	1	1	0	V3	V2 + 7/8 × (V3–V2)
0	1	0	1	1	1	V3	V3
0	1	1	0	0	0	V4	V3 + 1/8 × (V4–V3)
0	1	1	0	0	1	V4	V3 + 2/8 × (V4–V3)
0	1	1	0	1	0	V4	V3 + 3/8 × (V4–V3)
0	1	1	0	1	1	V4	V3 + 4/8 × (V4–V3)
0	1	1	1	0	0	V4	V3 + 5/8 × (V4–V3)
0	1	1	1	0	1	V4	V3 + 6/8 × (V4–V3)
0	1	1	1	1	0	V4	V3 + 7/8 × (V4–V3)
0	1	1	1	1	1	V4	V4
1	0	0	0	0	0	V5	V4 + 1/8 × (V5–V4)
1	0	0	0	0	1	V5	V4 + 2/8 × (V5–V4)
1	0	0	0	1	0	V5	V4 + 3/8 × (V5–V4)
1	0	0	0	1	1	V5	V4 + 4/8 × (V5–V4)
1	0	0	1	0	0	V5	V4 + 5/8 × (V5–V4)
1	0	0	1	0	1	V5	V4 + 6/8 × (V5–V4)
1	0	0	1	1	0	V5	V4 + 7/8 × (V5–V4)
1	0	0	1	1	1	V5	V5
1	0	1	0	0	0	V6	V5 + 1/8 × (V6–V5)
1	0	1	0	0	1	V6	V5 + 2/8 × (V6–V5)
1	0	1	0	1	0	V6	V5 + 3/8 × (V6–V5)
1	0	1	0	1	1	V6	V5 + 4/8 × (V6–V5)
1	0	1	1	0	0	V6	V5 + 5/8 × (V6–V5)
1	0	1	1	0	1	V6	V5 + 6/8 × (V6–V5)
1	0	1	1	1	0	V6	V5 + 7/8 × (V6–V5)
1	0	1	1	1	1	V6	V6
1	1	0	0	0	0	V7	V6 + 1/8 × (V7–V6)
1	1	0	0	0	1	V7	V6 + 2/8 × (V7–V6)
1	1	0	0	1	0	V7	V6 + 3/8 × (V7–V6)
1	1	0	0	1	1	V7	V6 + 4/8 × (V7–V6)
1	1	0	1	0	0	V7	V6 + 5/8 × (V7–V6)
1	1	0	1	0	1	V7	V6 + 6/8 × (V7–V6)
1	1	0	1	1	0	V7	V6 + 7/8 × (V7–V6)
1	1	0	1	1	1	V7	V7
1	1	1	0	0	0	V8	V7 + 1/8 × (V8–V7)
1	1	1	0	0	1	V8	V7 + 2/8 × (V8–V7)
1	1	1	0	1	0	V8	V7 + 3/8 × (V8–V7)
1	1	1	0	1	1	V8	V7 + 4/8 × (V8–V7)
1	1	1	1	0	0	V8	V7 + 5/8 × (V8–V7)
1	1	1	1	0	1	V8	V7 + 6/8 × (V8–V7)
1	1	1	1	1	0	V8	V7 + 7/8 × (V8–V7)
1	1	1	1	1	1	V8	V8

Note: 1st phase: The period in which 2-phase control signal CL4 is high and high output current operation is performed.
2nd phase: The period in which 2-phase control signal CL4 is low and low output current operation is performed.



Output Offset Voltage

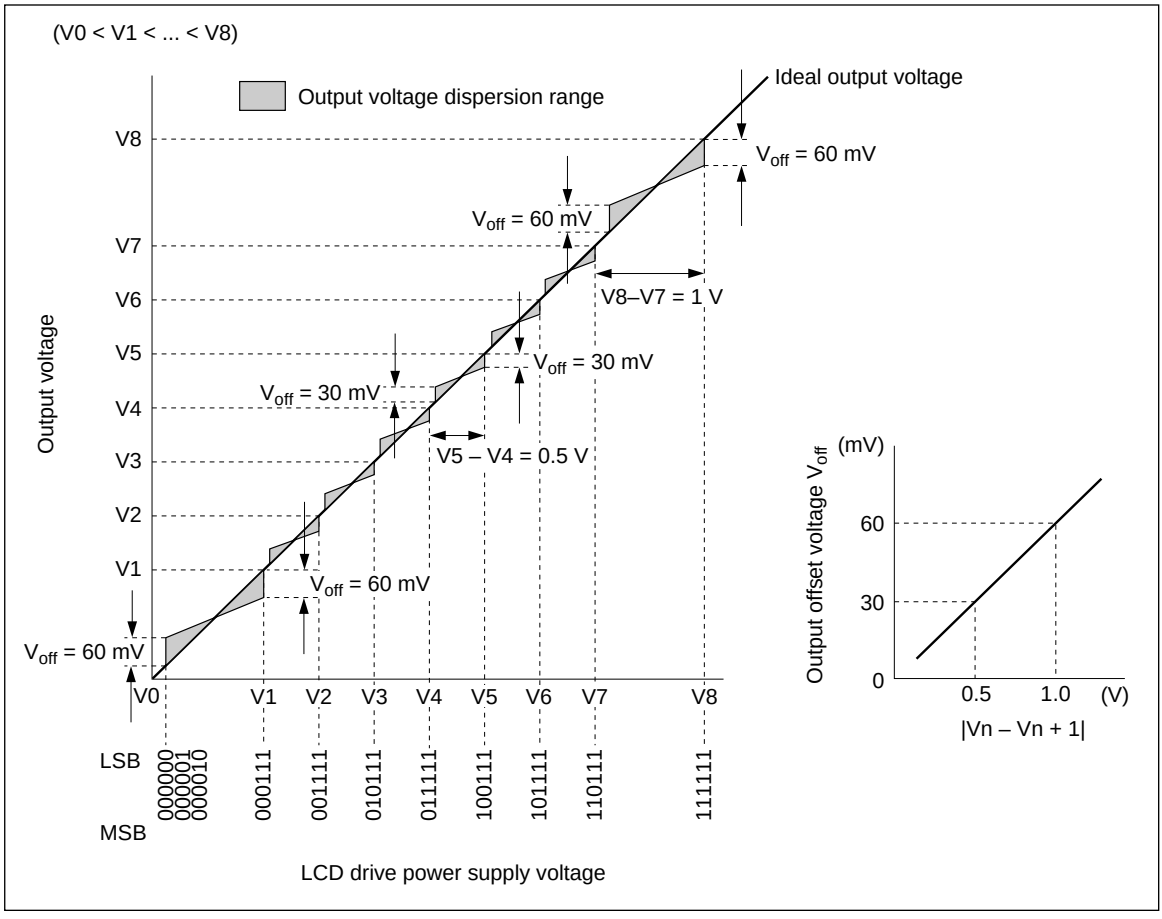
The HD66330T has an internal DA converter per output. The upper three bits of 6-bit display data select and apply the LCD drive power supply voltage level to the DA converter, and the lower three bits select and output one analog voltage level.

Output offset voltage Voff is defined as the difference between the actual output voltage and the ideal output voltage expected from the LCD drive power supply voltage and digital display data. The Voff can be considered as the total output voltage differences including the differences between LSIs, between different output pins of the same LSI, and that caused by concentrated current in a LSI due to a particular display pattern.

The figure below shows the characteristics of output voltage with respect to LCD drive power supply voltages. Since output offset voltage Voff depends on the difference between adjoining LCD drive power supply voltages |Vn – Vn + 1| (n = 0 to 7) output offset voltage will also decrease when the power supply voltage difference |Vn – Vn + 1| is decreased.

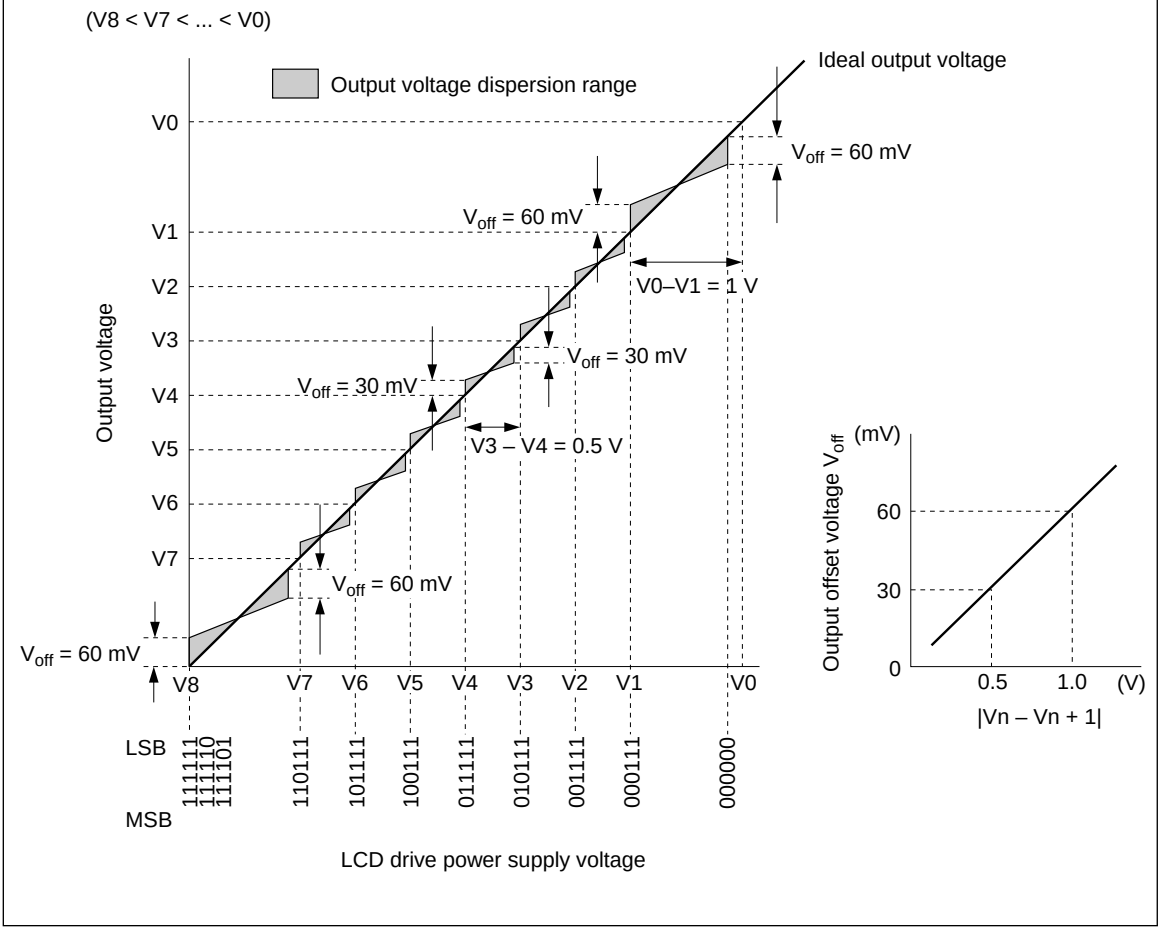
LCD Drive Power Supply Voltage Examples

	V0	V1	V2	V3	V4	V5	V6	V7	V8
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



LCD Drive Power Supply Voltage Examples

	V8	V7	V6	V5	V4	V3	V2	V1	V0
Voltage (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	5.0



2-Phase Operation

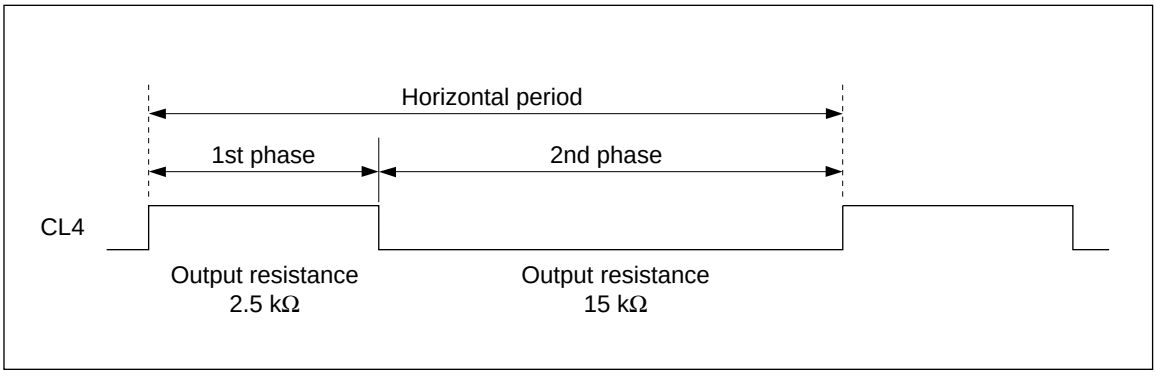
A high-speed low-power output switching function is provided by dividing the horizontal period into 1st-and 2nd-phase periods, where high output current operation and low output current operation are alternately performed.

During the 1st-phase period, the specified voltage is applied to the LCD panel quickly with a low output impedance of about 2.5 kΩ (high output current operation). Here, the applied voltage is selected by the upper three bits of display data.

During the 2nd-phase period, a voltage is applied corresponding to the display data with an output impedance of about 15 kΩ (low output current operation).

In general, since it is not required to secure the 1st phase in a 640 × 480-dot color panel (see the figure below for assumed load condition), CL4 can be fixed low.

This function is effective when the panel load is large or when a horizontal period is short and gray scale voltage must be applied quickly. For settings in the 1st-phase period, see note 4 in Electrical Characteristics.



Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage	V_{CC}	–0.3 to +7.0	V	1
Input voltage (1)	V_{t1}	–0.3 to +V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{t2}	–0.3 to +V_{CC} + 0.3	V	1, 3, 4
LCD power supply input current	I_t	±20	mA	5
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Notes: 1. Assuming GND = 0 V.

2. Applies to input pins CL1, CL2, CL4, SHL, and Dij, and I/O pins $\overline{EIO1}$ and $\overline{EIO2}$ when used as input.
3. Specifies voltage to be input to the LCD drive power supply pins.
   Either of the following relationships must hold:
   $V_{CC} \geq V8 \geq V7 \geq V6 \geq V5 \geq V4 \geq V3 \geq V2 \geq V1 \geq V0 \geq GND$ or
   $V_{CC} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7 \geq V8 \geq GND$
4. The following relationship must hold for V0 to V8 potentials:
   $|Vn - Vn + 1| \leq 2$ V (n = 0 to 7)
5. Specifies the maximum ratings for current in the LCD drive power supply input pins V0 to V8 (total current for both L and R pins).

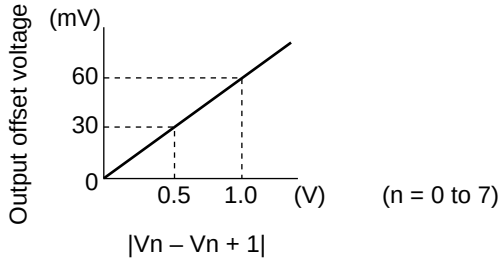
Electrical Characteristics

DC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Conditions	Notes
Input high-level voltage	V_{IH}	CL1, Cl2, SHL,Dij, CL4, EIO1(I), EIO2(I)	2.2		V_{CC}	V		
Input low-level voltage	V_{IL}		0		0.8	V		
Output high-level voltage	V_{OH}	EIO1(O), EIO2(O)	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	
Output low-level voltage	V_{OL}				0.4	V	I_{OL} = 0.4 mA	
Input leakage current (1)	I_{L1}	CL1, Cl2, SHL, Dij, CL4	–5		+5	µA		
Input leakage current (2)	I_{L2}	EIO1(I), EIO2(I)	–10		+10	µA		
LCD drive power supply input current	I_t	V0L–V8L, V0R–V8R	–10		+10	mA	Total of L and R pins |Vn – Vn + 1| = 1 V (n = 0 to 7)	
Output offset voltage	V_{off}	Y1–Y192	—		60	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	1
			—		30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Difference between output pins	V_{ref}	Y1–Y192	—		±30	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 1 V (n = 0 to 7)	2
			—		±15	mV	V_{CC} – GND = 5 V |Vn – Vn + 1| = 0.5 V (n = 0 to 7)	
Driver output ON resistance	R_{on1}	Y1–Y192	—		2.5	kΩ	1st phase V_{CC} – GND = 5 V	
	R_{on2}	Y1–Y192	—		15	kΩ	2nd phase V_{CC} – GND = 5 V	
Current consumption (1)	I_{p1}	Between V_{CC} and GND	—		20	mA	Data latch f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	3
Current consumption (2)	I_{p2}	Between V_{CC} and GND	—		1.5	mA	Standby f_{CL2} = 15 MHz, f_{CL1} = 33 kHz	

Notes: 1. Output offset voltage V_{off} is defined as difference between the actual output voltage and output voltage expected from the LCD drive power supply voltage and digital display data.

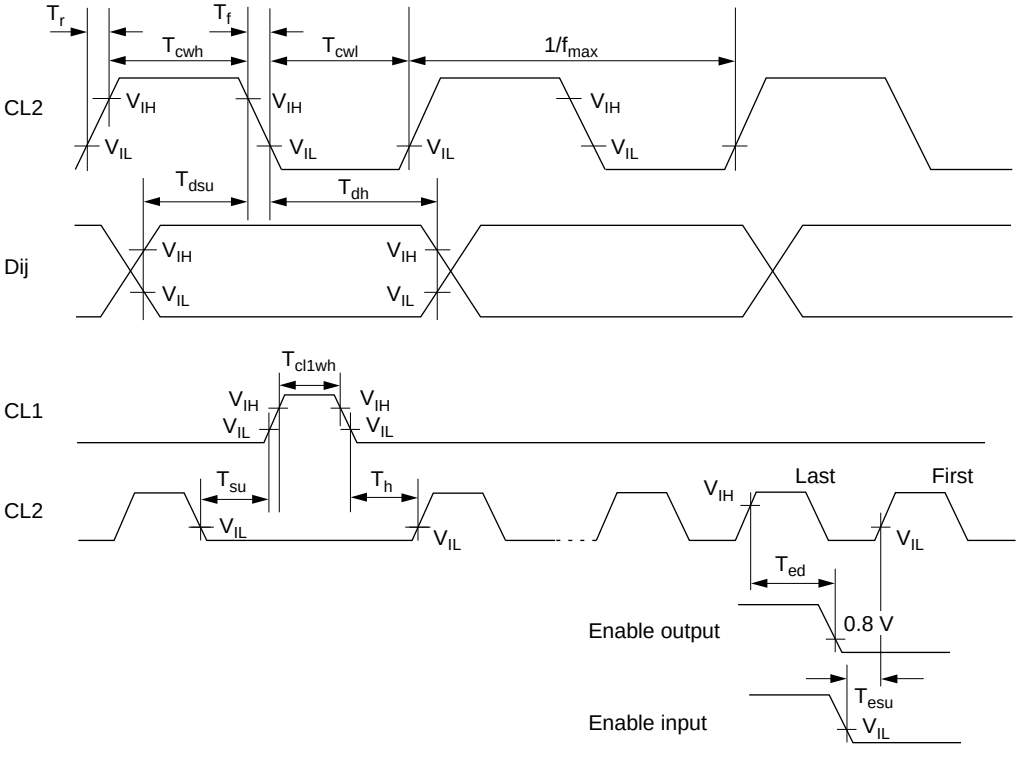
V_{off} shows the following characteristics with respect to voltage difference between adjoining LCD drive power supply pins |Vn – Vn + 1|.



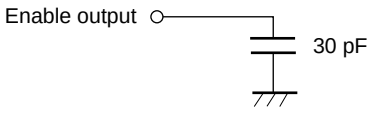
2. V_{ref} can be considered as the maximum total output voltage differences including the differences between LSIs, between output pins of the same LSI, and that caused by concentrated current in an LSI due to a particular display pattern.
3. Except for the current flowing in V0 to V8; outputs are unloaded.

AC Characteristics (V_{CC} – GND = 4.5 to 5.5 V, and T_a = –20 to +75°C, unless otherwise noted)

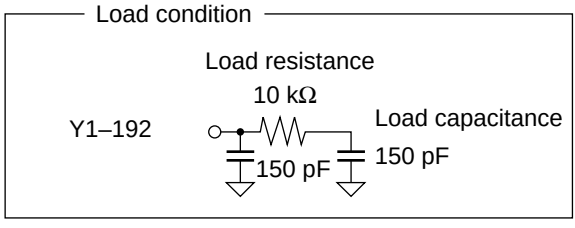
Item	Symbol	Applicable Pin	Min	Typ	Max	Unit	Test Condition	Notes
Operating frequency	f_{max}	CL2			35	MHz		
Clock high-level width	T_{cwh}	CL2	9			ns		
Clock low-level width	T_{cwl}	CL2	9			ns		
Clock rise time	T_r	CL1, CL2			5	ns		
Clock fall time	T_f	CL1, CL2			5	ns		
Clock setup time	T_{su}	CL1, CL2	50			ns		
Clock hold time	T_h	CL1, CL2	70			ns		
Data setup time	T_{dsu}	Dij, CL2	6			ns		
Data hold time	T_{dh}	Dij, CL2	6			ns		
Enable setup time	T_{esu}	EIO1, EIO2, CL2	4			ns		
Enable output delay time	T_{ed}	EIO1, EIO2, CL2			18	ns		1
CL1 high-level width	T_{cl1wh}	CL1	56			ns		
Driver output delay time	T_{dd}	CL1, Y1–Y192			20	µs		2, 3, 4

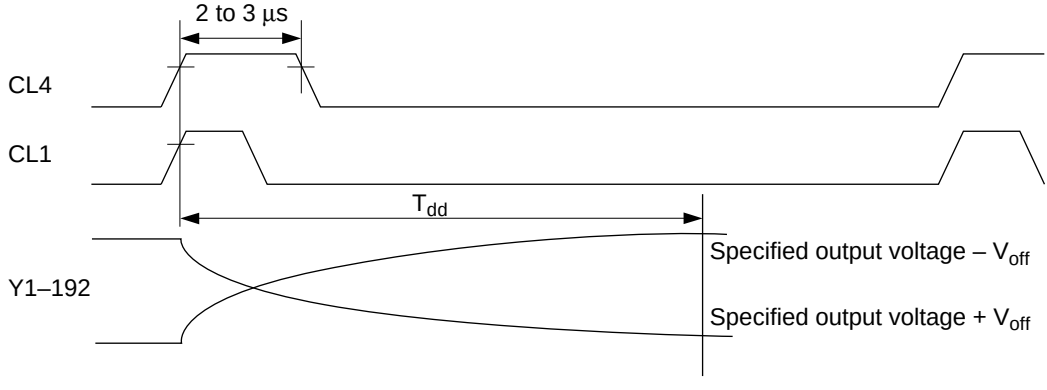


Notes: 1. The figure below shows the load condition for the enable output pins.

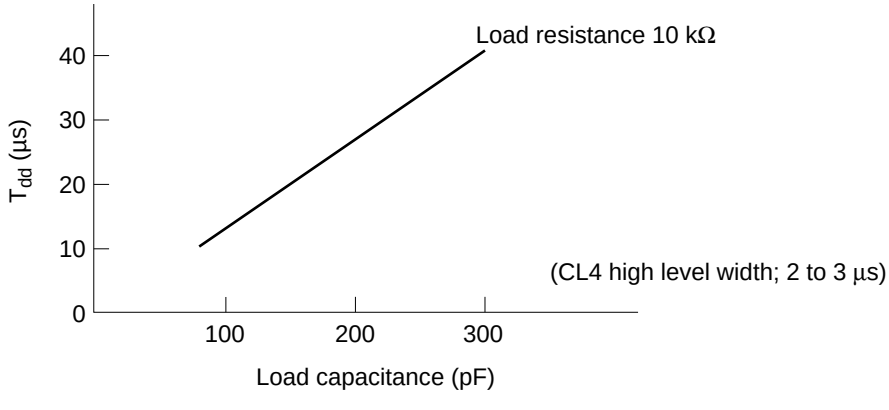


2. Specified by the following load condition and timing.





3. Driver output delay time T_{dd} has the following characteristics with respect to the load condition.



4. Driver output delay time T_{dd} has the following characteristics with respect to the CL4 high-level width.