# HD66410

## (RAM-Provided 128-Channel Driver for Dot-Matrix Graphic LCD)

Preliminary

HITACHI

## Description

The HD66410 drives and controls a dot-matrix graphic LCD using a bit-mapped display method. It provides a highly flexible display through its on-chip display RAM, in which each bit of data can be used to turn on or off one dot on the LCD panel.

A single HD66410 can display a maximum of 128 × 33 dots using its powerful display control functions. It features 24-channel annunciator output operating with 1/3 duty cycle that is available even during standby modes, which makes it suitable for time and other mark indications.

An MPU can access the HD66410 at any time because the MPU operations are asynchronous with the HD66410's system clock and display operations.

Its low-voltage operation at 2.2 to 3.6 V and the standby function provides low power-dissipation, making the HD66410 suitable for small portable device applications.

## Features

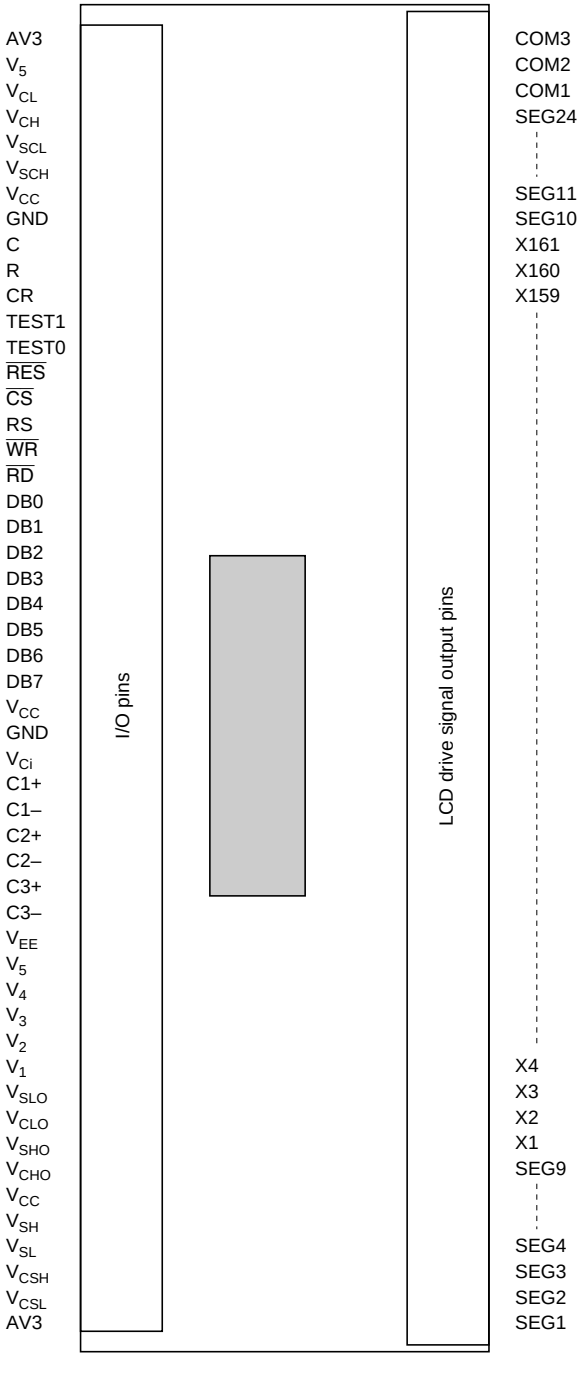
- 4.2-kbit (128 × 33-bit) bit-mapped display RAM
- 128 × 33 dots displayed using a single HD66410
  - 8 characters × 2 lines (16 × 16-dot character)
  - 21 characters × 4 lines (6 × 8-dot character)
- Annunciator display using dedicated output channels
  - Maximum of 72 segments displayed with 1/3 duty cycle
  - Available even during standby modes
- Flexible LCD driver configuration
  - Row output from both sides of an LCD panel
  - Row output from one side of an LCD panel
- Low power-dissipation suitable for long battery-based operation
  - Low-voltage operation: 2.2 to 3.6 V
  - Two standby modes: modes with and without annunciator display
- On-chip double to quadruple booster
- Versatile display control functions
  - Display data read/write
  - Display on/off
  - Column address inversion according to column driver layout
  - Vertical display scroll
  - Blink area select
  - Read-modify-write
- 80-system CPU interface through 8-bit asynchronous data bus
- On-chip oscillator combined with external resistors and capacitors
- Tape carrier package (TCP)

## Ordering Information

| Type No. | Package |
|---|---|
| HD66410Txx | TCP |

Hitachi semiconductor

## Pin Arrangement




Note: This figure is not drawn to a scale.

## Pin Description

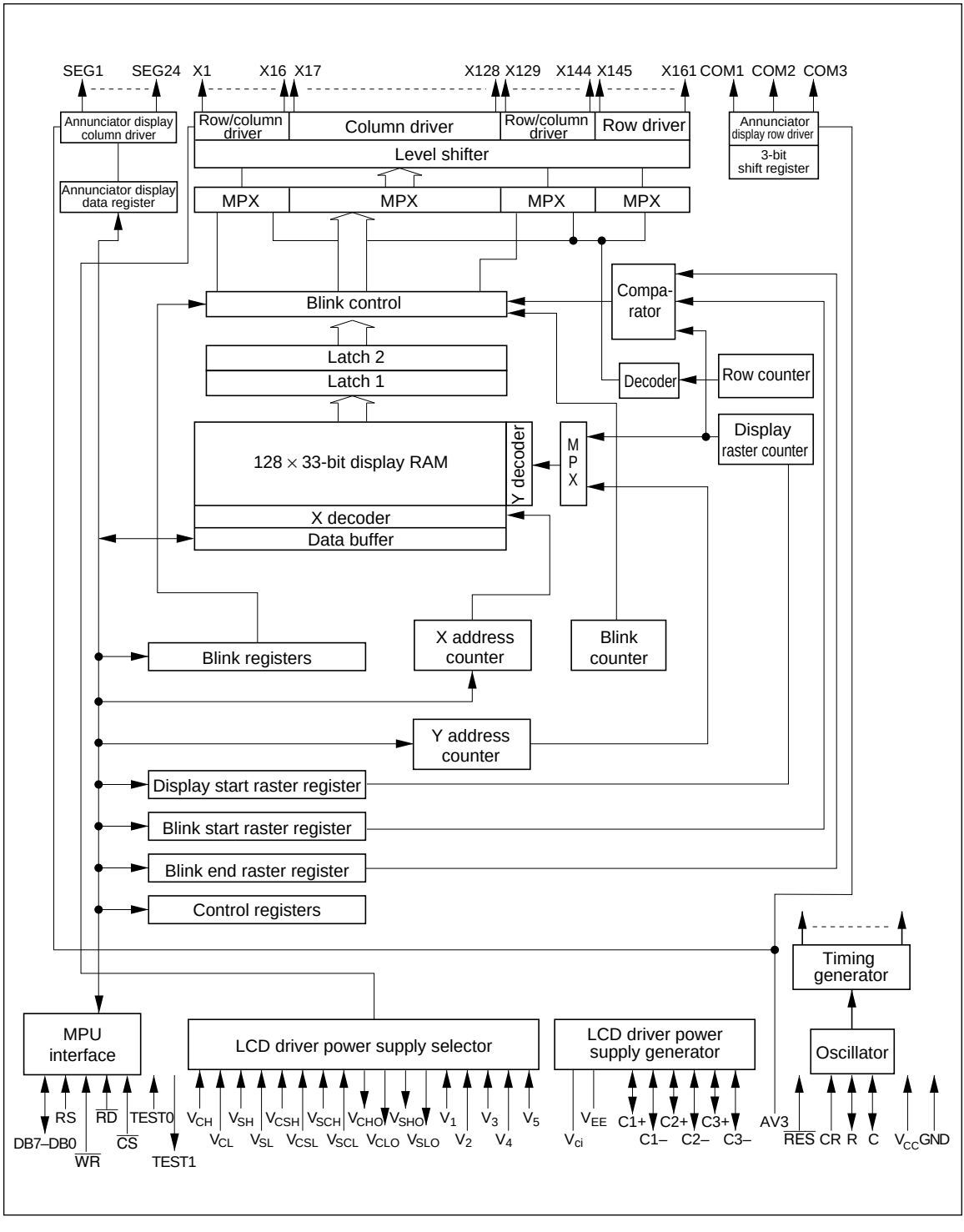
| Pin Name | Number of Pins | I/O | Connected to | Description |
|---|---|---|---|---|
| $V_{CC}$, GND | 5 | — | Power supply | $V_{CC}$: +2.2 to +3.6 V, GND: 0 V |
| Vci | 1 | — | Power supply | Inputs voltage to the booster to generate the base of the LCD drive voltages ($V_{EEC}$ and $V_{EEL}$); must be below $V_{CC}$. Vci: 0 to +3.6 V. |
| AV3 | 1 | — | Power supply | Supplies power to the internal annunciator drivers to generate the annunciator drive voltages using AV3 and $V_{CC}$. $V_{CC}$–AV3: 0 to 3.6 V; must be above GND. |
| $V_{EE}$ | 1 | I/O | Booster capacitors and V5 | Boosts and outputs the voltage input to the Vci pin; must be connected to the booster capacitors and V5 pin. |
| V1, V2, V3, V4, V5 | 5 | — | Resistive divider | Supplies several levels of power to the internal LCD drivers for dot-matrix display; must be applied with the appropriate level of bias for the LCD panel used. |
| C1+ to C3+, C1– to C3– | 6 | — | Booster capacitor | Must be connected to external capacitors according to the boosting ratio. |
| $V_{SHO}$, $V_{SLO}$ | 2 | O | VSH, VSL, VCSH, VCSL, VSCH, VSCL | Output voltage to be supplied to the internal column drivers. |
| $V_{CHO}$, $V_{CLO}$ | 2 | O | VCH, VCL, VCSH, VCSL, VSCH, VSCL | Output voltage to be supplied to the internal row drivers. |
| $V_{SH}$, $V_{SL}$ | 2 | I | VSHO, VSLO | Input voltage to be supplied to internal drivers X17 to X128. |
| $V_{CH}$, $V_{CL}$ | 2 | I | VCHO, VCLO | Input voltage to be supplied to internal drivers X145 to X160. |
| $V_{CSH}$, $V_{CSL}$ | 2 | I | VCHO, VCLO, VSHO, VSLO | Input voltage to be supplied to internal drivers X1 to X16. |
| $V_{SCH}$, $V_{SCL}$ | 2 | I | VCHO, VCLO, VSHO, VSLO | Input voltage to be supplied to internal drivers X129 to X144. |
| C, R, CR | 3 | I, I/O | Oscillator resistor and capacitor | Must be connected to external capacitors and resistors when using R-C oscillation. When using an external clock, it must be input to the CR pin. |
| $\overline{RES}$ | 1 | I | — | Resets the LSI internally when driven low. |
| $\overline{CS}$ | 1 | I | MPU | Selects the LSI, specifically internal registers (index and data registers) when driven low. |
| RS | 1 | I | MPU | Selects one of the internal registers; selects the index register when driven low and data registers when driven high. |
| $\overline{WR}$ | 1 | I | MPU | Inputs write strobe; allows a write access when driven low. |

| Pin Name | Number of Pins | I/O | Connected to | Description |
|---|---|---|---|---|
| $\overline{RD}$ | 1 | I | MPU | Inputs read strobe; allows a read access when driven low. |
| DB7 to DB0 | 8 | I/O | MPU | 8-bit three-state bidirectional data bus; transfers data between the HD66410 and MPU through this bus. |
| X1 to X16, X129 to X144 | 32 | O | Liquid crystal display | Output column or row drive signals; either column or row can be selected by programming. |
| X17 to X128 | 112 | O | Liquid crystal display | Output column drive signals. |
| X145 to X161 | 17 | O | Liquid crystal display | Output row drive signals. |
| COM1 to COM3 | 3 | O | Liquid crystal display | Output row drive signals for annunciator display; available even during standby modes. Can operate statically or with 1/3 duty cycle. |
| SEG1 to SEG24 | 24 | O | Liquid crystal display | Output column drive signals for annunciator display; available even during standby modes. |
| TEST0 | 1 | I | GND | Tests the LSI; must be grounded. |
| TEST1 | 1 | O | — | Tests the LSI; must be left unconnected. |

## Register List

| CS | RS | Index Register Bits | | | | | Register Symbol | Register Name | R/W | Data Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 4 | 3 | 2 | 1 | 0 | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | — | — | — | — | — | — | | | | | | | | | | | |
| 0 | 0 | — | — | — | — | — | IR | Index register | W | | | | IR4 | IR3 | IR2 | IR1 | IR0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | R0 | Control register 1 | W | | DISP | STBY | PWR | OSC | IDTY | CNF | ADC |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | R1 | Control register 2 | W | | | | | RMW | DDTY | INC | BLK |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | R2 | X address register | W | | | | | XA3 | XA2 | XA1 | XA0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | R3 | Y address register | W | | | YA5 | YA4 | YA3 | YA2 | YA1 | YA0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | R4 | Display memory access register | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | R5 | Display start raster register | W | | | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | R6 | Blink register 1 | W | BK0 | BK1 | BK2 | BK3 | BK4 | BK5 | BK6 | BK7 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | R7 | Blink register 2 | W | BK8 | BK9 | BK10 | BK11 | BK12 | BK13 | BK14 | BK15 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | R8 | Blink start raster register | W | | | BSL5 | BSL4 | BSL3 | BSL2 | BSL1 | BSL0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | R9 | Blink end raster register | W | | | BEL5 | BEL4 | BEL3 | BEL2 | BEL1 | BEL0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | | Reserved | | | | | | | | | |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | | Reserved | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | | Reserved | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | | Reserved | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | | Reserved | | | | | | | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | | Reserved | | | | | | | | | |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | A0 | Annunciator display data register 1 | W | IC1A | IC1B | IC1C | IC1D | IC1E | IC1F | IC1G | IC1H |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | A1 | Annunciator display data register 2 | W | IC2A | IC2B | IC2C | IC2D | IC2E | IC2F | IC2G | IC2H |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | A2 | Annunciator display data register 3 | W | IC3A | IC3B | IC3C | IC3D | IC3E | IC3F | IC3G | IC3H |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | A3 | Annunciator display data register 4 | W | IC1I | IC1J | IC1K | IC1L | IC1M | IC1N | IC1O | IC1P |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | A4 | Annunciator display data register 5 | W | IC2I | IC2J | IC2K | IC2L | IC2M | IC2N | IC2O | IC2P |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | A5 | Annunciator display data register 6 | W | IC3I | IC3J | IC3K | IC3L | IC3M | IC3N | IC3O | IC3P |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | A6 | Annunciator display data register 7 | W | IC1Q | IC1R | IC1S | IC1T | IC1U | IC1V | IC1W | IC1X |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | A7 | Annunciator display data register 8 | W | IC2Q | IC2R | IC2S | IC2T | IC2U | IC2V | IC2W | IC2X |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | A8 | Annunciator display data register 9 | W | IC3Q | IC3R | IC3S | IC3T | IC3U | IC3V | IC3W | IC3X |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | A9 | Annunciator blink register 1 | W | IP11 | IP10 | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | A10 | Annunciator blink register 2 | W | IP21 | IP20 | IB25 | IB24 | IB23 | IB22 | IB21 | IB20 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | A11 | Annunciator blink register 3 | W | IP31 | IP30 | IB35 | IB34 | IB33 | IB32 | IB31 | IB30 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | | Reserved | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | | Reserved | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | | Reserved | | | | | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | | Reserved | | | | | | | | | |

## Block Diagram



## System Description

The HD66410 comprises two kinds of independent LCD drivers: one operating with 1/33 or 1/17 duty cycle for dot-matrix displays and the other operating statically or with 1/3 duty cycle for annunciator displays. These drivers can display a maximum of 128 × 33 dots (eight 16 × 16-dot characters × 2 lines) on an LCD panel together with a 72-segment annunciator. Annunciator display is available even during standby modes, thus enabling constant display such as for a time function. The HD66410 can reduce power dissipation without affecting display because data is retained in the display RAM even during standby modes. An LCD system can be configured simply by attaching external capacitors and resistors (figure 1) since the HD66410 incorporates booster circuits.

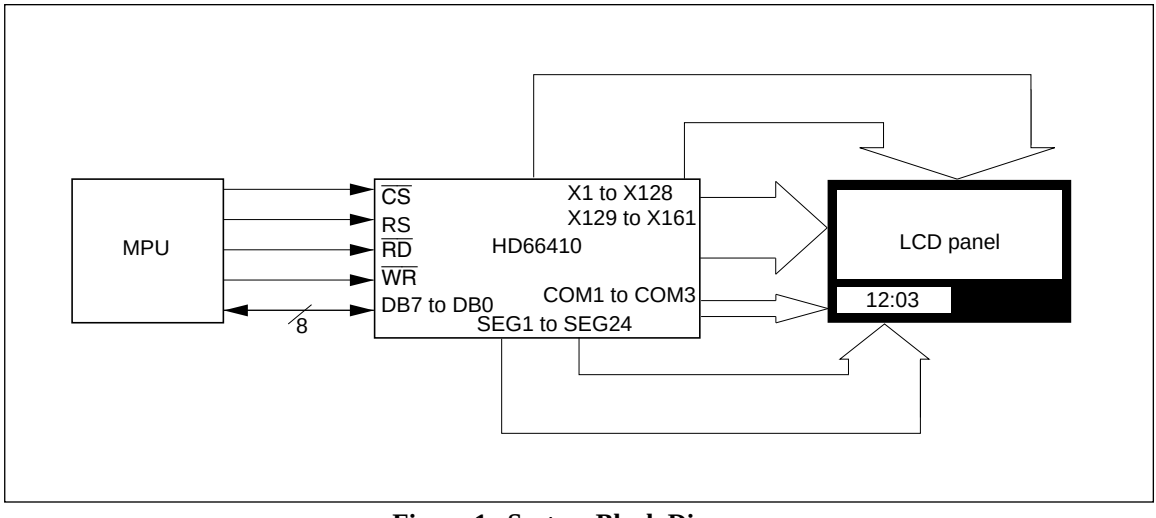



**Figure 1 System Block Diagram**

**MPU Interface**

The HD66410 can interface directly to an MPU through an 8-bit data bus or through an I/O port (figure 2). The MPU can access the HD66410 internal registers independent of internal clock timing.

The index register can be directly accessed but the other registers (data registers) cannot. Before accessing a data register, its register number must be written to the index register. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. An example of a register access sequence is shown in figure 3.

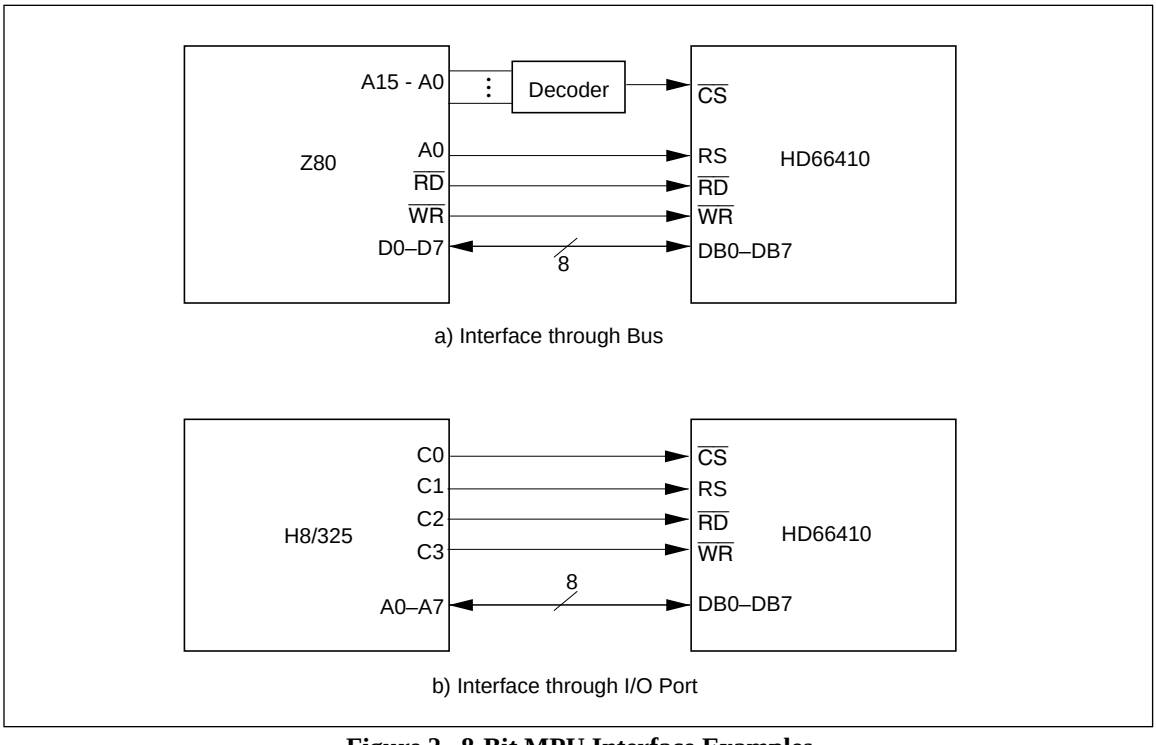



**Figure 2 8-Bit MPU Interface Examples**

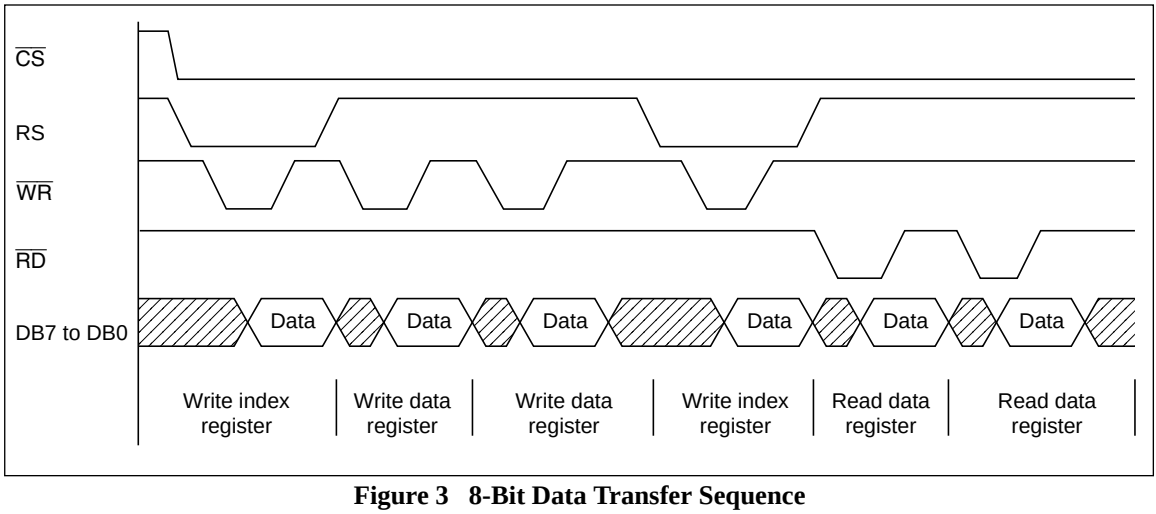



**Figure 3 8-Bit Data Transfer Sequence**

## LCD Driver Configuration

**Row/Column Output Assignment:** The HD66410 can assign LCD driver output pins X1 to X16 and X129 to X144 to either row or column output depending on the CNF bit value in control register 1, while X17 to X128 and X145 to X161 are fixed to column output and row output, respectively. With this function, row output can be positioned on either one side or two sides of an LCD panel. Figure 4 shows an example where 33-channel row output is positioned to the right of an LCD panel, with X129 to X144 assigned to row output and X1 to X16 assigned to column output. Figure 5 shows an example where 33-channel row output is divided into two and positioned to the right and left of the LCD panel, with X129 to X144 assigned to column output and X1 to X16 assigned to row output.

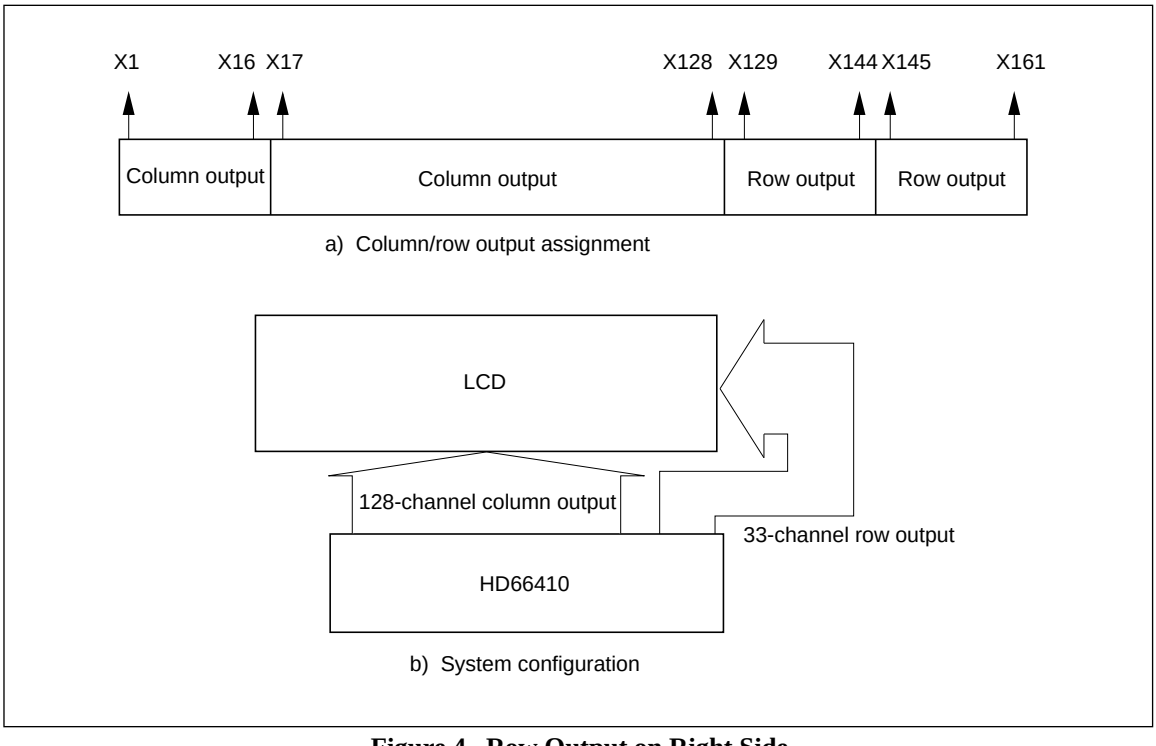
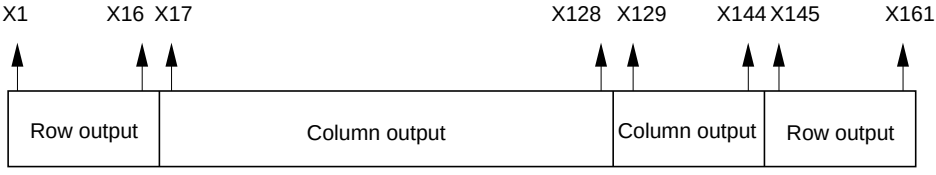
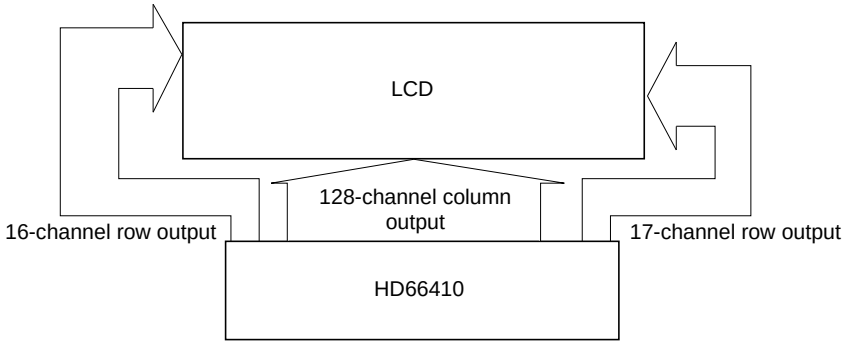



**Figure 4 Row Output on Right Side**




a) Column/row output assignment




b) System configuration

**Figure 5 Row Output on Right and Left Sides**

**Column Address Inversion According to LCD Driver Layout:** The HD66410 can always display data in address $0 on the top left of an LCD panel regardless of where it is positioned with respect to the panel. This is because the HD66410 can invert the positional relationship between display RAM addresses and LCD driver output pins by inverting RAM addresses. Specifically, the HD66410 outputs data in address $0 from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, the scan direction of row output is also inverted according to the situation, as shown in figure 6. Note that addresses and scan direction are inverted when data is written to the display RAM, and thus changing the ADC bit after data has been written has no effect. Therefore, hardware control bits such as CNF and ADC must be set immediately after reset is canceled, and must not be set while data is being displayed.

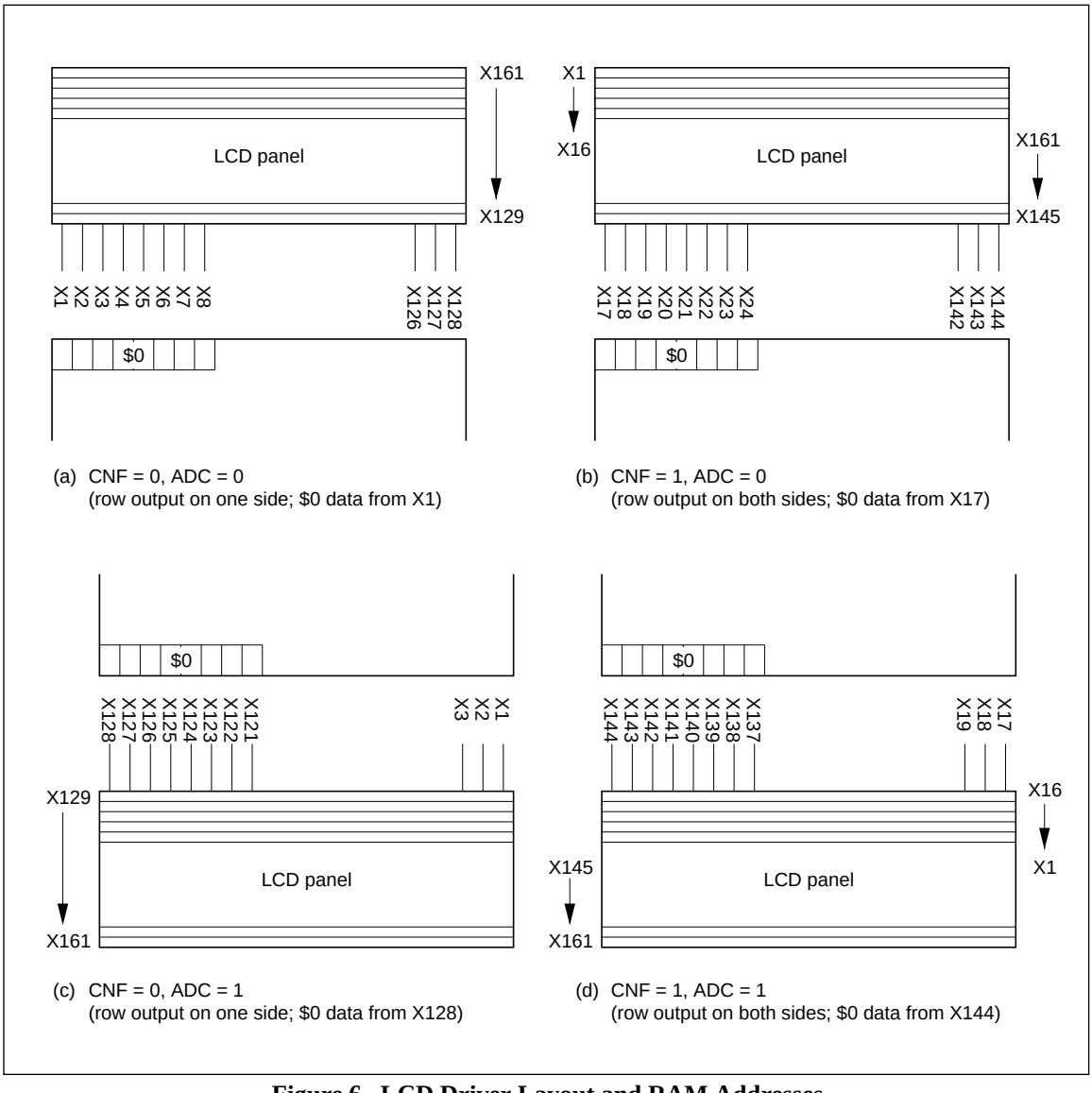



**Figure 6 LCD Driver Layout and RAM Addresses**

### Display RAM Configuration and Display

The HD66410 incorporates a bit-mapped display RAM. It has 128 bits in the X direction and 33 bits in the Y direction. The 128 bits are divided into sixteen 8-bit groups. As shown in figure 7, data written by the MPU is stored horizontally with the MSB at the far left and the LSB at the far right. A display data of 1 turns on (black) the corresponding dot of an LCD panel and 0 turns it off (transparent).

The ADC bit of control register 1 can control the positional relationship between X addresses of the RAM and LCD driver output (figure 8). Specifically, the data in address $0 is output from X1 (X17) when the ADC bit in control register 1 is 0, and from X128 (X144) otherwise. Here, data in each 8-bit group is also inverted. Because of this function, the data in X address $0 can be always displayed on the top left of an LCD panel with the MSB at the far left regardless of the LSI is positioned with respect to the panel.

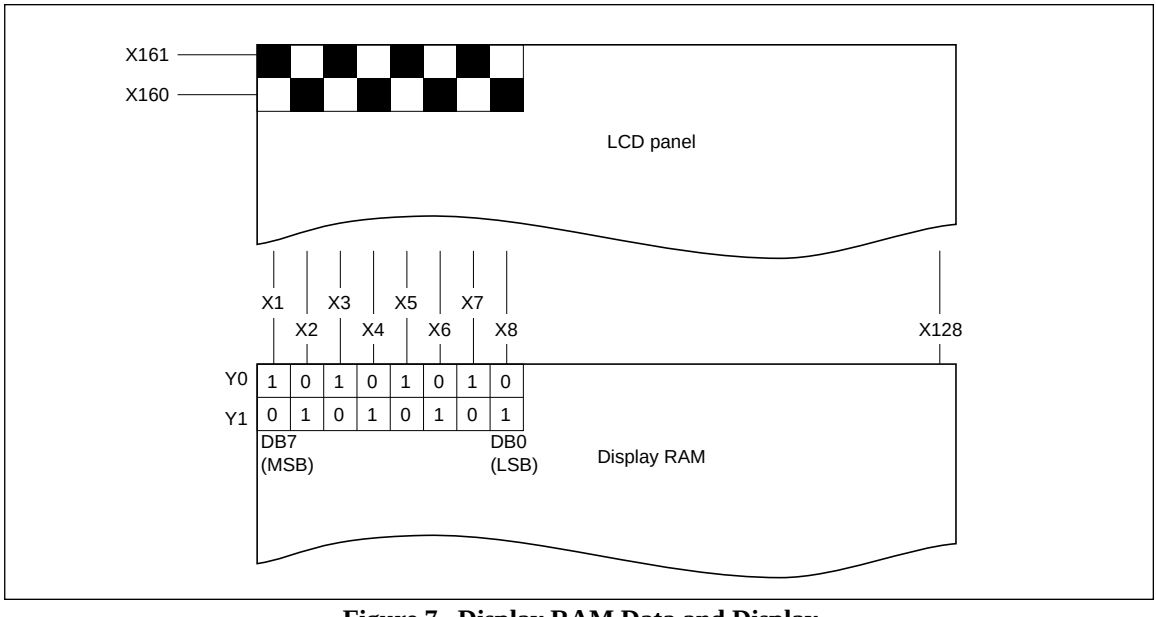



**Figure 7 Display RAM Data and Display**

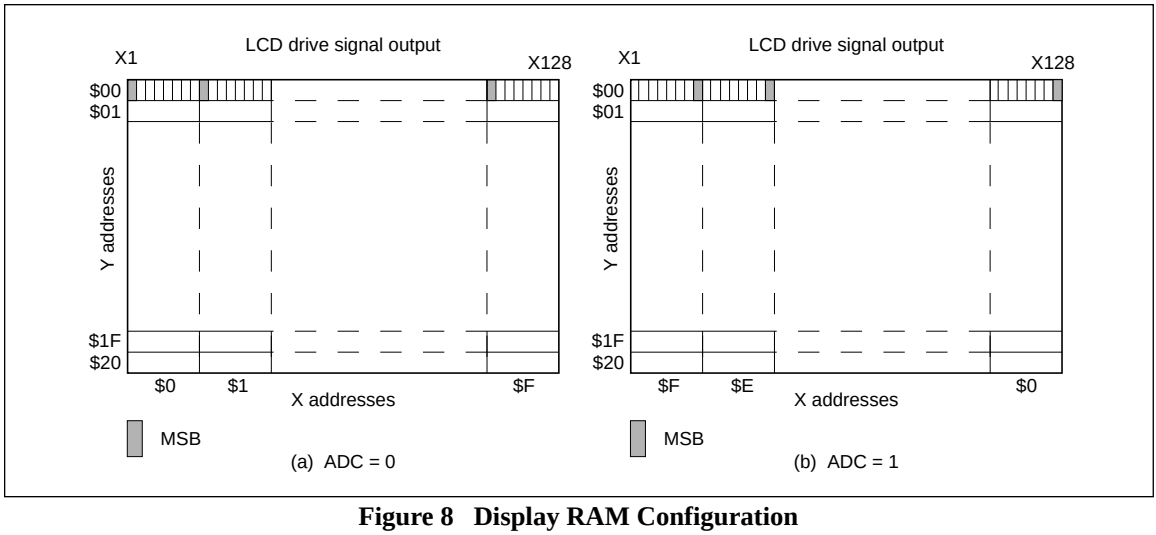



**Figure 8 Display RAM Configuration**

**Access to Internal Registers and Display RAM**

**Access to Internal Registers by the MPU:** The internal registers includes the index register and data registers. The index register can be accessed by driving both the $\overline{CS}$ and RS signals low. To access a data register, first write its register number to the index register with RS set to 0, and then access the data register with RS set to 1. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. Some data registers contain unused bits; they should be set to 0. Note that all data registers except the display memory access register can only be written to.

**Access to Display RAM by the MPU:** To access the display RAM, first write the RAM address desired to the X address register (R2) and the Y address register (R3). Then read/write the display memory access register (R4). Memory access by the MPU is independent of memory read by the HD66410 and is also asynchronous with the system clock, thus enabling an interface independent of HD66410's internal operations. However, when reading, data is temporarily latched into a HD66410's buffer and then output next time a read is performed in a subsequent cycle. This means that a dummy read is necessary after setting X and Y addresses. The memory read sequence is shown in figure 9.

X and Y addresses are automatically incremented after each memory access according to the INC bit value in control register 2; therefore, it is not necessary to update the addresses for each access. Figure 10 shows two cases of incrementing display RAM address. When the INC bit is 0, the Y address will be incremented up to $3F with the X address unchanged. However, actual memory is valid only within $00 to $20; accessing an invalid address is ignored. When the INC bit is 1, the X address will be incremented up to $F with the Y address unchanged. After address $F, the X address will return to $0; if more than 16 bytes of data are consecutively written, data will be overwritten at the same address.

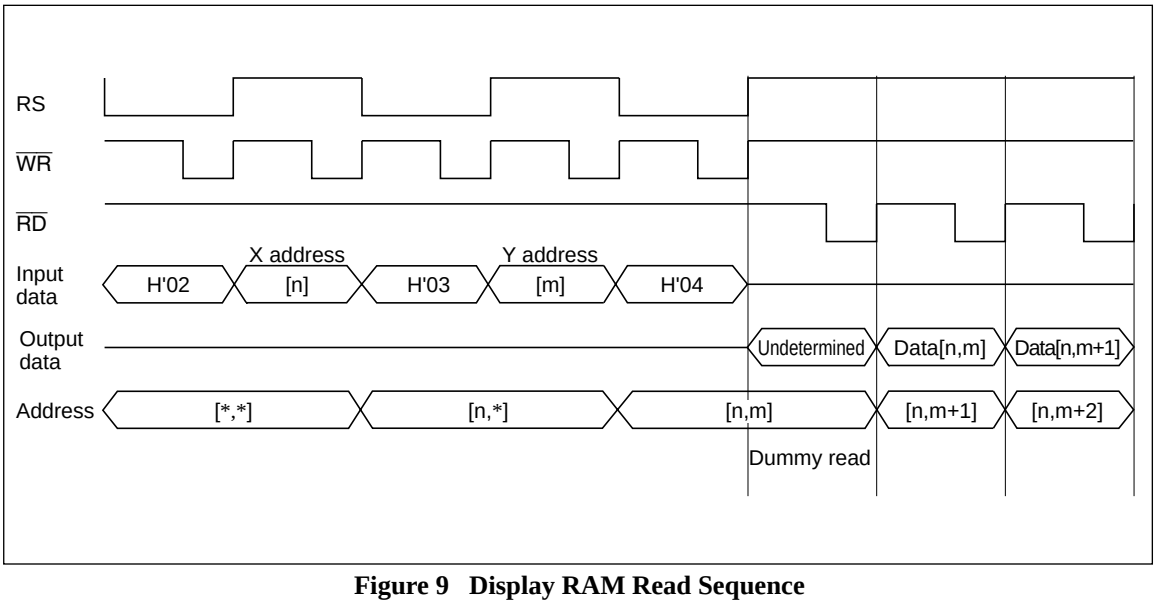



**Figure 9 Display RAM Read Sequence**

**Display RAM Reading by LCD Controller:** Data is read by the HD66410 to be displayed asynchronously with accesses by the MPU. However, because simultaneous access could damaging data in the display RAM, the HD66410 internally arbitrates access timing; access by the MPU usually has priority and so access by the HD66410 is placed between accesses by the MPU. Accordingly, an appropriate time must be secured (see the given electrical characteristics between two accesses by the MPU).

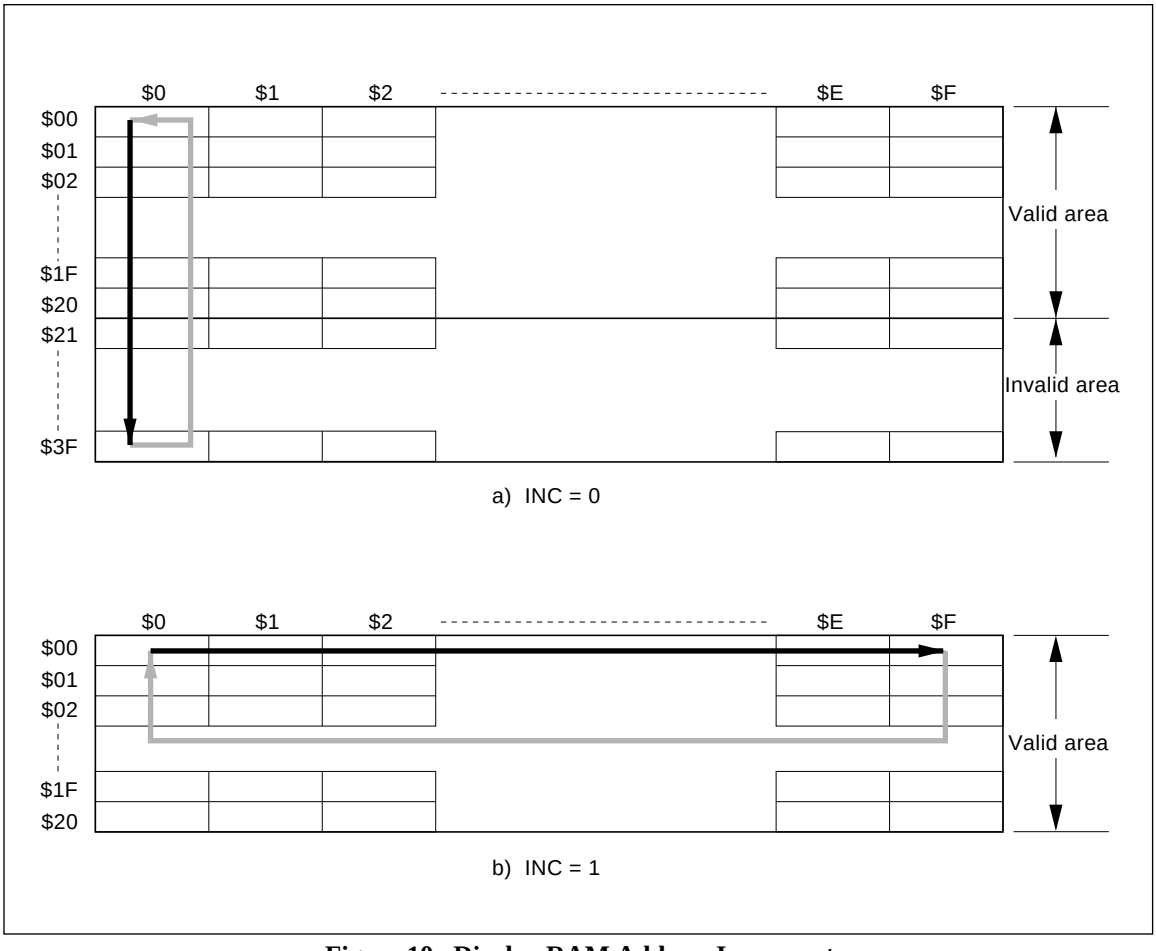



**Figure 10 Display RAM Address Increment**

### Vertical Scroll Function

The HD66410 can vertically scroll a display by varying the top raster to be displayed, which is specified by the display start raster register. Figure 11 shows a vertical scroll example. As shown, when the top raster to be displayed is set to 1, data in Y address $00 is displayed on the 33rd raster. To display another frame on the 33rd raster, therefore, data in Y address $00 must be modified after setting the top raster.

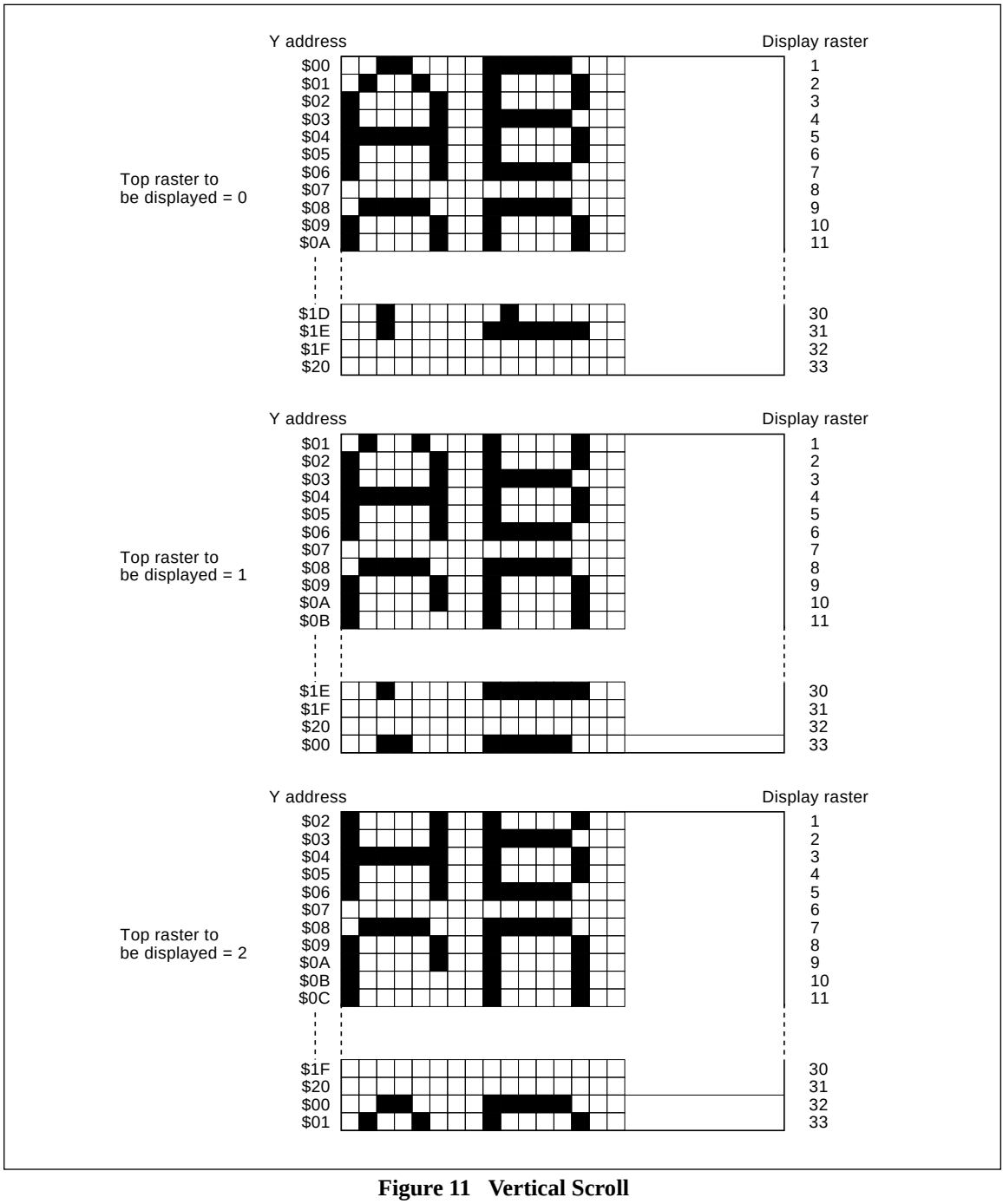



**Figure 11 Vertical Scroll**

### Blink Function

**Blinking Dot-Matrix Display Area:** The HD66410 can blink a specified area on the dot-matrix display. Blinking is achieved by repeatedly turning on and off the specified area at a frequency of one sixty-fourth the frame frequency. For example, when the frame frequency is 80 Hz, the area is turned on and off every 0.8 seconds.

The area to be blinked can be designated by specifying vertical and horizontal positions of the area. The vertical position, or the rasters to be blinked, are specified by the blink start raster register (R8) and blink end raster register (R9). The horizontal position, or the dots to be blinked in the specified rasters, are specified by the blink registers (R6 and R7) in an 8-dot group; each data bit in the blink registers controls its corresponding 8-dot group. The relationship between the registers and blink area is shown in figure 12. Setting the BLK bit to 1 in control register 2 after setting the above registers starts blinking the designated area. Note that since the area to be blinked is designated absolutely with respect to the display RAM, it will move along with a scrolling display (figure 13).

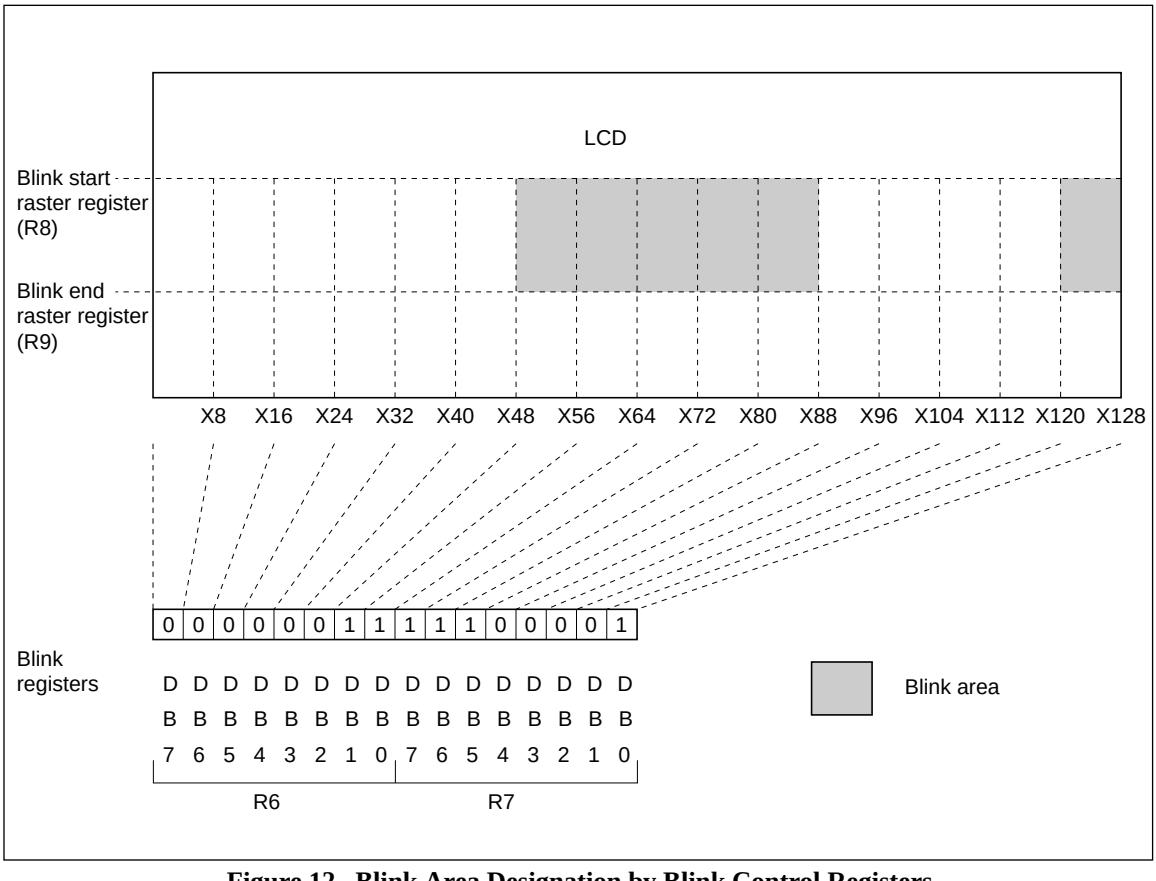
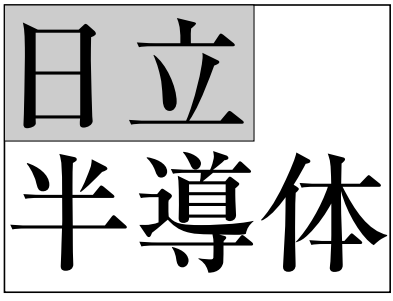
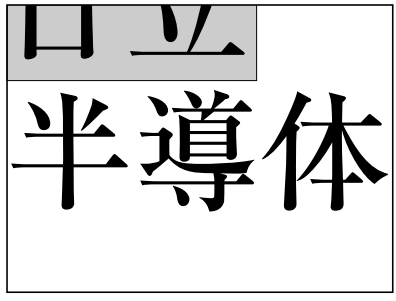



**Figure 12 Blink Area Designation by Blink Control Registers**




Display start raster = 0
Blink start raster = 0
Blink end raster = H'F




Display start raster = H'5
Blink start raster = H'5
Blink end raster = H'F

**Figure 13 Scrolling Blink Area**

**Blinking Annunciator Display Area:** The HD66410 can blink up to 18 dots among a maximum of 72 dots on the annunciator display. This function is controlled by a blink controller independent of that for the main dot-matrix display part. The dots to be blinked can be designated by annunciator blink registers 1, 2, and 3, each of which contains two bits to specify a block and six bits to specify dots to be blinked in the specified block (figures 14 and 15).

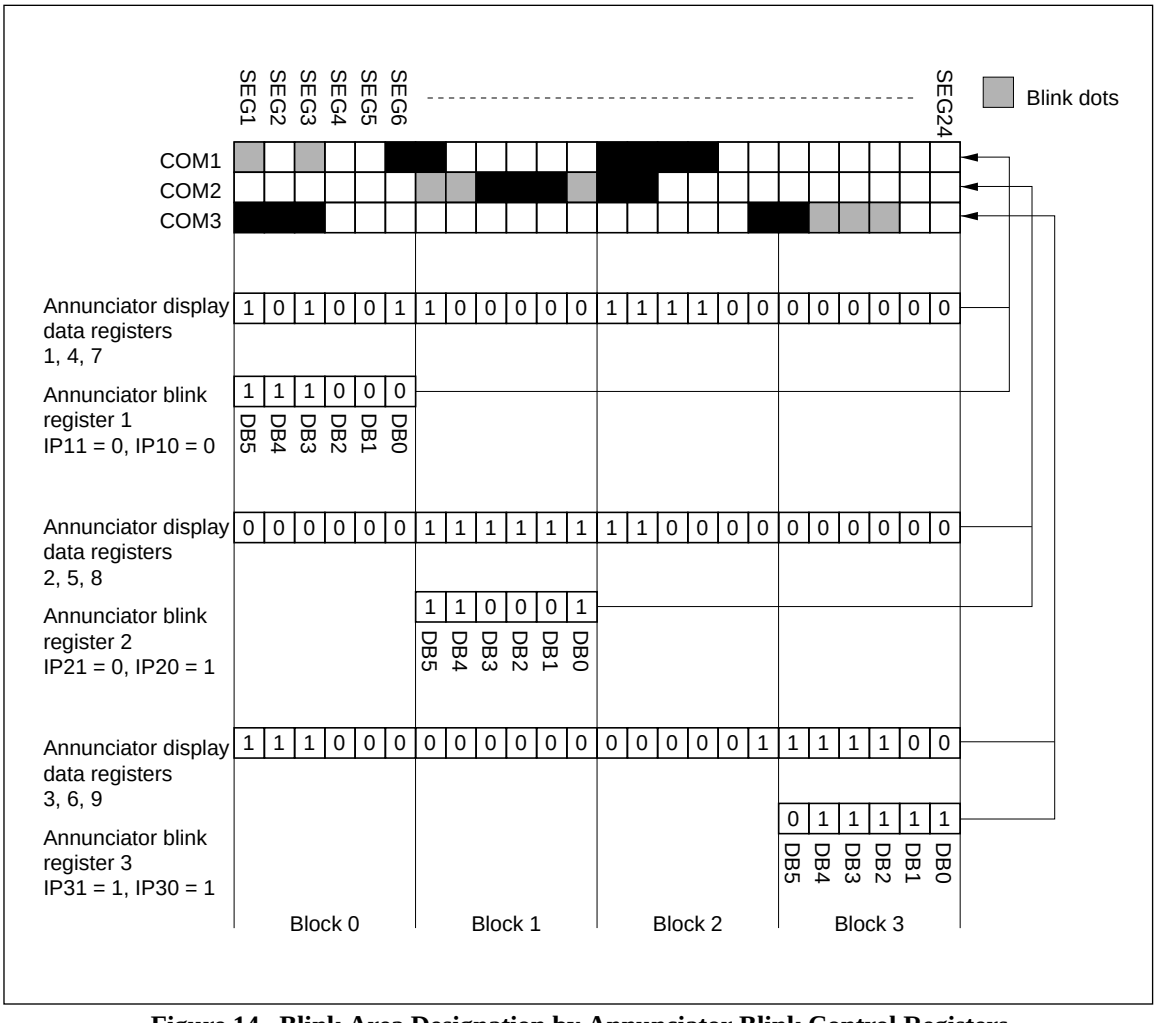
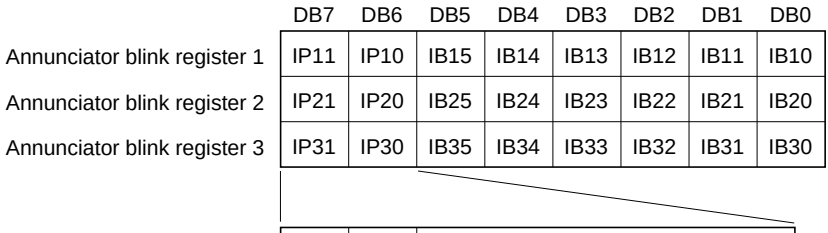



**Figure 14 Blink Area Designation by Annunciator Blink Control Registers**




| IPn1 | IPn0 | Blink Block |
|---|---|---|
| 0 | 0 | Block 0 (SEG1–SEG6) |
| 0 | 1 | Block 1 (SEG7–SEG12) |
| 1 | 0 | Block 2 (SEG13–SEG18) |
| 1 | 1 | Block 3 (SEG19–SEG24) |

IPn1, IPn0: Block select bits (n = 1, 2, 3)

**Figure 15 Annunciator Blink Registers**

**Power Down Modes**

The HD66410 has a standby function providing low power-dissipation, which is initiated by internal register settings. There are two standby modes: in one, all the HD66410 functions are inactive, and in the other, only the annunciator display function is active. In both modes, the internal booster halts but data in the display RAM and internal registers except the DISP bit is retained. However, only control registers can be accessed during standby modes. In the standby mode with annunciator display, the oscillator does not halt, thus dissipating more power than in the other standby mode. Table 1 lists the LCD driver output pin status during standby modes. Figure 16 shows the procedure for initiating and canceling a standby mode. Note that the cancelation procedure must be strictly followed to protect data in the display RAM.

**Table 1 Output Pin Status during Standby Modes**

| X1 to X161 | Output $V_{CC}$ (display off) | |
|---|---|---|
| COM1 to COM3 | OSC = 0 | Output $V_{CC}$ (display off) |
| | OSC = 1 | Output common signals (display on) |
| SEG1 to SEG24 | OSC = 0 | Output $V_{CC}$ (display off) |
| | OSC = 1 | Output segment signals (display on) |

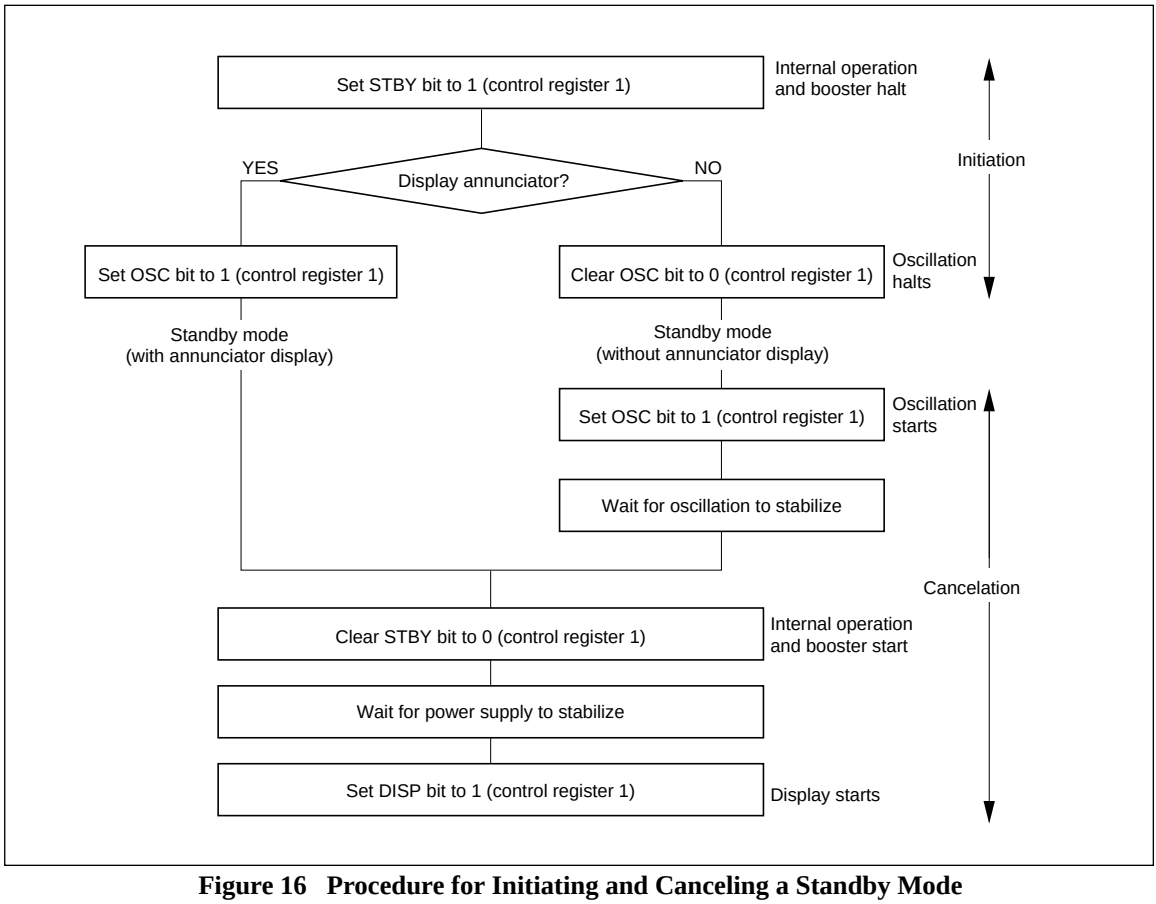



**Figure 16 Procedure for Initiating and Canceling a Standby Mode**

**Power On/Off Procedure**

Figure 17 shows the procedure for turning the power supply on and off. This procedure must be strictly followed to prevent incorrect display because the HD66410 incorporates all power supply circuits .

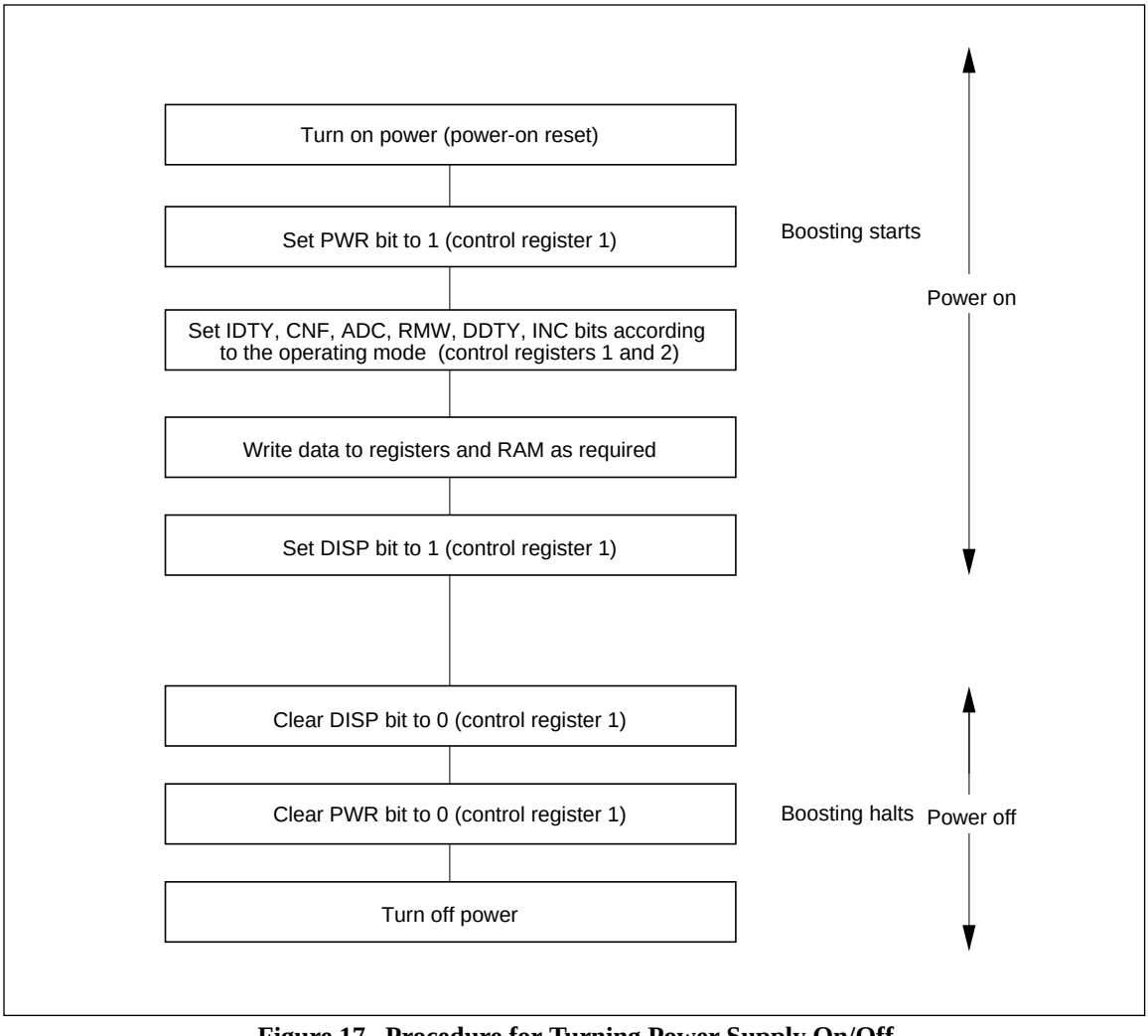



**Figure 17 Procedure for Turning Power Supply On/Off**

### Annunciator Display Function

The HD66410 can display up to 72 dots of annunciator using 24 segment (column) drivers (SEG1 to SEG24) and three common (row) drivers (COM1 to COM3). These drivers, independent of the display RAM, operate statically or with a 1/3 duty cycle. They are available even during standby modes, where dot-matrix display and the internal booster is turned off, making them suitable for time and other mark indications with reduced power dissipation.

The dots to be displayed are designated by annunciator display data registers 1 to 9. For static drive, only display data registers 1, 4, and 7 and row driver COM1 are used. A maximum of 18 turned-on dots can be blinked. For details on blinking, see the Blink Function section. Figure 18 shows the relationship between annunciator display data register bits and display positions. In the figure, alphanumerics in the ovals indicate the bit names of annunciator display data registers. Data value 1 turns on the corresponding dot on the panel, and data value 0 turns off the corresponding dot. Table 2 lists the annunciator display data registers.

**Table 2 Annunciator Display Data Register Bits**

| Register | | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| Annunciator display data register 1 | A0 | IC1A | IC1B | IC1C | IC1D | IC1E | IC1F | IC1G | IC1H |
| Annunciator display data register 2 | A1 | IC2A | IC2B | IC2C | IC2D | IC2E | IC2F | IC2G | IC2H |
| Annunciator display data register 3 | A2 | IC3A | IC3B | IC3C | IC3D | IC3E | IC3F | IC3G | IC3H |
| Annunciator display data register 4 | A3 | IC1I | IC1J | IC1K | IC1L | IC1M | IC1N | IC1O | IC1P |
| Annunciator display data register 5 | A4 | IC2I | IC2J | IC2K | IC2L | IC2M | IC2N | IC2O | IC2P |
| Annunciator display data register 6 | A5 | IC3I | IC3J | IC3K | IC3L | IC3M | IC3N | IC3O | IC3P |
| Annunciator display data register 7 | A6 | IC1Q | IC1R | IC1S | IC1T | IC1U | IC1V | IC1W | IC1X |
| Annunciator display data register 8 | A7 | IC2Q | IC2R | IC2S | IC2T | IC2U | IC2V | IC2W | IC2X |
| Annunciator display data register 9 | A8 | IC3Q | IC3R | IC3S | IC3T | IC3U | IC3V | IC3W | IC3X |

Note: Only annunciator display data registers 1, 4, and 7 are used for static display.

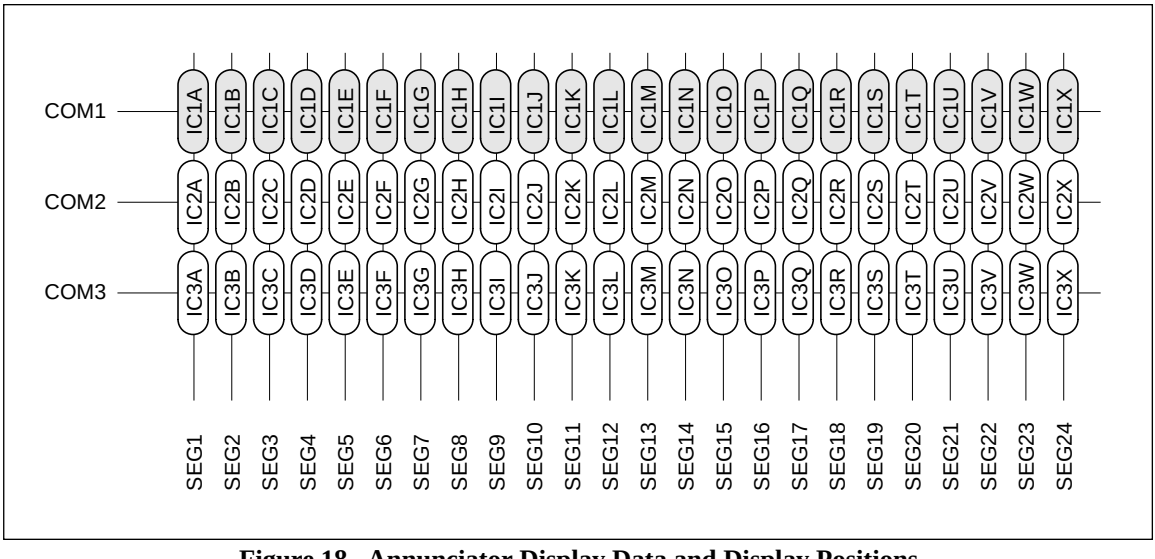



**Figure 18 Annunciator Display Data and Display Positions**

### Oscillator

The HD66410 incorporates an R-C oscillator with low power-dissipation, in which the oscillation frequency can be adjusted by appropriate selection of oscillator resistor Rf and capacitor Cf. The adjusted clock signal is used for system internal circuits; thus, if this oscillator is not used, an appropriate clock signal must be externally input through the CR pin. In this case, the C and R pins must be left unconnected. Figure 19 shows oscillator connections.

### Clock and Frame Frequency

The HD66410 generates the frame frequency (LCD drive frequency) by dividing the input clock frequency by 132. The division ratio is the same for all LCD duty cycles.

The frame frequency is usually 70 to 90 Hz; when the frame frequency is 80 Hz, for example, the input clock frequency must be 10.56 kHz.

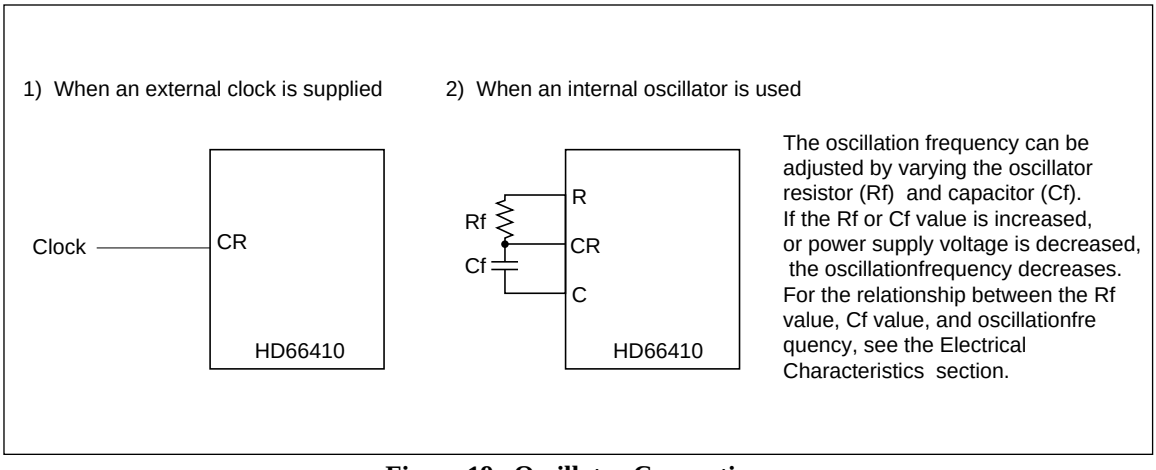
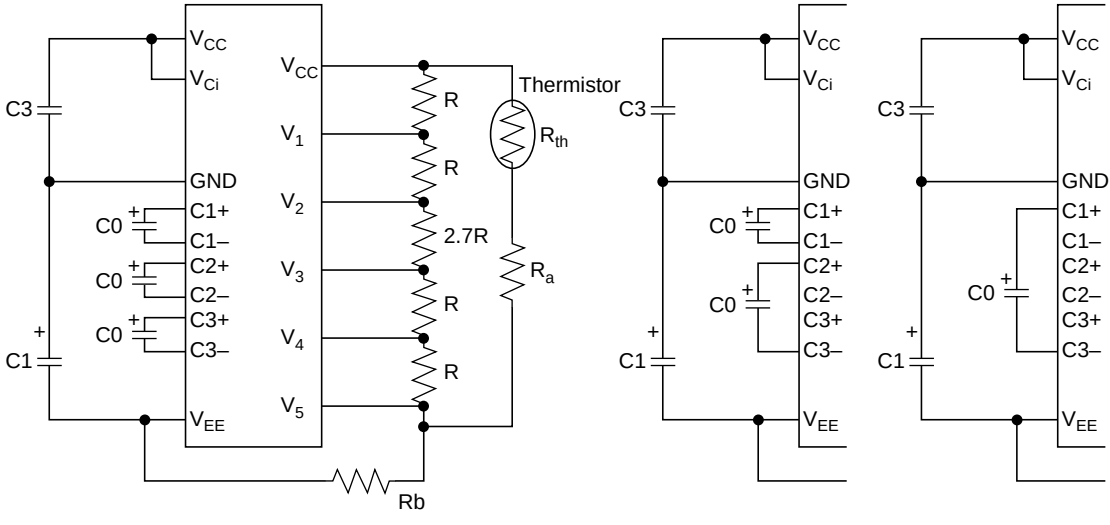



**Figure 19 Oscillator Connections**

**Power Supply Circuits**

The HD66410 incorporates a double to quadruple booster to supply power to LCD drivers. The booster is automatically turned off during standby mode, dissipating no power. If the current capacity provided is insufficient for the user system, external power supply circuits are necessary. In this case, the internal power supply can be turned off by register settings. Figure 20 shows examples of power supply circuits for different boosting ratios.

**Booster:** The internal booster raises the input voltage between $V_{CC}$ and GND two to four times every raster by turning on the internal power supply with capacitors attached between C1+ and C1-, C2+ and C2-, C3+ and C3-, and to $V_{EE}$. The booster uses the system clock, and thus the internal oscillator must be operating to activate the booster (if the internal oscillator has been selected to generate the system clock).




C0 ≥ 1.0 µF
C0 ≥ 2.2 µF

a) Quadruple boosting

C2–, C3+: open

b) Triple boosting

C1–, C2+, C2–, C3+: open

c) Double boosting

Notes: 1. Adjust the power supply voltage and capacitance of external capacitors according to the characteristics of the LCD used because the output voltage ($V_{EE}$) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to the Electrical Characteristics section for details.

2. Adjust the power supply voltage so that the output voltage ($V_{EE}$) after boosting will not exceed the absolute maximum rating of the LCD power supply voltage (13 V).

3. Vci is both a reference voltage and power supply for the booster; it needs to be supplied with at least three times the current consumed by the LCD drivers including the current flowing in the resistive divider. Make sure that Vci is below $V_{CC}$.

4. Be sure to connect polarized capacitors correctly.

**Figure 20 Power Supply Circuit Examples**

**LCD Drive Voltage Power Supply Levels:** To drive the LCD, a 6-level power supply is necessary. These levels can be usually generated by dividing the $V_{CC}$–V5 power supply using resistive dividers. If the total resistance is small, current consumption increases, and if the total resistance is large, display quality degrades. Appropriate resistance should be selected for the user system.

**Brightness Adjust:** The booster drives liquid crystals with a voltage after raising the voltage supplied to the Vci pin two to four times. Accordingly, brightness can be adjusted by varying the Vci level. Attaching a thermister is recommended to vary the voltage according to the thermal characteristics of liquid crystals.

**Row/Column Output Switchover:** LCD column drivers use $V_{CC}$, V2, V3, and V5, while row drivers use $V_{CC}$, V1, V4, and V5. These voltage levels are switched to AC and are output to an LCD panel. Since the HD66410 can assign X1 to X16 and X129 to X144 to either row or column output, the power supply connection must be externally changed according to the assignment, which is determined by the CNF bit value in control register 1. The select and deselect levels for row output are temporarily output from the $V_{CHO}$ and $V_{CLO}$ pins, and the two levels for column output are output from the $V_{SHO}$ and $V_{SLO}$ pins; these outputs must be connected according to row and column output assignment as shown in figure 21.

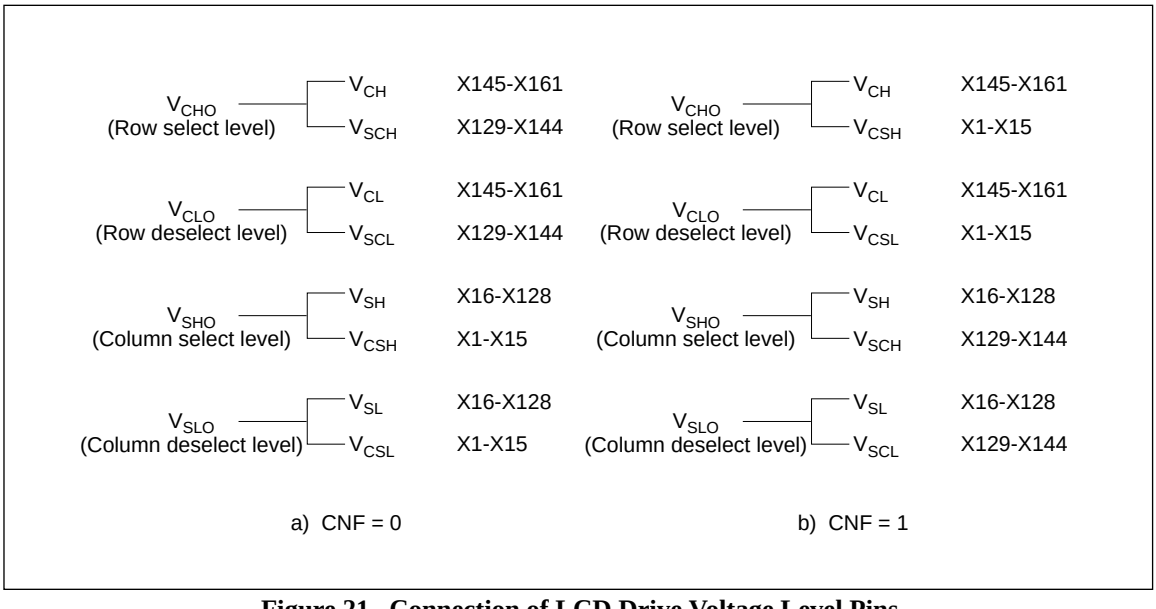



**Figure 21 Connection of LCD Drive Voltage Level Pins**

**Reset**

The low $\overline{\text{RESET}}$ signal initializes the HD66410, clearing all the bits in the internal registers. During reset, the internal registers cannot be accessed.

Note that if the reset conditions specified in the Electric Characteristics section are not satisfied, the HD66410 will not be correctly initialized. In this case, the internal registers of the HD66410 must be initialized by software.

**Initial Setting of Internal Registers:** All the internal register bits are cleared to 0. Details are listed below.

- Data registers (DR: R0 to R9, A0 to A11)
  - — Normal operation
  - — Oscillator is active
  - — Display is off (including annunciator display)
  - — Booster is not used
  - — Y address of display RAM is incremented
  - — 1/33 duty cycle
  - — X and Y addresses are 0
  - — Data in address $0 is output from the X1 pin
  - — Blink function is inactive

**Initial Setting of Pins:**

- Bus interface pins
  During reset, the bus interface pins do not accept signals to access internal registers; data is undefined when read.

- LCD driver output pins
  During reset, all the LCD driver output pins (X1 to X161, SEG1 to SEG33, COM1 to COM3) output $V_{CC}$-level voltage, regardless of data value in the display RAM, turning off the LCD. Here, the output voltage is not alternated. Note that the same voltage ($V_{CC}$) is applied to both column and row output pins to prevent liquid crystals from degrading.

- Booster output pins
  Since the PWR bit in control register 1 is 0 during reset, the booster halts. Accordingly, the output state of the $V_{EE}$ pin depends on the value of the booster's external capacitor.

## Internal Registers

The HD66410 has one index register and 22 data registers, all of which can be accessed asynchronously with the internal clock. All the registers except the display memory access register are write-only. Accessing unused bits or addresses affects nothing; unused bits should be set to 0 when written to.

**Index Register (IR):** The index register (figure 22) selects one of 22 data registers. The index register itself is selected when both the $\overline{CS}$ and RS signals are low. Data bits 7 to 5 are unused; they should be set to 0 when written to.

**Control Register 1 (R0):** Control register 1 (figure 23) controls general operations of the HD66410. Each bit has its own function as described below. Data bit 7 bit is unused; it should be set to 0 when written to.

- DSP bit
  DSP = 1: Display on
  DSP = 0: Display off (all LCD driver output pins output $V_{CC}$ level)

- STBY bit
  STBY = 1: Internal operation and booster halt; display off
  STBY = 0: Normal operation
  The STBY bit does not affect the state of PWR and DISP bit.

- PWR bit
  PWR = 1: Booster active
  PWR = 0: Booster inactive

- OSC bit
  OSC = 1: Internal operation and booster halt; oscillator does not halt to provide annunciator display
  OSC = 0: Internal operation, booster, and oscillator halt
  The OSC bit is valid only when the STBY bit is 1.

- IDTY bit
  IDTY = 1: Annunciator display signals are operating statically
  IDTY = 0: Annunciator display signals are operating with 1/3 duty cycle

- CNF bit
  CNF = 1: Row output on both sides of the LCD panel
  CNF = 0: Row output on one side of the LCD panel

- ADC bit
  ADC = 1: Data in X address $0 is output from X128 or X144; row signals are scanned from X129 to X161.
  ADC = 0: Data in X address $0 is output from X1 or X17; row signals are scanned from X161 to X129.

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| IR | Set value | | | | Register number | | | | |

**Figure 22 Index Register (IR)**

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R0 | Set value | | DISP | STBY | PWR | OSC | IDTY | CNF | ADC |

**Figure 23 Control Register 1 (R0)**

**Control Register 2 (R1):** Control register 2 (figure 24) controls general operations of the HD66410. Each bit has its own function as described below. Data bits 7 to 4 are unused; they should be set to 0 when written to.

- RMW bit
  RMW = 1: Read-modify-write mode
  Address is incremented only after write access
  RMW = 0: Address is incremented after both write and read accesses

- DDTY bit
  DDTY = 1: 1/17 display duty cycle
  DDTY = 0: 1/33 display duty cycle

- INC bit
  INC = 1: X address is incremented for each access
  INC = 0: Y address is incremented for each access

- BLK bit
  BLK = 1: Blink function is used
  BLK = 0: Blink function is not used
  The blink counter is reset when the BLK bit is set to 0. It starts counting and at the same time initiates blinking when the BLK bit is set to 1.

**X Address Register (R2):** The X address register (figure 25) designates the X address of the display RAM to be accessed by the MPU. The set value must range from $0 to $F; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bits 7 to 3 are unused; they should be set to 0 when written to.

**Y Address Register (R3):** The Y address register (figure 26) designates the Y address of the display RAM to be accessed by the MPU. The set value must range from $00 to $20; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bit 7 is unused; it should be set to 0 when written to.

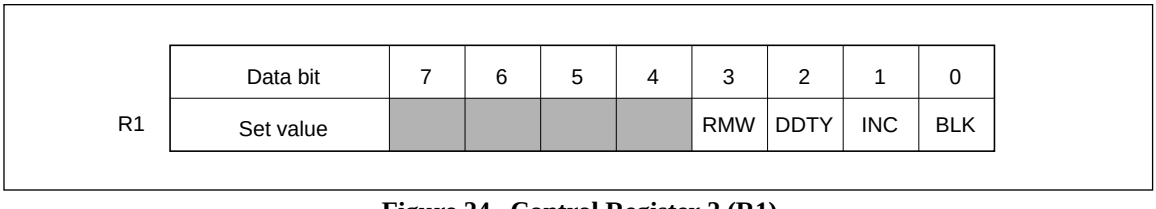



**Figure 24 Control Register 2 (R1)**

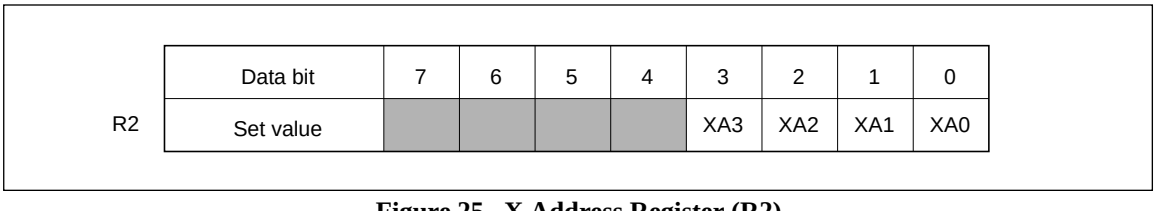



**Figure 25 X Address Register (R2)**

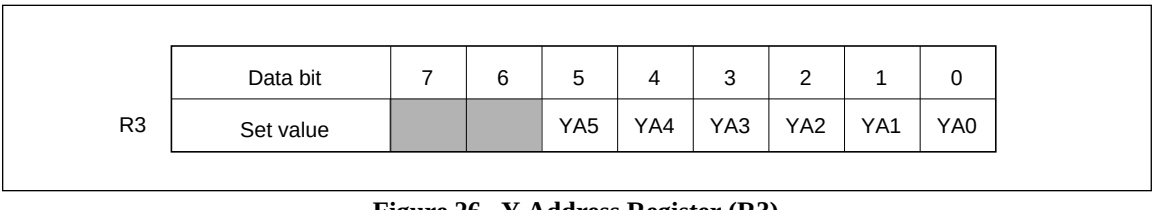



**Figure 26 Y Address Register (R3)**

**Display Memory Access Register (R4):** The display memory access register (figure 27) is used to access the display RAM. If this register is write-accessed, data is directly written to the display RAM. If this register is read-accessed, data is first latched to this register from the display RAM and sent out to the data bus on the next read; therefore, a dummy read access is necessary after setting the display RAM address.

**Display Start Raster Register (R5):** The display start raster register (figure 28) designates the raster to be displayed at the top of the LCD panel. Varying the set value scrolls the display vertically. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, data may not be displayed correctly. Data bits 7 and 6 are unused; they should be set to 0 when written to.

**Blink Registers (R6, R7):** The blink bit registers (figure 29) designate the 8-bit groups to be blinked. Setting a bit to 1 blinks the corresponding 8-bit group. Any number of groups can be blinked; setting all the bits to 1 will blink the entire LCD panel. These bits are valid only when the BLK bit of control register 2 is 1.

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R4 | Set value | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Figure 27 Display Memory Access Register (R4)**

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R5 | Set value | | | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 |

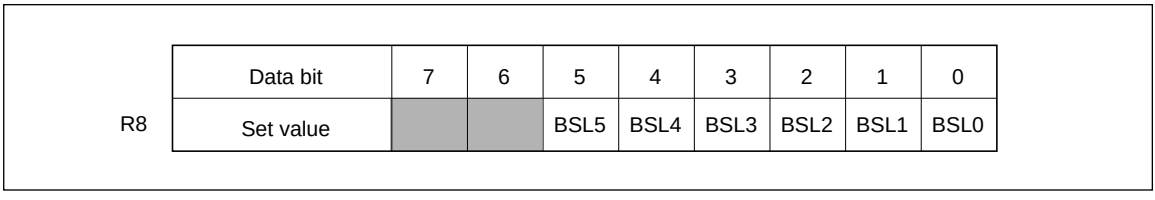
**Figure 28 Display Start Raster Register (R5)**

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R6 | Set value | BK0 | BK1 | BK2 | BK3 | BK4 | BK5 | BK6 | BK7 |
| R7 | Set value | BK8 | BK9 | BK10 | BK11 | BK12 | BK13 | BK14 | BK15 |

**Figure 29 Blink Registers (R6, R7)**

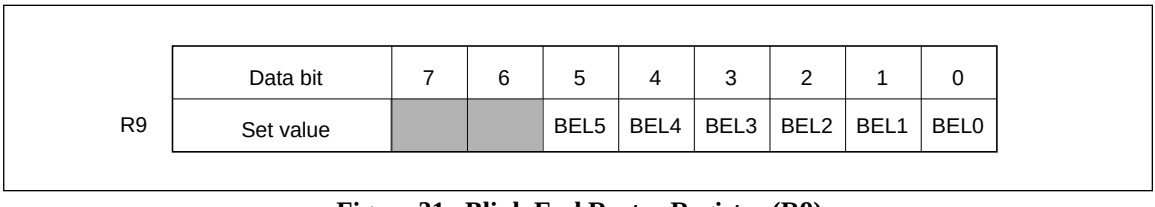
**Blink Start Raster Register (R8):** The blink start raster register (figure 30) designates the top raster in the area to be blinked. The set value must be one less than the actual top raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. If the value is set outside these ranges, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.

**Blink End Raster Register (R9):** The blink end raster register (figure 31) designates the bottom raster in the area to be blinked. The area to be blinked is designated by the blink registers, blink start raster register, and blink end raster register. The set value must be one less than the actual bottom raster and range from 0 to 32 for 1/33 duty cycle and from 0 to 16 for 1/17 duty cycle. It must also be greater than the value set in the blink start raster register. If an inappropriate value is set, operations may not be correct. Data bits 7 and 6 are unused; they should be set to 0 when written to.



| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R8 | Set value | | | BSL5 | BSL4 | BSL3 | BSL2 | BSL1 | BSL0 |

**Figure 30 Blink Start Raster Register (R8)**



| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| R9 | Set value | | | BEL5 | BEL4 | BEL3 | BEL2 | BEL1 | BEL0 |

**Figure 31 Blink End Raster Register (R9)**

**Annunciator Display Data Registers (A0 to A8):** The annunciator display data registers (figure 32) store data for annunciator (icon) display. Setting a data bit to 1 turns on the corresponding dot on the LCD panel.

**Annunciator Blink Registers (A9 to A11):** The annunciator blink registers (figure 33) designate bits to be blinked on the annunciator display. For details, see the Blink Function section.

- IPn1, IPn0 bits (n = 1, 2, 3)
  These bits select annunciator blocks to be blinked.
  IPn1, IPn0 = 0, 0: Block 0 is selected (SEG1 to SEG6)
  IPn1, IPn0 = 0, 1: Block 1 is selected (SEG7 to SEG12)
  IPn1, IPn0 = 1, 0: Block 2 is selected (SEG13 to SEG18)
  IPn1, IPn0 = 1, 1: Block 3 is selected (SEG19 to SEG24)
- IBn5, IBn0 bits (n = 1, 2, 3)
  These bits select bits to be blinked in the selected blocks.

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| A0 | Set value | IC1A | IC1B | IC1C | IC1D | IC1E | IC1F | IC1G | IC1H |
| A1 | Set value | IC2A | IC2B | IC2C | IC2D | IC2E | IC2F | IC2G | IC2H |
| A2 | Set value | IC3A | IC3B | IC3C | IC3D | IC3E | IC3F | IC3G | IC3H |
| A3 | Set value | IC1I | IC1J | IC1K | IC1L | IC1M | IC1N | IC1O | IC1P |
| A4 | Set value | IC2I | IC2J | IC2K | IC2L | IC2M | C2N | IC2O | IC2P |
| A5 | Set value | IC3I | IC3J | IC3K | IC3L | IC3M | C3N | IC3O | IC3P |
| A6 | Set value | IC1Q | IC1R | IIC1S | IC1T | IC1U | IIC1V | IIC1W | IC1X |
| A7 | Set value | IC2Q | IC2R | IC2S | IC2T | IC2U | IC2V | IC2W | IC2X |
| A8 | Set value | IC3Q | IC3R | IC3S | IC3T | IC3U | IC3V | IC3W | IC3X |

**Figure 32 Annunciator Display Data Registers (A0 to A8)**

| | Data bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| A9 | Set value | IP11 | IP10 | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 |
| A10 | Set value | IP21 | IP20 | IB25 | IB24 | IB23 | IB22 | IB21 | IB20 |
| A11 | Set value | IP31 | IP30 | IB35 | IB34 | IB33 | IB32 | IB31 | IB30 |

**Figure 33 Annunciator Blink Registers (A9 to A11)**

## Absolute Maximum Ratings

| Item | | Symbol | Ratings | Unit | Notes |
|---|---|---|---|---|---|
| Power supply voltage | Logic circuit | $V_{CC}$ | –0.3 to +7.0 | V | 1 |
| | LCD drive circuits | $V_{EE}$ | $V_{CC}$ – 18.0 to $V_{CC}$ + 0.3 | V | |
| Input voltage 1 | | $V_{T1}$ | –0.3 to VCC + 0.3 | V | 1, 2 |
| Input voltage 2 | | $V_{T2}$ | $V_{EE}$ – 0.3 to $V_{CC}$ + 0.3 | V | 1, 3 |
| Operating temperature | | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | | $T_{stg}$ | –40 to +125 | °C | |

Notes: 1. Measured relative to GND.

2. Applies to pins CR, DB7 to DB0, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, RS, $\overline{RES}$, TEST0, AV3.
3. Applies to pins V1, V2, V3, V4, V5, C1+, C1–, C2+, C2–, C3+, C3–, $V_{SH}$, $V_{SL}$, $V_{CH}$, $V_{CL}$, $V_{SCH}$, $V_{SCL}$, $V_{CSH}$, $V_{CSL}$.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics to prevent malfunction or unreliability.

## Electrical Characteristics

**Table 3 DC Characteristics ($V_{CC}$ = 2.2 to 3.6 V, GND = 0 V, $V_{CC}$–V5 = 6 to 15 V, Ta = –20 to +75°C)**

| Item | Symbol | Applicable Pins | Min | Typ | Max | Unit | Measurement Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input leakage current (1) | $I_{IL1}$ | Except for DB0 to DB7 | –1.0 | — | 1.0 | µA | $V_{IN} = V_{CC}$ to GND | |
| Input leakage current (2) | $I_{IL1}$ | DB7 to DB0 | –2.5 | — | 2.5 | µA | $V_{IN} = V_{CC}$ to GND | |
| Driver “on” resistance (1) | $R_{COM}$ | X1 to X16, X129 to X161 | — | — | 20 | kΩ | $I_{ON}$ = 100 µA<br>$V_{CC}$ – V5 = 8 V | |
| Driver “on” resistance (2) | $R_{SEG}$ | X17 to X128 | — | — | 30 | kΩ | $I_{ON}$ = 100 µA<br>$V_{CC}$ – V5 = 8 V | |
| Driver “on” resistance (3) | $R_{ICON}$ | $COM_1$ to $COM_3$, $SEG_1$ to $SEG_{24}$ | — | — | 50 | kΩ | $I_{ON}$ = 100 µA | |
| Input high voltage | $V_{IH1}$ | | $0.7 \times V_{CC}$ | — | $V_{CC}$ | V | | |
| Input low voltage | $V_{IL1}$ | | 0 | — | $0.3 \times V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | | $0.8 \times V_{CC}$ | — | — | V | $I_{OH}$ = –50 µA | |
| Output low voltage | $V_{OL}$ | | — | — | $0.2 \times V_{CC}$ | V | $I_{OL}$ = 50 µA | |
| Current consumption during display | $I_{DISP}$ | | | | T.B.D. | µA | | 1 |
| Current consumption during standby (1) | $I_{STB1}$ | | | | T.B.D. | µA | Annunciator displayed | 2 |
| Current consumption during standby (2) | $I_{STB2}$ | | | | T.B.D. | µA | Annunciator not displayed | 3 |
| Current consumption during RAM access | $I_{CC}$ | | | | T.B.D. | µA | | |

Notes: 1. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply to the input circuit. To avoid this, $V_{IH}$ and $V_{IL}$ must be held to $V_{CC}$ and GND levels, respectively.

2. Measured when STBY bit = 1 and OSC (ICON) bit = 1

3. Measured when STBY bit = 1 and OSC (ICON) bit = 0

**Table 4 Booster Characteristics**

| Item | Symbol | Min | Typ | Max | Unit | Measurement Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Output voltage | $V_{FF}$ | 10.0 | 11.0 | — | V | | 1 |
| Input voltage | $V_{ci}$ | — | — | 3.6 | V | | 2 |

Notes: 1. Measured when $V_{CC}$ = 3.0 V, Io (load current) = 0.25 mA, C = 1 µF, $f_{OSC}$ (oscillation frequency) = 10 kHz, and the input voltage is boosted four times.
2. Input voltage must be below $V_{CC}$.

## AC Characteristics

**Table 5 Clock Characteristics ($V_{CC}$ = 2.2 to 3.6 V, GND = 0 V, Ta = –20 to +75°C)**

| Item | Symbol | Min | Typ | Max | Unit | Measurement Conditions | Notes |
|---|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{OSC}$ | 7 | 10 | 13 | kHz | C = 100 pF, R = 470 kΩ | |
| External clock frequency | $f_{CP}$ | 5 | 10 | 20 | kHz | | |
| External clock duty cycle | Duty | 45 | 50 | 55 | % | | |
| External clock rise time | $t_r$ | — | — | 0.2 | µS | | |
| External clock fall time | $t_f$ | — | — | 0.2 | µS | | |

**Table 6 MPU Interface ($V_{CC}$ = 2.2 to 3.6 V, GND = 0 V, Ta = –20 to +75°C)**

| Item | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{RD}$ low-level width | $t_{WRDL}$ | 450 | — | ns | |
| $\overline{RD}$ high-level width | $t_{WRDH}$ | 450 | — | ns | |
| $\overline{WR}$ low-level width | $t_{WWRL}$ | 450 | — | ns | |
| $\overline{WR}$ high-level width | $t_{WWRH}$ | 450 | — | ns | |
| Address setup time | $t_{AS}$ | 0 | — | ns | |
| Address hold time | $t_{AH}$ | 0 | — | ns | |
| Data delay time | $t_{DDR}$ | — | 300 | ns | |
| Data output hold time | $t_{DHR}$ | 10 | — | ns | |
| Data setup time | $t_{DSW}$ | 100 | — | ns | |
| Data hold time | $t_{DHW}$ | 0 | — | ns | |

**Table 7 Reset Timing**

| Item | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{RES}$ low-level width | $t_{RES}$ | 1 | — | ms | |

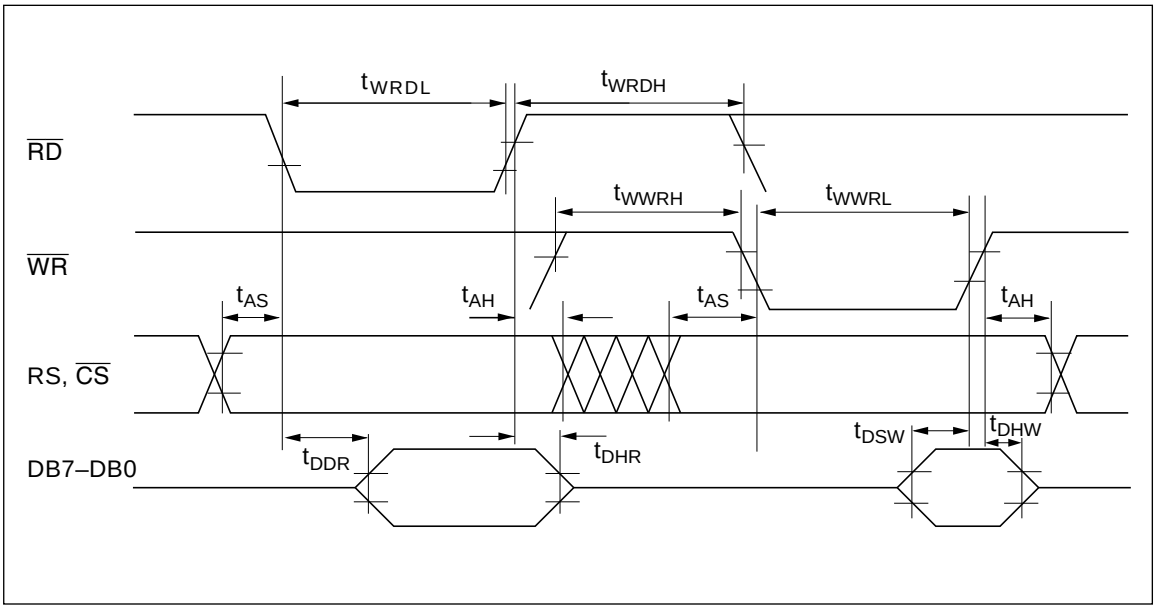



**Figure 34 MPU Interface**