HD66503

(240-Channel Common Driver with Internal LCD Timing Circuit)

HITACHI

Description

The HD66503 is a common driver for liquid crystal dot-matrix graphic display systems. This device incorporates a 240 liquid crystal driver and an oscillator, and generates timing signals (alternating signals and frame synchronizing signals) required for the liquid crystal display. It also achieves low current consumption of 100 µA through the CMOS process. Combined with the HD66520, a 160-channel column driver with an internal RAM, the HD66503 is optimal for use in displays for portable information tools.

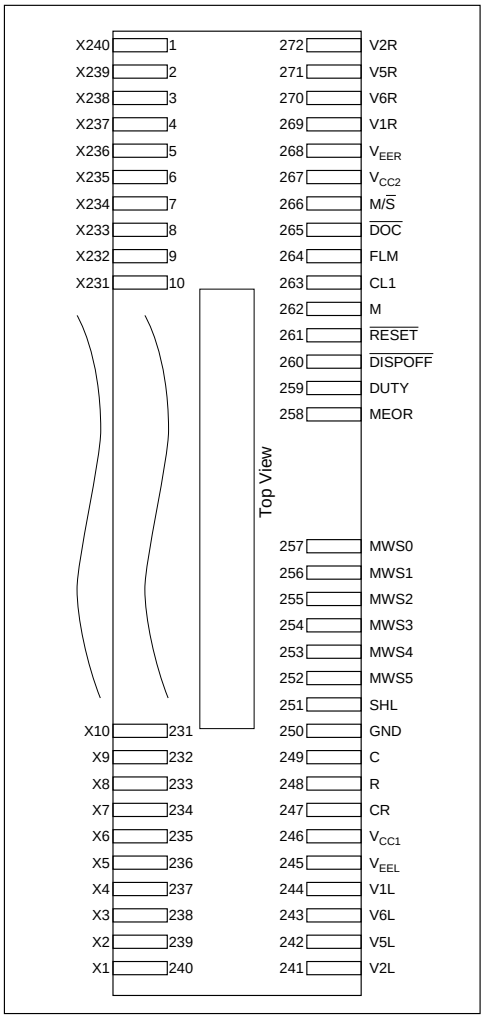
Features

- LCD timing generator: 1/120, 1/240 duty cycle internal generator
- Alternating signal waveform generator: Pin programmable 2 to 63 line inversion
- Recommended display duty cycle: 1/120, 1/240 (master mode): 1/120 to 1/240 (slave mode)
- Number of LCD driver: 240
- Power supply voltage: 2.7 to 5.5V
- High voltage: 8 to 28-V LCD drive voltage
- Low power consumption: 100 µA (during display)
- Internal display off function
- Oscillator circuit with standby function: 130 kHz (max)
- Display timing operation clock: 65 kHz (max) (operating at 1/2 system clock)
- Package: 272-pin TCP
- CMOS process

Ordering Information

Type No.	TCP	Outer Lead Pitch (µm)
HD66503TA0	Straight TCP	200
HD66503TB0	Folding TCP	200

Pin Arrangement



Note : This figure does not specify the tape carrier package dimensions.

Pin Description

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Power supply	V_{CC1}, V_{CC2}	246 267	V_{CC}	Power supply	2	V_{CC}–GND: logic power supply
	GND	250	GND	Power supply	1	
	V_{EEL}, V_{EER}	245 268	V_{EE}	Power supply	2	V_{CC}–V_{EE}: LCD drive circuits power supply
	V1L, R	244 269	V1	Input	2	LCD drive level power supply See Figure 1.
	V2L, R	241 272	V2	Input	2	
	V5L, R	242 271	V5	Input	2	
	V6L, R	243 270	V6	Input	2	
Control signals	M/$\overline{S}$	266	Master/slave	Input	1	Controls the initiation and termination of the LCD timing generator. In addition, the input/output is determined of 4 signal pins: display data transfer clock (CL1); first line marker (FLM); alternating signal (M); and display off control ($\overline{DOC}$). See Table 1 for details.
	DUTY	259	Duty	Input	1	Selects the display duty cycle. Low level: 1/120 display duty ratio High level: 1/240 display duty ratio
	MWS0 to MWS5	257 256 255 254 253 252	MWS0 MWS1 MWS2 MWS3 MWS4 MWS5	Input	6	The number of line in the line alternating waveform is set during master mode. The number of lines can be set between 10 and 63. When using the external alternating signal or during slave mode, set the number of lines to 0. See Table 2.
	MEOR	258	M Exclusive-OR	Input	1	During master mode, the signals alternating waveform output from pin M is selected. During low level, the line alternating waveform is output from pin M. During high level, pin M outputs an EOR (exclusive OR) waveform between a line alternating waveform and frame alternating waveform. Set the pin to low during slave mode. See Table 3.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
Control signals	CR, R, C	247 248 249	CR R C		3	These pins are used as shown in Figure 4 in master mode, and as shown in Figure 5 in slave mode.
	$\overline{\text{RESET}}$	261	Reset	Input	1	The following initiation will be proceeded by setting to initiation. 1) Stops the internal oscillator or the external oscillator clock input. 2) Initializes the counters of the liquid crystal display timing generator and alternating signal (M) generator. 3) Set display off control output ($\overline{\text{DOC}}$) to low and turns off display. After reset, display off control output ($\overline{\text{DOC}}$) will stay low for four more frame cycles (four clocks of FLM signals) to prevent error display at initiation. The electrical characteristics are shown in Table 4. See Figure 2. However, when reset is performed during operation, RAM data in the HD66520 which is used together with the HD66503 may be destroyed. Therefore, write data to the RAM again.
LCD timing	CL1	263	Clock 1	I/O	1	The bidirectional shift register shifts data at the falling edge of CL1. During master mode, this pin-outputs a data transfer clock with a two times larger cycle than the internal oscillator (or the cycle of the external clock) with a duty of 50%. During slave mode, this pin inputs the external data transfer clock.
	FLM	264	First line marker	I/O	1	During master mode, pin FLM outputs the first line marker. During slave mode, this pin inputs the external data first line marker. The shift direction of the first line marker is determined by DUTY and SHL signal as follows. Set signal DUTY to high during slave mode. See Table 5.
	M	262	M	I/O	1	Pin M inputs and outputs the alternating signal of the LCD output.

Classi-fication	Symbol	Pin No.	Pin Name	I/O	Number of Pins	Functions
LCD timing	SHL	251	Shift left	Input	1	Pin SHL switches the shift direction of the shift register. Refer to FLM for details.
	$\overline{\text{DISPOFF}}$	260	Display off	Input	1	Turns off the LCD. During master mode, liquid crystal drive output X1 to X240 can be set to level V1 by setting the pin to low. By setting the HD66520 to level V1 in the same way, the data on the display can be erased. During slave mode, set $\overline{\text{DISPOFF}}$ high.
	$\overline{\text{DOC}}$	265	Display off control	I/O	1	Controls the display-off function. During master mode, pin $\overline{\text{DOC}}$ becomes an output pin and controls display off after reset and display off according to signal $\overline{\text{DISPOFF}}$. In this case, connect this signal to the HD66520's pin $\overline{\text{DISPOFF}}$. During slave mode, pin $\overline{\text{DOC}}$ becomes an input pin for display off control signal. In this case, connect this signal to the master HD66503's pin $\overline{\text{DOC}}$.
LCD drive output	X1 to X240	240 to 1	X1 to X240	Output	240	Selects one from among four levels (V1, V2, V5, and V6) depending on the combination of M signal and display data. See Figure 3.

Note: 30 input/outputs (excluding driver block)

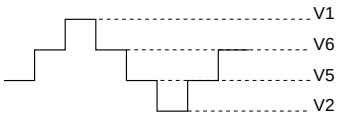


Figure 1 LCD Drive Levels

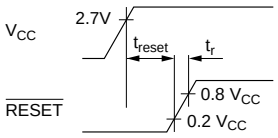


Figure 2 Reset Pin Operation

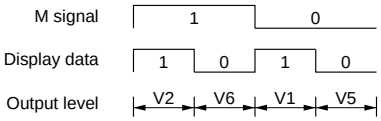


Figure 3 LCD Drive Output

Table 1 M/$\overline{S}$ Signal Status

M/$\overline{S}$	Mode	LCD Timing Generator	CL1, FLM, M, $\overline{DOC}$ Input/Output State
H	Master	1/120 or 1/240 duty cycle control	Output
L	Slave	Stop	Input

Table 2 MSW0 to MSW5 Signals Status

Number of Lines	MWS5	MWS4	MWS3	MWS2	MWS1	MWS0	Line Alternating Waveform	Pin M State
0	0	0	0	0	0	0	—	Input
1	0	0	0	0	0	1	Disable	Output
2	0	0	0	0	1	0	2-line alternation	
3 to 63	0 to 1	0 to 1	0 to 1	0 to 1	1 to 1	1 to 1	3-line alternation to 63-line alternation	

Table 3 MEOR Signal Status

Mode	MEOR	Types of Alternating Waveforms Output by Pin M
Master	H	Line alternating waveform ⊕ frame alternating waveform
	L	Line alternating waveform
Slave	L	—

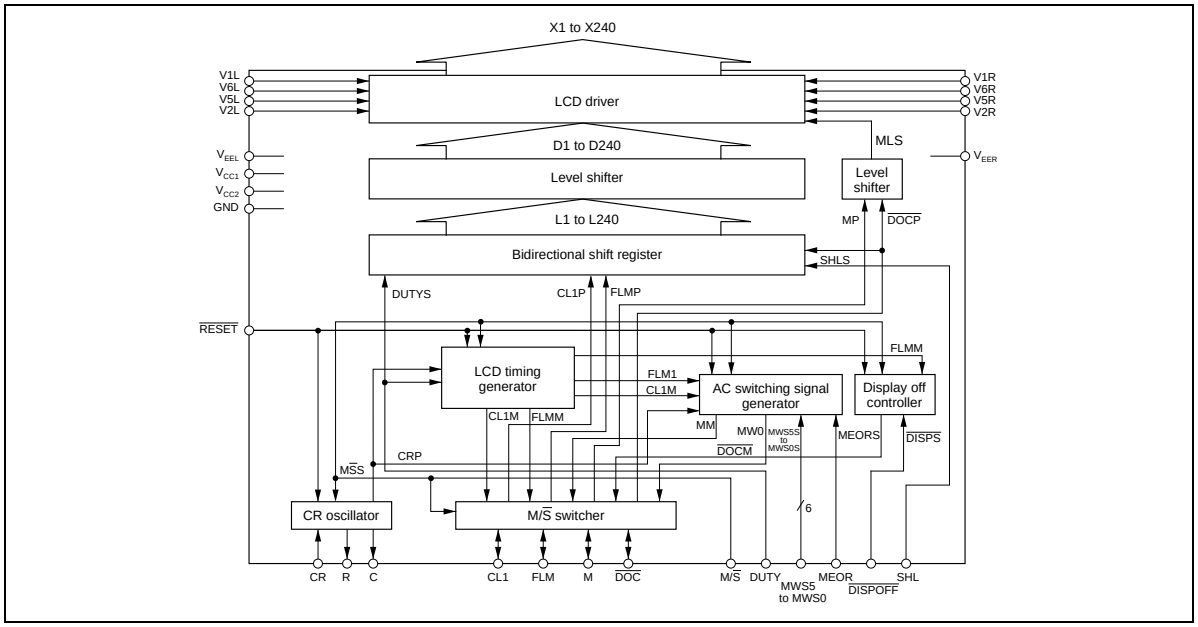
Table 4 Power Supply Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{reset}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Table 5 FLM Status Control

Mode	DUTY	SHL	Shift Direction of First Line Marker
Master	H	H	X240 → X1
		L	X1 → X240
	L	H	X120 → X1, X240 → X121
		L	X1 → X120, X121 → X240
Slave	H	H	X240 → X1
		L	X1 → X240

Internal Block Diagram



1. **CR Oscillator:** The CR oscillator generates the HD66503 operation clock. During master mode, since the operation clock is needed, connect oscillation resistor R_f with oscillation capacitor C_f as follows. When the external clock is used, input external clock to pin CR and open pins C and R (Figure 4).
   When using the HD66503 during slave mode, the operation clock will not be needed; therefore, connect pin CR to V_{CC} and open pins C and R (Figure 5).
2. **Liquid Crystal Timing Generator:** The liquid crystal timing generator creates various signals for the LCD. During master mode ($M/\overline{S} = V_{CC}$), the generator operates the HD66503's internal circuitry as a common internal driver using the generated LCD signals. In addition, signals CL1, M, and $\overline{DOC}$ created by this generator can synchronously display data on a liquid crystal display by inputting them into the RAM-provided segment driver HD66520 used together with HD66503. During slave mode ($M/\overline{S}$ = GND), this generator stops; the slave HD66503 operates based on signals CL1, M, $\overline{DOC}$, and FLM generated by the master HD66503.
3. **$M/\overline{S}$ Switcher:** Controls the input and output of LCD signals CL1, FLM, M, and $\overline{DOC}$.
   This circuit outputs data when $M/\overline{S} = V_{CC}$ (master mode) and inputs data when $M/\overline{S}$ = GND (slave mode).
4. **Alternating Signal Generator:** Generates the alternating signal for the liquid crystal display. Since the alternating signal decreases cross talk, it can alternate among 2 to 63 lines. The number of lines are specified with pins MWS0 to MWS5 is set to either V_{CC} or GND.
   Moreover, the alternating signal can be externally input by grounding pins MWS0 to MWS5. In this case, the alternating signal is input from pin M.

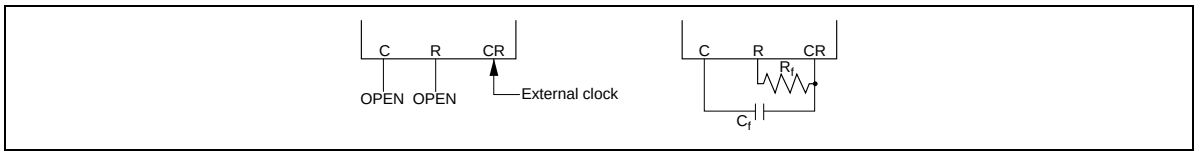


Figure 4 Oscillator Connection in Master Mode

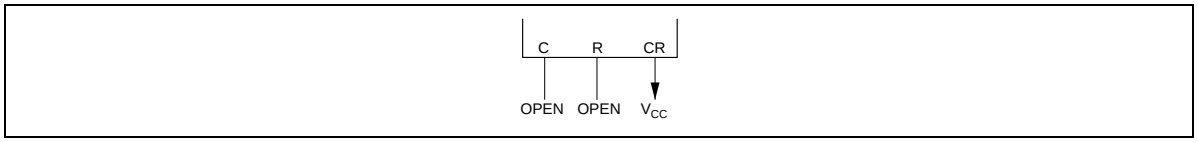


Figure 5 Oscillator Connection in Slave Mode

5. **Display Off Control Circuit:** Controls display-off function by using external display off signal $\overline{\text{DISPS}}$ and automatic display off signal FLMM generated by the liquid crystal timing generator. Automatic display off signal FLMM is an internal signal that is used to turn off the display in four frames after signal reset is released. As a result, it is possible to turn off display using the display off signal that is sent randomly from an external LSI and automatically prevent incorrect display after reset release.
6. **Bidirectional Shift Register:** This is a 240-bit bidirectional shift register. This register can change the shift direction using signal SHL. During master mode, the scan signal of the common driver can be generated by sequentially shifting first line marker signal FLM generated internally. During slave mode, a scan signal is generated by sequentially shifting first line marker signal FLM input from pin FLM.
7. **Level Shifter:** Boosts the logic signal to a high voltage signal for the LCD.
8. **LCD Drive Circuit:** One of the LCD levels V1, V2, V5, and V6 are selected and output via pin X according to the combination of the data in the bidirectional shift register and signal M.

Table 6 Output Level of LCD Circuit

Data in the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

Internal Function Description

1. **Generation of Signals CL1 and FLM:** Signal CL1 shifts the scanning signal of the common driver. It is a 50% duty-ratio clock that changes level synchronously with the rising edge of oscillator clock CR.

   FLM is a clock signal that is output once every 240 CL1 clock cycles for a duty of 1/240 (DUTY = V_{CC}), and every 120 CL1 clock cycles for a duty of 1/120 (DUTY = GND).
2. **Generation of Signal M:** Signal M alternates current in the LCD. It alternates the current to decrease cross talk after a certain number of lines ranging from 2 to 63 lines. The number of lines can be specified with pins MWS0 to MWS5 by setting each pin to either V_{CC} or GND (H or L). In addition, when pin MEOR is connected to GND, signal M is a simple line alternating waveform, and when pin MEOR is connected to V_{CC}, signal M is an EOR (exclusive OR) of line alternating waveform and frame alternating waveform.

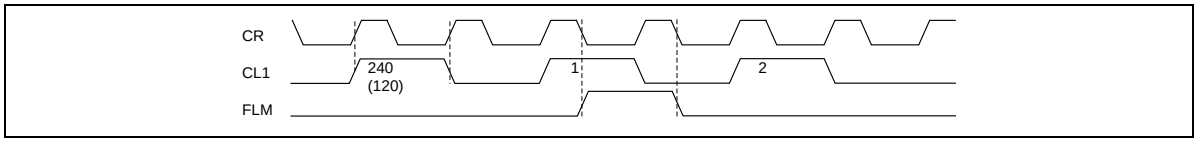


Figure 6 Generation of Signals CL1 and FLM

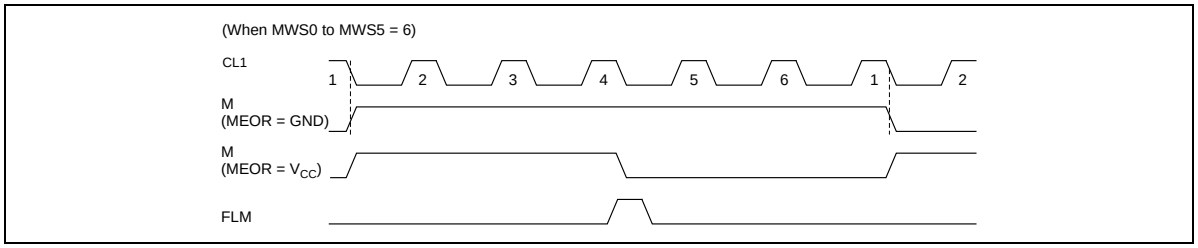


Figure 7 Generation of Signal M

3. Auto Display-Off Control: This functions prevents incorrect display after reset release. The display is turned off four frames following after reset release. In addition, the display off control signal shown in Figure 8 is output by pin $\overline{\text{DOC}}$. This pin is connected to pin $\overline{\text{DISPOFF}}$ of the HD66520.

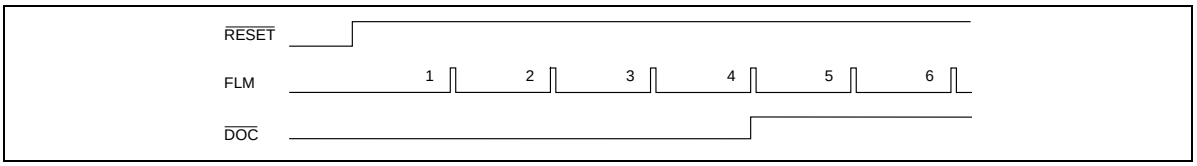


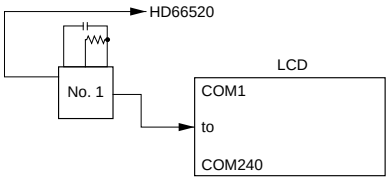
Figure 8 Automatic Display-Off Control Function

Application Example

Outline of HD66503 System Configuration

The HD66503 system configuration is outlined in Figures 9 and 10. Refer to the connection list (Table 7) for connection details.

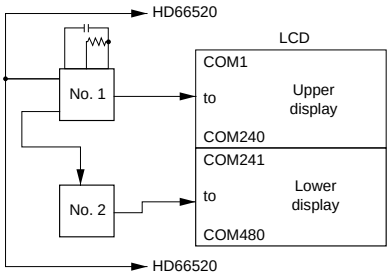
- When a single HD66503 is used to configure a small display (Figure 9)
- When two HD66503s are used to configure a large display (Figure 10)



	No. 1
When using the internal oscillator	Refer to connection list A
When using an external clock	Refer to connection list D

Note: One HD66503 drives common signals and supplies timing signal to the HD66520.

Figure 9 When Using a Single HD66503



	No. 1	No. 2
When using the internal oscillator	Refer to connection list B	Refer to connection list C
When using an external clock	Refer to connection list E	Refer to connection list C

Note: Upper and lower displays are driven by separate HD66503s to ensure display quality. No. 1 operates in master mode, and No. 2 operates in slave mode.

Figure 10 When Using Two HD66503s

HD66503 Connection List

Table 7 HD66503 Connection List

Connection Example	M/S	DUTY	MWS0, MWS1, MWS2, MWS3, MWS4, MWS5	MEOR	RESET	DISPOFF	CR	R	C	CL1	FLM	M	DOC	SHL	X1 to X240
A	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	R_f	R_f		To CL1 of HD66520	To FLM of HD66520	To M of HD66520	To DISPOFF of HD66520	L	COM1 to COM240
							C_f		C_f					H	COM240 to COM1
B	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	R_f	R_f		To CL1 of HD66520 HD66503	To FLM of HD66520 HD66503	To M of HD66520 HD66503	To DOC of HD66503	L	COM1 to COM240
							C_f		C_f				T0 DISPOFF of HD66520	H	COM240 to COM1
C	L	H	Sets the number of lines for alternating the current	L	From CPU or external reset circuit	H	H	—	—	From CL1 of HD66503	From FLM of HD66503	From M of HD66503	From DOC of HD66503	L	COM241 to COM480
														H	COM480 to COM241
D	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	From external oscillator	—	—	To CL1 of HD66520	To FLM of HD66520	To M of HD66520	To DISPOFF of HD66520	L	COM1 to COM240
														H	COM240 to COM1
E	H	H	Sets the number of lines for alternating the current	H	From CPU or external reset circuit	From controller	From external oscillator	—	—	To CL1 of HD66520 HD66503	To FLM of HD66520 HD66503	To M of HD66520 HD66503	To DOC of HD66503	L	COM1 to COM240
													To DISPOFF of HD66520	H	COM240 to COM1

Notes: H = V_{CC} (Fixed)
L = GND (Fixed)
"—" means "open"
R_f: Oscillation resistor
C_f: Oscillation capacitor

Example of System Configuration (1)

Figure 11 shows a system configuration for a 240 × 160-dot LCD panel using segment driver HD66520 with internal bit-map RAM. All required functions can be prepared for liquid crystal display with just two chips except for liquid crystal display power supply circuit functions. Refer to Timing Chart (1) for details.

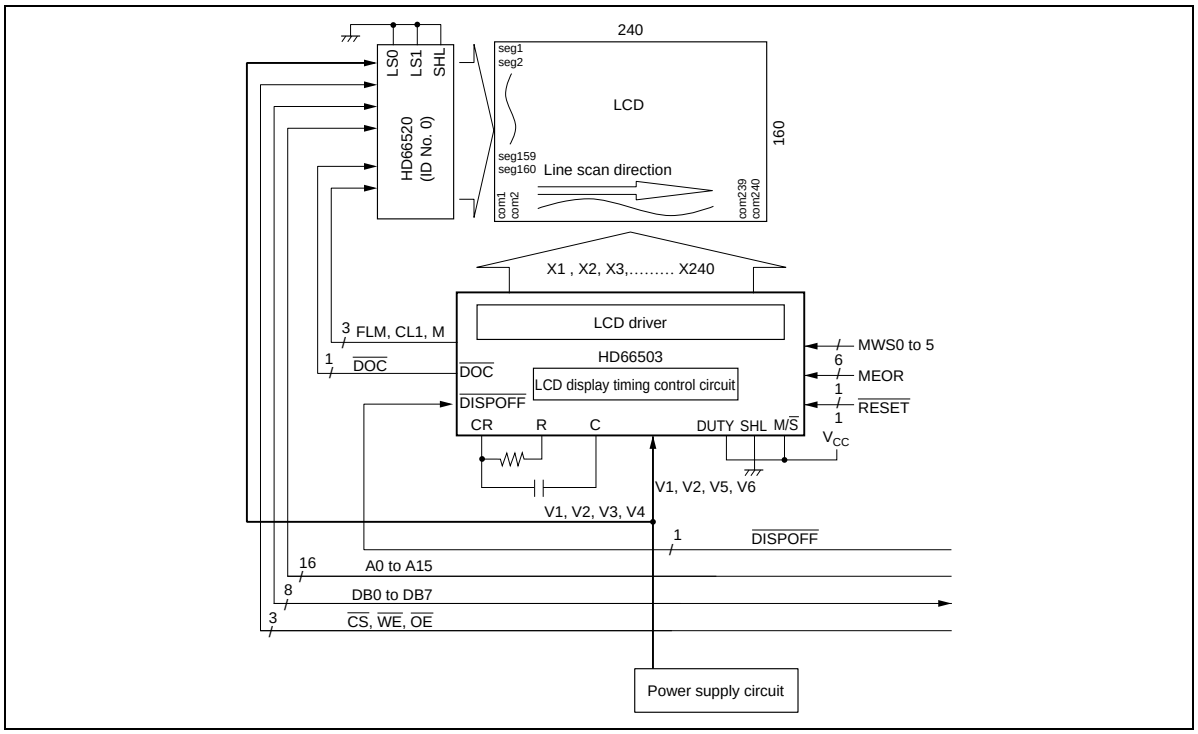


Figure 11 System Configuration (1)

Example of System Configuration (2)

Figure 12 shows a system configuration for a 240 × 320-dot LCD panel using segment driver HD66520 with internal bit-map RAM. Refer to Timing Chart (1) for details.

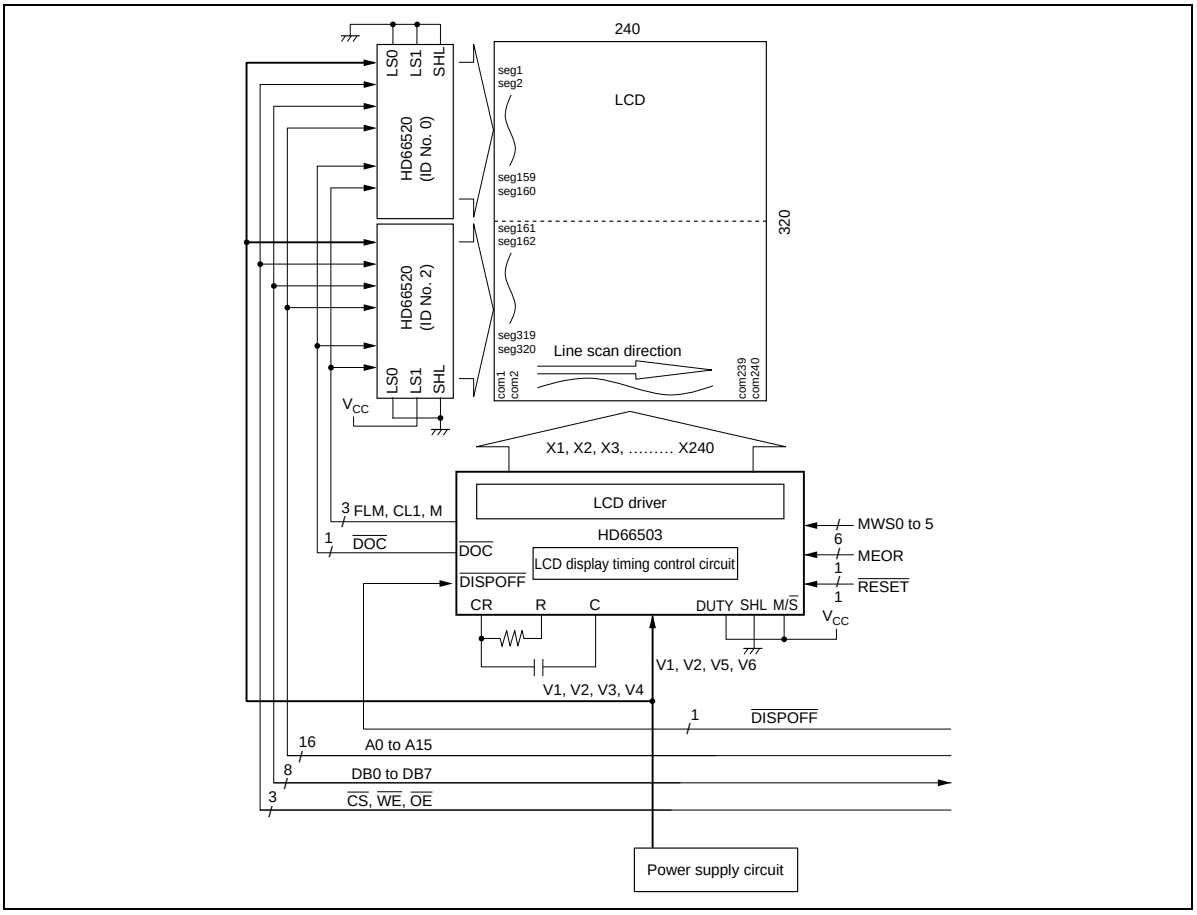


Figure 12 System Configuration (2)

Timing Chart (1)

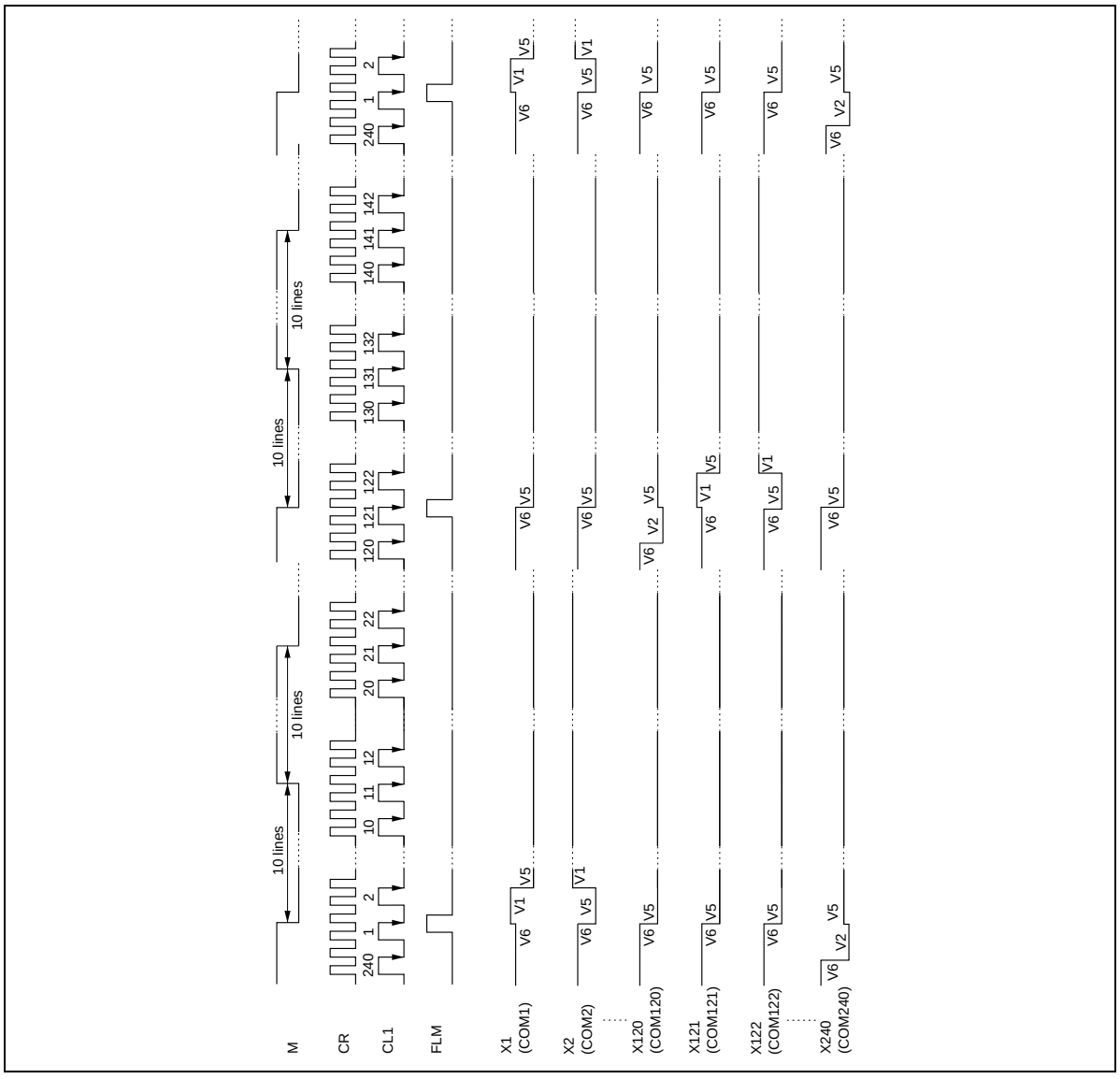


Figure 13 Timing Chart (1)

Example of System Configuration (3)

Figure 14 shows a system configuration for a 320 × 480-dot LCD panel using segment driver HD66520 with internal bit-map RAM. Refer to Timing Chart (2) for details.

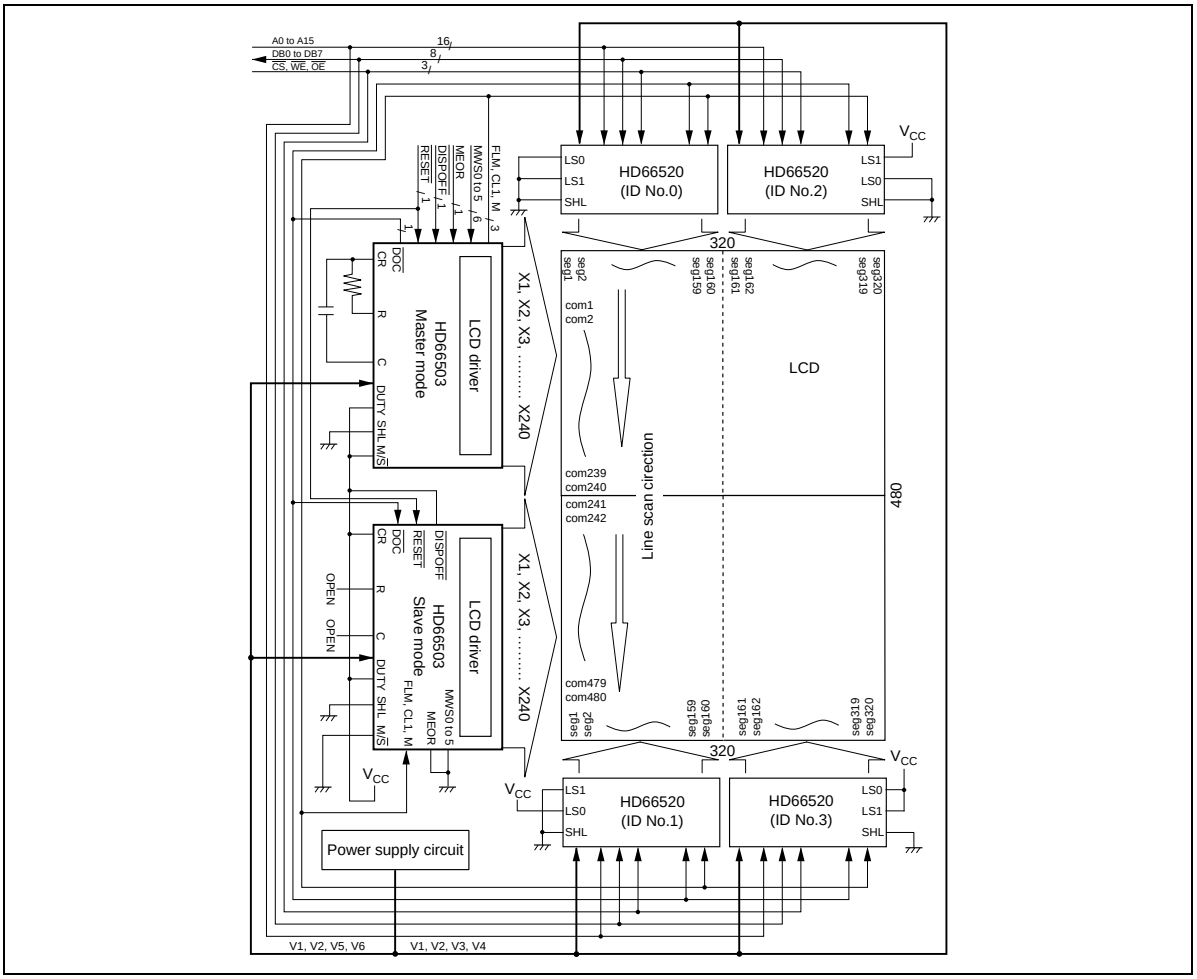


Figure 14 System Configuration (3)

Timing Chart (2)

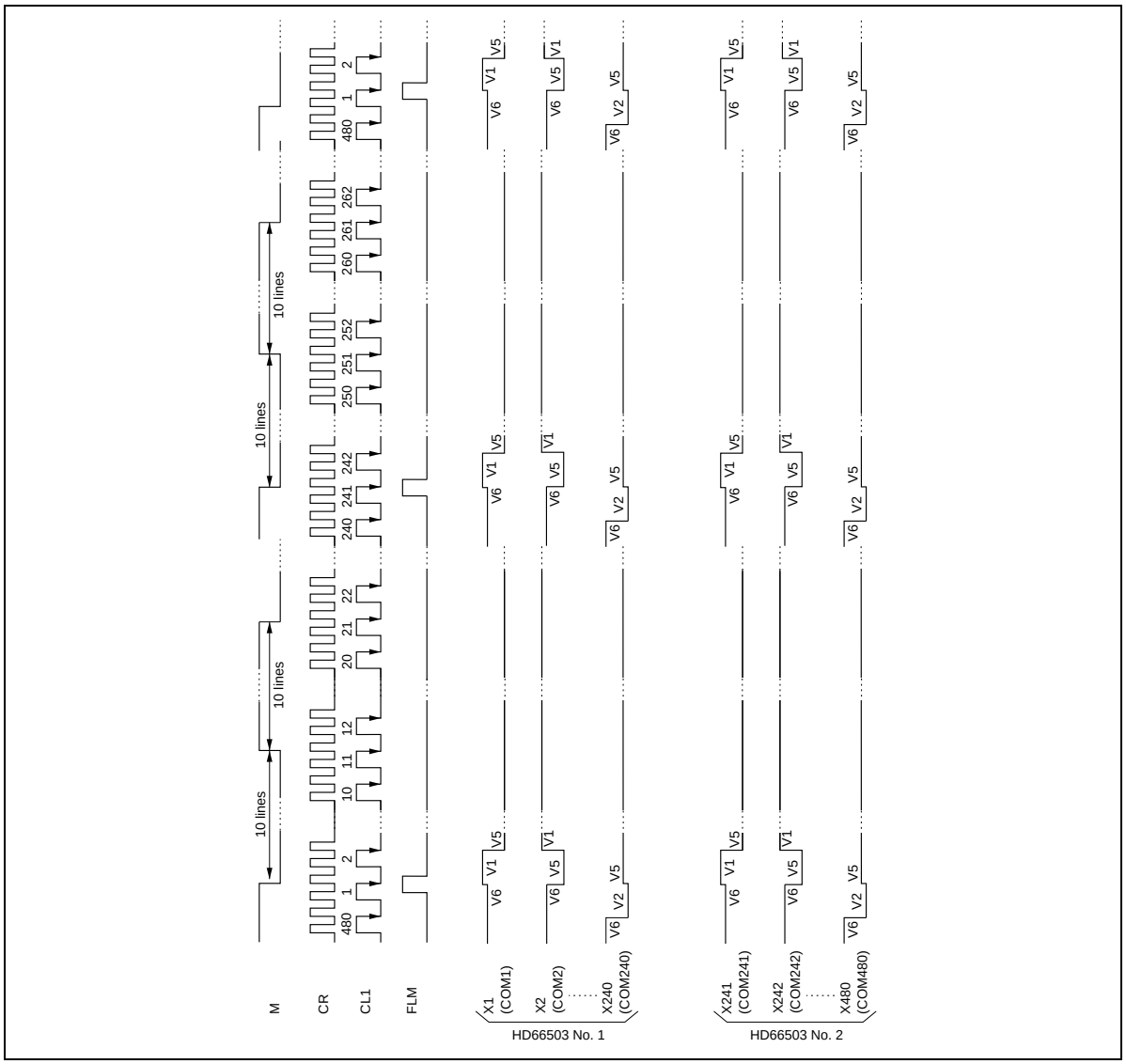
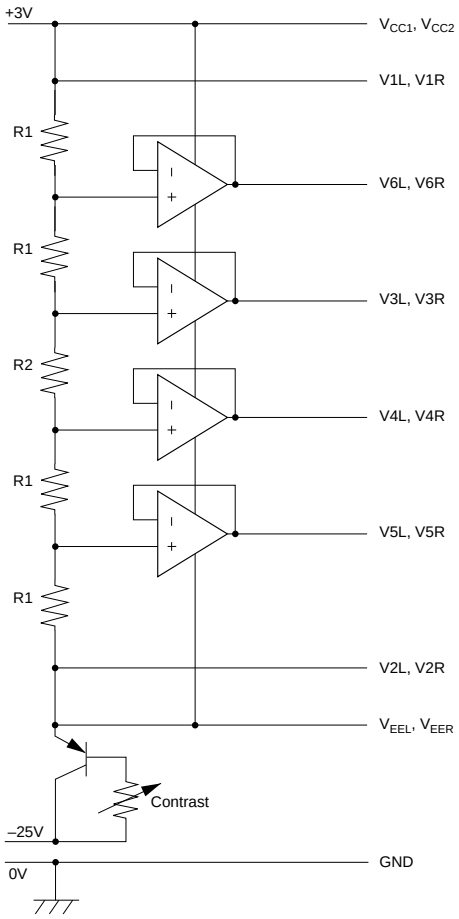


Figure 15 Timing Chart (2)

Power Supply Circuit



Note: The values of R1 and R2 vary with the LCD panel used. When the bias factor is 1/15, for example, the values of R1 and R2 can be determined as follows:

$$\frac{R1}{4R1 + R2} = \frac{1}{15}$$

If R1 = 3 kΩ, then R2 = 33 kΩ

Figure 16 Power Supply Circuit

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	2
	LCD drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3	V	5
Input voltage (1)		VT1	–0.3 to V_{CC} + 0.3	V	2, 3
Input voltage (2)		VT2	V_{EE} – 0.3 to V_{CC} + 0.3	V	4, 5
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

2. Measured relative to GND (0V).

3. Applies to all input pins except for V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R, and to input/output pins in high-impedance state.

4. Applies to pins V1L, V1R, V2L, V2R, V5L, V5R, V6L, and V6R.

5. Apply the same voltage to pairs V1L and V1R, V2L and V2R, V5L and V5R, V6L and V6R, and V_{EEL} and V_{EER}.
   It is important to preserve the relationships $V_{CC1} = V_{CC2} \geq V1L = V1R \geq V6L = V6R \geq V5L = V5R \geq V2L = V2R \geq V_{EEL} = V_{EER}$

Electrical Characteristics

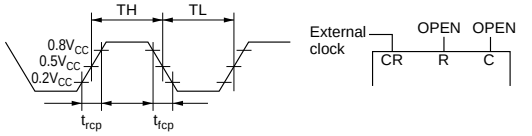
DC Characteristics (V_{CC} = 2.7 to 5.5V, V_{CC}–V_{EE} = 8 to 28V, GND = 0V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Measurement Condition	Notes
Input high level voltage	VIH	0.8 V_{CC}	—	V_{CC}	V		1
Input low level voltage	VIL	0	—	0.2 V_{CC}	V		1
Output high level voltage	VOH	V_{CC}–0.4	—	—	V	I_{OH} = –0.4 mA	2
Output low level voltage	VOL	—	—	0.4	V	I_{OL} = +0.4 mA	2
Driver “on” resistance	R_{ON}	—	—	2.0	kΩ	V_{CC}–V_{EE} = 28V, load current: ±150 µA	13, 14
Input leakage current (1)	I_{IL1}	–1.0	—	1.0	µA	VIN = 0 to V_{CC}	1
Input leakage current (2)	I_{IL2}	–25	—	25	µA	VIN = V_{EE} to V_{CC}	3
Operating frequency (1)	f_{opr1}	10	—	200	kHz	Master mode (external clock operation)	4
Operating frequency (2)	f_{opr2}	5	—	500	kHz	Slave mode	5
Oscillation frequency (1)	f_{OSC1}	70	100	130	kHz	C_f = 100 pF ±5%, R_f = 51 kΩ ±2%	6, 12
Oscillation frequency (2)	f_{OSC2}	21	30	39	kHz	C_f = 100 pF ±5%, R_f = 180 kΩ ±2%	6, 12
Power consumption (1)	I_{GND1}	—	—	80	µA	Master mode 1/240 duty cycle, C_f = 100 pF, R_f = 180 kΩ V_{CC}–GND = 3V, V_{CC}–V_{EE} = 28V	7, 8
Power consumption (2)	I_{GND2}	—	—	20	µA	Master mode 1/240 duty cycle external clock f_{opr1} = 30 kHz V_{CC}–GND = 3V, V_{CC}–V_{EE} = 28V	7, 9
Power consumption (3)	I_{GND3}	—	—	10	µA	Slave mode 1/240 duty cycle during operation f_{CL} = 15 kHz V_{CC}–GND = 3V, V_{CC}–V_{EE} = 28V	7, 10

Item	Symbol	Min	Typ	Max	Unit	Measurement Condition	Notes
Power consumption	I_{EE}	—	—	20	µA	Master mode 1/240 duty cycle, C_f = 100 pF, R_f = 180 kΩ V_{CC}–GND = 3V V_{CC}–V_{EE} = 28V,	7, 11

Notes: 1. Applies to input pins MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, $\overline{\text{RESET}}$, and CR, and when inputting to input/output pins CL1, FLM, $\overline{\text{DOC}}$, and M.

2. Applies when outputting from input/output pins CL1, FLM, $\overline{\text{DOC}}$, and M.
3. Applies to V1L/R, V2L/R, V5L/R, and V6L/R. X1 to X240 are open.
4. Figure 17 shows the external clock specifications:



$$\text{Duty} = \frac{TH}{TH + TL} \times 100\%$$

	Min	Typ	Max	Unit
Duty	45	50	55	%
t_{rcp}	—	—	50	ns
t_{fcp}	—	—	50	ns

Figure 17 External Clock

5. Regulates to operation frequency limits of the bidirectional shift register in the slavemode.
6. Connect resistance Rf and capacitance Cf as follows:

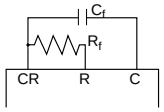


Figure 18 Timing Components

7. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to V_{cc} and GND levels, respectively.
8. This value is specified for the current flowing through GND under the following conditions: Internal oscillation circuit is used. Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, and $\overline{\text{RESET}}$ is connected to V_{cc}. Oscillator is set as described in note 6.
9. This value is specified for the current flowing through GND under the following conditions: Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{\text{DISPOFF}}$, M/$\overline{\text{S}}$, and $\overline{\text{RESET}}$ is connected to V_{cc}. Oscillator is set as described in note 4.

10. This value is specified for the current flowing through GND under the following conditions: Each terminal of MEOR, MWS0 to MWS5, DUTY, SHL, $\overline{DOC}$, $\overline{DISPOFF}$, $\overline{RESET}$, and CR is connected to V_{CC}, M/$\overline{S}$ to GND, and frequency of CL1, FLM, M is respectively established as follows.

    f_{CL1} = 15 kHz, f_{FLM} = 62.5 Hz, f_M = 120 Hz

11. This value is specified for the current flowing through V_{EE} under the following condition described in note 8. Do not connect any lines to pin X.
12. Figure 19 shows a typical relation among ocsillation frequency R_f and C_f. Oscillation frequency may vary with mounting conditions.

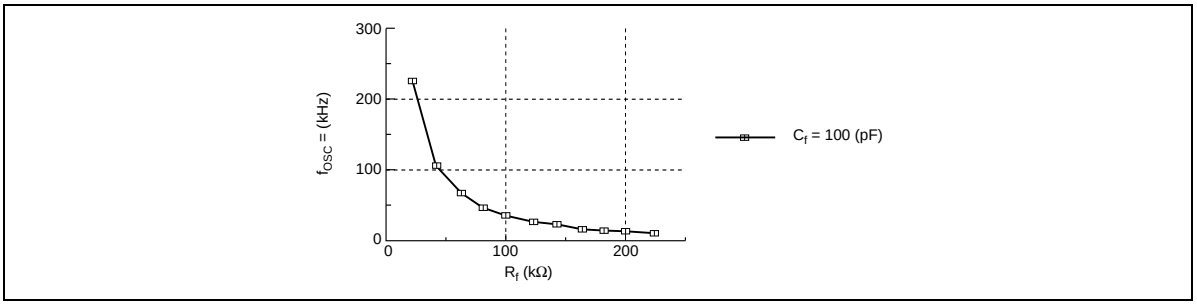


Figure 19 Ocsillation Frequency Characteristics

13. Indicates the resistance between one pin from X1 to X240 and another pin from the V pins V1L/R, V2L/R, V5L/R, and V6L/R, when a load current is applied to the X pin; defined under the following conditions:

    V_{CC}–V_{EE} = 28 (V)
    V1L/R, V6L/R = V_{CC}–1/10 (V_{CC}–V_{EE})
    V5L/R, V2L/R = V_{EE} + 1/10 (V_{CC}–V_{EE})

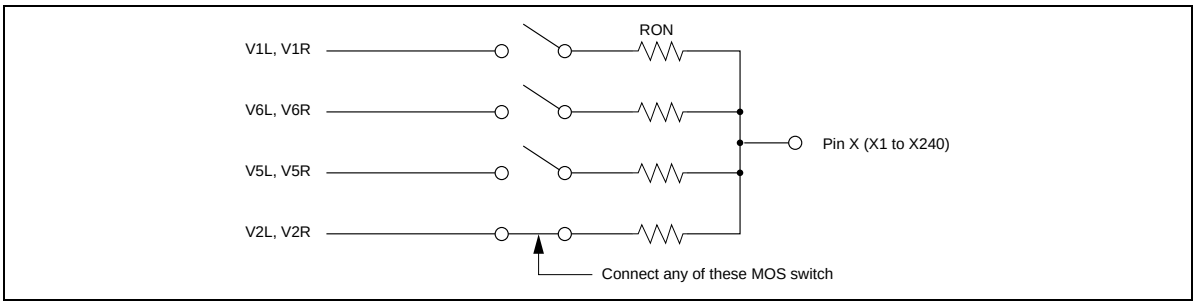


Figure 20 On Resistance Conditions

14. V1L/R and V6L/R should be near the V_{CC} level, and V5L/R and V2L/R should be near the V_{EE} level. All these voltage pairs should be separated by less than ΔV, which is the range within which R_{ON}, the LCD drive circuits' output impedance is stable. Note that ΔV depend on power supply voltages V_{CC}–V_{EE}. See Figure 21.

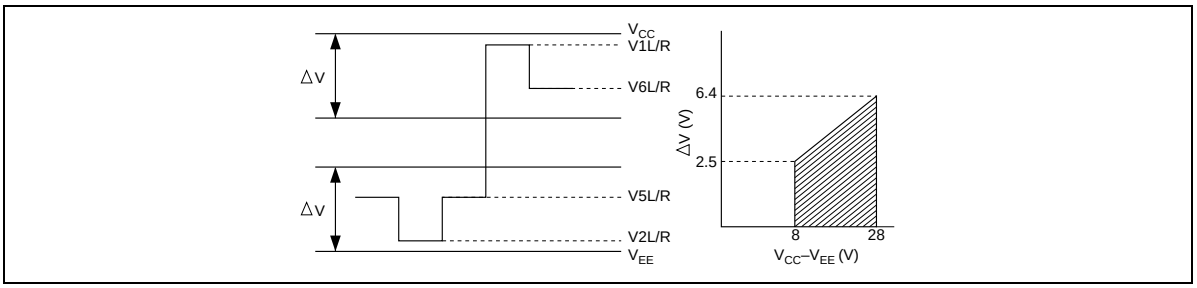


Figure 21 Relationship between Driver Output Waveform

AC Characteristics (V_{CC} = 2.7 to 5.5V, V_{CC}–V_{EE} = 8 to 28V, GND = 0V, Ta = –20 to +75°C)

Slave Mode (M/$\overline{S}$ = GND)

Item	Symbol	Min	Typ	Max	Unit	Notes
CL1 high-level width	t_{CWH}	500	—	—	ns	1
CL1 low-level width	t_{CWL}	500	—	—	ns	1
FLM setup time	t_{FS}	100	—	—	ns	1
FLM hold time	t_{FH}	100	—	—	ns	1
CL1 rise time	t_r	—	—	50	ns	1
CL1 fall time	t_f	—	—	50	ns	1

Note: 1. Based on the load circuit shown in Figure 22.

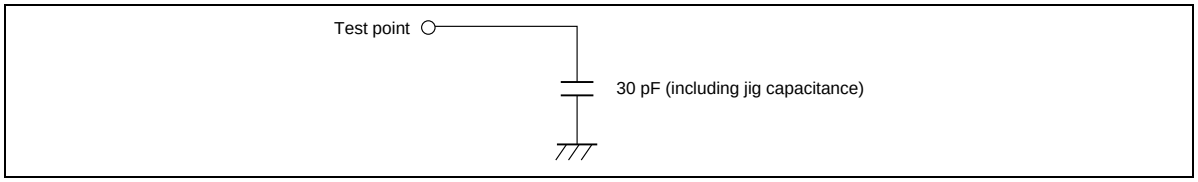


Figure 22 Load Circuit

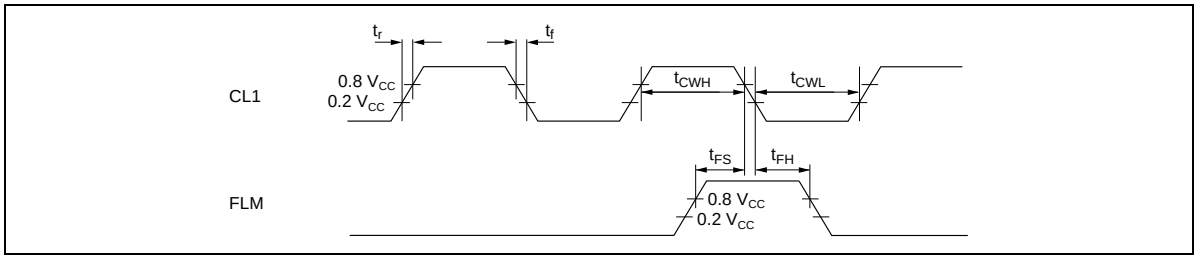


Figure 23 Slave Mode Timing

Master Mode ($M/\overline{S} = V_{CC}$)

Item	Symbol	Min	Typ	Max	Unit	Notes
CL1 delay time	t_{DCL1}	—	—	1	µs	
FLM delay time	t_{DFLM}	—	—	1	µs	
M delay time	t_{DM}	—	—	500	ns	
FLM setup time	t_{FS}	$t_{osc}/2 - 500$	—	—	ns	

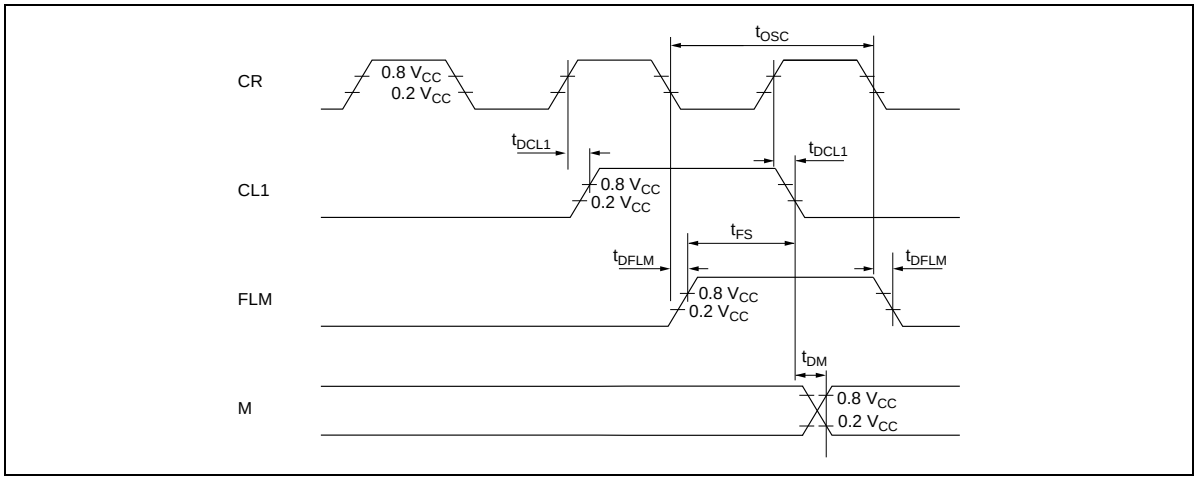


Figure 24 Master Mode Timing