HD66712 (LCD-II/F12)

(Dot-Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD66712 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, numbers, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a serial or a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimum system can be interfaced with this controller/driver.

A single HD66712 is capable of displaying a single 24-character line, two 24-character lines, or four 12-character lines.

The HD66712 software is upwardly compatible with the LCDII (HD44780) which allows the user to easily replace an LCD-II with an HD66712. In addition, the HD66712 is equipped with functions such as segment displays for icon marks, a 4-line display mode, and a horizontal smooth scroll, and thus supports various display forms. This achieves various display forms. The HD66712 character generator ROM is extended to generate 240 5 × 8 dot characters.

The low-voltage operation (2.7 V) of the HD66712, combined with a low-power mode, is suitable for any portable battery-driven product requiring low power consumption.

Features

- 5 × 8 dot matrix possible
- Clock-synchronized serial interface capability; can interface with 4- or 8-bit MPU
- Low-power operation support:
  - 2.7 to 5.5 V (low voltage)
  - Wide liquid-crystal voltage range: 3.0 to 13.0 V max.
- Booster for liquid crystal voltage
  - Two/three times (13 V max.)
- High-speed MPU bus interface (2MHz at 5-V operation)
- Extension driver interface
- Character display and independent 60-icon mark display possible
- Horizontal smooth scroll by 6-dot font width display possible
- 80 × 8-bit display RAM (80 characters max.)
- 9,600-bit character generator ROM
  - 240 characters (5 × 8 dot)
- 64 × 8-bit character generator RAM
  - 8 characters (5 × 8 dot)
- 16 × 8-bit segment icon mark
  - 96-segment icon mark
- 34-common × 60-segment liquid crystal display driver
- Programmable duty cycle (See list 1)
- Software upwardly compatible with HD44780
- Wide range of instruction functions:
  - Functions compatible with LCD-II: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
  - Additional functions: Icon mark control, 4-line display, horizontal smooth scroll, 6-dot character width control, white-black inverting blinking cursor
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)

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- Internal oscillator with an external resistor
- Low power consumption
- QFP 1420-128 pin, TCP-128 pin, bare-chip

List 1 Programmable Duty Cycles

		5-Dot Font Width			
		Single-Chip Operation		With Extension Driver	
Number of Lines	Duty Ratio	Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 24-character line	60	One 52-character line	80
2	1/33	Two 24-character lines	60	Two 32-character lines	80
4	1/33	Four 24-character lines	60	Four 20-character lines	80

		6-Dot Font Width			
		Single-Chip Operation		With Extension Driver	
Number of Lines	Duty Ratio	Displayed Characters	Icons	Displayed Characters	Icons
1	1/17	One 20-character line	60	One 50-character line	96
2	1/33	Two 20-character lines	60	Two 30-character lines	96
4	1/33	Four 10-character lines	60	Four 20-character lines	96

Ordering Information

Type No.	Package	CGROM
HD66712A00FS	QFP1420-128 (FP-128)	Japanese standard
HD66712A00TA0	Standard TCP-128	
HD66712A00TB0*	Folding TCP-128	
HCD66712A00	Chip	
HCD66712A01	Chip	Communication
HD66712A02FS	QFP1420-128 (FP-128)	European font
HCD66712A02	Chip	
HCD66712A03	Chip	Japanese + European font
HD66712BxxFS	QFP1420-128 (FP-128)	Custom font
HCD66712Bxx	Chip	

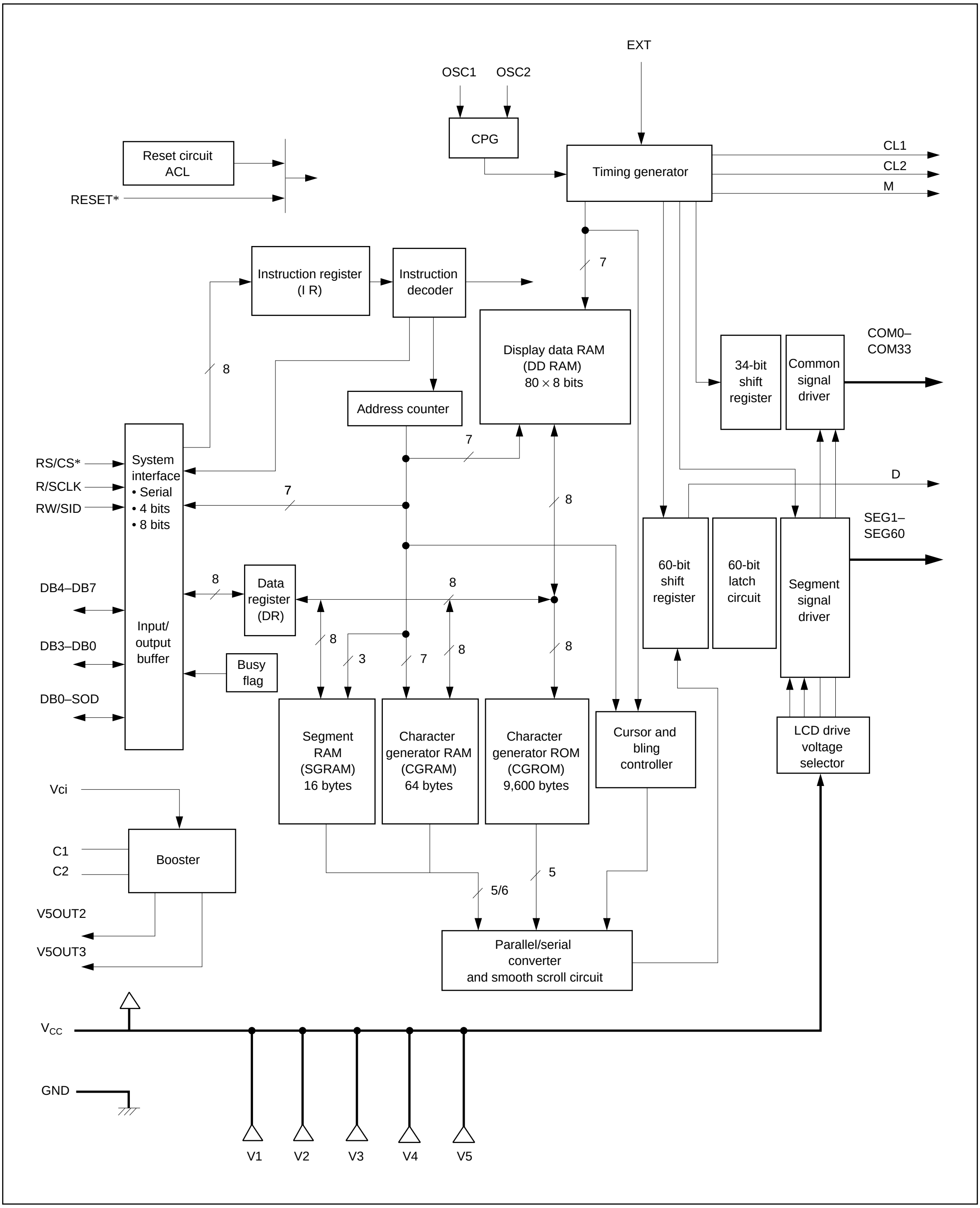
Note: Bxx = ROM code No.
* Under development

LCD-II Family Comparison

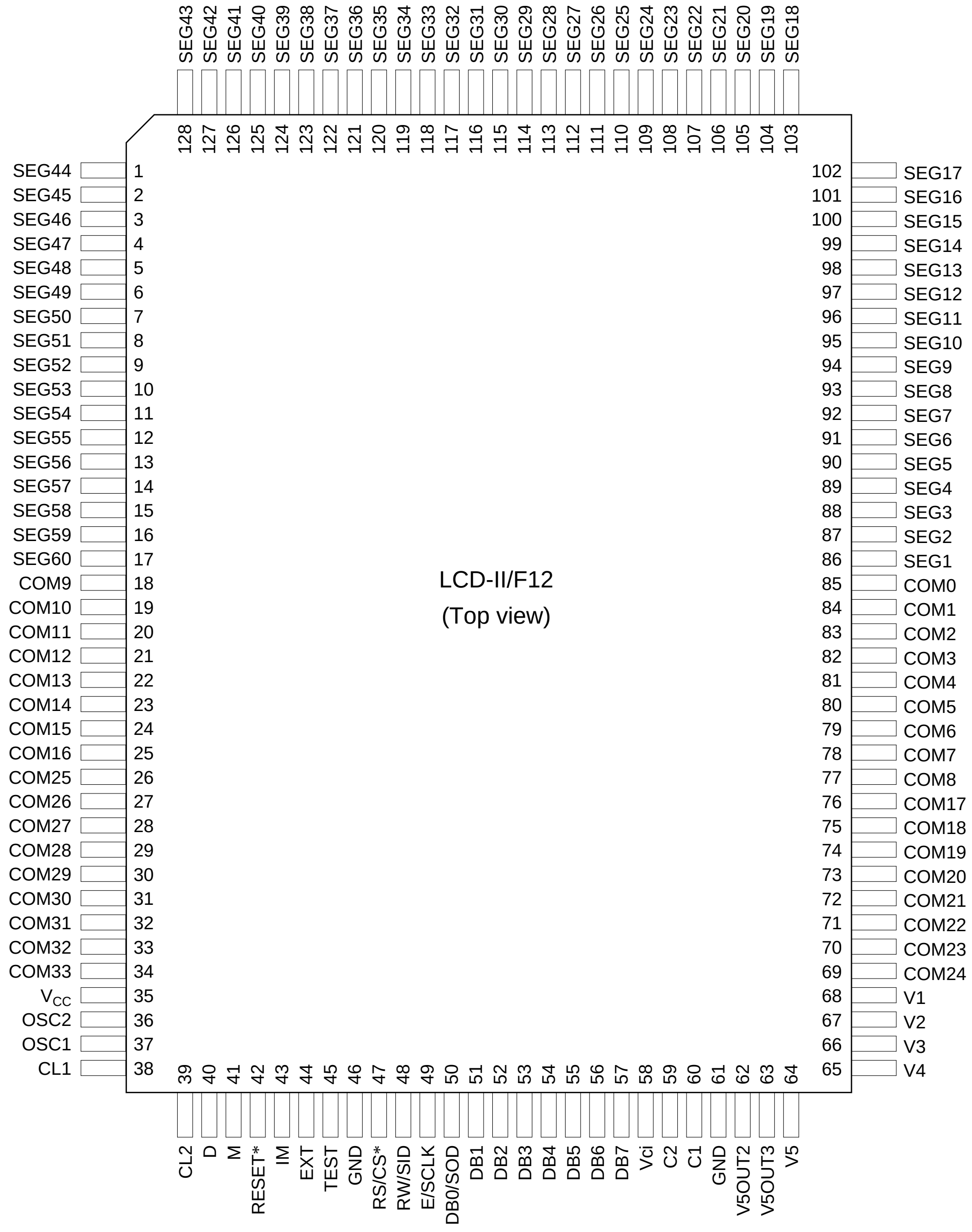
Item	LCD-II (HD44780U)	LCD-II/E20 (HD66702)	LCD-II/F8 (HD66710)	LCD-II/F12 HD66712
Power supply voltage	2.7 V to 5.5 V	5 V ±10 % (standard) 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 V to 11 V	3.0 V to 8.3 V	3.0 V to 13.0 V	3.0 V to 13.0 V
Maximum display digits per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines
Segment display	None	None	40 segments	60 segments
Display duty cycle	1/8, 1/11, and 1/16	1/8, 1/11, and 1/16	1/17 and 1/33	1/17 and 1/33
CGROM	9,920 bits (208 5 × 8 dot characters and 32 5 × 10 dot characters)	7,200 bits (160 5 × 7 dot characters and 32 5 × 10 dot characters)	9,600 bits (240 5 × 8 dot characters)	9,600 bits (240 5 × 8 dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes
SEGRAM	None	None	8 bytes	16 bytes
Segment signals	40	100	40	60
Common signals	16	16	33	34
Liquid crystal drive waveform	A	B	B	B
Bleeder resistor for LCD power supply	External (adjustable)	External (adjustable)	External (adjustable)	External (adjustable)
Clock source	External resistor or external clock	External resistor or external clock	External resistor or external clock	External resistor or external clock
R_f oscillation frequency (frame frequency)	270 kHz ±30% (59 to 110 Hz for 1/8 and 1/16 duty cycle; 43 to 80 Hz for 1/11 duty cycle)	320 kHz ±30% (70 to 130 Hz for 1/8 and 1/16 duty cycle; 51 to 95 Hz for 1/11 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)	270 kHz ±30% (56 to 103 Hz for 1/17 duty cycle; 57 to 106 Hz for 1/33 duty cycle)
R_f resistance	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	68 kΩ: 5-V operation; 56 kΩ: (3-V operation)	91 kΩ: 5-V operation; 75 kΩ: 3-V operation	91 kΩ: 5-V operation; 75 kΩ: 3-V operation

Item	**LCD-II (HD44780U)**	**LCD-II/E20 (HD66702)**	**LCD-II/F8 (HD66710)**	**LCD-II/F12 HD66712**
Liquid crystal voltage booster circuit	None	None	2–3 times step-up circuit	2–3 times step-up circuit
Extension driver control signal	Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal
Reset function	Power on automatic reset	Power on automatic reset	Power on automatic reset	Power on automatic reset or Reset input
Instructions	LCD-II (HD44780)	Fully compatible with the LCD-II	Upper compatible with the LCD-II	Upper compatible with the LCD-II
Number of displayed lines	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
Low power mode	None	None	Available	Available
Horizontal scroll	Character unit	Character unit	Dot unit	Dot unit
Bus interface	4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial; 4 bits/8 bits
CPU bus timing	2 MHz: 5-V operation; 1 MHz: 3-V operation	1 MHz	2 MHz: 5-V operation; 1 MHz: 3-V operation	2 MHz: 5-V operation; 1 MHz: 3-V operation
Package	QFP-1420-80 80-pin bare chip	LQFP-2020–144 144-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip	QFP-1420-128 TCP-128 128-pin bare chip

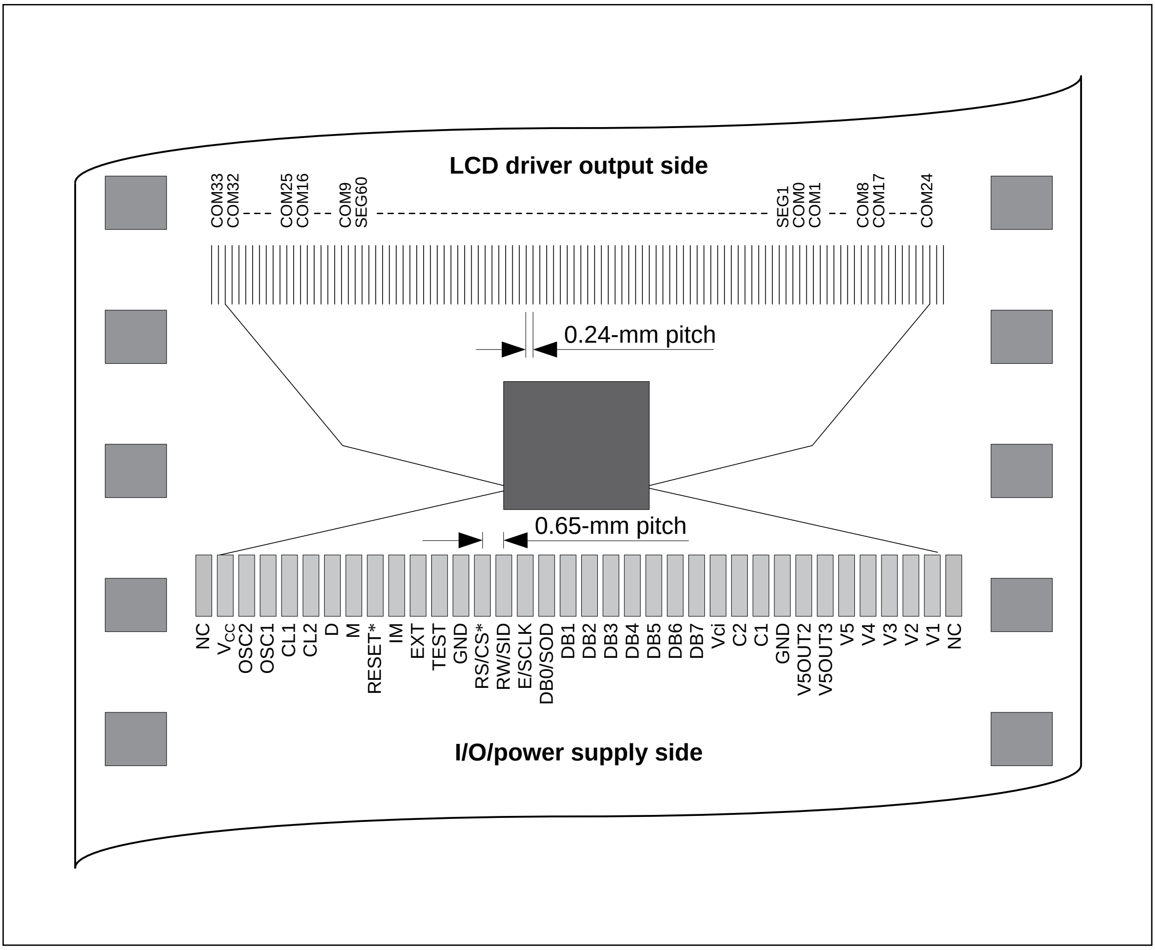
HD66712 Block Diagram


EXT
OSC1
OSC2
CPG
Timing generator
CL1
CL2
M
Reset circuit ACL
RESET*
Instruction register (I R)
Instruction decoder
7
8
Display data RAM (DD RAM) 80 × 8 bits
34-bit shift register
Common signal driver
COM0–COM33
Address counter
7
System interface
• Serial
• 4 bits
• 8 bits
RS/CS*
R/SCLK
RW/SID
7
8
D
SEG1–SEG60
60-bit shift register
60-bit latch circuit
Segment signal driver
DB4–DB7
DB3–DB0
DB0–SOD
Input/ output buffer
Data register (DR)
8
8
Busy flag
8
3
7
8
8
Segment RAM (SGRAM) 16 bytes
Character generator RAM (CGRAM) 64 bytes
Character generator ROM (CGROM) 9,600 bytes
Cursor and bling controller
LCD drive voltage selector
Vci
C1
C2
Booster
V5OUT2
V5OUT3
5/6
5
Parallel/serial converter and smooth scroll circuit
V_{CC}
GND
V1
V2
V3
V4
V5

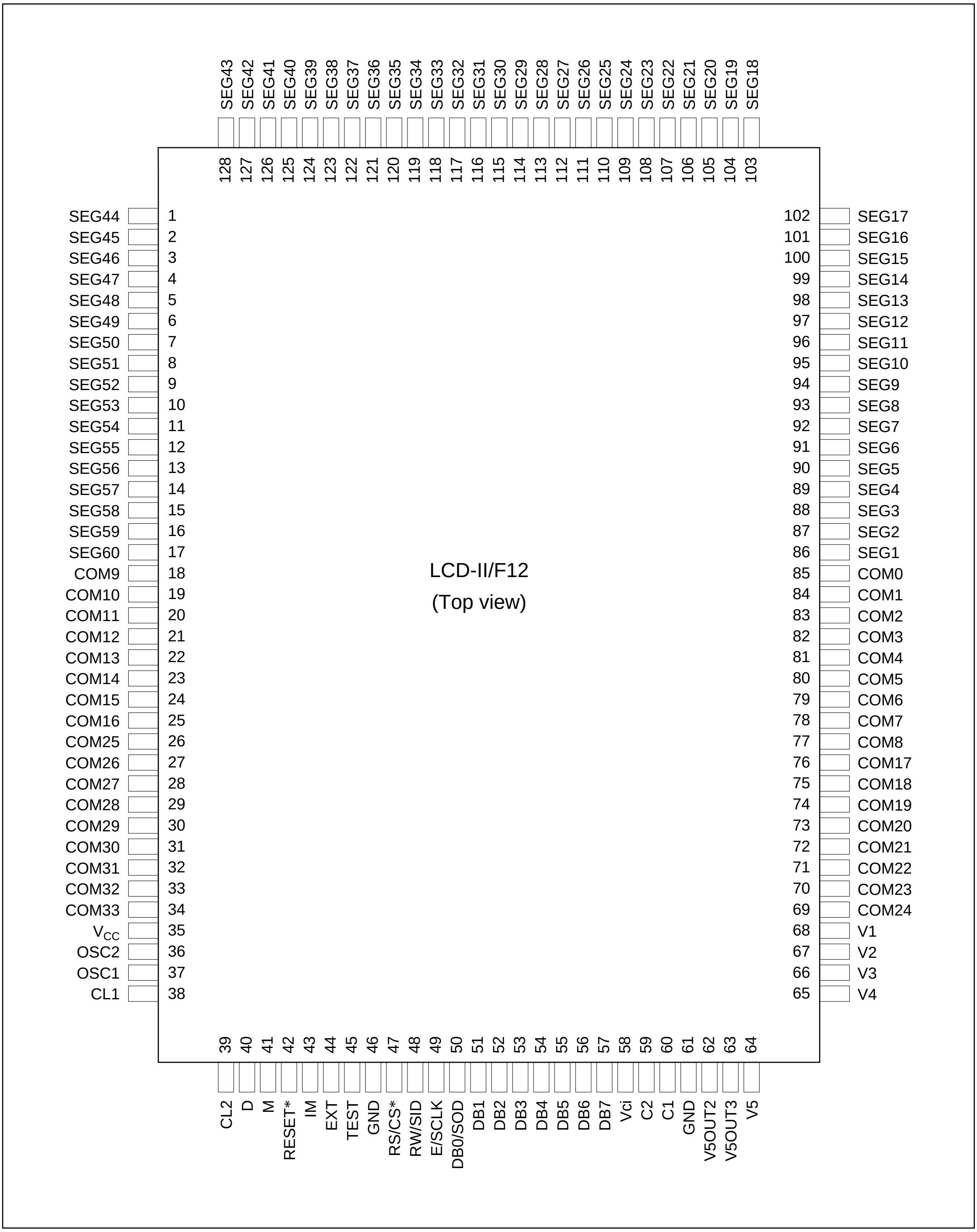
HD66712 Pin Arrangement


LCD-II/F12
(Top view)
1 SEG44
2 SEG45
3 SEG46
4 SEG47
5 SEG48
6 SEG49
7 SEG50
8 SEG51
9 SEG52
10 SEG53
11 SEG54
12 SEG55
13 SEG56
14 SEG57
15 SEG58
16 SEG59
17 SEG60
18 COM9
19 COM10
20 COM11
21 COM12
22 COM13
23 COM14
24 COM15
25 COM16
26 COM25
27 COM26
28 COM27
29 COM28
30 COM29
31 COM30
32 COM31
33 COM32
34 COM33
35 V_{CC}
36 OSC2
37 OSC1
38 CL1
39 CL2
40 D
41 M
42 RESET*
43 IM
44 EXT
45 TEST
46 GND
47 RS/CS*
48 RW/SID
49 E/SCLK
50 DB0/SOD
51 DB1
52 DB2
53 DB3
54 DB4
55 DB5
56 DB6
57 DB7
58 Vci
59 C2
60 C1
61 GND
62 V5OUT2
63 V5OUT3
64 V5
65 V4
66 V3
67 V2
68 V1
69 COM24
70 COM23
71 COM22
72 COM21
73 COM20
74 COM19
75 COM18
76 COM17
77 COM8
78 COM7
79 COM6
80 COM5
81 COM4
82 COM3
83 COM2
84 COM1
85 COM0
86 SEG1
87 SEG2
88 SEG3
89 SEG4
90 SEG5
91 SEG6
92 SEG7
93 SEG8
94 SEG9
95 SEG10
96 SEG11
97 SEG12
98 SEG13
99 SEG14
100 SEG15
101 SEG16
102 SEG17
103 SEG18
104 SEG19
105 SEG20
106 SEG21
107 SEG22
108 SEG23
109 SEG24
110 SEG25
111 SEG26
112 SEG27
113 SEG28
114 SEG29
115 SEG30
116 SEG31
117 SEG32
118 SEG33
119 SEG34
120 SEG35
121 SEG36
122 SEG37
123 SEG38
124 SEG39
125 SEG40
126 SEG41
127 SEG42
128 SEG43

TCP Dimensions


LCD driver output side
COM33
COM32
COM25
COM16
COM9
SEG60
SEG1
COM0
COM1
COM8
COM17
COM24
0.24-mm pitch
0.65-mm pitch
NC
V_{CC}
OSC2
OSC1
CL1
CL2
D
M
RESET*
IM
EXT
TEST
GND
RS/CS*
RW/SID
E/SCLK
DB0/SOD
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Vci
C2
C1
GND
V5OUT2
V5OUT3
V5
V4
V3
V2
V1
NC
I/O/power supply side

HD66712 Pad Arrangement


SEG43 128
SEG42 127
SEG41 126
SEG40 125
SEG39 124
SEG38 123
SEG37 122
SEG36 121
SEG35 120
SEG34 119
SEG33 118
SEG32 117
SEG31 116
SEG30 115
SEG29 114
SEG28 113
SEG27 112
SEG26 111
SEG25 110
SEG24 109
SEG23 108
SEG22 107
SEG21 106
SEG20 105
SEG19 104
SEG18 103
SEG44 1
SEG45 2
SEG46 3
SEG47 4
SEG48 5
SEG49 6
SEG50 7
SEG51 8
SEG52 9
SEG53 10
SEG54 11
SEG55 12
SEG56 13
SEG57 14
SEG58 15
SEG59 16
SEG60 17
COM9 18
COM10 19
COM11 20
COM12 21
COM13 22
COM14 23
COM15 24
COM16 25
COM25 26
COM26 27
COM27 28
COM28 29
COM29 30
COM30 31
COM31 32
COM32 33
COM33 34
V_{CC} 35
OSC2 36
OSC1 37
CL1 38
LCD-II/F12
(Top view)
102 SEG17
101 SEG16
100 SEG15
99 SEG14
98 SEG13
97 SEG12
96 SEG11
95 SEG10
94 SEG9
93 SEG8
92 SEG7
91 SEG6
90 SEG5
89 SEG4
88 SEG3
87 SEG2
86 SEG1
85 COM0
84 COM1
83 COM2
82 COM3
81 COM4
80 COM5
79 COM6
78 COM7
77 COM8
76 COM17
75 COM18
74 COM19
73 COM20
72 COM21
71 COM22
70 COM23
69 COM24
68 V1
67 V2
66 V3
65 V4
39 CL2
40 D
41 M
42 RESET*
43 IM
44 EXT
45 TEST
46 GND
47 RS/CS*
48 RW/SID
49 E/SCLK
50 DB0/SOD
51 DB1
52 DB2
53 DB3
54 DB4
55 DB5
56 DB6
57 DB7
58 Vci
59 C2
60 C1
61 GND
62 V5OUT2
63 V5OUT3
64 V5

Pin Functions

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
IM	1	I	—	Selects interface mode with the MPU; Low: Serial mode High: 4-bit/8-bit bus mode (Bus width is specified by instruction.)
RS/CS*	1	I	MPU	Selects registers during bus mode: Low: Instruction register (write); Busy flag, address counter (read) High: Data register (write/read) Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
RW/SID	1	I	MPU	Selects read/write during bus mode; Low: Write High: Read Inputs serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Inputs (Receives) serial clock during serial mode.
DB_4 to DB_7	4	I/O	MPU	Four high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. DB_7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB_1 to DB_3	3	I/O	MPU	Three low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66712. Open these pins during 4-bit operation or serial mode since they are not used.
DB0/ SOD	1	I/O /O	MPU	The lowest bidirectional data bit (DB0) during 8-bit bus mode. Open these pins during 4-bit mode since they are not used. Outputs (transfers) serial data during serial mode. Open this pin if reading (transfer) is not performed.
COM_0 to COM_{33}	34	O	LCD	Common signals; those that are not used become non-selected waveforms. At 1/17 duty rate, COM_1 to COM_{16} are used for character display, COM_0 and COM_{17} for icon display, and COM_{18} to COM_{33} become non-selected waveforms. At 1/33 duty rate, COM_1 to COM_{32} are used for character display, and COM_0 and COM_{33} for icon display. Because two COM signals output the same level simultaneously, apply them according to the wiring pattern of the display device.
SEG_1 to SEG_{60}	60	O	LCD	Segment output signals

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
CL1	1	O	Extension driver	When EXT = high, outputs the extension driver latch pulse.
CL2	1	O	Extension driver	When EXT = high, outputs the extension driver shift clock.
D	1	O	Extension driver	When EXT = high, outputs extension driver data; data from the 61st dot on is output.
M	1	O	Extension driver	When EXT = high, outputs the extension driver AC signal.
EXT	1	I	—	When EXT = high, outputs the extension driver control signal. When EXT = low, the signal becomes tristate and can suppress consumption current.
V_1 to V_5	5	—	Power supply	Power supply for LCD drive V_{CC} –V_5 = 13 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC_1/OSC_2	2	—	Oscillation resistor clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to $OSC_{1.}$
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci is reference voltage and power supply for the booster. Vci = 2.0 V to 5.0 V ≤ Vci
V_5OUT_2	1	O	V_5 pin/ booster capacitance	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V_5OUT_3	1	O	V_5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitance	External capacitance should be connected here when using the booster.
RESET*	1	I	—	Reset pin. Initialized to “low.”
TEST	1	I	—	Test pin. Should be wired to ground.

Function Description

System Interface

The HD66712 has three types of system interfaces: synchronized serial, 4-bit bus, and 8-bit bus. The serial interface is selected by the IM-pin, and the 4/8-bit bus interface is selected by the DL bit in the instruction register.

The HD66712 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEGRAM). The MPU can only write to IR, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEGRAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEGRAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEGRAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM or CG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEGRAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the registor selector (RS) signal in the 4/8 bit bus interface, and by the RS bit in start byte data in synchronized serial interface (table 2).

Busy Flag (BF)

When the busy flag is 1, the HD66712 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output from DB_7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEGRAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB_0 to DB_6 when RS = 0 and $R/\overline{W}$ = 1 (table 2).

Table 2 Resistor Selection

RS	$R/\overline{W}$	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DD RAM) that is not used for display can be used as general data RAM.

The DD RAM address (A_{DD}) is set in the address counter (AC) as a hexadecimal number, as shown in figure 1.

The relationship between DD RAM addresses and positions on the liquid crystal display is described and shown on the following pages for a variety of cases.

	MSB						LSB
AC	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Example: DD RAM address 4E

1	0	0	1	1	1	0

Figure 1 DD RAM Address

- 1-line display (N = 0, and NW = 0)

  — Case 1: When there are fewer than 80 display characters, the display begins at the beginning of DD RAM. For example, when 24 5-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 2.

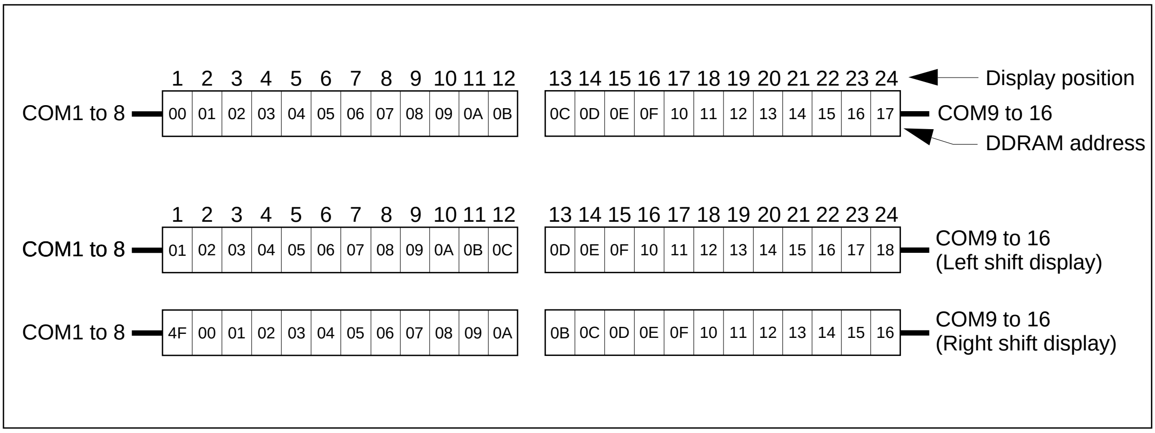
  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

  When 20 6-dot font-width characters are displayed using one HD66712, the display is generated as shown in figure 3. Note that COM9 to COM16 begins at address (0A)H in this case 20 characters are displayed.

  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.

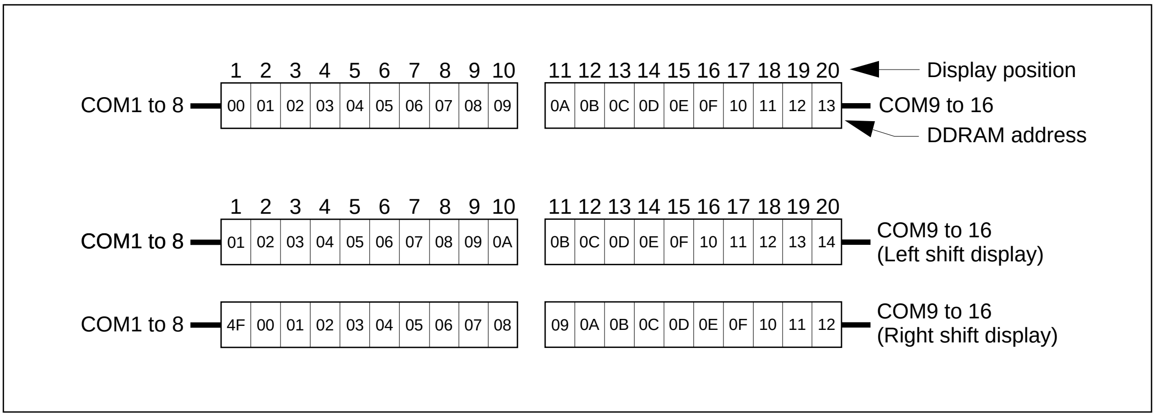
  — Case 2: Figure 4 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to display 24 6-dot font-width characters. In this case, COM9 to COM16 begins at (0A)H.

  When a display shift is performed, the DD RAM addresses shift as well as shown in the figure.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
COM1 to 8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	COM9 to 16
COM1 to 8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	COM9 to 16 (Left shift display)
COM1 to 8	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	COM9 to 16 (Right shift display)

Figure 2 1-Line by 24-Character Display (5-Dot Font Width)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
COM1 to 8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	COM9 to 16
COM1 to 8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	COM9 to 16 (Left shift display)
COM1 to 8	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	COM9 to 16 (Right shift display)

Figure 3 1-Line by 20-Character Display (6-Dot Font Width)

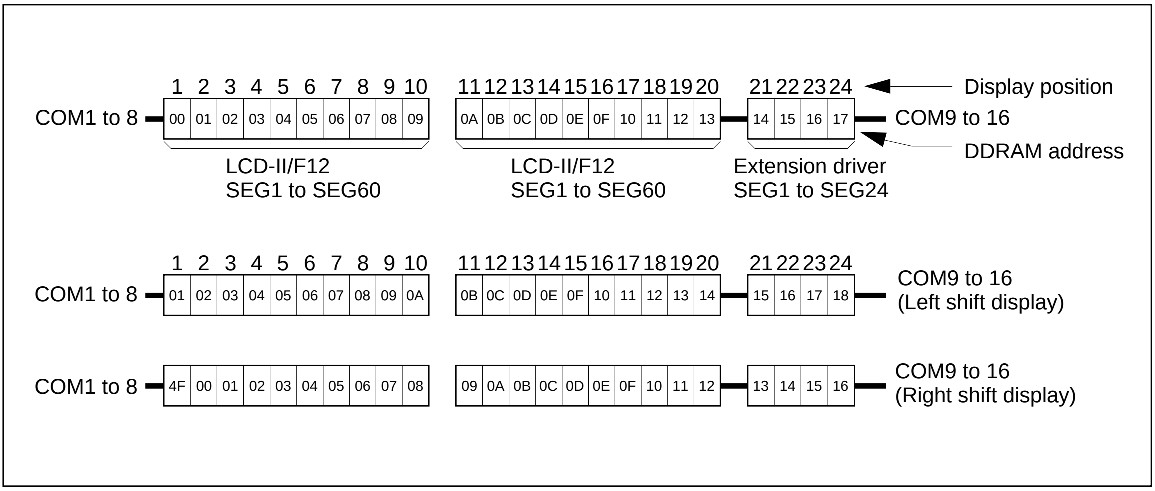
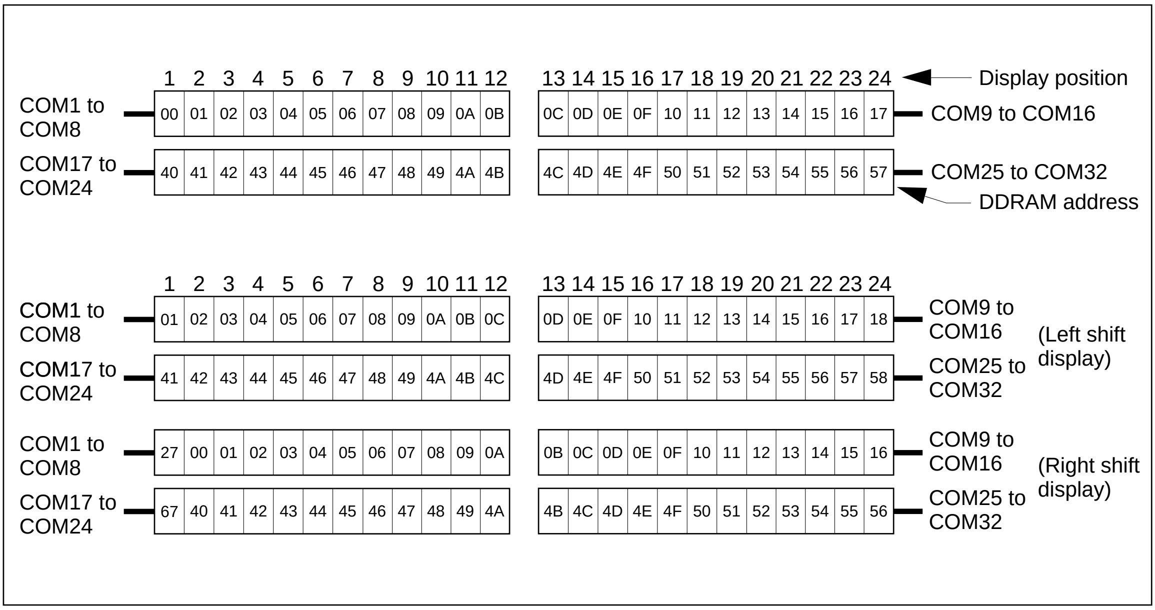

1 2 3 4 5 6 7 8 9 10
11 12 13 14 15 16 17 18 19 20
21 22 23 24
Display position
COM1 to 8
00 01 02 03 04 05 06 07 08 09
0A 0B 0C 0D 0E 0F 10 11 12 13
14 15 16 17
COM9 to 16
DDRAM address
LCD-II/F12
SEG1 to SEG60
LCD-II/F12
SEG1 to SEG60
Extension driver
SEG1 to SEG24
1 2 3 4 5 6 7 8 9 10
11 12 13 14 15 16 17 18 19 20
21 22 23 24
COM1 to 8
01 02 03 04 05 06 07 08 09 0A
0B 0C 0D 0E 0F 10 11 12 13 14
15 16 17 18
COM9 to 16
(Left shift display)
COM1 to 8
4F 00 01 02 03 04 05 06 07 08
09 0A 0B 0C 0D 0E 0F 10 11 12
13 14 15 16
COM9 to 16
(Right shift display)

Figure 4 1-Line by 24-Character Display (6-Dot Font Width)

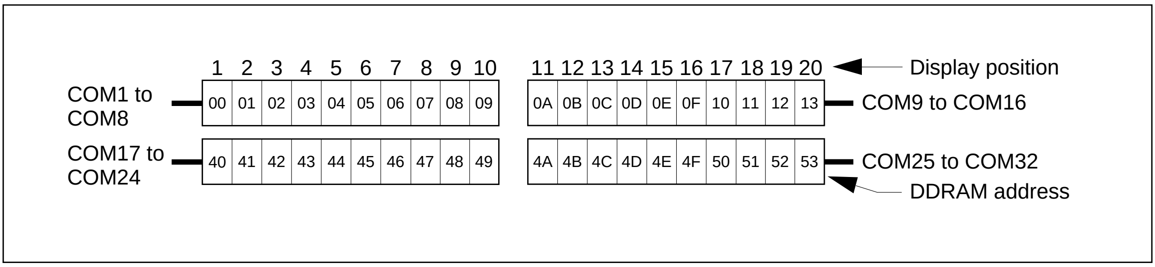
- 2-line display (N = 1, and NW = 0)
  - — Case 1: The first line is displayed from COM1 to COM16, and the second line is displayed from COM17 to COM32. Note that the last address of the first line and the first address of the second line are not consecutive. Figure 5 shows an example where a 5-dot font-width 24 × 2-line display is performed using one HD66712. Here, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H. When a display shift is performed, the DD RAM addresses shift as shown. Figure 6 shows an example where a 6-dot font-width 20 × 2-line display is performed using one HD66712. COM9 to COM16 begins at (0A)H, and COM25 to COM32 at (4A)H.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	COM9 to COM16
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	COM25 to COM32

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		
COM1 to COM8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	COM9 to COM16	(Left shift display)
COM17 to COM24	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	COM25 to COM32	
COM1 to COM8	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	COM9 to COM16	(Right shift display)
COM17 to COM24	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	COM25 to COM32	

Figure 5 2-Line by 24-Character Display (5-Dot Font Width)



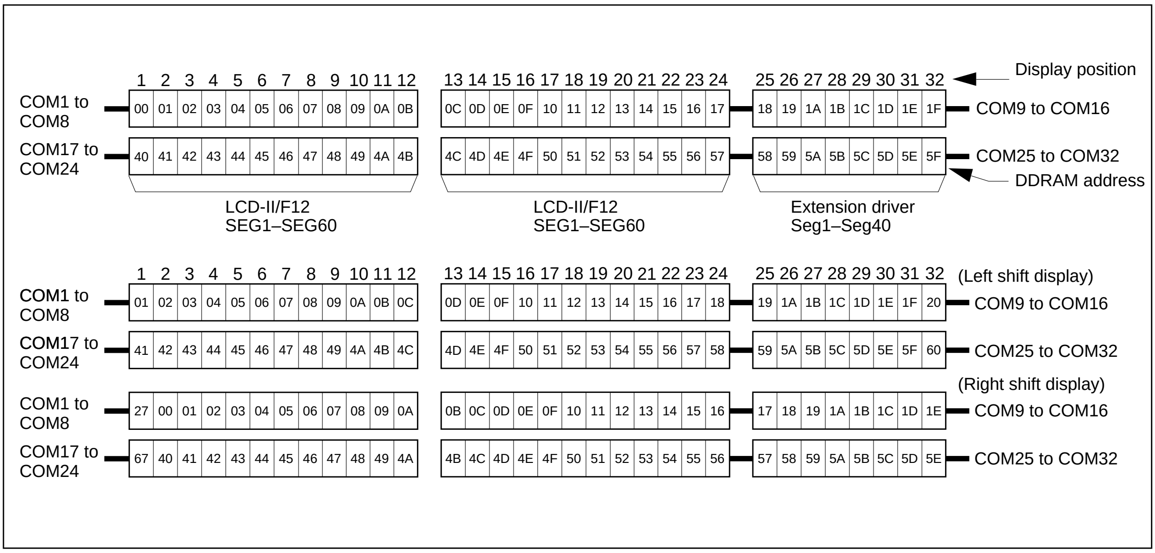
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	COM9 to COM16
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	COM25 to COM32

Figure 6 2-Line by 20-Character Display (6-Dot Font Width)

— Case 2: Figure 7 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters to 32 5-dot font-width characters.

In this case, COM9 to COM16 begins at (0C)H, and COM25 to COM32 at (4C)H.

When a display shift is performed, the DD RAM addresses shift as shown.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	COM9 to COM16
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	COM25 to COM32

(Left shift display)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
COM1 to COM8	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	COM9 to COM16
COM17 to COM24	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	COM25 to COM32

(Right shift display)

COM1 to COM8	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	COM9 to COM16
COM17 to COM24	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	COM25 to COM32

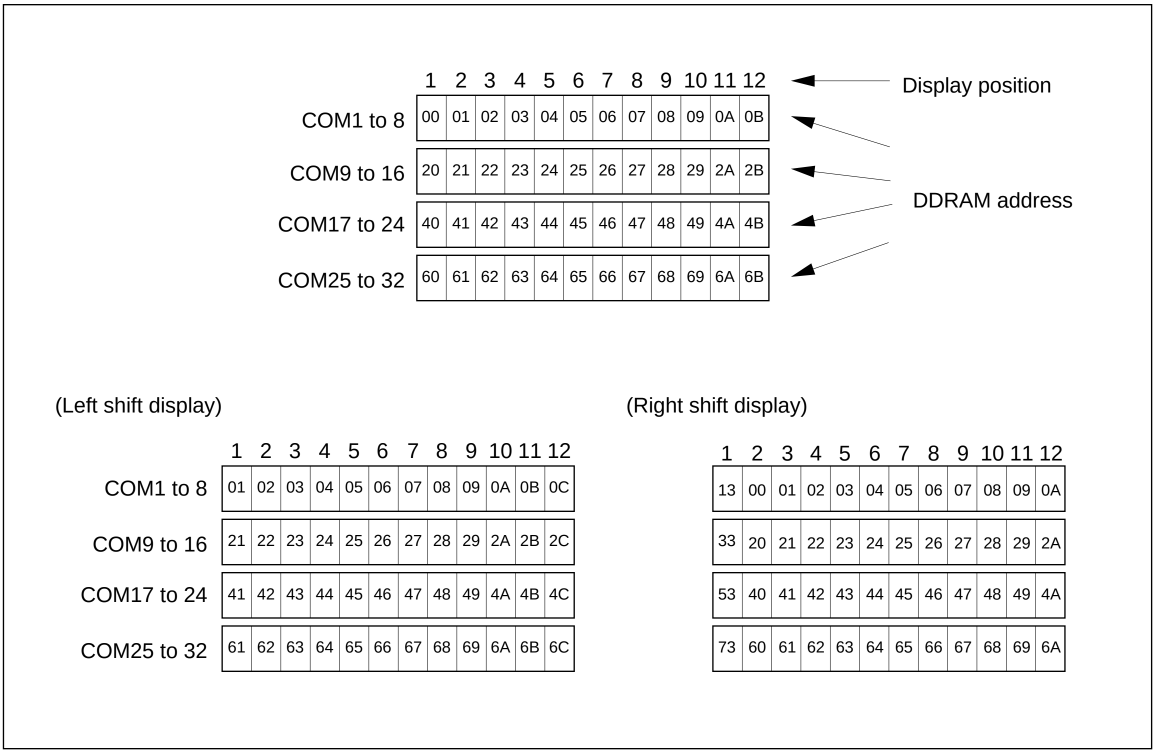
Figure 7 2-Line by 32 Character Display (5-Dot Font Width)

- 4-line display (NW = 1)

  — Case 1: The first line is displayed from COM1 to COM8, the second line is displayed from COM9 to COM16, the third line is displayed from COM17 to COM24, and the fourth line is displayed from COM25 to COM32.

Note that the DD RAM addresses of each line are not consecutive. Figure 8 shows an example where a 12 × 4-line display is performed using one HD66712.

When a display shift is performed, the DD RAM addresses shift as shown.



	1	2	3	4	5	6	7	8	9	10	11	12
COM1 to 8	00	01	02	03	04	05	06	07	08	09	0A	0B
COM9 to 16	20	21	22	23	24	25	26	27	28	29	2A	2B
COM17 to 24	40	41	42	43	44	45	46	47	48	49	4A	4B
COM25 to 32	60	61	62	63	64	65	66	67	68	69	6A	6B

(Left shift display)

	1	2	3	4	5	6	7	8	9	10	11	12
COM1 to 8	01	02	03	04	05	06	07	08	09	0A	0B	0C
COM9 to 16	21	22	23	24	25	26	27	28	29	2A	2B	2C
COM17 to 24	41	42	43	44	45	46	47	48	49	4A	4B	4C
COM25 to 32	61	62	63	64	65	66	67	68	69	6A	6B	6C

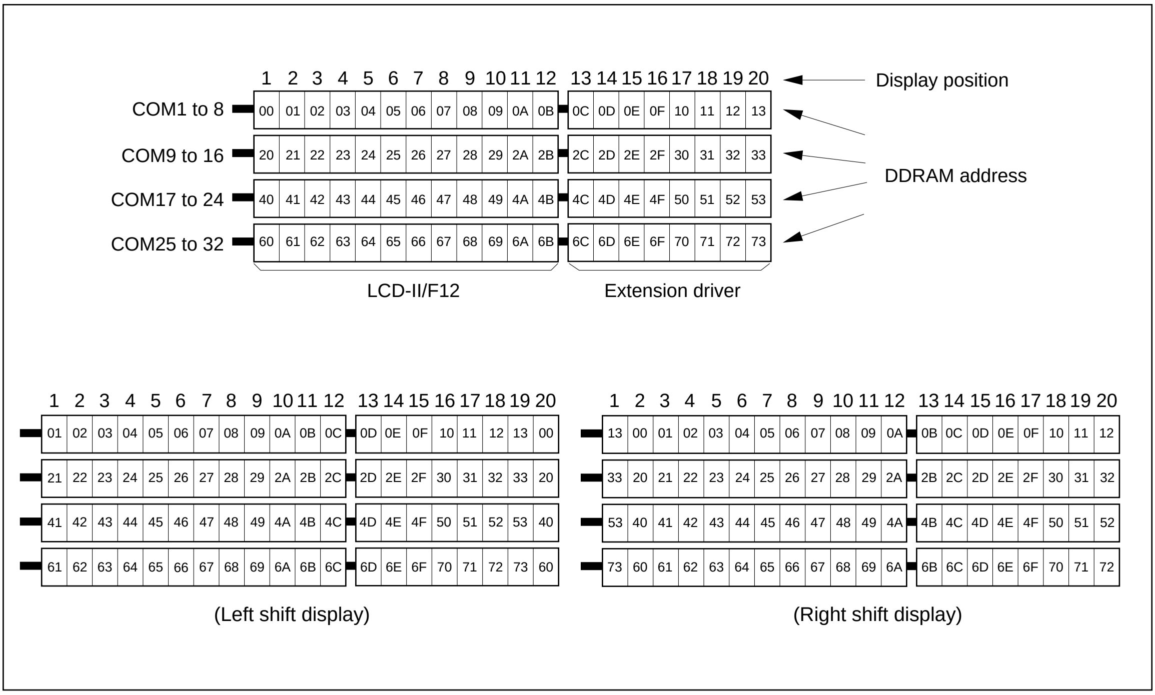
(Right shift display)

1	2	3	4	5	6	7	8	9	10	11	12
13	00	01	02	03	04	05	06	07	08	09	0A
33	20	21	22	23	24	25	26	27	28	29	2A
53	40	41	42	43	44	45	46	47	48	49	4A
73	60	61	62	63	64	65	66	67	68	69	6A

Figure 8 4-Line Display

— Case 2: Figure 9 shows the case where the EXT pin is fixed high and the HD66712 and the 40-output extension driver are used to extend the number of display characters.

When a display shift is performed, the DD RAM addresses shift as shown.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1 to 8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
COM9 to 16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33
COM17 to 24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
COM25 to 32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

(Left shift display)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	00
21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	20
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	40
61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	60

(Right shift display)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
13	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
33	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32
53	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52
73	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72

Figure 9 4-Line by 20-Character Display

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3 to 6). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see "Modifying Character Patterns.")

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 3 to 6 to show the character patterns stored in CG RAM.

See table 7 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to enable control of segments such as an icon and a mark by the user program.

For a 1-line display, SEGRAM is read from the COM0 and the COM17 output, and for 2- or 4-line displays, it is read from the COM0 and the COM33 output, to perform 60-segment display (80-segment display when using the extension driver).

As shown in table 8, bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

SEGRAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 34 common signal drivers and 60 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

Character pattern data is sent serially through a 60-bit shift register and latched when all needed data has arrived. The latched data then enables the driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66712 drives from the head display.

Cursor/Blink Control Circuit

The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

For example (figure 10), when the address counter is (08)H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Scroll Control Circuit

The scroll control circuit is used to perform a smooth-scroll in the unit of dot. When the number of characters to be displayed is greater than that possible at one time on the liquid crystal module, this horizontal smooth scroll can be used to display all characters.

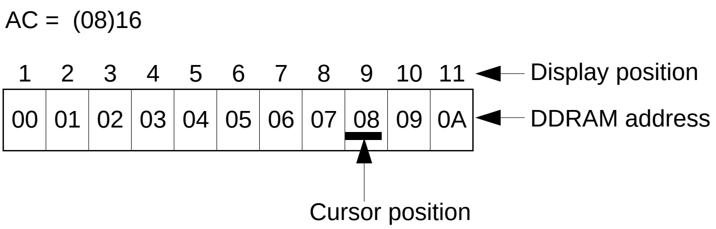
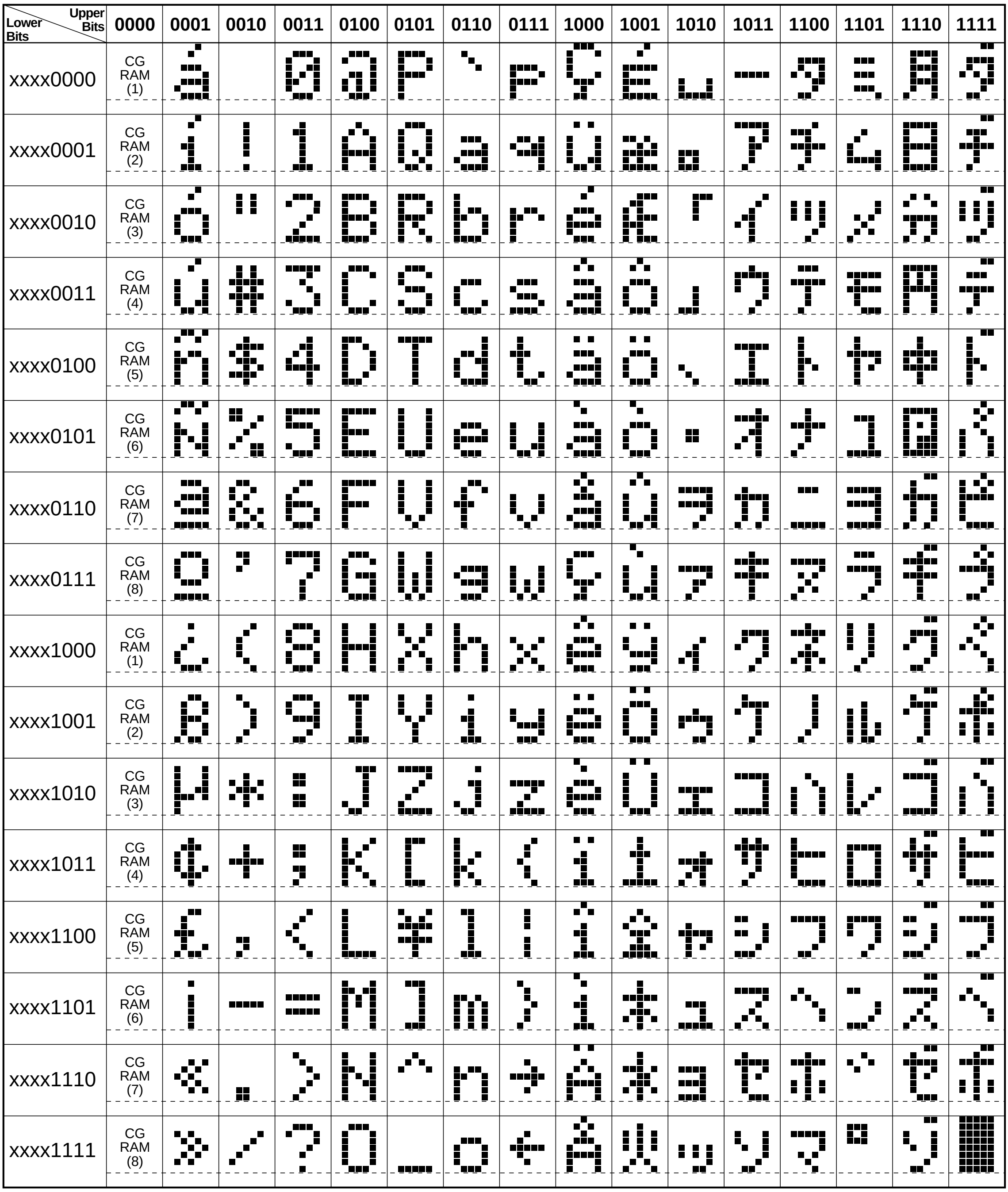

AC = (08)16
1 2 3 4 5 6 7 8 9 10 11
Display position
00 01 02 03 04 05 06 07 08 09 0A
DDRAM address
Cursor position

Figure 10 Cursor/Blink Display Example

Table 3 Relationship between Character Codes and Character Patterns (ROM Code: A00)

Upper Bits Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
xxxx0001	CG RAM (2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
xxxx0010	CG RAM (3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
xxxx0011	CG RAM (4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
xxxx0100	CG RAM (5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
xxxx0101	CG RAM (6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
xxxx0110	CG RAM (7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	CG RAM (8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
xxxx1000	CG RAM (1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
xxxx1001	CG RAM (2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	CG RAM (3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
xxxx1011	CG RAM (4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	CG RAM (5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
xxxx1101	CG RAM (6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
xxxx1110	CG RAM (7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
xxxx1111	CG RAM (8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

Table 4 Relationship between Character Codes and Character Pattern (ROM Code: A01)



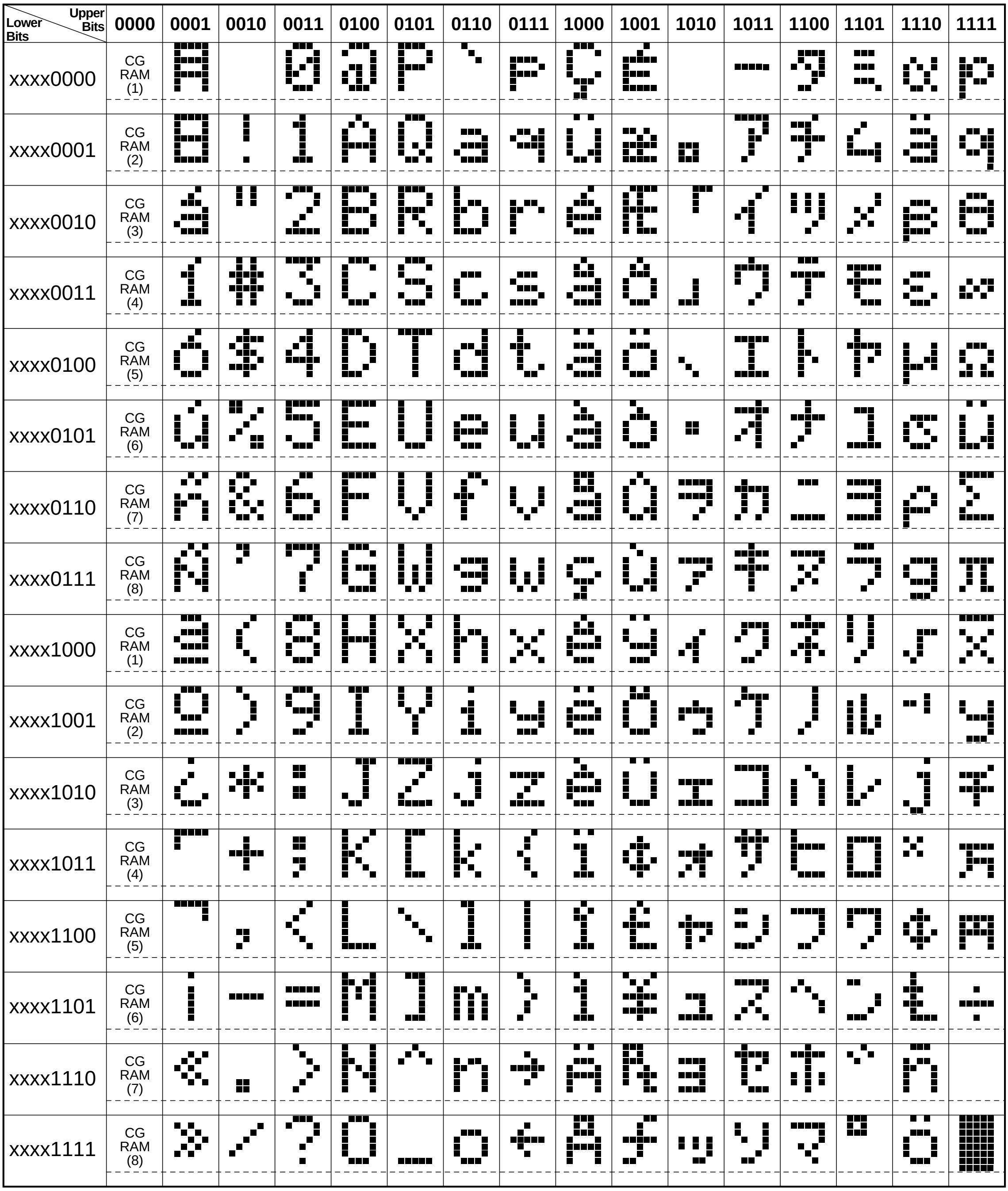
Upper Bits / Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	á		0	@	P	`	p	Ç	É	␣	ー	タ	ミ	月	ダ
xxxx0001	CG RAM (2)	í	!	1	A	Q	a	q	ü	æ	。	ア	チ	ム	日	ヂ
xxxx0010	CG RAM (3)	ó	"	2	B	R	b	r	é	Æ	「	イ	ツ	メ	分	ヅ
xxxx0011	CG RAM (4)	ú	#	3	C	S	c	s	â	ô	」	ウ	テ	モ	円	デ
xxxx0100	CG RAM (5)	ñ	$	4	D	T	d	t	ä	ö	、	エ	ト	ヤ	中	ド
xxxx0101	CG RAM (6)	Ñ	%	5	E	U	e	u	à	ò	・	オ	ナ	ユ	[illegible]	パ
xxxx0110	CG RAM (7)	ª	&	6	F	V	f	v	å	û	ヲ	カ	ニ	ヨ	ガ	ピ
xxxx0111	CG RAM (8)	º	'	7	G	W	g	w	ç	ù	ァ	キ	ヌ	ラ	ギ	プ
xxxx1000	CG RAM (1)	¿	(	8	H	X	h	x	ê	ÿ	ィ	ク	ネ	リ	グ	ペ
xxxx1001	CG RAM (2)	ß	)	9	I	Y	i	y	ë	Ö	ゥ	ケ	ノ	ル	ゲ	ポ
xxxx1010	CG RAM (3)	µ	*	:	J	Z	j	z	è	Ü	ェ	コ	ハ	レ	ゴ	バ
xxxx1011	CG RAM (4)	¢	+	;	K	[	k	{	ï	土	ォ	サ	ヒ	ロ	ザ	ビ
xxxx1100	CG RAM (5)	£	,	<	L	¥	l	|	î	金	ャ	シ	フ	ワ	ジ	ブ
xxxx1101	CG RAM (6)	¡	-	=	M	]	m	}	ì	木	ュ	ス	ヘ	ン	ズ	ベ
xxxx1110	CG RAM (7)	«	.	>	N	^	n	→	Ä	水	ョ	セ	ホ	゛	ゼ	ボ
xxxx1111	CG RAM (8)	»	/	?	O	_	o	←	Å	火	ッ	ソ	マ	゜	ゾ	█

Table 5 Relationship between Character Codes and Character Patterns (ROM Code: A02)

Upper Bits Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	▶		0	@	P	`	p	Б	α	‖	°	À	Ð	à	ð
xxxx0001	CG RAM (2)	◀	!	1	A	Q	a	q	Д	♪	¡	±	Á	Ñ	á	ñ
xxxx0010	CG RAM (3)	“	"	2	B	R	b	r	Ж	Γ	¢	²	Â	Ò	â	ò
xxxx0011	CG RAM (4)	”	#	3	C	S	c	s	З	π	£	³	Ã	Ó	ã	ó
xxxx0100	CG RAM (5)	⏫	$	4	D	T	d	t	И	Σ	¤	₧	Ä	Ô	ä	ô
xxxx0101	CG RAM (6)	⏬	%	5	E	U	e	u	Й	σ	¥	µ	Å	Õ	å	õ
xxxx0110	CG RAM (7)	●	&	6	F	V	f	v	Л	♬	¦	¶	Æ	Ö	æ	ö
xxxx0111	CG RAM (8)	↵	'	7	G	W	g	w	П	τ	§	·	Ç	×	ç	÷
xxxx1000	CG RAM (1)	↑	(	8	H	X	h	x	У	🔔	ƒ	ω	È	Φ	è	φ
xxxx1001	CG RAM (2)	↓	)	9	I	Y	i	y	Ц	Θ	©	¹	É	Ù	é	ù
xxxx1010	CG RAM (3)	→	*	:	J	Z	j	z	Ч	Ω	ª	º	Ê	Ú	ê	ú
xxxx1011	CG RAM (4)	←	+	;	K	[	k	{	Ш	δ	«	»	Ë	Û	ë	û
xxxx1100	CG RAM (5)	≤	,	<	L	\	l	|	Щ	∞	Ю	¼	Ì	Ü	ì	ü
xxxx1101	CG RAM (6)	≥	-	=	M	]	m	}	Ъ	♥	Я	½	Í	Ý	í	ý
xxxx1110	CG RAM (7)	▲	.	>	N	^	n	~	Ы	ε	®	¾	Î	Þ	î	þ
xxxx1111	CG RAM (8)	▼	/	?	O	_	o	⌂	Э	∩	‘	¿	Ï	ß	ï	ÿ

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

Table 6 Relationship between Character Codes and Character Pattern (ROM Code: A03)



Upper Bits / Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)	月		0	@	P	`	p	Ç	É		ー	タ	ミ	α	p
xxxx0001	CG RAM (2)	日	!	1	A	Q	a	q	ü	æ	。	ア	チ	ム	ä	q
xxxx0010	CG RAM (3)	á	"	2	B	R	b	r	é	Æ	「	イ	ツ	メ	β	θ
xxxx0011	CG RAM (4)	í	#	3	C	S	c	s	â	ô	」	ウ	テ	モ	ε	∞
xxxx0100	CG RAM (5)	ó	$	4	D	T	d	t	ä	ö	、	エ	ト	ヤ	μ	Ω
xxxx0101	CG RAM (6)	ú	%	5	E	U	e	u	à	ò	・	オ	ナ	ユ	σ	ü
xxxx0110	CG RAM (7)	ñ	&	6	F	V	f	v	å	û	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	CG RAM (8)	Ñ	'	7	G	W	g	w	ç	ù	ァ	キ	ヌ	ラ	g	π
xxxx1000	CG RAM (1)	ª	(	8	H	X	h	x	ê	ÿ	ィ	ク	ネ	リ	√	x̄
xxxx1001	CG RAM (2)	º	)	9	I	Y	i	y	ë	Ö	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	CG RAM (3)	¿	*	:	J	Z	j	z	è	Ü	ェ	コ	ハ	レ	j	千
xxxx1011	CG RAM (4)	⌐	+	;	K	[	k	{	ï	¢	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	CG RAM (5)	¬	,	<	L	\	l	|	î	£	ャ	シ	フ	ワ	¢	円
xxxx1101	CG RAM (6)	¡	-	=	M	]	m	}	ì	¥	ュ	ス	ヘ	ン	Ł	÷
xxxx1110	CG RAM (7)	«	.	>	N	^	n	→	Ä	₧	ョ	セ	ホ	゛	ñ	
xxxx1111	CG RAM (8)	»	/	?	O	_	o	←	Å	ƒ	ッ	ソ	マ	゜	ö	█

Table 7 Example of Relationships between Character Code (DDRAM) and Character Pattern(CGRAM Data)

a) When character pattern is 5 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
			↓						↓		0	0	1		↓		1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
			↓						↓		0	0	1		↓		1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

a) When character pattern is 6 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
			↓						↓		0	0	1		↓	0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
			↓						↓		0	0	1		↓	0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.

3. The character data is stored with the rightmost character element in bit 0, as shown in the figure above. Characters of 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters of 6 dots in width (FW = 1) are stored in bits 0 to 5.

4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected.

Bit 3 of the character code is invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.

5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.

6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CGRAM.

When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display.

When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

* Indicates no effect.

Table 8 Relationship between SEGRAM Addresses and Display Patterns

SEGRAM address				SEGRAM data															
				a) 5-dot font width								b) 6-dot font width							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	*	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	*	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	*	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	*	S56	S7	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	*	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	*	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	*	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	*	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96
				Blinking control			Pattern on/off					Blinking control		Pattern on/off					

Notes:
1. Data set to SEGRAM is output when COM0 and COM17 are selected, as for a 1-line display, and output when COM0 and COM33 are selected, as for a 2-line or a 4-line display. COM0 and COM17 for a 1-line display and COM0 and COM33 for a 2-line or a 4-line display are the same signals.
2. S1 to S96 are pin numbers of the segment output driver. S1 is positioned to the left of the display. When the LCD-II/F12 is used by one chip, segments from S1 to S60 are displayed. An extension driver displays the segments after S61.
3. After S80 output at 5-dot font and S96 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on.off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEGRAM.

   When bit 7 is 1, only a bit set to “1” of the lower six bits is blinked on the display.

   When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the SEGRAM data correspond to display selection, and zeros to non-selection.

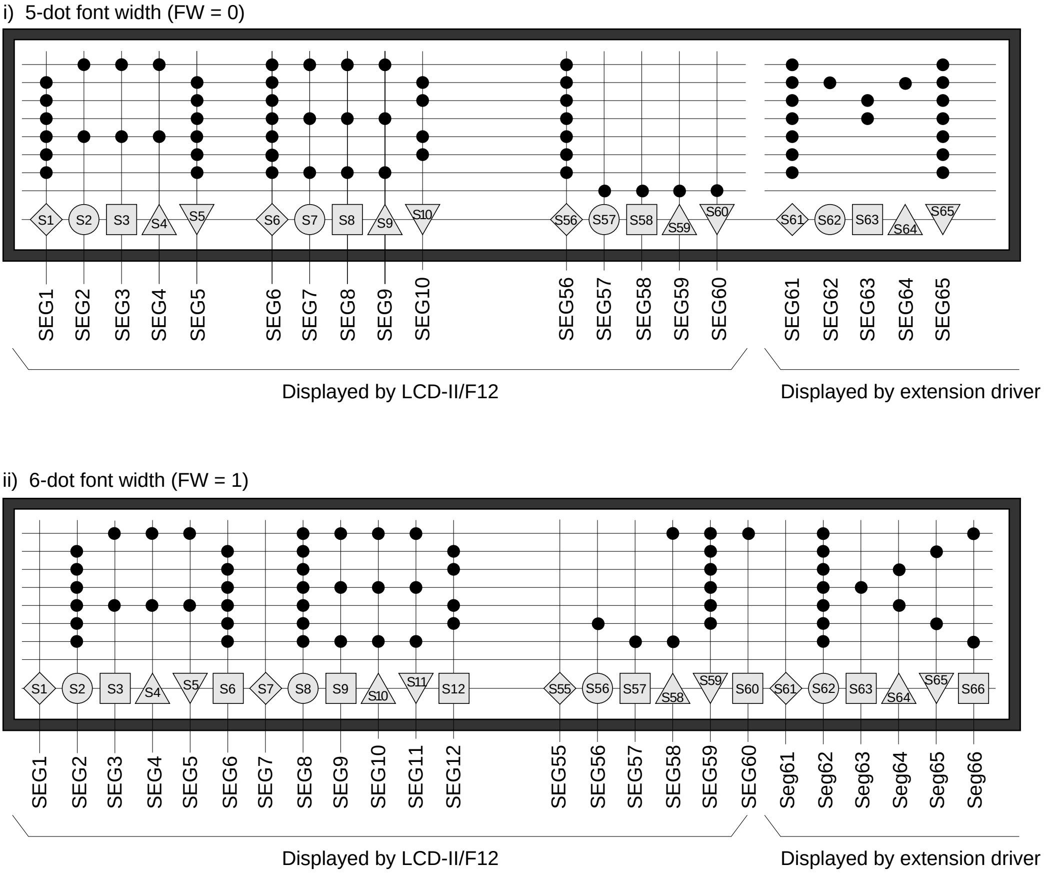

i) 5-dot font width (FW = 0)
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S56
S57
S58
S59
S60
S61
S62
S63
S64
S65
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG56
SEG57
SEG58
SEG59
SEG60
SEG61
SEG62
SEG63
SEG64
SEG65
Displayed by LCD-II/F12
Displayed by extension driver
ii) 6-dot font width (FW = 1)
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S55
S56
S57
S58
S59
S60
S61
S62
S63
S64
S65
S66
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG55
SEG56
SEG57
SEG58
SEG59
SEG60
Seg61
Seg62
Seg63
Seg64
Seg65
Seg66
Displayed by LCD-II/F12
Displayed by extension driver

Figure 11 Correspondence between SEGRAM and Segment Display

Modifying Character Patterns

- Character pattern development procedure

  The following operations correspond to the numbers listed in figure 12:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

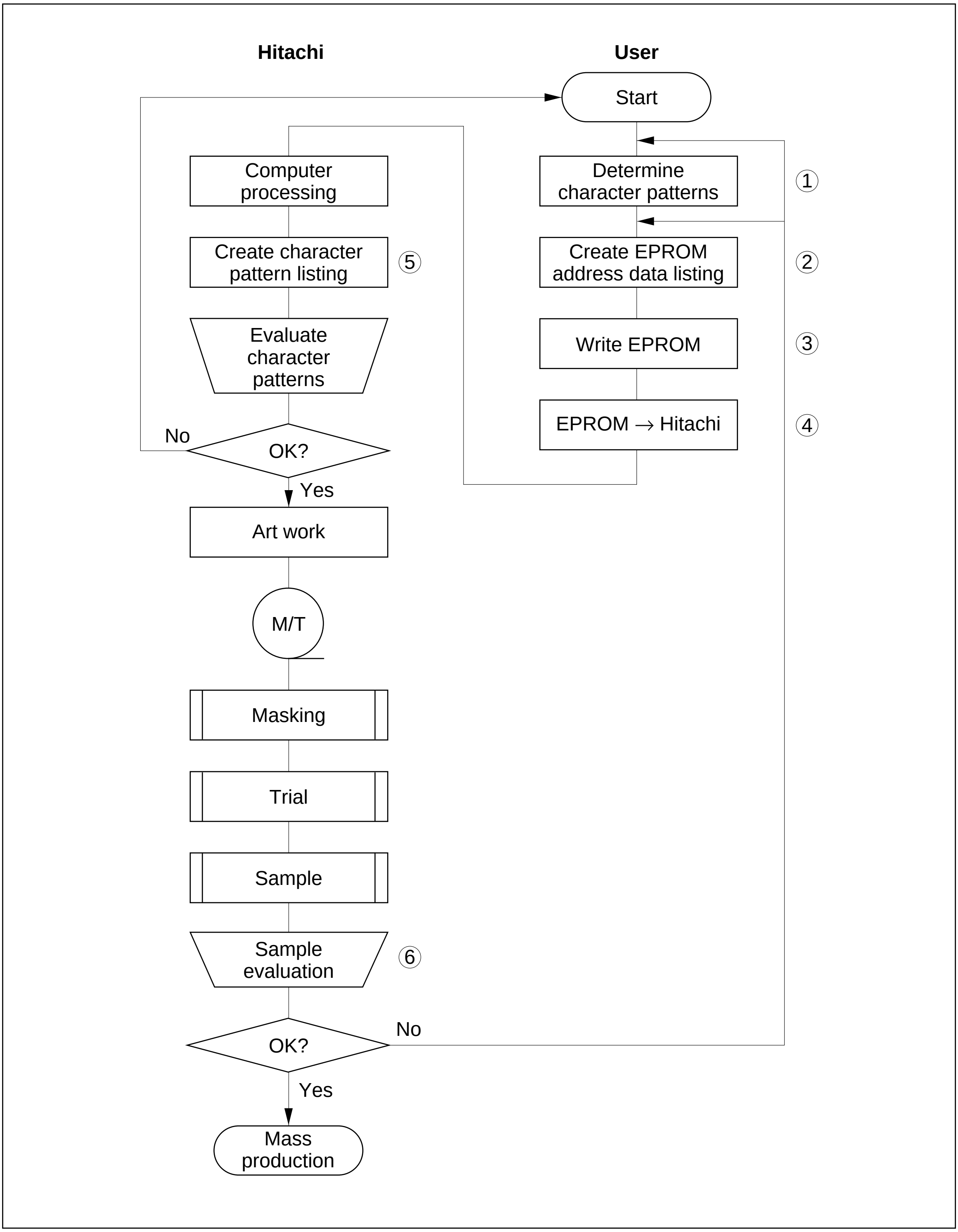

Hitachi
User
Start
Computer processing
Determine character patterns
①
Create character pattern listing
⑤
Create EPROM address data listing
②
Evaluate character patterns
Write EPROM
③
EPROM → Hitachi
④
No
OK?
Yes
Art work
M/T
Masking
Trial
Sample
Sample evaluation
⑥
OK?
No
Yes
Mass production

Figure 12 Character Pattern Development Procedure

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

- Programming to EPROM

  The HD66712 character generator ROM can generate 240 5 × 8 dot character patterns. Table 9 shows correspondence between the EPROM address data and the character pattern.

Handling Unused Character Patterns

1. EPROM data outside the character pattern area: This is ignored by the character generator ROM for display operation so any data is acceptable.
2. EPROM data in CG RAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66712 EPROM: According to the user application, these are handled in either of two ways:
   - a When unused character patterns are not programmed: If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   - b When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 9 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)

EPROM Address												MSB		Data		LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0

Character code "0" Line position

Notes: 1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify the line position of the character pattern. EPROM address A3 should be set to "0."
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as "1," and unlit areas as "0."
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits 0_7 to 0_5 are invalid. 0 should be written in all bits.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66712 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the V_{CC} rises to 2.7 V.

1. Display clear:
   (20)H to all DDRAM

2. Set functions:
   DL = 1: 8-bit interface data
   N = 1: 2-line display
   RE = 0: Extension register write disable
   BE = 0: CGRAM/SEGRAM blink off
   LP = 0: Not in low power mode

3. Control display on/off:
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blinking off

4. Set entry mode:
   I/D = 1: Increment by 1
   S = 0: No shift

5. Set extension function:
   FW = 0: 5-dot character width
   B/W = 0: Normal cursor (eighth line)
   NW = 0: 1- or 2-line display (depending on N)

6. Enable scroll:
   HSE = 0000: Scroll unable

7. Set scroll amount:
   HDS = 000000: Not scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66712.

Initializing by Hardware Reset Input

The LCD-II/F12 also has a reset input pin: RESET*. If this pin is made low during operation, an internal reset and initialization is performed. This pin is ignored, however, during the internal reset period at power-on.

Interfacing to the MPU

The HD66712 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB_0 to DB_3 are disabled. The data transfer between the HD66712 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

- For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

- When the IM pin is low, the HD66712 uses a serial interface. See “Transferring Serial Data.”

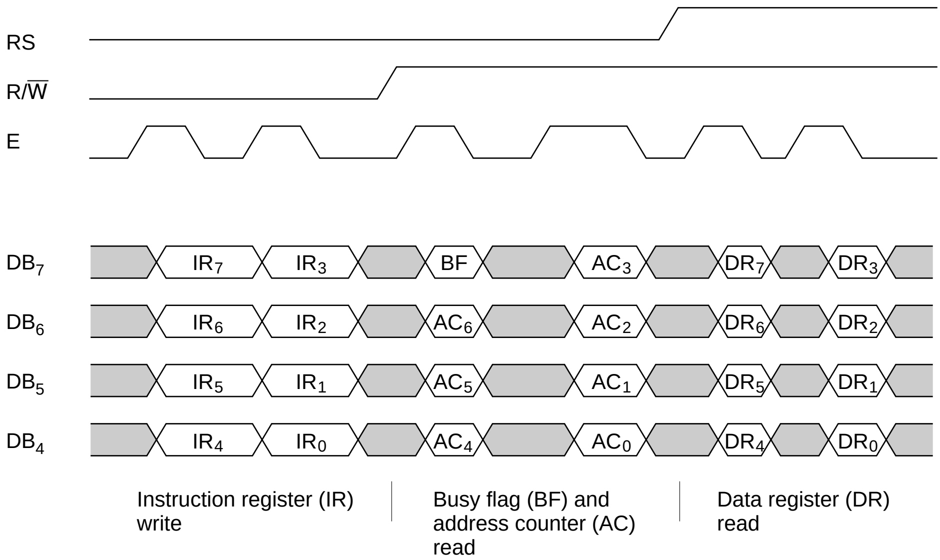

RS
R/$\overline{W}$
E
DB_7
DB_6
DB_5
DB_4
IR_7
IR_3
BF
AC_3
DR_7
DR_3
IR_6
IR_2
AC_6
AC_2
DR_6
DR_2
IR_5
IR_1
AC_5
AC_1
DR_5
DR_1
IR_4
IR_0
AC_4
AC_0
DR_4
DR_0
Instruction register (IR) write
Busy flag (BF) and address counter (AC) read
Data register (DR) read

Figure 13 4-Bit Transfer Example

Transferring Serial Data

When the IM pin (interface mode) is low, the HD66712 enters serial interface mode. A three-line clock-synchronous transfer method is used. The HD66712 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66712 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the LCD-II/F12 can be reset and serial transfer synchronized by making chip select (CS*) high.

Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In the case of a minimum 1 to 1 transfer system with the LCD-II/F12 used as a receiver only, an interface can be established by the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS*) should be fixed to low.

The transfer clock (SCLK) is independent from operational clock (CLK) of the LCD-II/F12. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see continuous transfer) must be considered since the LCD-II/F12 does not have an internal transmit/receive buffer.

To begin with, transfer the start byte. By receiving five consecutive bits (synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCD-II/F12 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/$\overline{\text{W}}$ bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail below.

- Receiving (write)

  After receiving the start synchronization bits, the R/$\overline{\text{W}}$ bit (= 0), and the RS bit with the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are continuously received with R/$\overline{\text{W}}$ bit and RS bit unchanged, continuous transfer is possible (see “Continuous Transfer” below).

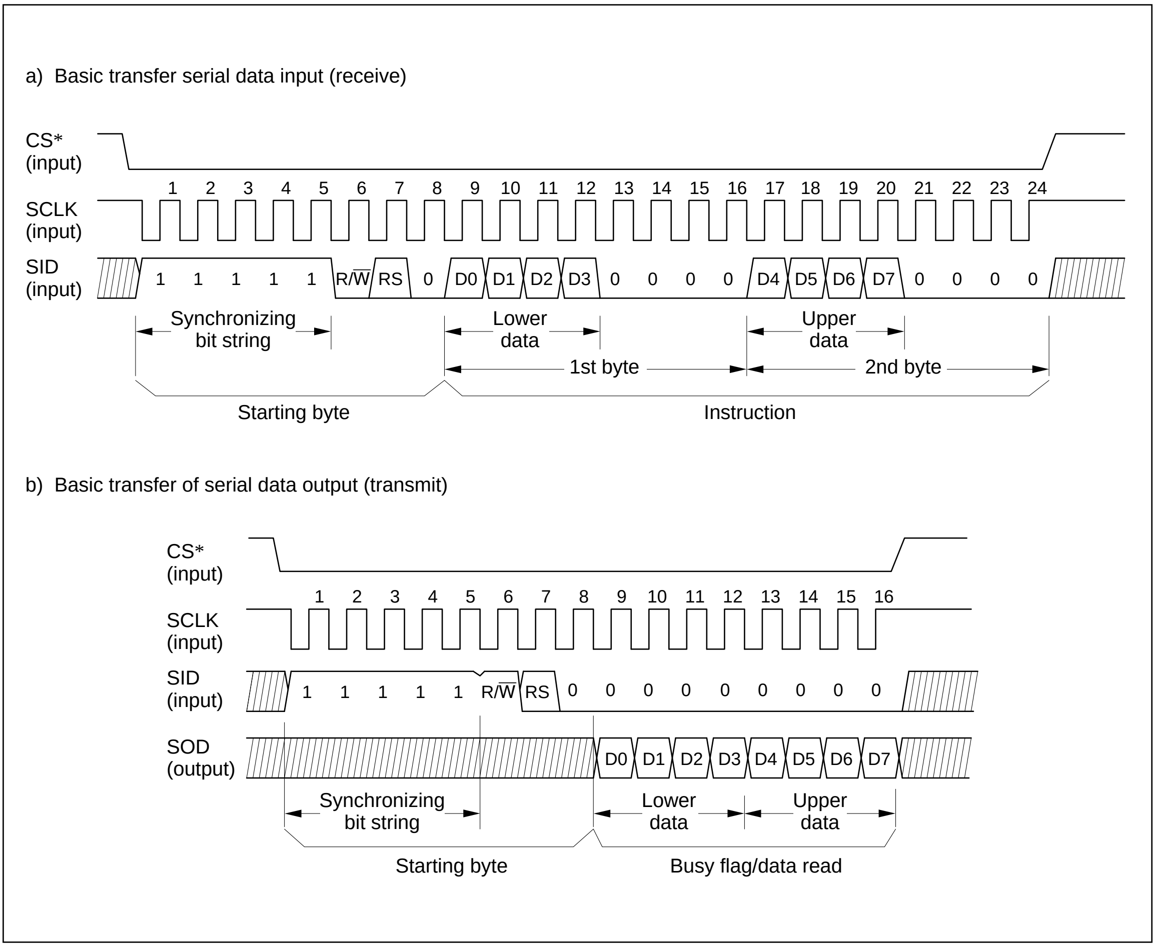

a) Basic transfer serial data input (receive)
CS*
(input)
SCLK
(input)
SID
(input)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
1 1 1 1 1 R/W̄ RS 0 D0 D1 D2 D3 0 0 0 0 D4 D5 D6 D7 0 0 0 0
Synchronizing bit string
Lower data
Upper data
1st byte
2nd byte
Starting byte
Instruction
b) Basic transfer of serial data output (transmit)
CS*
(input)
SCLK
(input)
SID
(input)
SOD
(output)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
1 1 1 1 1 R/W̄ RS 0 0 0 0 0 0 0 0 0
D0 D1 D2 D3 D4 D5 D6 D7
Synchronizing bit string
Lower data
Upper data
Starting byte
Busy flag/data read

Figure 14 Basic Procedure for Transferring Serial Data

- Transmitting (read)

  After receiving the start synchronization bits, the R/$\overline{W}$ bit (= 1), and the RS bit with the start byte, 8-bit read data is transmitted in the same way as receiving. When read data is continuously transmitted with R/$\overline{W}$ bit and RS bit unchanged, continuous transfer is possible (see “Continuous Transfer” below).

  Even at the time of the transmission (the data output), since the HD66712 monitors the start synchronization bit string (“11111”) by the SID input, the HD66712 receives the R/W bit and RS bit after detecting the start synchronization. Therefore, in the case of a continuous transfer, fix the SID input “0.”

- Continuous transfer

  When instructions are continuously received with the R/$\overline{W}$ bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

  After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it.

  To execute the next instruction, the instruction execution time of the LCD-II/F12 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

  In addition, if the next unit of data is read before read execution of previous data is completed for busy flag/address counter/RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, it is possible to transfer without reading the busy flag if wiring for transmission (SOD pin) needs to be reduced or if the burden of polling on the CPU needs to be removed. In this case, insert a transfer wait so that the current instruction first completes execution during instruction transfer.

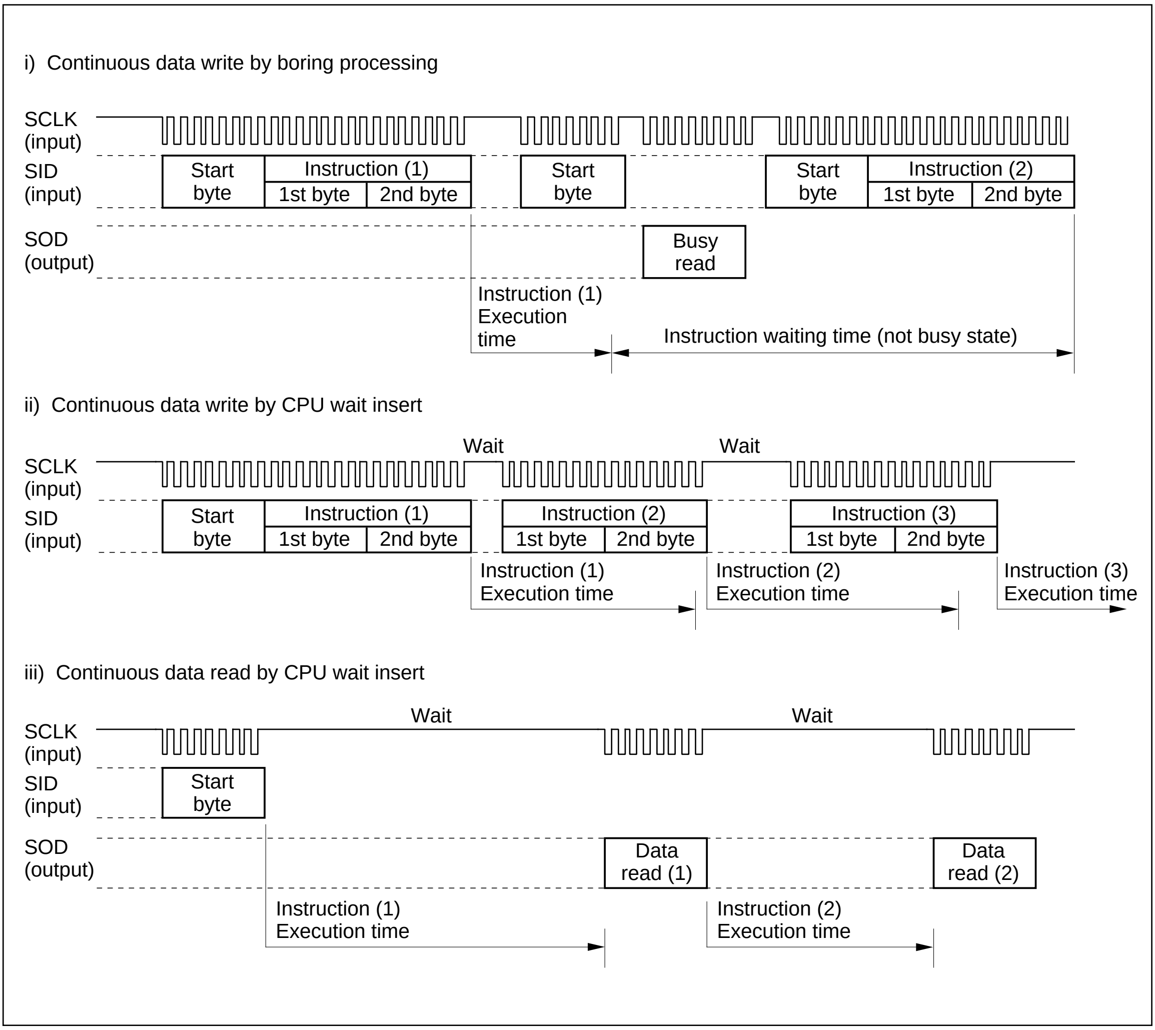

i) Continuous data write by boring processing
SCLK (input)
SID (input)
Start byte
Instruction (1)
1st byte
2nd byte
Start byte
Start byte
Instruction (2)
1st byte
2nd byte
SOD (output)
Busy read
Instruction (1) Execution time
Instruction waiting time (not busy state)
ii) Continuous data write by CPU wait insert
Wait
Wait
SCLK (input)
SID (input)
Start byte
Instruction (1)
1st byte
2nd byte
Instruction (2)
1st byte
2nd byte
Instruction (3)
1st byte
2nd byte
Instruction (1) Execution time
Instruction (2) Execution time
Instruction (3) Execution time
iii) Continuous data read by CPU wait insert
Wait
Wait
SCLK (input)
SID (input)
Start byte
SOD (output)
Data read (1)
Data read (2)
Instruction (1) Execution time
Instruction (2) Execution time

Figure 15 Procedure for Continuous Data Transfer

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66712 can be controlled by the MPU. Before starting internal operation of the HD66712, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66712 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write (R/$\overline{\text{W}}$), and the data bus (DB_0 to DB_7), make up the HD66712 instructions (table 12). There are four categories of instructions that:

- Designate HD66712 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66712 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 10) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66712 is not in the busy state (BF = 1) before sending an instruction from the MPU to the HD66712. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 12 for the list of each instruction execution time.

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). In addition, flicker may occur in a moment at the time of this instruction issue.

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. In a low power mode (LP = 1), do not set S = 1 because the whole display does not normally shift.

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all blank dots and displayed characters at a speed of 370-ms intervals when f_{cp} or f_{OSC} is 270 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to f_{OSC} or the reciprocal of f_{cp}. For example, when f_{cp} is 300 kHz, 370 × 270/300 = 333 ms.)

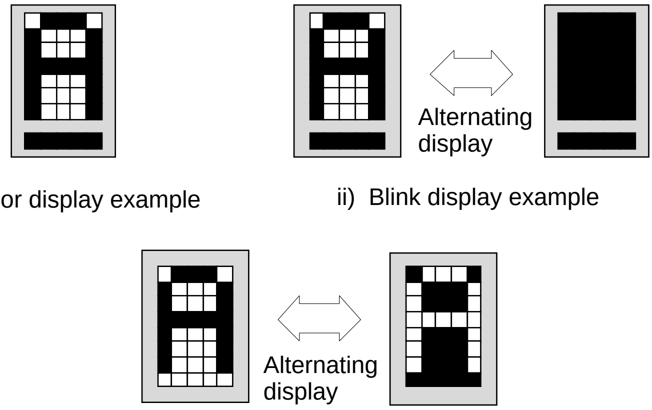
Extended Function Set

When the extended register enable bit (RE) is 1, FW, B/W, and NW bit shown below are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the left most bit, and the font is displayed with a 5-bit character width. If the FW bit is changed, data in DD RAM and CG RAM SEG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See “Oscillator Circuit” for details.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white inversion. At this time, bits C and B in display on/off control register are “Don’t care.” When f_{CP} or f_{OSC} is 270 kHz, display is changed by switching every 370 ms.

NW: When NW is 1, 4-line display is performed. At this time, bit N in the function set register is “Don’t care.”

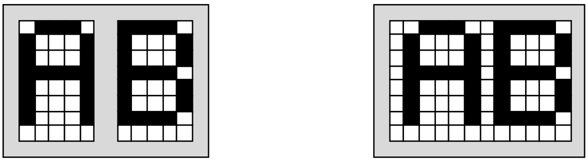


i) Cursor display example

ii) Blink display example

iii) White-black inverting display example

a) Cursor blink width control



i) 5-dot character width

ii) 6-dot character width

b) Font width control

Figure 16 Example of Display Control

Cursor or Display Shift

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 10). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. In a 4-line display, the cursor moves to the second line when it passes the 20th character of the line. Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position. When this instruction is executed, extended register enable bit (RE) is reset.

The address counter (AC) contents will not change if the only action performed is a display shift. In low power mode (LP = 1), whole-display shift cannot be normally performed.

Scroll Enable

When extended register enable bit (RE) is 1, scroll enable bits can be set.

This HSE resister specifies scrolled line with the scroll quantity register. This register consists of 4 bits for each display line, so a specified line can be shifted by dot unit. When the bit 0 of HSE is 1 in four line mode (NW = 1), the first line can be shifted, and the bit 1 is specified to shift the second line, the bit 2 is specified for the third line, and bit 3 is specified for the fourth line. When it shifts the first line in two line mode (N = 1, NW = 0), both the bit 0 and bit 1 should be set to 1. The bit 2 and bit 3 is specified for the second line.

In 1 line mode (N = 0, NW = 0), the bit 0 and bit 1 should be specified.

Function Set

Only when the extended register enable bit (RE) is 1, the BE and the LP bits shown below can be accessed. Bits DL and N can be accessed regardless of RE.

DL: Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0. When 4-bit length is selected, data must be sent or received twice.

N: When bit NW in the extended function set is 0, a 1- or a 2-line display is set. When N is 0, 1-line display is selected; when N is 1, 2-line display is selected. When NW is 1, a 4-line display is set. At this time, N is “Don’t care.”

Note: After changing the N or NW or LP bit, please issue the Return Home or Clear Display instruction to cancel to shift display.

RE: When bit RE is 1, bit BE in the extended function set register, the SEGRAM address set register, and the function set register can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

To maintain compatibility with the HD44780, the RE bit should be fixed to 0.

Table 10 Shift Function

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

BE: When the RE bit is 1, this bit can be rewritten. When this bit is 1, the user font in CGRAM and the segment in SEGRAM can be blinked according to the upper two bits of CGRAM and SEGRAM.

LP: When bit RE is 1, this bit can be rewritten. When LP is set to 1 and the EXT pin is low (without an extended driver), the HD66712 operates in low power mode. In 1-line display mode, the HD66712 operates on a 4-division clock, and in a 2-line or a 4-line display mode, the HD66712 operates on a 2-division clock. According to these operations, instruction execution takes four times or twice as long. Note that in low power mode, display shift cannot be performed. The frame frequency is reduced to 5/6 that of normal operation. See “Oscillator Circuit” for details.

Note: Perform the DL, N, NW, and FW fucntions at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, if bits N, NW, or FW are changed after other instructions are executed, RAM contents may be broken.

Set CG RAM Address

A CG RAM address can be set while the RE bit is cleared to 0.

Set CG RAM address into the address counter displayed by binary AAAAAA. After this address set, data is written to or read from the MPU for CG RAM.

Set SEGRAM Address

Only when the extended register enable (RE) bit is 1, HS2 to HS0 and the SEGRAM address can be set.

The SEGRAM address in the binary form AAAA is set to the address counter. After this address set, SEGRAM can be written to or read from by the MPU.

Set DD RAM Address

A DD RAM address can be set while the RE bit is cleared to 0. Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

After this address set, data is written to or read from the MPU for DD RAM.

However, when N and NW is 0 (1-line display), AAAAAAA can be (00)H to (4F)H. When N is 1 and NW is 0 (2-line display), AAAAAAA is (00)H to (27)H for the first line, and (40)H to (67)H for the second line. When NW is 1 (4-line display), AAAAAAA is (00)H to (13)H for the first line, (20)H to (33)H for the second line, (40)H to (53)H for the third line, and (60)H to (73)H for the fourth line.

Set Scroll Quantity

When extended registor enable bit (RE) is 1, HDS5 to HDS0 can be set.

HDS5 to HDS0 specifies horizontal scroll quantity to the left of the display in dot units. The HD66712 uses the unused DDRAM area to execute a desired horizontal smooth scroll from 1 to 48 dots.

Note: When performing a horizontal scroll as described above by connecting an extended driver, the maximum number of characters per line decreases by the quantity set by the above horizontal scroll. For example, when the maximum 24-dot scroll quantity (4 characters) is used with 6-dot font width and 4-line display, the maximum numbers of characters is 20 – 4 = 16. Notice that in low power mode (LP = 1), display shift and scroll cannot be performed.

Read Busy Flag and Address

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG, DD, and SEGRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for CG RAM, DD RAM, and SEGRAM address set instructions.

Write Data to CG, DD, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG, DD or SEGRAM. CG, DD or SEGRAM is selected by the previous specification of the address set instruction (CG RAM address set / DD RAM address set / SEGRAM address set). After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG, DD, or SEG RAM. CG, DD or SEGRAM is selected by the previous specification of the address set instruction. If no address is specified, the first data read will be invalid. When executing serial read instructions, the next address is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

Table 11 HS5 to HS0 Settings

HDS5	HDS4	HDS3	HDS2	HDS1	HDS0	Description
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift the display position to the left by one dot.
0	0	0	0	1	0	Shift the display position to the left by two dots.
0	0	0	0	1	1	Shift the display position to the left by three dots.
				⋮		
1	0	1	1	1	1	Shift the display position to the left by forty-seven dots.
1	1	*	*	*	*	Shift the display position to the left by forty-eight dots.

Table 12 Instructions

Instruction	RE Bit	Code										Description	Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0/1	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.52 ms
Return home	0/1	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 IN address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0/1	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Extension function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Sets a font width, a black-white inverting cursor (B/W), and a 4-line display (NW).	37 µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	37 µs
Scroll enable	1	0	0	0	0	0	1	HSE	HSE	HSE	HSE	Specifies which display lines to undergo horizontal smooth scroll.	37 µs
Function set	0	0	0	0	0	1	DL	N	RE	—	—	Sets interface data length (DL), number of display lines (L), and extension register write enable (RE).	37 µs
	1	0	0	0	0	1	DL	N	RE	BE	LP	Sets CGRAM/SEGRAM blinking enable (BE), and power-down mode (LP). LP is available when the EXT pin is low.	37 µs
Set CGRAM address	0	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	37 µs
Set SEGRAM address set	1	0	0	0	1	*	*	A_{SEG}	A_{SEG}	A_{SEG}	A_{SEG}	Sets SEGRAM address. SEGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	0	1	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	37 µs
Set scroll quantity	1	0	0	1	*	HDS	HDS	HDS	HDS	HDS	HDS	Sets horizontal dot scroll quantity.	37 µs

Table 12 Instructions (cont)

		Code											
Instruction	**RE Bit**	**RS**	**R/W**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	**Description**	**Execution Time (Max) (when f_{cp} or f_{OSC} is 270 kHz)**
Read busy flag & address	0/1	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write data to RAM	0/1	1	0			Write data						Writes data into DD RAM, CG RAM, or SEGRAM.	7 µs t_{ADD} = 5.5 µs*
Read data from RAM	0/1	1	1			Read data						Reads data from DD RAM, CG RAM, or SEGRAM.	37 µs t_{ADD} = 5.5 µs*

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
D = 1: Display on
C = 1: Cursor on
B = 1: Blink on
FW = 1: 6-dot font width
B/W = 1: Black-white inverting cursor on
NW = 1: Four lines
NW = 0: One or two lines
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
RE = 1: Extension register access enable
BE = 1: CGRAM/SEGRAM blinking enable
LP = 1: Low-power mode
BF = 1: Internally operating
BF = 0: Instructions acceptable

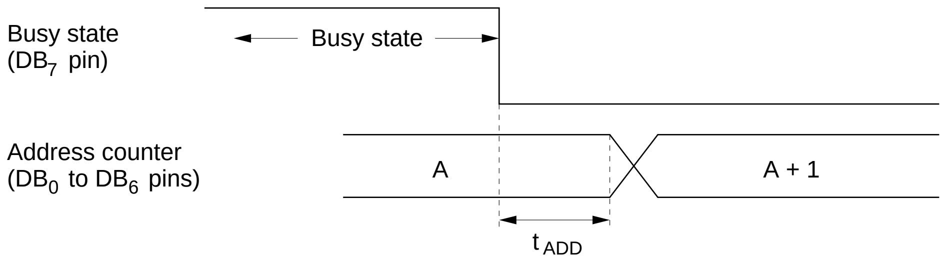
DD RAM: Display data RAM
A_{DD}: DD RAM address (corresponds to cursor address)
CG RAM: Character generator RAM
A_{CG}: CG RAM address
SEGRAM: Segment RAM
A_{SEG}: Segment RAM address
HSE: Specifies horizontal scroll lines
HDS: Horizontal dot scroll quantity
AC: Address counter used for both DD, CG, and SEG RAM addresses.

Note: 1. — indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 17, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. Extension time changes as frequency changes. For example, when f is 300 kHz, the execution time is: 37 µs × 270/300 = 33 µs.

3. Execution time in a low-power mode (LP = 1 and EXT = low) becomes four times for a 1-line mode, and twice for a 2- or 4-line mode.


Busy state
(DB$_7$ pin)
Busy state
Address counter
(DB$_0$ to DB$_6$ pins)
A
A + 1
t_{ADD}

t_{ADD} depends on the operation frequency.
$t_{ADD} = 1.5/(f_{cp}$ or $f_{OSC})$ seconds

Figure 17 Address Counter Update

Interfacing the HD66712

Interface with 8-Bit MPUs: The HD66712 can interface directly with an 8-bit MPU using the E clock, or with an 8-bit MCU through an I/O port. When the number of I/O ports in the MCU, or the interfacing bus width, if limited, a 4-bit interface function is used.

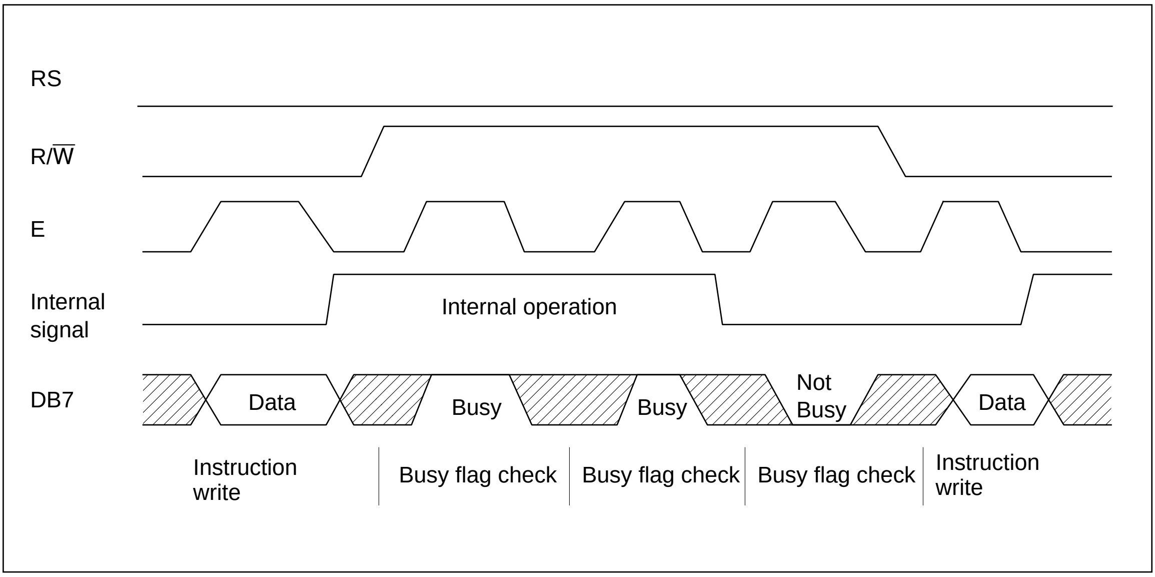

RS
R/W̄
E
Internal signal
Internal operation
DB7
Data
Busy
Busy
Not Busy
Data
Instruction write
Busy flag check
Busy flag check
Busy flag check
Instruction write

Figure 18 Example of 8-Bit Data Transfer Timing Sequence

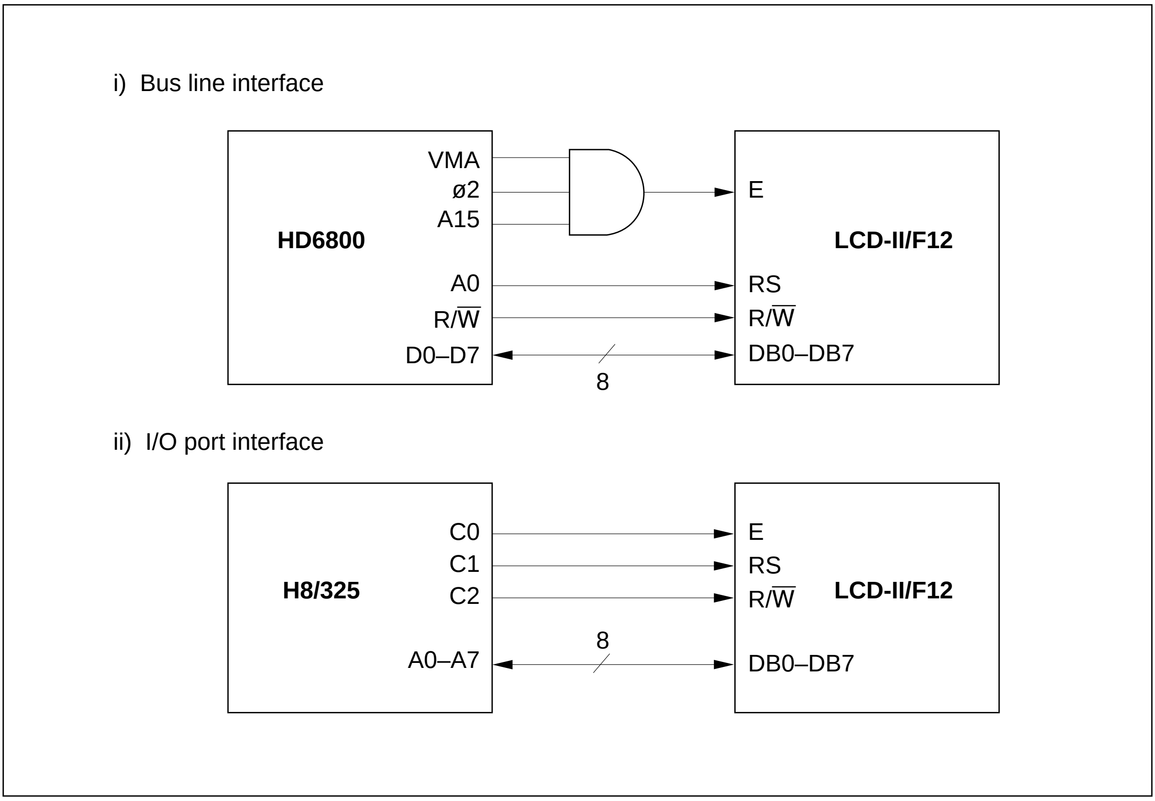

i) Bus line interface
HD6800
VMA
ø2
A15
A0
R/$\overline{W}$
D0–D7
8
E
LCD-II/F12
RS
R/$\overline{W}$
DB0–DB7
ii) I/O port interface
H8/325
C0
C1
C2
A0–A7
8
E
RS
R/$\overline{W}$
LCD-II/F12
DB0–DB7

Figure 19 8-Bit MPU Interface

Interface with 4-Bit MPUs: The HD66712 can interface with a 4-bit MCU through an I/O port. 4-bit data representing high and low order bits must be transferred sequentially.

The DL bit in function-set selects 4-bit or 8-bit interface data length.

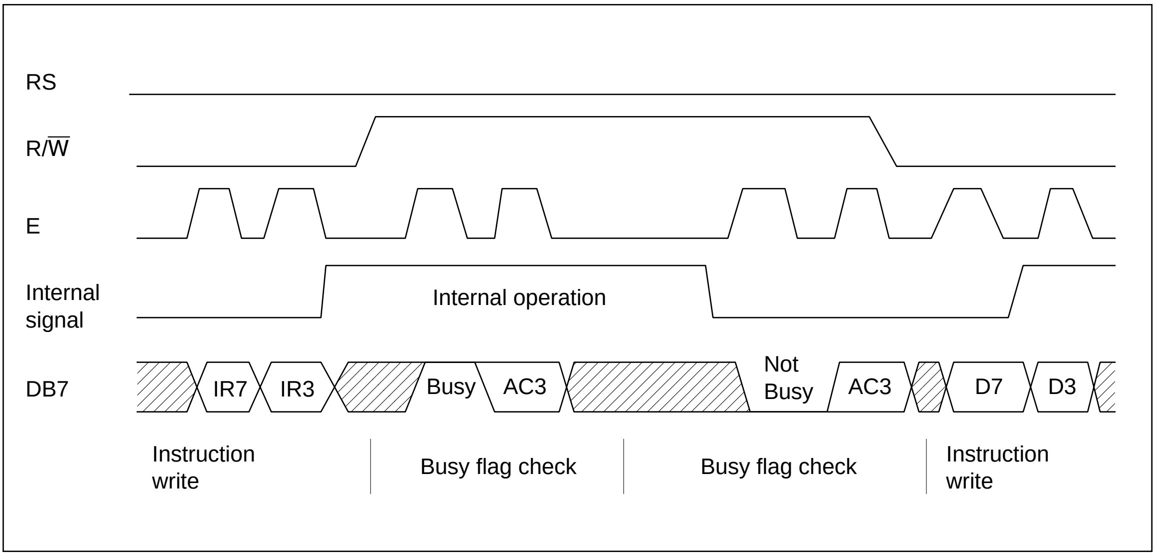

RS
R/$\overline{W}$
E
Internal signal
Internal operation
DB7
IR7
IR3
Busy
AC3
Not Busy
AC3
D7
D3
Instruction write
Busy flag check
Busy flag check
Instruction write

Figure 20 Example of 4-Bit Data Transfer Timing Sequence

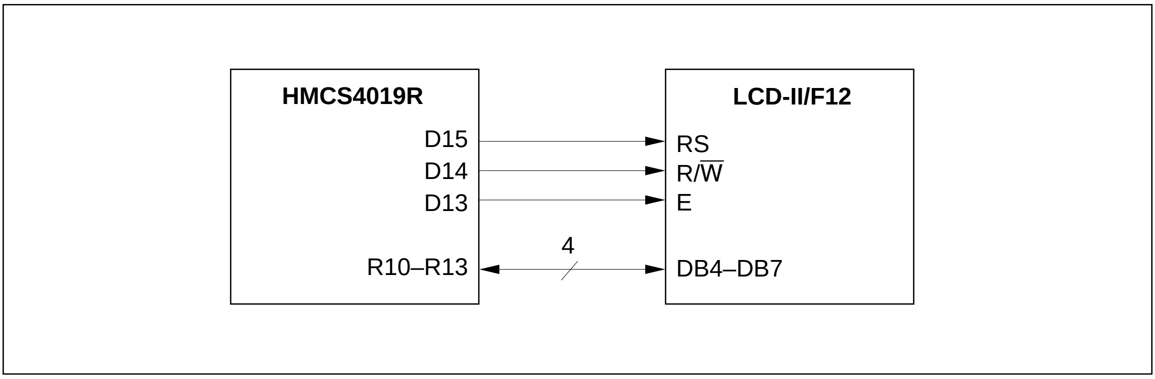
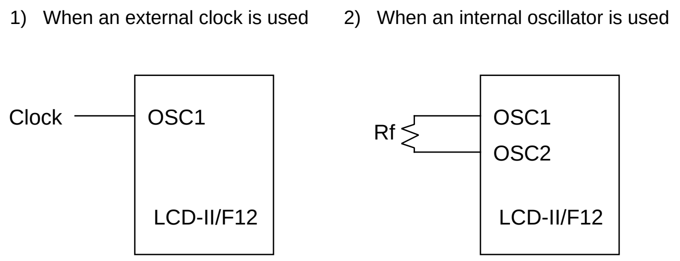

HMCS4019R
D15
D14
D13
R10–R13
4
LCD-II/F12
RS
R/$\overline{W}$
E
DB4–DB7

Figure 21 4-bit MPU Interface

Oscillator Circuit

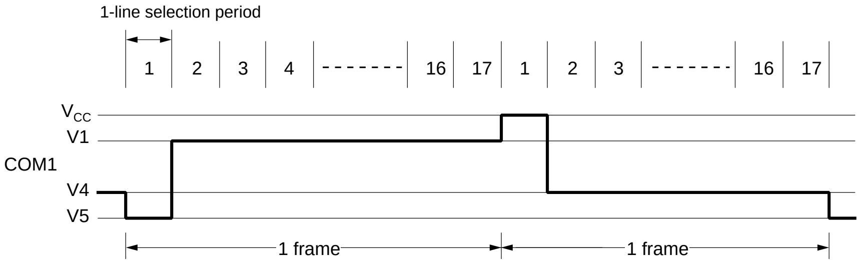

1) When an external clock is used
2) When an internal oscillator is used
Clock
OSC1
LCD-II/F12
Rf
OSC1
OSC2
LCD-II/F12

The oscillator frequency can be adjusted by oscillator resistance (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistor is as follows.

- Rf = 91 kΩ ± 2% (V_{CC} = 5 V)
- Rf = 75 kΩ ± 2% (V_{CC} = 3 V)

Figure 22 Oscillator Circuit

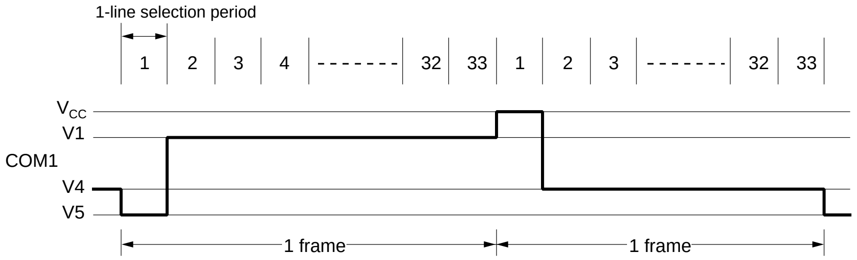
(1) 1 /17 duty cycle


1-line selection period
1
2
3
4
16
17
1
2
3
16
17
V_{CC}
V1
COM1
V4
V5
1 frame
1 frame

	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	200 clocks	240 clocks	60 clocks	72 clocks
Frame frequency	79.4 Hz	66.2 Hz	66.2 Hz	55.1 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

(2) 1 /33 duty cycle


1-line selection period
1
2
3
4
32
33
1
2
3
32
33
V_{CC}
V1
COM1
V4
V5
1 frame
1 frame

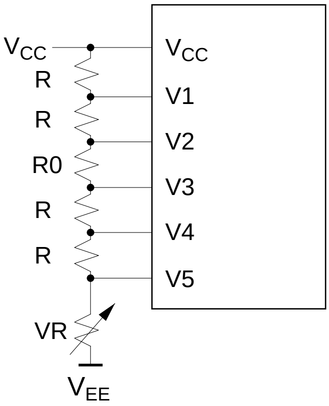
	Normal Display Mode (LP = 0)		Low Power Mode (LP = 1)	
Item	**5-Dot Font Width**	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
Line selection period	100 clocks	120 clocks	60 clocks	72 clocks
Frame frequency	81.8 Hz	68.2 Hz	68.2 Hz	56.8 Hz

Note: At the calculation example above for displayed frame frequency, all oscillator frequencies are 270 kHz (1 clock = 3.7 µs).

Figure 23 Frame Frequency

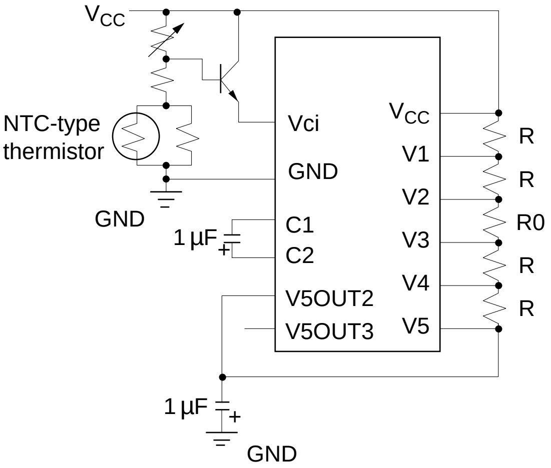
Power Supply for Liquid Crystal Display Drive

1) When an external power supply is used

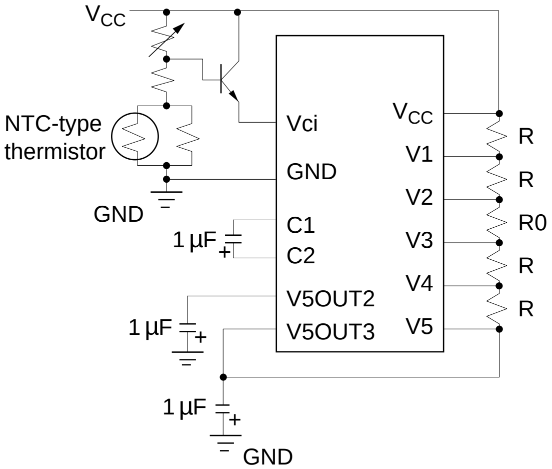

V_{CC}
R
R
R0
R
R
VR
V_{EE}
V_{CC}
V1
V2
V3
V4
V5

2) When an internal booster is used

(Boosting twice)


V_{CC}
NTC-type thermistor
GND
1 µF
+
1 µF
+
GND
Vci
GND
C1
C2
V5OUT2
V5OUT3
V_{CC}
V1
V2
V3
V4
V5
R
R
R0
R
R

(Boosting three times)


V_{CC}
NTC-type thermistor
GND
1 µF
+
1 µF
+
1 µF
+
GND
Vci
GND
C1
C2
V5OUT2
V5OUT3
V_{CC}
V1
V2
V3
V4
V5
R
R
R0
R
R

Notes:
1. Boosting output voltage should not exceed the power supply voltage (2) (15 V max.) in the absolute maximum ratings. Especially, voltage of over 5 V should not be input to the reference voltage (Vci) when boosting three times.
2. Vci input terminal is used for reference voltage and power supply for the internal booster. Input current into the Vci pin needs three times or more of load current through the bleeder resistor for LCD. So, when it adjusts LCD driving voltage (Vlcd), input voltage should be controlled with transistor to supply LCD load current. Please notice connection (+/–) when it uses capacitors with poler.
3. The Vci must be set below the power supply (V_{CC}).

Table 13 Duty Factor and Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2/4
Duty factor		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

Note: R changes depending on the size of liquid crystal panel. Normally, R must be 4.7 kΩ to 20 kΩ.

Extension Driver LSI Interface

By bringing the EXT pin high, extended driver interface signals (CL1, CL2, D, and M) are output.

Table 14 Relationships between the Number of Display Lines and 40-Output Extension Driver

	Controller					
	LCD-II/F12		LCD-II/F8		HD44780	HD66702
Display Lines	5-Dot Width	6-Dot Width	5-Dot Width	6-Dot Width	5-Dot Width	5-Dot Width
16 × 2 lines	Not required	Not required	Not required	1	1	Not required
20 × 2 lines	Not required	Not required	1	1	2	Not required
24 × 2 lines	Not required	1	1	2	2	1
40 × 2 lines	Disabled	Disabled	Disabled	Disabled	4	3
12 × 4 lines	Not required	1	1	1	Disabled	Disabled
16 × 4 lines	1	1	1	2	Disabled	Disabled
20 × 4 lines	1	2	2	3	Disabled	Disabled

Note: The number of display lines can be extended to 32 × 2 lines or 20 × 4 lines in the LCD-II/F12.
The number of display lines can be extended to 30 × 2 lines or 20 × 4 lines in the LCD-II/F8.

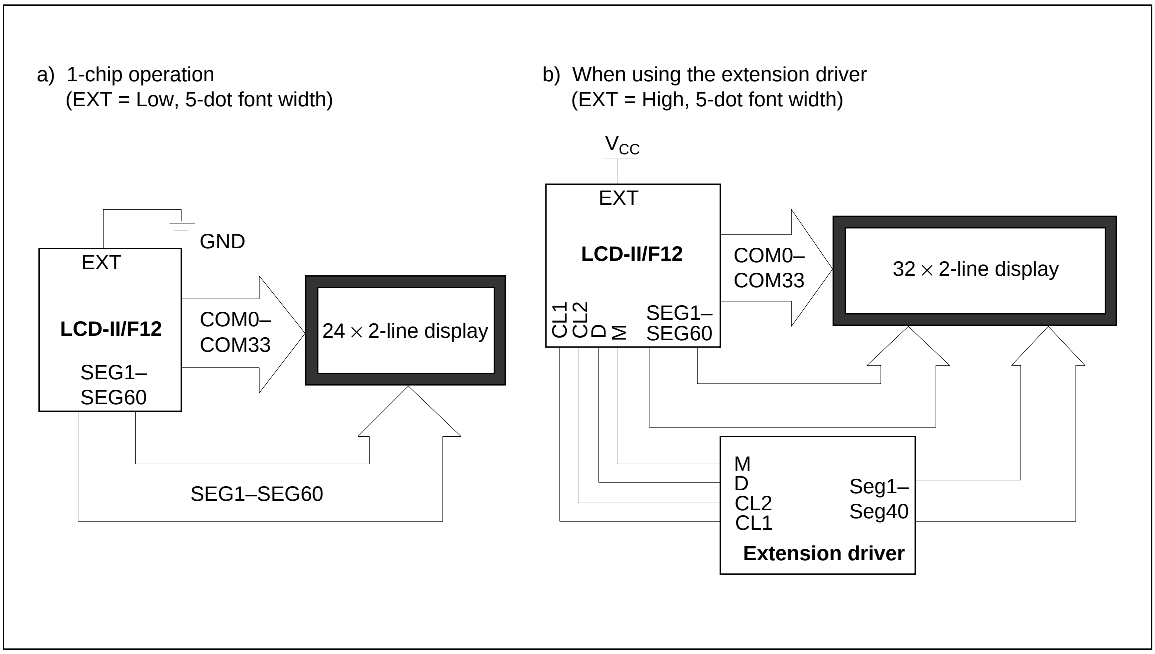

a) 1-chip operation
(EXT = Low, 5-dot font width)
GND
EXT
LCD-II/F12
SEG1–
SEG60
COM0–
COM33
24 × 2-line display
SEG1–SEG60
b) When using the extension driver
(EXT = High, 5-dot font width)
VCC
EXT
LCD-II/F12
CL1
CL2
D
M
SEG1–
SEG60
COM0–
COM33
32 × 2-line display
M
D
CL2
CL1
Seg1–
Seg40
Extension driver

Figure 24 HD66712 and the Extension Driver Connection

Table 15 Display Start Address in Each Mode

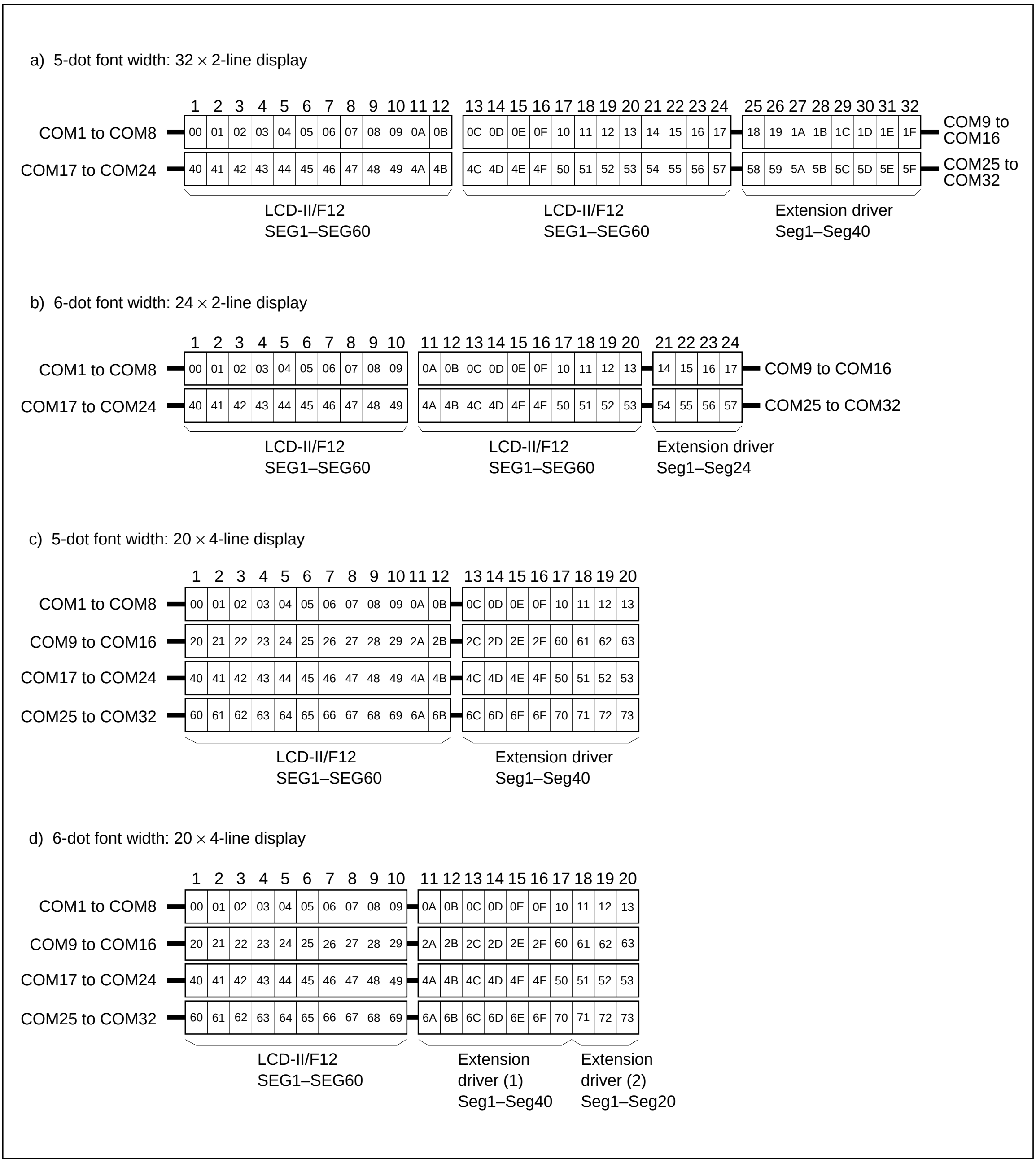
	Number of Lines				
	1-Line Mode		2-Line Mode		4-Line Mode
Output	**5 Dot**	**6 Dot**	**5 Dot**	**6 Dot**	**5 Dot/6 Dot**
COM1–COM8	D00±1	D00±1	D00±1	D00±1	D00±1
COM9–COM16	D0C±1	D0A±1	D0C±1	D0A±1	D20±1
COM17–COM24	—	—	D40±1	D40±1	D40±1
COM25–COM32	—	—	D4C±1	D4A±1	D60±1
COM0/COM17	S00	S00	—	—	—
COM0/COM33	—	—	S00	S00	S00

Notes: 1. The number of display lines is determined by setting the N/NW bit. The font width is determined by the FW bit.

2. D** is the start address of display data RAM (DDRAM).

3. S** is the start address of segment RAM (SEGRAM).

4. ±1 following D** indicates increment or decrement at display shift.



a) 5-dot font width: 32 × 2-line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	COM9 to COM16
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	COM25 to COM32

LCD-II/F12 SEG1–SEG60 (1–12); LCD-II/F12 SEG1–SEG60 (13–24); Extension driver Seg1–Seg40 (25–32)

b) 6-dot font width: 24 × 2-line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	COM9 to COM16
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	COM25 to COM32

LCD-II/F12 SEG1–SEG60 (1–10); LCD-II/F12 SEG1–SEG60 (11–20); Extension driver Seg1–Seg24 (21–24)

c) 5-dot font width: 20 × 4-line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
COM9 to COM16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	60	61	62	63
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
COM25 to COM32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

LCD-II/F12 SEG1–SEG60 (1–12); Extension driver Seg1–Seg40 (13–20)

d) 6-dot font width: 20 × 4-line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1 to COM8	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
COM9 to COM16	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	60	61	62	63
COM17 to COM24	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
COM25 to COM32	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

LCD-II/F12 SEG1–SEG60 (1–10); Extension driver (1) Seg1–Seg40 (11–17); Extension driver (2) Seg1–Seg20 (18–20)

Figure 25 Correspondence between the Display Position at Extension Display and the DDRAM Address

Interface to Liquid Crystal Display

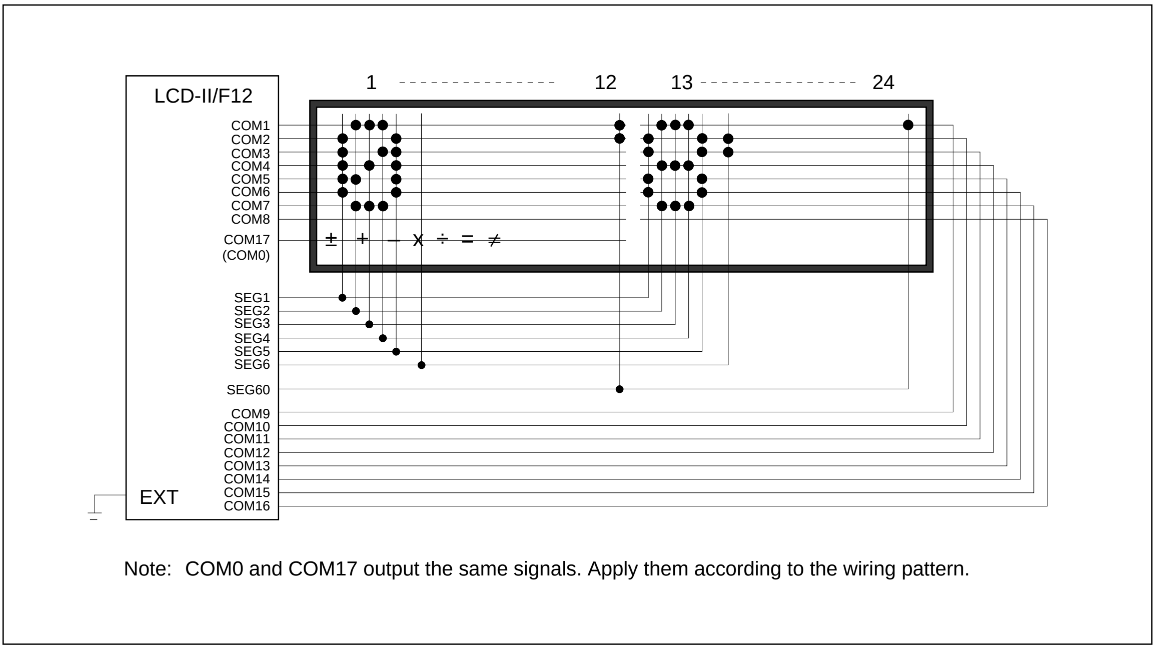
Set the extended driver control signal output, the number of display lines, and the font width with the EXT pin, an extended register NW, and the FW bit, respectively. The relationship between the number of display lines, EXT pin, and register value is given below.

Table 16 Relationship between Display Lines, EXT Pin, and Register Setting

		5 Dot Font						6 Dot Font						
				Registor Setting						Registor Setting				
No. of Lines	**No. of Character**	**EXT Pin**	**Extended Driver**	**N**	**RE**	**NW**	**FW**	**EXT Pin**	**Extended Driver**	**N**	**RE**	**NW**	**FW**	**Duty**
1	20	L	—	0	0	0	0	L	—	0	1	0	1	1/17
	24	L	—	0	0	0	0	H	1	0	1	0	1	1/17
	40	H	2	0	0	0	0	H	3	0	1	0	1	1/17
2	20	L	—	1	0	0	0	L	—	1	1	0	1	1/33
	24	L	—	1	0	0	0	H	1	1	1	0	1	1/33
	32	H	1	1	0	0	0	H	2	1	1	0	1	1/33
4	12	L	—	*	1	1	0	H	1	*	1	1	1	1/33
	16	H	1	*	1	1	0	H	1	*	1	1	1	1/33
	20	H	1	*	1	1	0	H	2	*	1	1	1	1/33

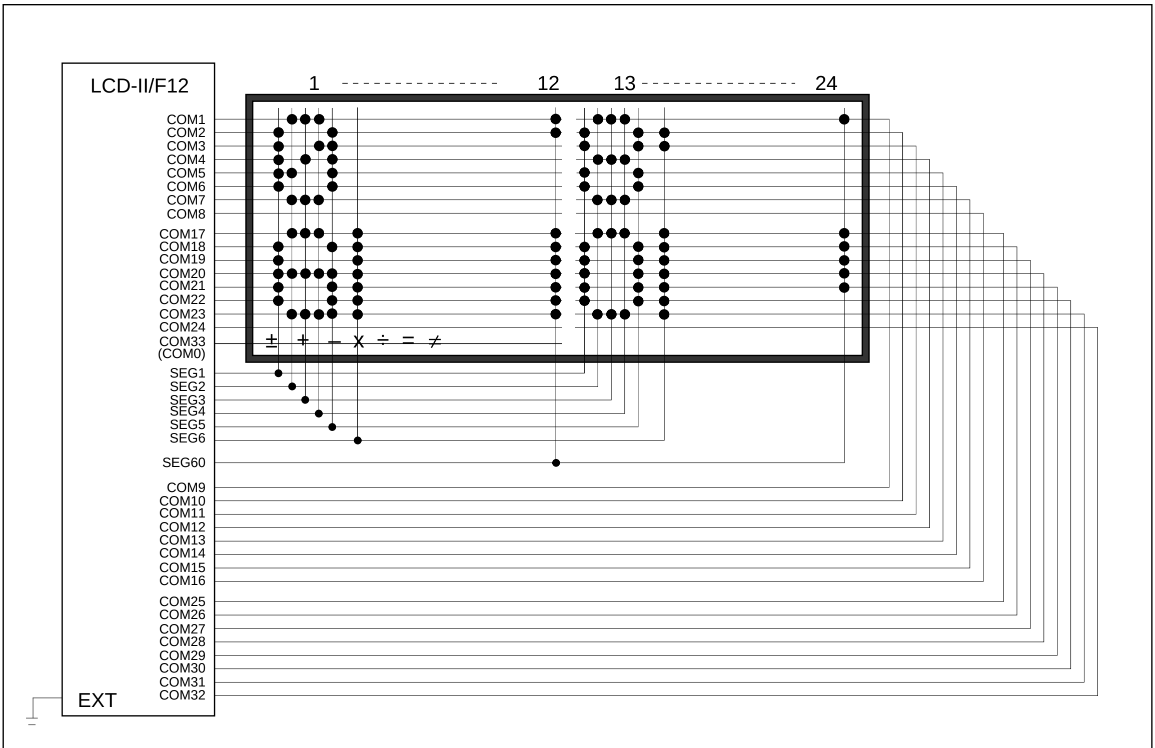
Note: — means not required.

- Example of 5-dot font width connection


LCD-II/F12
1
12
13
24
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM17
(COM0)
± + – x ÷ = ≠
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG60
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
EXT

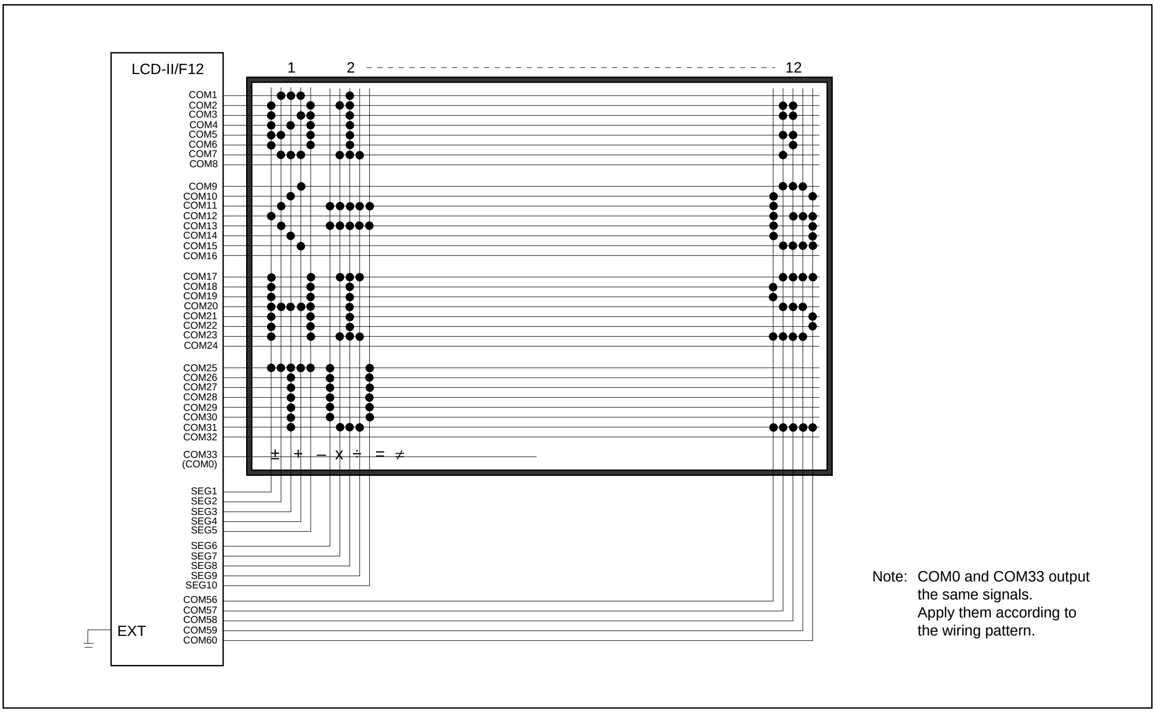
Note: COM0 and COM17 output the same signals. Apply them according to the wiring pattern.

Figure 26 24 × 1-Line + 60-Segment Display (5-Dot Font, 1/17 Duty)


LCD-II/F12
1
12
13
24
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM33
(COM0)
± + – x ÷ = ≠
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG60
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM25
COM26
COM27
COM28
COM29
COM30
COM31
COM32
EXT

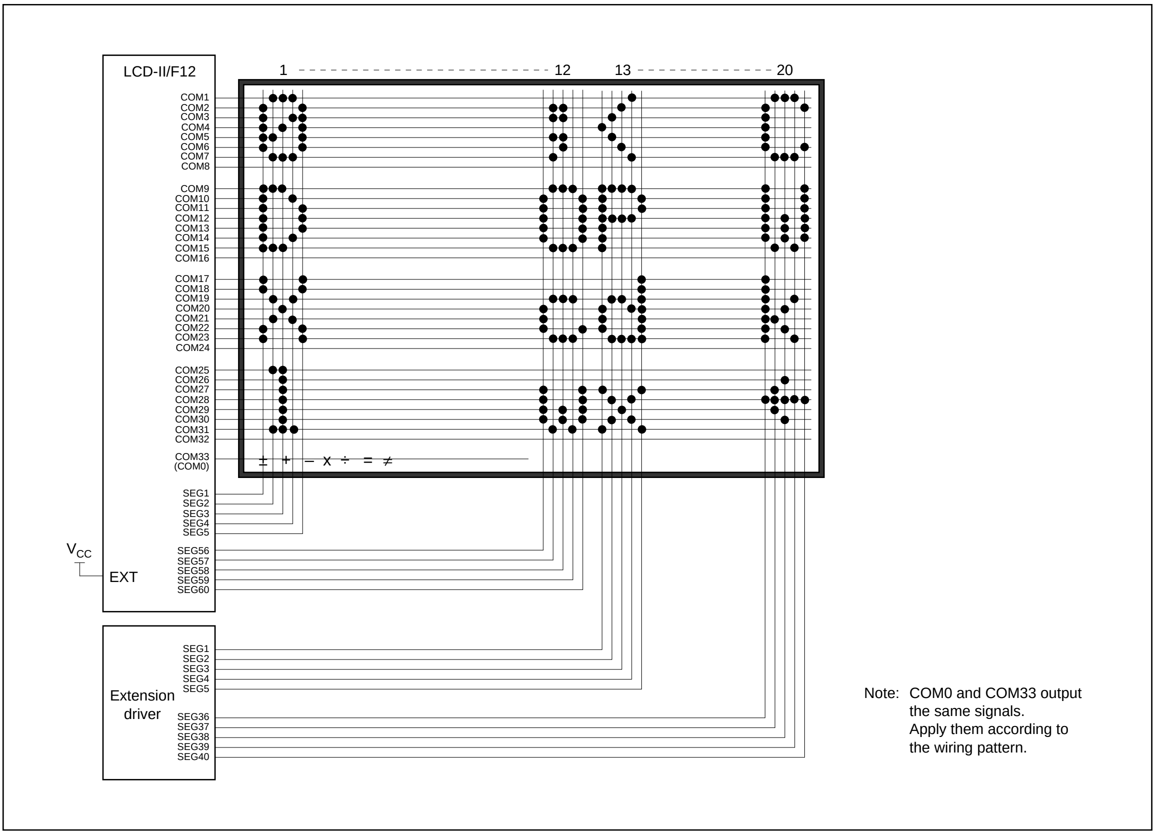
Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 27 24 × 1-Line + 60-Segment Display (5-Dot Font, 1/33 Duty)


LCD-II/F12
1
2
12
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM25
COM26
COM27
COM28
COM29
COM30
COM31
COM32
COM33
(COM0)
± + – x ÷ = ≠
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
COM56
COM57
COM58
COM59
COM60
EXT

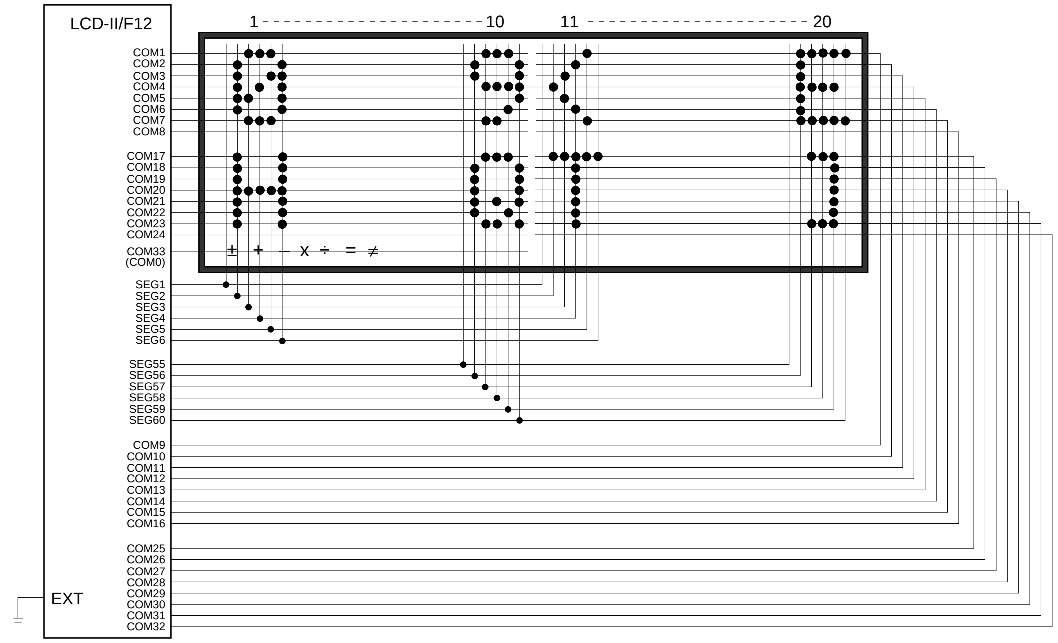
Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 28 12 × 4-Line + 60 Segment Display (5-Dot Font, 1/33 Duty)


LCD-II/F12
1
12
13
20
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM25
COM26
COM27
COM28
COM29
COM30
COM31
COM32
COM33
(COM0)
± + – x ÷ = ≠
SEG1
SEG2
SEG3
SEG4
SEG5
V_{CC}
EXT
SEG56
SEG57
SEG58
SEG59
SEG60
Extension driver
SEG1
SEG2
SEG3
SEG4
SEG5
SEG36
SEG37
SEG38
SEG39
SEG40

Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 29 20 × 4-Line + 80 Segment Display (5-Dot Font, 1/33 Duty)


LCD-II/F12
1
10
11
20
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM33
(COM0)
± + – x ÷ = ≠
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG55
SEG56
SEG57
SEG58
SEG59
SEG60
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM25
COM26
COM27
COM28
COM29
COM30
COM31
COM32
EXT

Note: COM0 and COM33 output the same signals. Apply them according to the wiring pattern.

Figure 30 20 × 2-Line + 60 Segment Display (6-Dot Font, 1/33 Duty)

Instruction and Display Correspondence

- 8-bit operation, 24-digit × 1-line display with internal reset

  Refer to table 17 for an example of an 24-digit × 1-line display in 8-bit operation. The LCD-II/F12 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, a character unit scroll can be performed by a display shift instruction. A dot unit smooth scroll can also be performed by a horizontal scroll instruction. Since data of display RAM (DDRAM) is not changed by a display shift instruction, the display can be returned to the first set display when the return home operation is performed.

- 4-bit operation, 24-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (see table 18). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB_0 to DB_3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions. Thus, DB_4 to DB_7 of the function set instruction is written twice.

- 8-bit operation, 24-digit × 2-line display with internal reset

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 16 characters in the first line, the DD RAM address must be again set after the 16th character is completed. (See table 19.)

  The display shift is performed for the first and second lines. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

- 8-bit operation, 12-digit × 4-line display with internal reset

  The RE bit must be set by the function set instruction and then the NW bit must be set by an extension function set instruction. In this case, 4-line display is always performed regardless of the N bit setting (see table 20).

  In a 4-line display, the cursor automatically moves from the first to the second line after the 20th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must be set again after the 8th character is completed. Display shifts are performed on all lines simultaneously.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the LCD-II/F12 must be initialized by instructions. See the section, Initializing by Instruction.

Table 17 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step	Instruction											
No.	**RS**	**R/$\overline{W}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Display**	**Operation**
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 1-line display. Bit 2 must always be cleared.
	RS	R/$\overline{W}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
	0	0	0	0	1	1	0	0	*	*		
3	Return home											Return both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		
4	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
5	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
6	Write data to CG RAM/DD RAM										H_	Writes H. DD RAM has already been selected by initialization when the power was turned on.
	1	0	0	1	0	0	1	0	0	0		
7	Write data to CG RAM/DD RAM										HI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	⋮										⋮	
9	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
10	Entry mode set										HITACHI_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
11	Write data to CG RAM/DD RAM										ITACHI _	Writes a space.
	1	0	0	0	1	0	0	0	0	0		

Table 17 8-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset (cont)

Step	Instruction											
No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
12	Write data to CG RAM/DD RAM										TACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
13						⋮					⋮	
14	Write data to CG RAM/DD RAM										MICROKO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
15	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
16	Cursor or display shift										MICROKO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	*	*		
17	Write data to CG RAM/DD RAM										ICROCO	Writes C over K. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
18	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	*	*		
19	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	*	*		
20	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
21						⋮					⋮	
22	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 18 4-Bit Operation, 24-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction										Display	Operation
	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0		
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 4-bit operation. Clear bit 2. In this case, operation is handled as 8 bits by initialization. *[1]
	RS	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
	0	0	0	0	1	0	—	—	—	—		
	—	—	—	—	—	—	—	—	—	—		
3	Function set											Sets 4-bit operation and selects 1-line display. Clear BE, LP bits. 4-bit operation starts from this step.
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	1	0	0	—	—	—	—		
4	Function set											Sets 4-bit operation and selects 1 line display. Clear bit 2 (RE).
	0	0	0	0	1	0	—	—	—	—		
	0	0	0	0	*	*	—	—	—	—		
5	Return home											Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	0	1	0	—	—	—	—		
6	Display on/off control										_	Turns on display and cursor. Entire display is in space mode because of initialization.
	0	0	0	0	0	0	—	—	—	—		
	0	0	1	1	1	0	—	—	—	—		
7	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
	0	0	0	0	0	0	—	—	—	—		
	0	0	0	1	1	0	—	—	—	—		
8	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	—	—	—	—		
	1	0	1	0	0	0	—	—	—	—		
					. . .							Based on 8-bit operation after this instruction.

Note: The control is the same as for 8-bit operation beyond step #8.

1. When DB3 to DB0 pins are open in 4-bit mode, the RE, BE, LP bits are set to “1” at step #2. So, these bits are clear to “0” at step #3.

Table 19 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset

Step	Instruction											
No.	**RS**	**R/$\overline{W}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Display**	**Operation**
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets to 8-bit operation and selects 2-line display. Clear bit 2.
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
	0	0	0	0	1	1	1	0	*	*		
3	Display on/off control										_	Turns on display and cursor. All display is in space mode because of initialization.
	0	0	0	0	0	0	1	1	1	0		
4	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CG RAM/DD RAM										H_	Writes “H.” DD RAM has already been selected by initialization at power-on.
	1	0	0	1	0	0	1	0	0	0		
6					: : : :						: : : :	
7	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
8	Set DD RAM address										HITACHI _	Sets DD RAM address so that the cursor is positioned at the head of the second line.
	0	0	1	1	0	0	0	0	0	0		

Table 19 8-Bit Operation, 24-Digit × 2-Line Display Example with Internal Reset (cont)

Step	Instruction											
No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CG RAM/DD RAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
10					⋮						⋮	
11	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
12	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
13	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
14					⋮						⋮	
15	Return home										H̲ITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 20 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset

Step	Instruction											
No.	**RS**	**$R/\overline{W}$**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Display**	**Operation**
1	Power supply on (the HD66712 is initialized by the internal reset circuit)											Initialized. No display.
2	Function set											Sets 8-bit operation and enables write to the extension register.
	0	0	0	0	1	1	0	1	*	*		
3	4-line mode set											Sets 4-line operation.
	0	0	0	0	0	0	1	0	0	1		
4	Return home											Return both display and cursor to the original position.
	0	0	0	0	0	0	0	0	1	0		
5	Function set Inhibit write to extension register											Inhibits write to extension register. Invalidates selection of 1-line/2-line by bit 3.
	0	0	0	0	1	1	0	0	*	*		
6	Display on/off control										_	Turns on display and cursor. Entire display is cleared because of initialization.
	0	0	0	0	0	0	1	1	1	0		
7	Entry mode set										_	Sets mode to increment the address by one and to shift the cursor to the right when writing to RAM. Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
8	Write data to CG RAM/DD RAM										H_	Writes H. DDRAM has already been selected by initialization.
	1	0	0	1	0	0	1	0	0	0		
9					⋮						⋮	

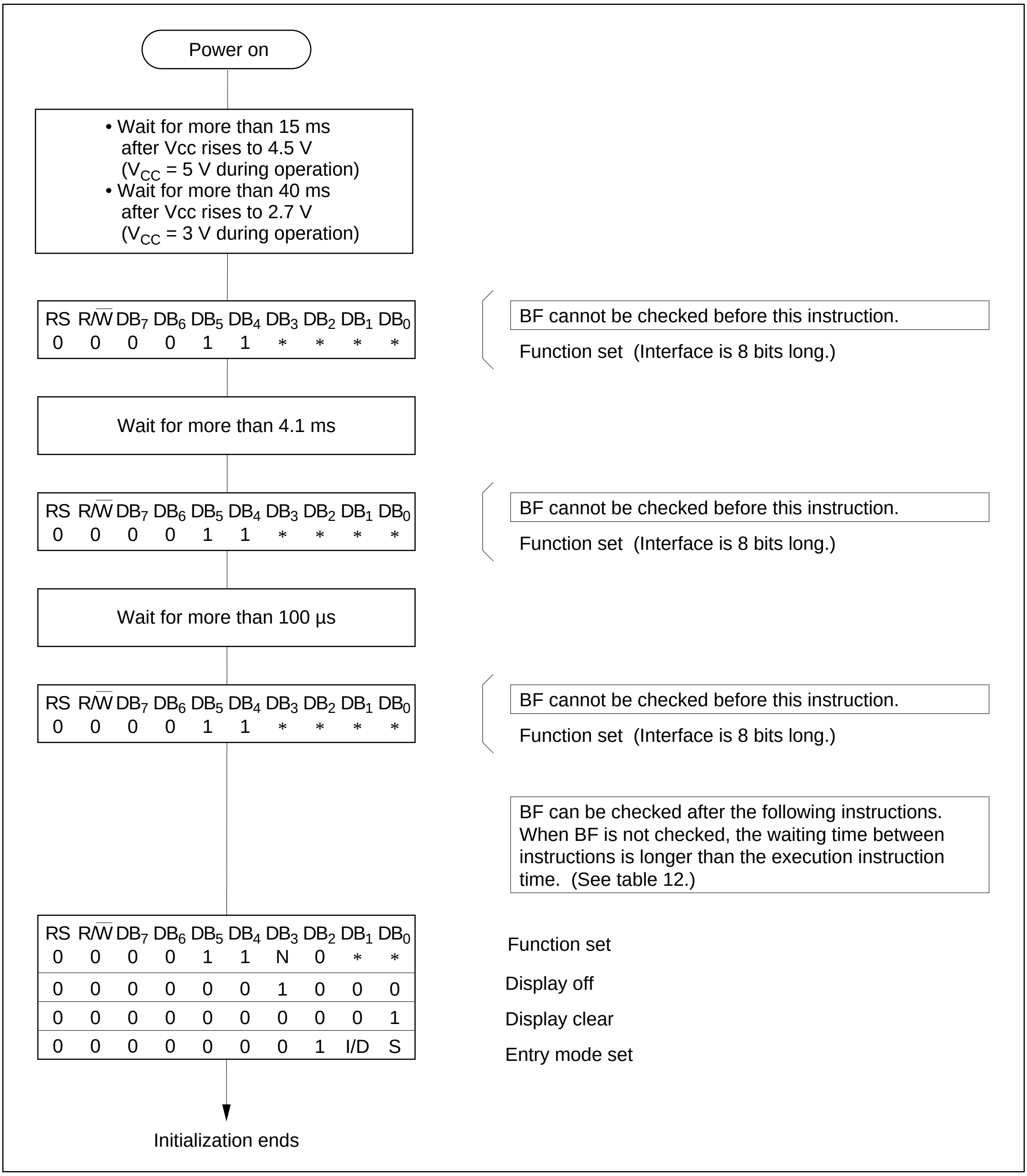
Table 20 8-Bit Operation, 12-Digit × 4-Line Display Example with Internal Reset (cont)

Step	Instruction											
No.	RS	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
10	Write data to CG RAM/DD RAM										HITACHI_	Writes I.
	1	0	0	1	0	0	1	0	0	1		
11	Set DD RAM address										HITACHI _	Sets DD RAM address to (20)H so that the cursor is positioned at the beginning of the second line.
	0	0	1	0	1	0	0	0	0	0		
12	Write data to CG RAM										HITACHI 0_	Writes 0.
	1	0	0	0	1	1	0	0	0	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

- Initializing when a length of interface is 8-bit system. (See figure 31.)
- Initializing when a length of interface is 4-bit system. (See figure 32.)



- Wait for more than 15 ms after Vcc rises to 4.5 V (V_{CC} = 5 V during operation)
- Wait for more than 40 ms after Vcc rises to 2.7 V (V_{CC} = 3 V during operation)

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

Wait for more than 4.1 ms

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

Wait for more than 100 μs

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	0	1	1	*	*	*	*

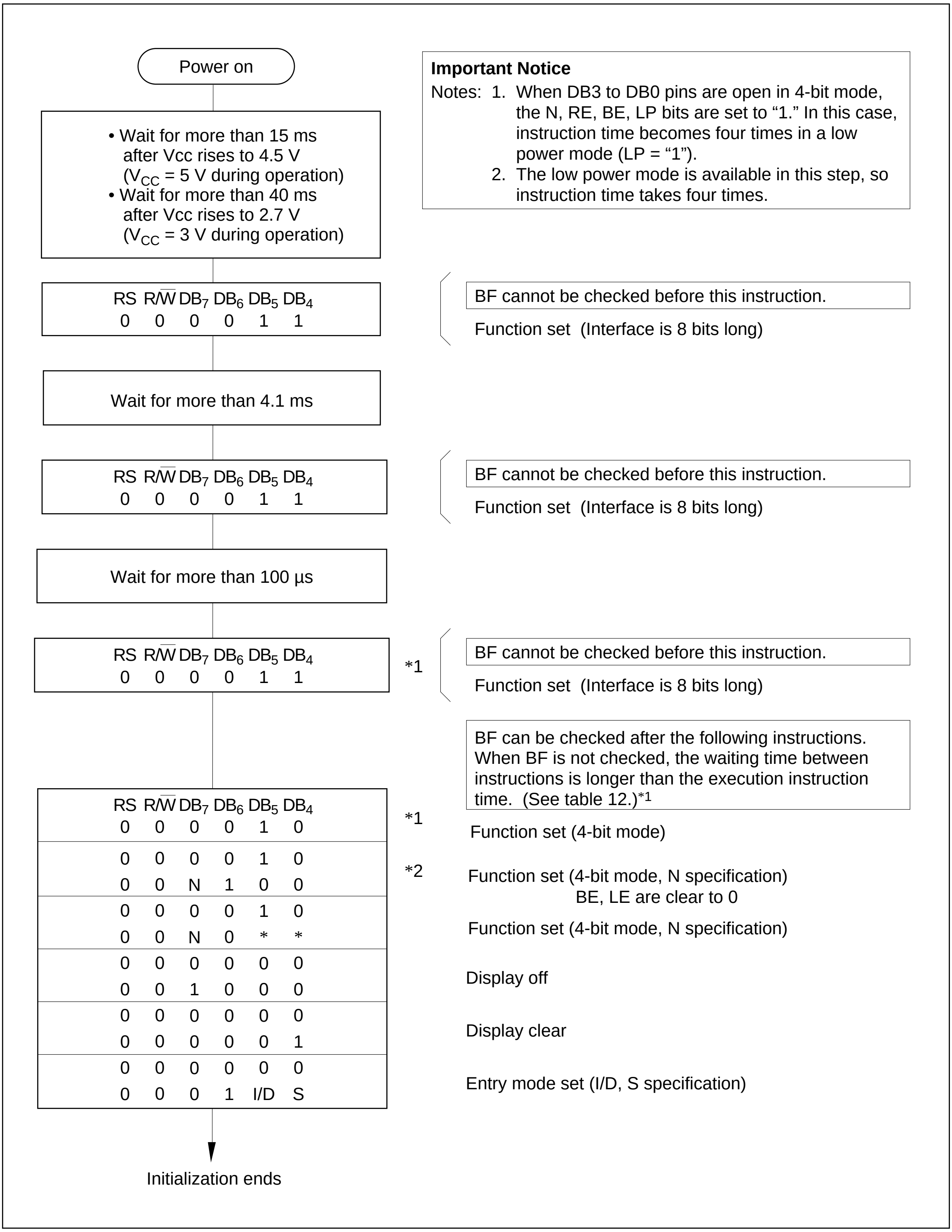
BF cannot be checked before this instruction.

Function set (Interface is 8 bits long.)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See table 12.)

RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
0	0	0	0	1	1	N	0	*	*	Function set
0	0	0	0	0	0	1	0	0	0	Display off
0	0	0	0	0	0	0	0	0	1	Display clear
0	0	0	0	0	0	0	1	I/D	S	Entry mode set

Figure 31 Initializing Flow of 8-Bit Interface


Power on
• Wait for more than 15 ms after Vcc rises to 4.5 V (V_{CC} = 5 V during operation)
• Wait for more than 40 ms after Vcc rises to 2.7 V (V_{CC} = 3 V during operation)
RS R/$\overline{W}$ DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
Function set (Interface is 8 bits long)
Wait for more than 4.1 ms
RS R/$\overline{W}$ DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
Function set (Interface is 8 bits long)
Wait for more than 100 µs
RS R/$\overline{W}$ DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 1
*1
Function set (Interface is 8 bits long)
RS R/$\overline{W}$ DB_7 DB_6 DB_5 DB_4
0 0 0 0 1 0
*1
Function set (4-bit mode)
0 0 0 0 1 0
0 0 N 1 0 0
*2
Function set (4-bit mode, N specification) BE, LE are clear to 0
0 0 0 0 1 0
0 0 N 0 * *
Function set (4-bit mode, N specification)
0 0 0 0 0 0
0 0 1 0 0 0
Display off
0 0 0 0 0 0
0 0 0 0 0 1
Display clear
0 0 0 0 0 0
0 0 0 1 I/D S
Entry mode set (I/D, S specification)
Initialization ends

Important Notice

Notes:
1. When DB3 to DB0 pins are open in 4-bit mode, the N, RE, BE, LP bits are set to "1." In this case, instruction time becomes four times in a low power mode (LP = "1").
2. The low power mode is available in this step, so instruction time takes four times.

BF cannot be checked before this instruction.

BF cannot be checked before this instruction.

BF cannot be checked before this instruction.

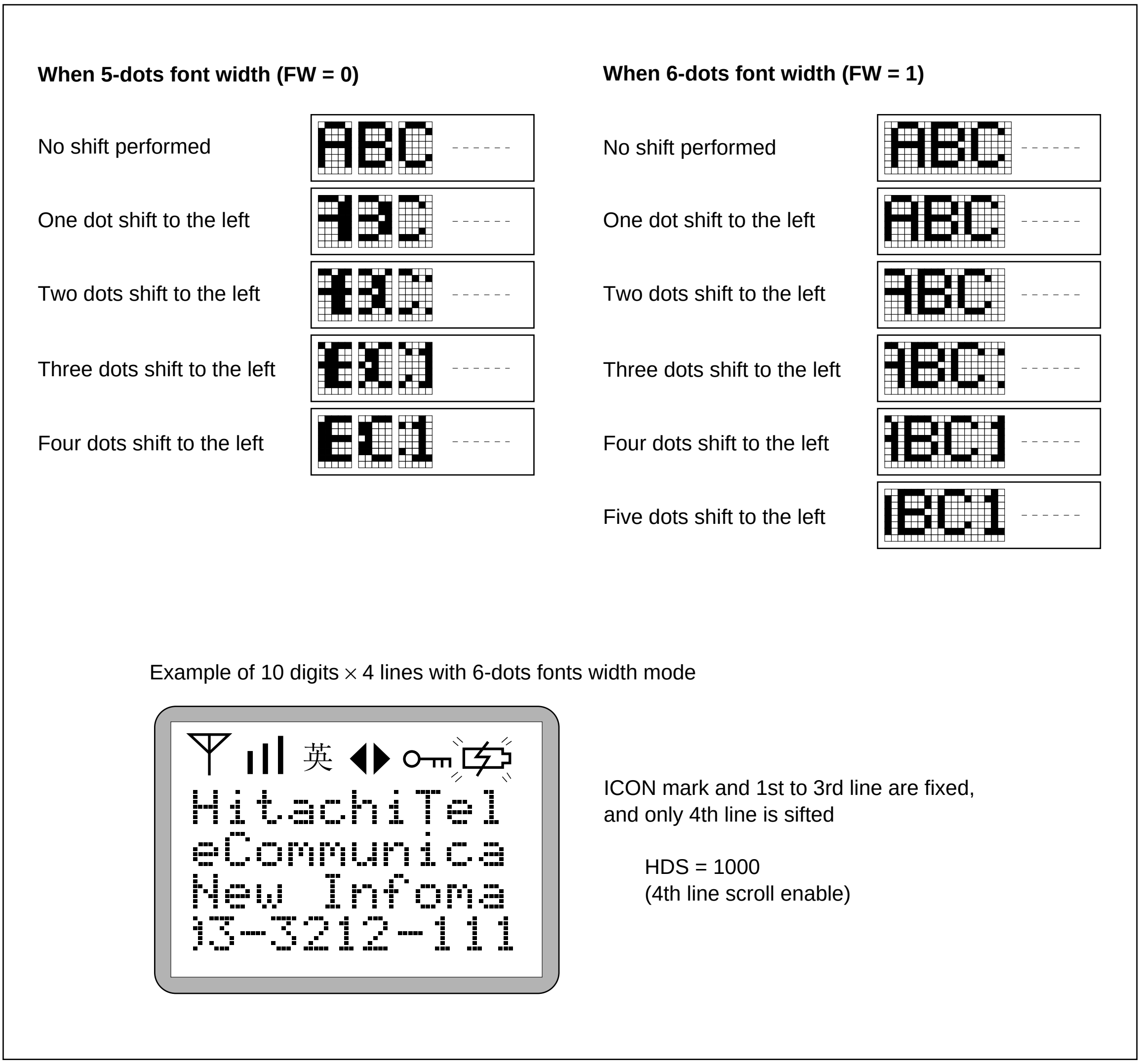
BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See table 12.)*1

Figure 32 Initializing Flow of 4-Bit Interface

Horizontal Dot Scroll

Dot unit scrolls are performed by setting the horizontal dot scroll quantity resister (HDS) when the extension register is enabled (RE = “1”). And the shifted line can be selected with the scroll enable register (HDE). So, it can control dot unit shifts by each display line.

To scroll smoothly, LCD-II/F12 supports 6 dots-font width mode (FW = 1). The below figures are examples of scroll display.


When 5-dots font width (FW = 0)
No shift performed
One dot shift to the left
Two dots shift to the left
Three dots shift to the left
Four dots shift to the left
When 6-dots font width (FW = 1)
No shift performed
One dot shift to the left
Two dots shift to the left
Three dots shift to the left
Four dots shift to the left
Five dots shift to the left
英
HitachiTel
eCommunica
New Infoma
3-3212-111

Example of 10 digits × 4 lines with 6-dots fonts width mode

ICON mark and 1st to 3rd line are fixed,
and only 4th line is sifted

HDS = 1000
(4th line scroll enable)

Figure 33 Example of Dot Scroll Display

6-dots font width mode (FW = 1)
4 line display mode (NW = 1)

	RS	$R/\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	1	DL	N	**1**	BE	LP	Enable extension resistor.
2	0	0	0	0	0	1	**1**	**0**	**0**	**0**	4th line scroll enable.
3	0	0	1	0	**0**	**0**	**0**	**0**	**0**	**1**	One dot shift in 4th line to the left.
			CPU Wait								
4	0	0	1	0	**0**	**0**	**0**	**0**	**1**	**0**	Two dots shift in 4th line to the left.
			CPU Wait								
5	0	0	1	0	**0**	**0**	**0**	**0**	**1**	**1**	Three dots shift in 4th line to the left.
			CPU Wait								
6	0	0	1	0	**0**	**0**	**0**	**1**	**0**	**0**	Four dots shift in 4th line to the left.
			CPU Wait								
49	0	0	1	1	**1**	**0**	**1**	**1**	**1**	**1**	47 dots shift in 4th line to the left.
			CPU Wait								
50	0	0	1	0	**1**	**1**	**0**	**0**	**0**	**0**	48 dots shift in 4th line to the left.

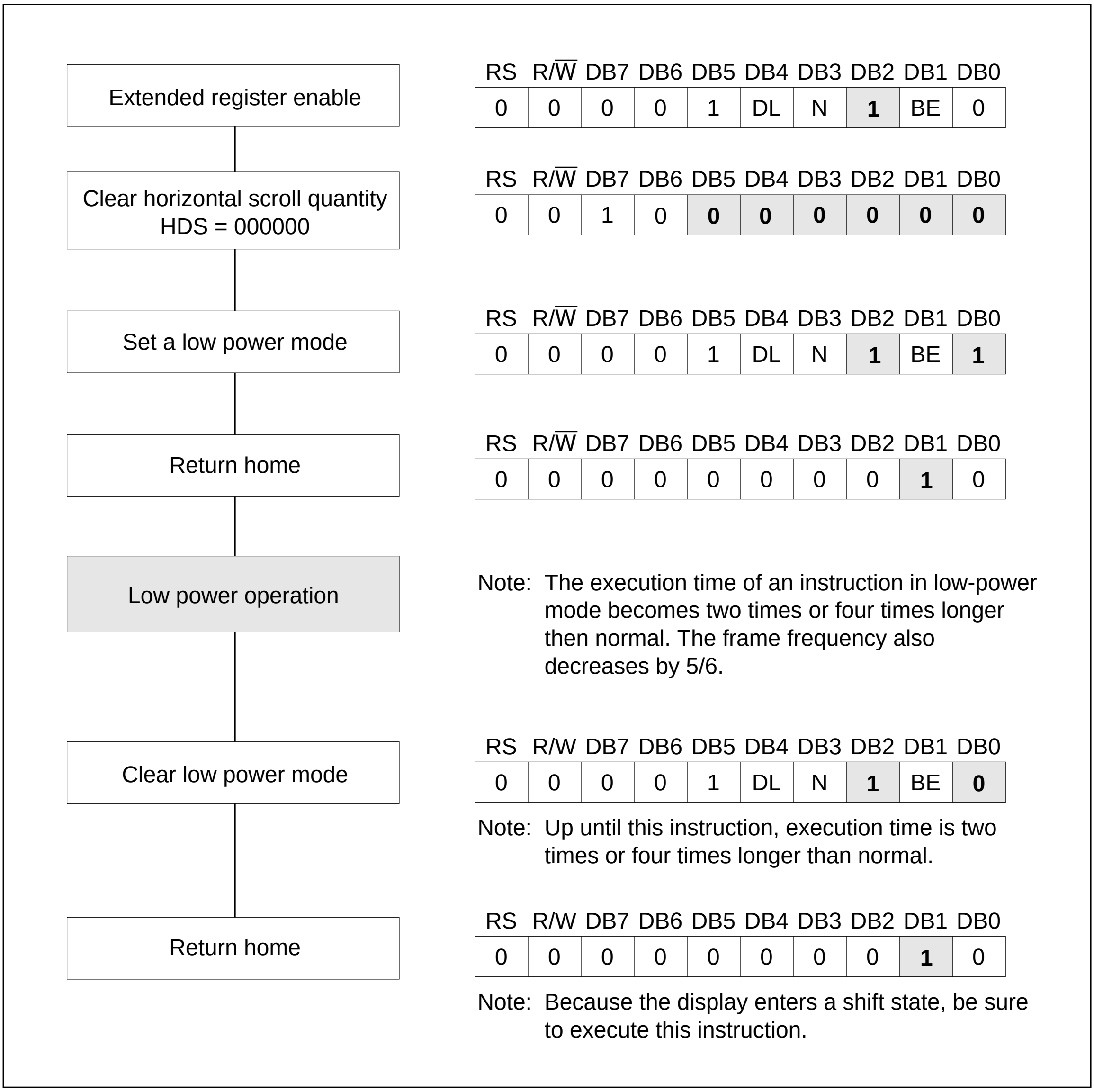
Note: When perfoming a dot scroll with an extended driver, the maximum number or characters per line decreases by quantity set by the dot scroll. For example, when the maximum 24-dot scroll quantity (4 characters) is used with 6-dot font width and 4-line display, the maximum numbers of character is 20 – 4 = 16. Notice that in low power mode (LP = 1), display shift and dot scroll cannot be performed.

Figure 34 Method of Smooth Scroll Display

Low Power Mode

When the extension driver is not used (EXT = Low) with extension register enabled (RE = 1), the HD66712 enters low power mode by setting the low-power mode bit (LP) to 1. During low-power mode, as the internal operation clock is divided by 2 (2-line/4-line display mode) or by 4 (1-line display mode), the execution time of each instruction becomes two times or four times longer than normal. In addition, as the frame frequency decreases to 5/6, display quality might be affected.

In addition, since the display is not shifted in low power mode, display shift must be cleared with the return home instruction before setting low power mode. The amount of horizontal scroll must also be cleared (HDS = 000000). Moreover, because the display enters a shift state after clearing low-power mode, the home return instruction must be used to clear display shift at that time.



Extended register enable

RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	**1**	BE	0

Clear horizontal scroll quantity HDS = 000000

RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	**0**	**0**	**0**	**0**	**0**	**0**

Set a low power mode

RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	**1**	BE	**1**

Return home

RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	**1**	0

Low power operation

Note: The execution time of an instruction in low-power mode becomes two times or four times longer then normal. The frame frequency also decreases by 5/6.

Clear low power mode

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	**1**	BE	**0**

Note: Up until this instruction, execution time is two times or four times longer than normal.

Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	**1**	0

Note: Because the display enters a shift state, be sure to execute this instruction.

Figure 35 Usage of Low Power Mode

Absolute Maximum Ratings*

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{CC}–V_5	V	–0.3 to +15.0	1, 2
Input voltage	V_t	V	–0.3 to V_{CC} +0.3	1
Operating temperature	T_{opr}	°C	–20 to +75	3
Storage temperature	T_{stg}	°C	–55 to +125	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Input high voltage (1) (except OSC_1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		6
Input low voltage (1) (except OSC_1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V	V_{CC} = 2.7 to 3.0 V	6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC_1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC_1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D_0–D_7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$-I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D_0–D_7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D_0–D_7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$-I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D_0–D_7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM) V_{LCD} = 4 V	13
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG) V_{LCD} = 4 V	13
I/O leakage current	I_{LI}	–1	—	1	μA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (D_0–D_7, RESET* pin)	–Ip	10	50	120	μA	V_{CC} = 3 V Vin = 0 V	
Power supply current	Icc	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD1}	3.0	—	13.0	V	V_{CC}–V_5, 1/5 bias	16
	V_{LCD2}	3.0	—	13.0	V	V_{CC}–V_5, 1/6.7 bias	16

Note: * Refer to Electrical Characteristics Notes following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	V_{ci} = 4.5 V, I_0 = 0.25 mA, C = 1 μF, f_{OSC} = 270 kHz T_a = 25°C	18, 19
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.7	—	V	V_{ci} = 2.7 V, I_0 = 0.25 mA, C = 1 μF, f_{OSC} = 270 kHz T_a = 25°C	18, 19
Input voltage	V_{Ci}	2.0	—	5.0	V	Vci ≤ V_{CC} Ta = 25°C	18, 19 20

Note: * Refer to Electrical Characteristics Notes following these tables.

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C^{*3})

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C^{*3})

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	125	270	410	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	190	270	350	kHz	R_f = 91 kΩ, V_{CC} = 5 V	12

Note: * Refer to the Electrical Characteristics Notes section following these tables.

System Interface Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C^{*3})

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	1000	—	—	ns	Figure 37
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 38
Serial clock (high level width)	t_{SCH}	400	—	—	ns	
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	0	—	—		

System Interface Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C^{*3})

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 36
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{cycE}	500	—	—	ns	Figure 37
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	μs	Figure 38
Serial clock (high level width)	t_{SCH}	200	—	—	ns	
Serial clock (low level width)	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	0	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 39
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Reset Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 40

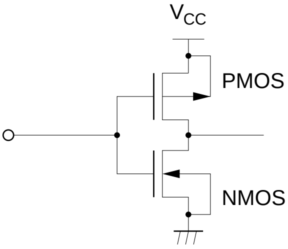
Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 41
Power supply off time	t_{OFF}	1	—	—		

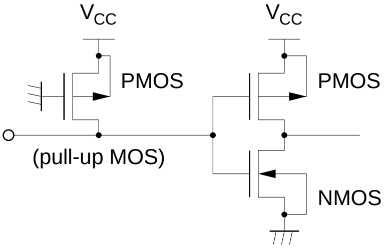
Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are also exceeded, the LSI may malfunction or exhibit poor reliability.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

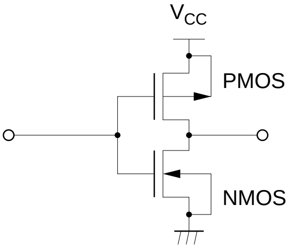
Input pin
Pin: E/SCLK, RS/CS*, RW/SID, IM,
EXT, TEST (MOS without pull-up)


VCC
PMOS
NMOS

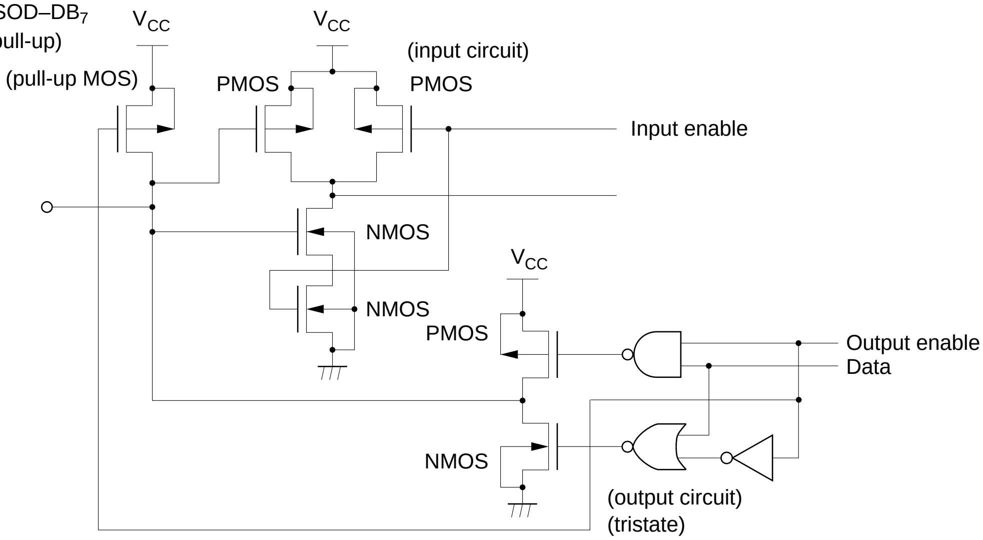
Pins: RESET* (MOS with pull-up)


VCC
PMOS
(pull-up MOS)
VCC
PMOS
NMOS

Output pin
Pins: CL_1, CL_2, M, D

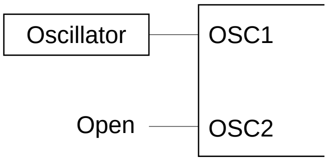

VCC
PMOS
NMOS

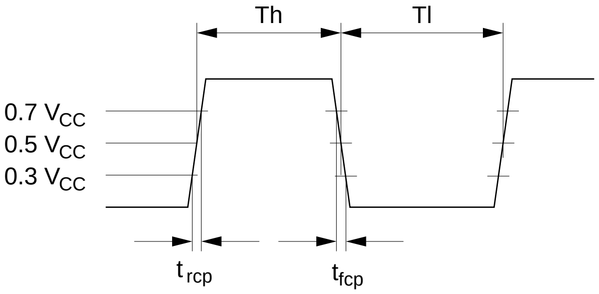
I/O Pin
Pins: DB_0/SOD–DB_7
(MOS with pull-up)


VCC
(pull-up MOS)
VCC
PMOS
(input circuit)
PMOS
Input enable
NMOS
VCC
NMOS
PMOS
Output enable
Data
NMOS
(output circuit)
(tristate)

6. Applies to input pins and I/O pins, excluding the OSC_1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

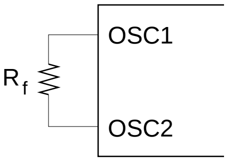
11. Applies only to external clock operation.


Oscillator
OSC1
Open
OSC2


Th
Tl
0.7 V_{CC}
0.5 V_{CC}
0.3 V_{CC}
t_{rcp}
t_{fcp}

$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

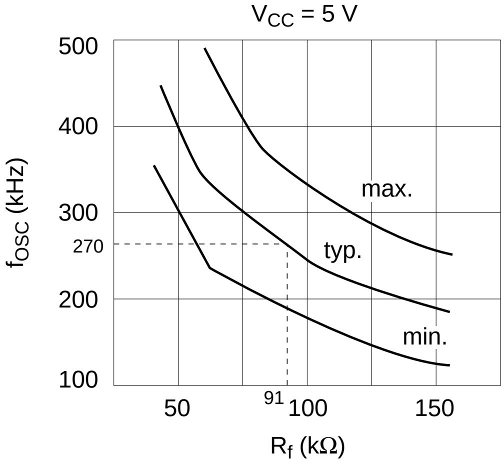
12. Applies only to the internal oscillator operation using oscillation resistor R_f.

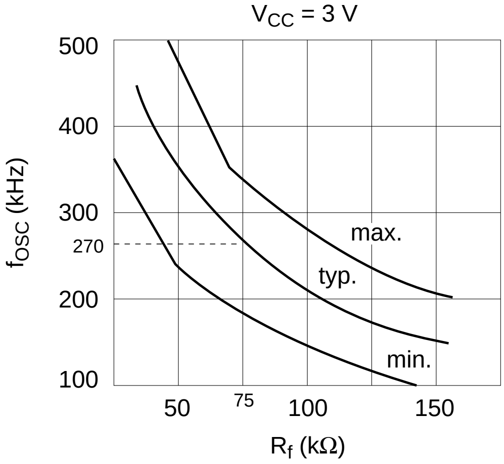

OSC1
R_f
OSC2

R_f: 75 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
R_f: 91 kΩ ± 2% (when V_{CC} = 4 V to 5 V)

Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

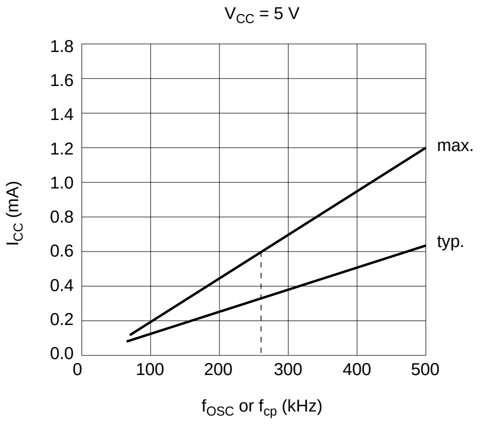


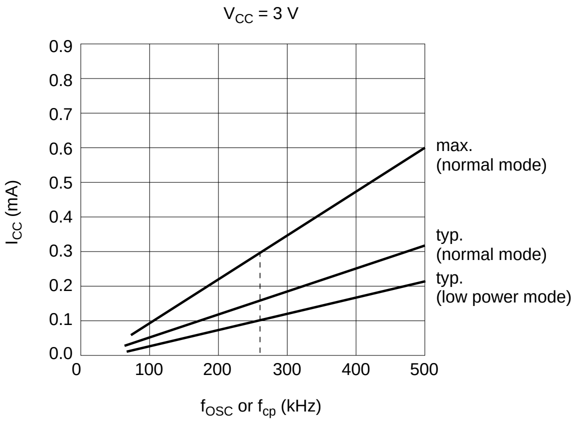


13. R_{COM} is the resistance between the power supply pins (V_{CC}, V_1, V_4, V_5) and each common signal pin (COM_0 to COM_{33}).

R_{SEG} is the resistance between the power supply pins (V_{CC}, V_2, V_3, V_5) and each segment signal pin (SEG_1 to SEG_{60}).

14. The following graphs show the relationship between operation frequency and current consumption.





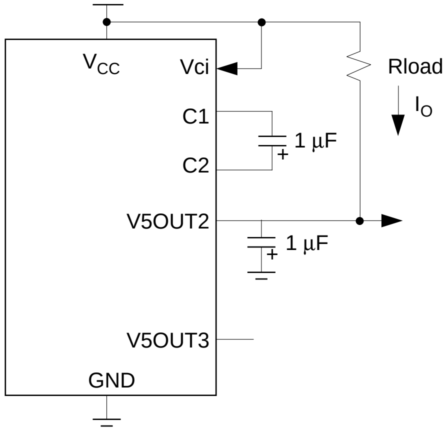
15. Applies to the OSC_1 pin.

16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V_1, V_2, V_3, V_4, V_5) when there is no load.

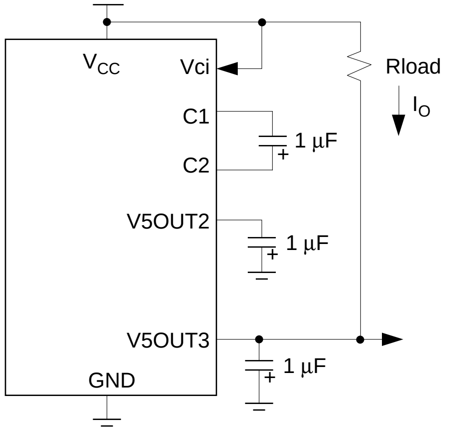
17. The TEST pin must be fixed to ground, and the IM or EXT pin must also be connected to V_{CC} or ground.

18. Booster characteristics test circuits are shown below.

(Boosting twice)


V_{CC}
Vci
C1
C2
V5OUT2
V5OUT3
GND
1 µF
+
1 µF
+
Rload
I_O

(Boosting three times)

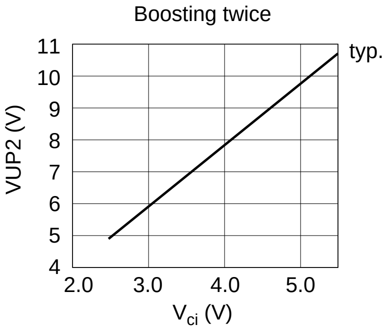

V_{CC}
Vci
C1
C2
V5OUT2
V5OUT3
GND
1 µF
+
1 µF
+
1 µF
+
Rload
I_O

19. Reference data

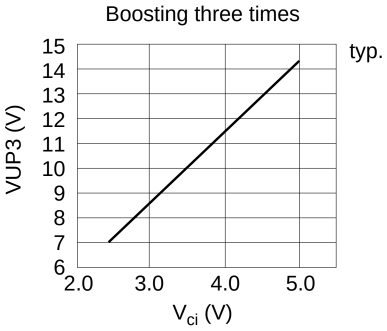
The following graphs show the liquid crystal voltage booster characteristics.

VUP2 = V_{CC}–V5OUT2
VUP3 = V_{CC}–V5OUT3

(1) VUP2, VUP3 vs V_{ci}

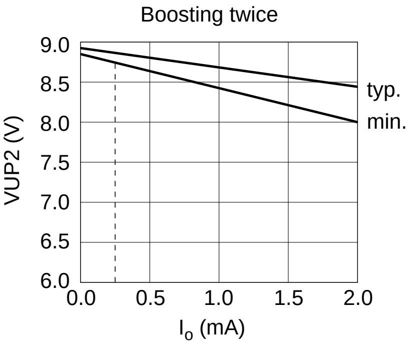


Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz,
T_a = 25°C, Rload = 25 kΩ

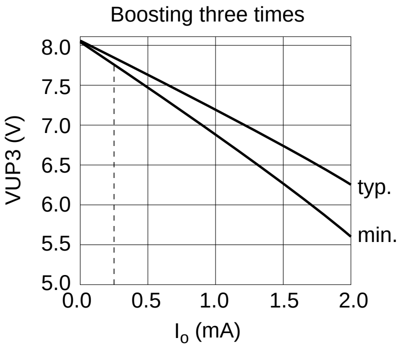


Test condition: $V_{ci} = V_{CC}$, f_{cp} = 270 kHz,
Ta = 25°C, Rload = 25 kΩ

(2) VUP2, VUP3 vs I_o

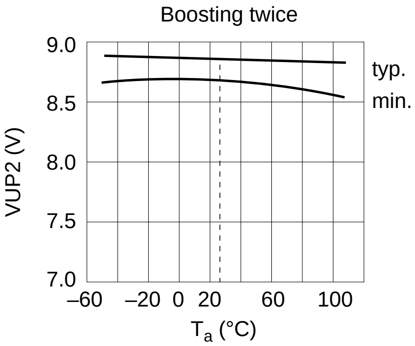


Test condition: $V_{ci} = V_{CC}$ = 4.5 V,
R_f = 91 kΩ, T_a = 25°C

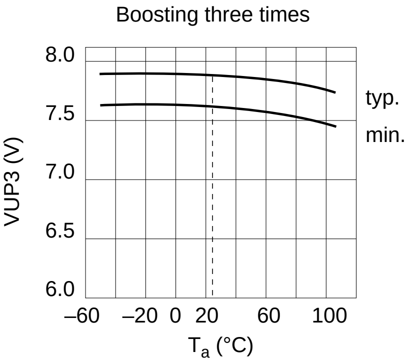


Test condition: $V_{ci} = V_{CC}$ = 2.7 V,
R_f = 75 kΩ, T_a = 25°C

(3) VUP2, VUP3 vs T_a



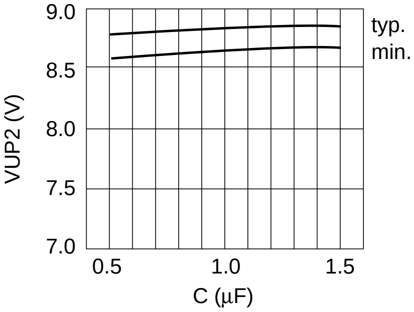
Test condition: $V_{ci} = V_{CC}$ = 4.5 V,
R_f = 91 kΩ, I_o = 0.25 mA



Test condition: $V_{ci} = V_{CC}$ = 2.7 V,
R_f = 75 kΩ, I_o = 0.25 mA

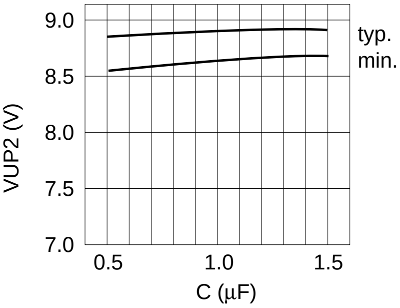
(4) VUP2, VUP3 vs capacitance

Boosting twice



Test condition: $V_{ci} = V_{CC} = 4.5$ V,
$R_f = 91$ kΩ, $I_o = 0.25$ mA

Boosting three times



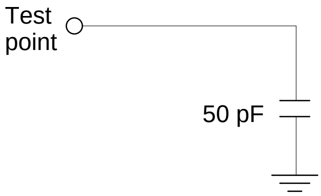
Test condition: $V_{ci} = V_{CC} = 2.7$ V,
$R_f = 75$ kΩ, $I_o = 0.25$ mA

20. Must maintain (“High”) $V_{CC} \geq V_{ci}$ (“Low”).

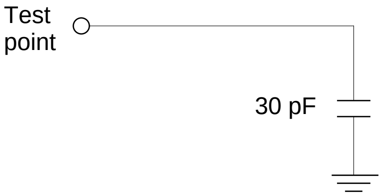
Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0–DB7, SOD


Test point
50 pF

Segment extension signals: CL1, CL2, D, M


Test point
30 pF

Timing Characteristics

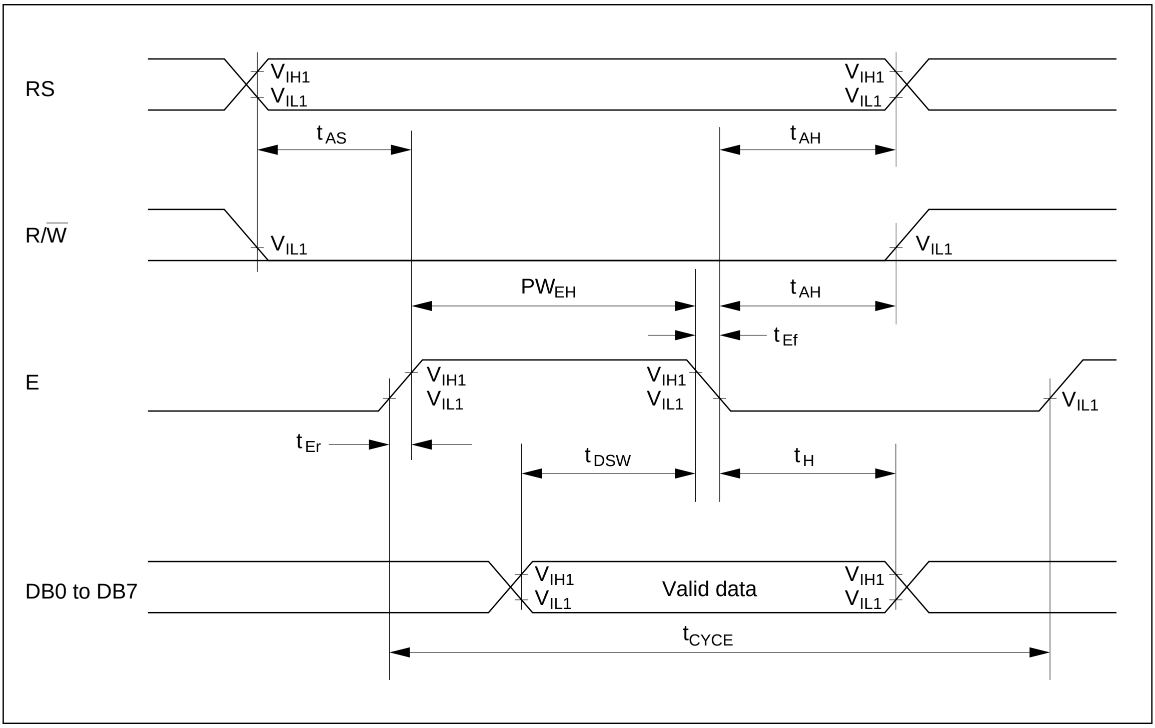

RS
R/W̄
E
DB0 to DB7
V_{IH1}
V_{IL1}
t_{AS}
t_{AH}
PW_{EH}
t_{Ef}
t_{Er}
t_{DSW}
t_H
Valid data
t_{CYCE}

Figure 36 Bus Write Operation

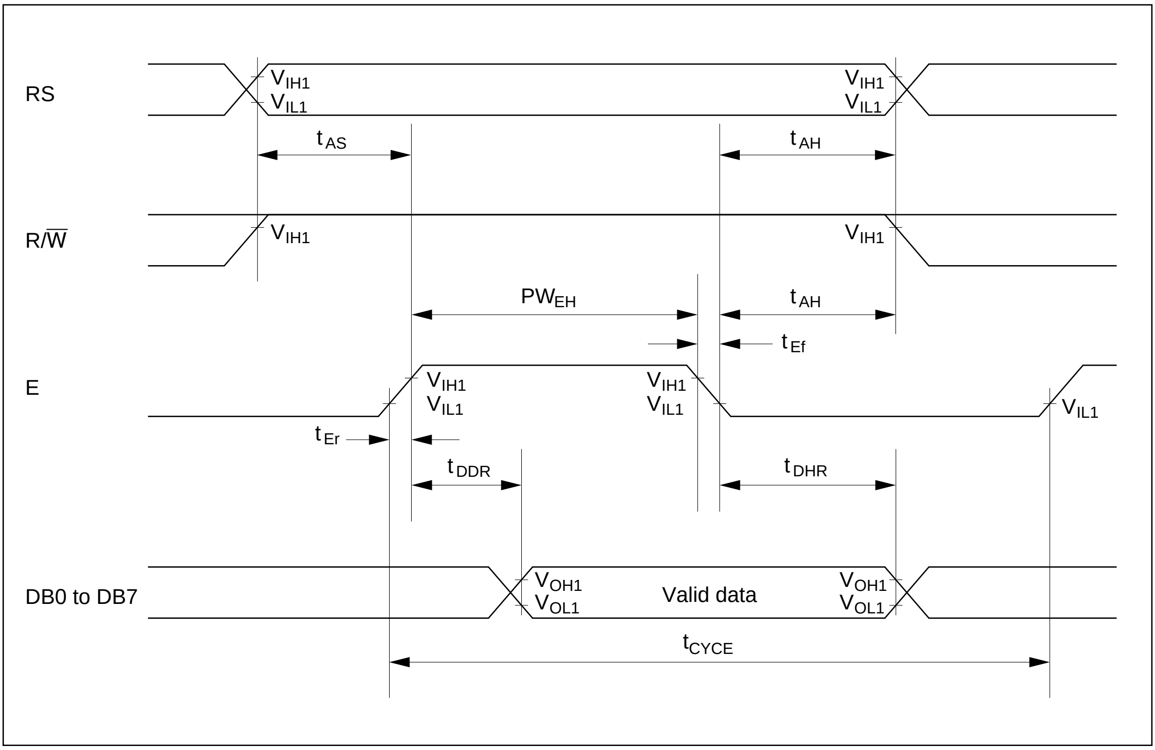

RS
R/W̄
E
DB0 to DB7
V_{IH1}
V_{IL1}
t_{AS}
t_{AH}
PW_{EH}
t_{Ef}
t_{Er}
t_{DDR}
t_{DHR}
V_{OH1}
V_{OL1}
Valid data
t_{CYCE}

Figure 37 Bus Read Operation

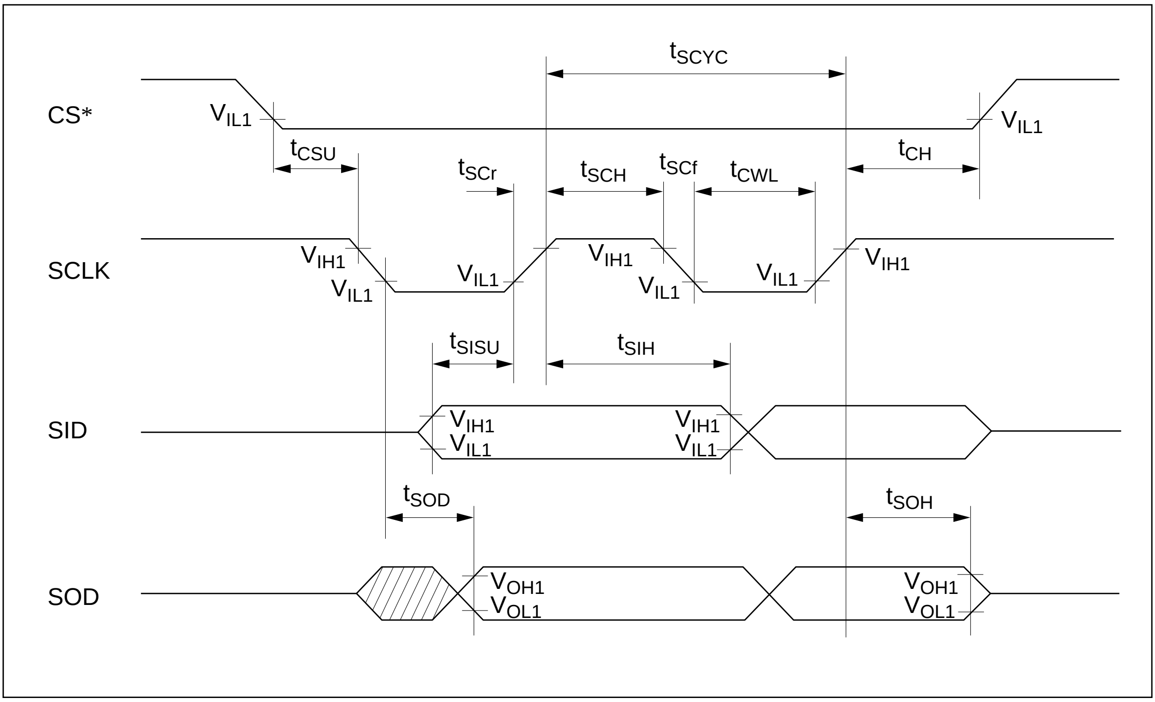

t$_{SCYC}$
CS*
V$_{IL1}$
V$_{IL1}$
t$_{CSU}$
t$_{SCr}$
t$_{SCH}$
t$_{SCf}$
t$_{CWL}$
t$_{CH}$
SCLK
V$_{IH1}$
V$_{IL1}$
V$_{IL1}$
V$_{IH1}$
V$_{IL1}$
V$_{IL1}$
V$_{IH1}$
t$_{SISU}$
t$_{SIH}$
SID
V$_{IH1}$
V$_{IL1}$
V$_{IH1}$
V$_{IL1}$
t$_{SOD}$
t$_{SOH}$
SOD
V$_{OH1}$
V$_{OL1}$
V$_{OH1}$
V$_{OL1}$

Figure 38 Serial Interface Timing

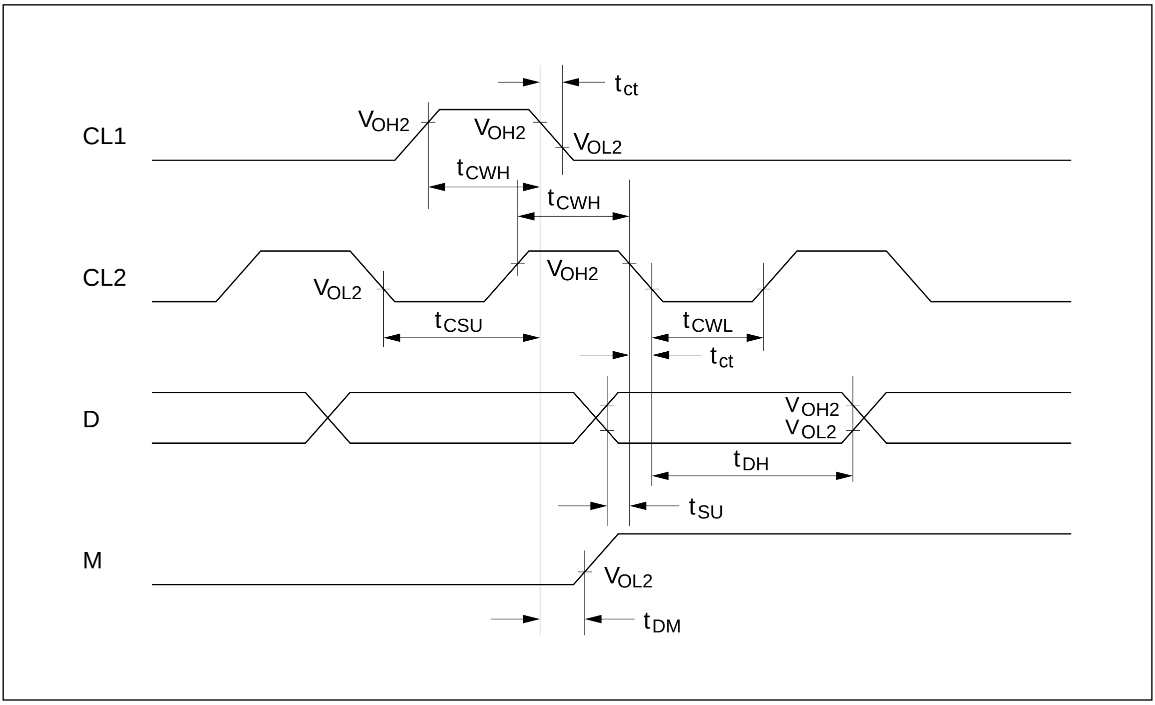
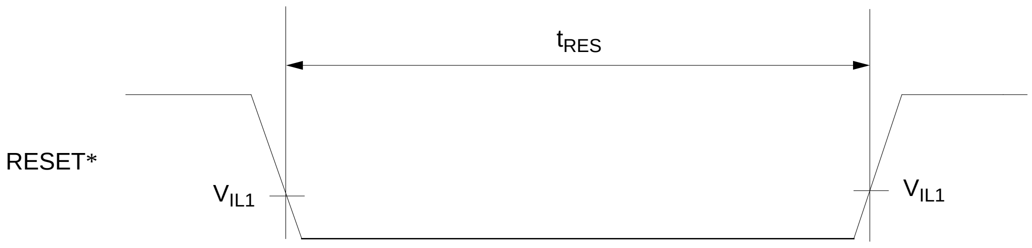
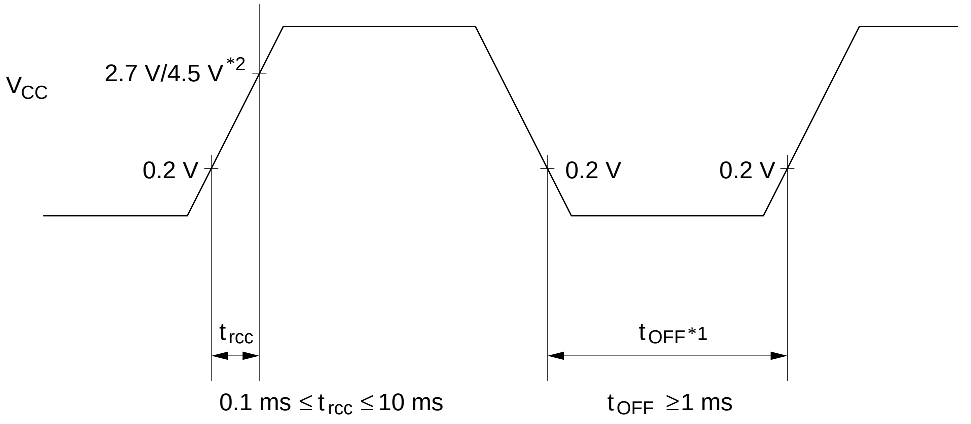

t$_{ct}$
CL1
V$_{OH2}$
V$_{OH2}$
V$_{OL2}$
t$_{CWH}$
t$_{CWH}$
CL2
V$_{OL2}$
V$_{OH2}$
t$_{CSU}$
t$_{CWL}$
t$_{ct}$
D
V$_{OH2}$
V$_{OL2}$
t$_{DH}$
t$_{SU}$
M
V$_{OL2}$
t$_{DM}$

Figure 39 Interface Timing with Extension Driver


t_{RES}
RESET*
V_{IL1}
V_{IL1}

Note: When power is supplied, initializing by the internal reset circuit has priority. Accordingly, the above RESET* input is ignored during internal reset period.

Figure 40 Reset Timing


V_{CC}
2.7 V/4.5 V *2
0.2 V
0.2 V
0.2 V
t_{rcc}
t_{OFF}*1
0.1 ms ≤ t_{rcc} ≤ 10 ms
t_{OFF} ≥1 ms

Notes:
1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, initialized by instruction. (Refer to the Initializing by Instruction section.)

Figure 41 Power Supply Sequence