HD66720 (LCD-II/K8)

(Panel Controller/Driver for Dot-Matrix Liquid Crystal Display with Key-Matrix)

Preliminary

HITACHI

Description

The HD66720 dot-matrix liquid crystal display controller (LCD) and driver LSI incorporates a key-scan function and an LED display function, and displays alphanumeric character and symbols. A single HD66720 is capable of displaying a single 10-character line or two 8-character lines. In addition, a single line of up to 40 characters can be displayed with extension drivers.

Since the HD66720 incorporates a 5 × 6 matrix key scan circuit and two LED drive circuits, it can control front panels of telephone, car stereos, audio equipment, printers, or facsimiles with a single chip. A three-line clock synchronous serial transfer method is adopted for interfacing with a microcomputer, which greatly decreases the number of interface signals and makes it easy to miniaturize systems.

This LSI is especially suitable for panels which can display five European languages (English, French, German, Italian, and Spanish), as used in new media products including car tuners for the radio data system (RDS), mini disc players (MD), and digital compact cassette players (DCC), personal handly phone, cellular phone.

Features

- Control and drive of a dot matrix LCD with built-in scanning
- Wide field-of-division display with low duty cycle of 1/9 (1 line) and 1/17 (2 lines)
- 10-character single line (5 × 8-dot font) and 50-segment display with a single chip (two 8-character line display by setting a register)
- Maximum 40-character single line display with extension drivers (see list 1)
- Built-in key scan matrix buffer circuit: 5 × 6 (30 keys) input (at strobe cycle: 5 ms to 40 ms, f_{osc} = 160 kHz)
- Wake-up function with IRQ signal after key stroke
- Two general purpose output ports (for LED displays, etc.)
- Serial bus interface: Three-line clock synchronous serial transfer
- Booster for liquid crystal drive voltage: Two/three times power supply
- Maximum 40-character display RAM
- Character generator ROM: 240 5 × 8-dot characters
- Character generator RAM: 8 user characters
- 80-segment RAM
- Horizontal smooth scroll: Displayed line selection and displayed character selection scroll possible
- Oscillator (external resistor needed) and power-on reset circuit incorporated
- Wide range of operating power supply voltage: 2.7 to 5.5 V
  Liquid crystal display voltage: 3.0 to 11.0 V
- QFP 1420-100 (0.65-mm pitch), TQFP 1414-100 (0.5-mm pitch), bare-chip

Hitachi semiconductor

List 1 Programmable Duty Cycles

		5-Dot Font Width					
		Single-Chip Operation		With Single HD44100R		Maximum Display Extension	
Number of Lines	Duty Ratio	Displayed Characters	Segments	Displayed Characters	Segments	Displayed Characters	Segments
1	1/9	10	50	18	80	40	80
2	1/17	8	42	16	80	20	82

		6-Dot Font Width					
		Single-Chip Operation		With Single HD44100R		Maximum Display Extension	
Number of Lines	Duty Ratio	Displayed Characters	Segments	Displayed Characters	Segments	Displayed Characters	Segments
1	1/9	8	50	15	90	40	96
2	1/17	7	42	13	82	20	96

List 2 Ordering Information

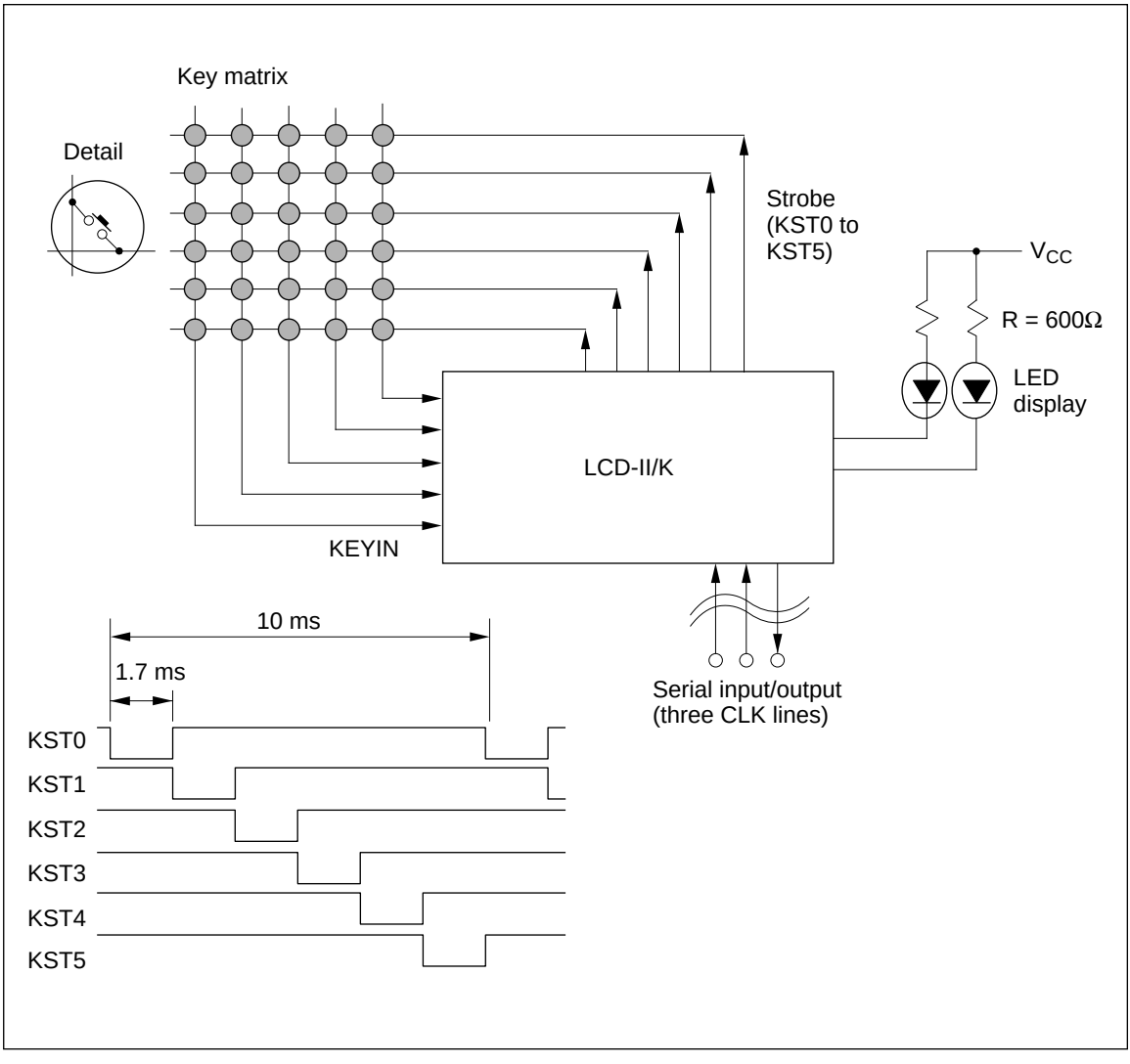
Type No.	Package	CGROM
HD66720A03FS	FP-100A	Japanese + European font
HD66720A03TF	TFP-100B	
HCD66720A03	Chip	

LCD-II Family Comparison

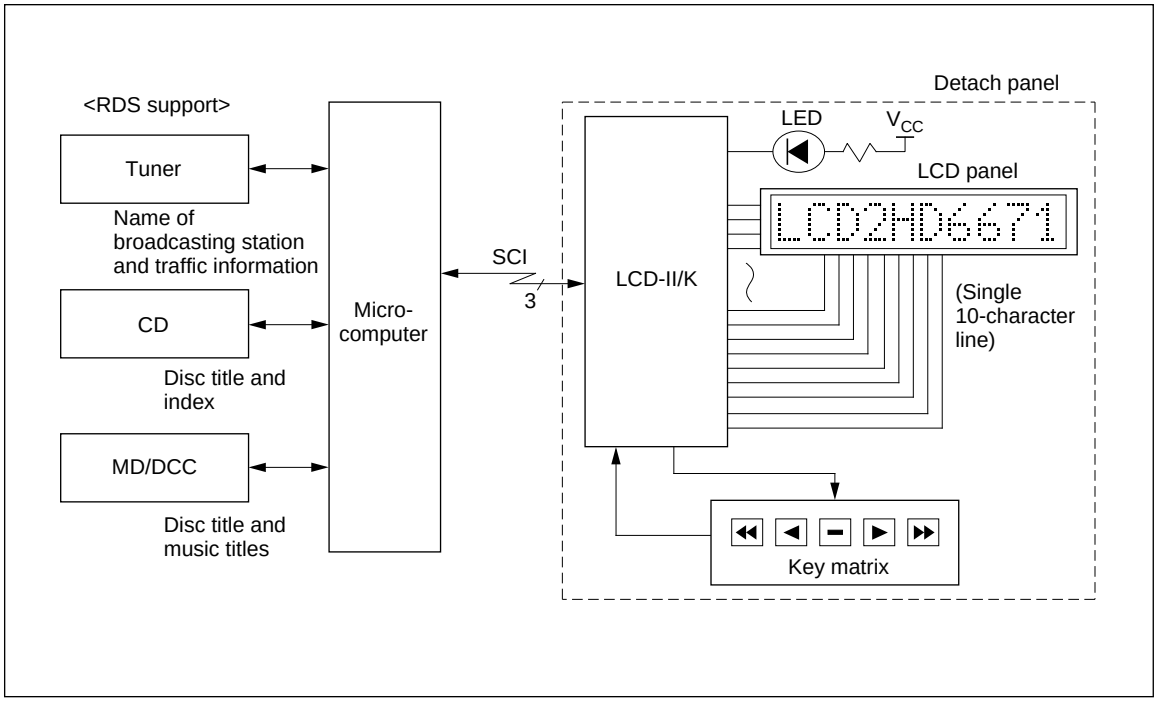
Item	LCD-II HD44780U	LCD-II/E20 HD66702R	LCD-II/F8 HD66710	LCD-II/F12 HD66712	LCD-II/K8 HD66720
Power supply voltage	2.7 V to 5.5 V	5 V ± 10% (standard), 2.7 V to 5.5 V (low voltage)	2.7 V to 5.5 V	2.7 V to 5.5 V	2.7 V to 5.5 V
Liquid crystal drive voltage	3.0 V to 11.0 V	3.0 V to 8.3 V	3.0 V to 13.0 V	3.0 V to 13.0 V	3.0 V to 11.0 V
Maximum display characters per chip	8 characters × 2 lines	20 characters × 2 lines	16 characters × 2 lines/ 8 characters × 4 lines	24 characters × 2 lines/ 12 characters × 4 lines	10 characters × 1 line/ 8 characters × 2 lines
Segment display	None	None	40 segments	60 segments (80 segments with extension)	50 segments (80 segments with extension)
Display duty cycle	1/8, 1/11, 1/16	1/8, 1/11, 1/16	1/17, 1/33	1/17, 1/33	1/9, 1/17
Key scan circuit	None	None	None	None	5 × 6 (30 circuits)
LED display circuit	None	None	None	None	2 circuits
CGROM	9,920 bits (208 5 × 8-dot characters and 32 5 × 10-dot characters)	7,200 bits (160 5 × 7-dot characters and 32 5 × 10-dot characters)	9,600 bits (240 5 × 8-dot characters)	9,600 bits (240 5 × 8-dot characters)	9,600 bits (240 5 × 8-dot characters)
CGRAM	64 bytes	64 bytes	64 bytes	64 bytes	64 bytes
DDRAM	80 bytes	80 bytes	80 bytes	80 bytes	40 bytes
SEGRAM	None	None	8 bytes	16 bytes	16 bytes
Segment signal	40 signals	100 signals	40 signals	60 signals	50 signals (42 signals)
Common signal	16 signals	16 signals	33 signals	34 signals	9 signals (17 signals)
Liquid crystal waveform	A	B	B	B	B

Item		LCD-II HD44780U	LCD-II/E20 HD66702R	LCD-II/F8 HD66710	LCD-II/F12 HD66712	LCD-II/K8 HD66720
Clock generator	Clock source	External resistor External clock input	External resistor External clock input	External resistor External clock input	External resistor External clock input	External resistor External clock input
	Rf oscillation frequency	270 kHz ± 30%	320 kHz ± 30%	270 kHz ± 30%	270 kHz ± 30%	160 kHz ± 30%
	Frame frequency	59 to 110 Hz for 1/8 and 1/16 duty cycles; 43 to 80 Hz for 1/11 duty cycle	70 to 130 Hz for 1/8 and 1/16 duty cycles; 51 to 95 Hz for 1/11 duty cycle	56 to 103 Hz for 1/7 duty cycles; 57 to 106 Hz for 1/33 duty cycle	56 to 103 Hz for 1/7 duty cycles; 57 to 106 Hz for 1/33 duty cycle	58 to 108 Hz for 1/9 duty cycles; 62 to 115 Hz for 1/17 duty cycle
	Rf resistance	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	68 kΩ for standard version; 56 kΩ for L version	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	91 kΩ for 5-V operation; 75 kΩ for 3-V operation	200 kΩ for 5-V operation; 160 kΩ for 3-V operation
Liquid crystal display voltage booster circuit		None	None	2–3 times step-up circuit	2–3 times step-up circuit	2–3 times step-up circuit
Extension driver control signal		Independent control signal	Independent control signal	Used in common with a driver output pin	Independent control signal	Independent control signal
Reset function		Internal reset	Internal reset	Internal reset	Internal reset and input	Internal reset and input
Instructions		LCD-II (HD44780)	Fully compatible with the LCD-II	Upwardly compatible with the LCD-II	Upwardly compatible with the LCD-II	Upwardly compatible with the LCD-II
Horizontal scroll		Character unit	Character unit	Dot unit	Dot unit and line unit scroll	Dot unit and line unit scroll
Number of displayed lines		1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1 or 2
Low power mode		None	None	Available	Available	Available
Bus interface		4 bits/8 bits	4 bits/8 bits	4 bits/8 bits	Serial/4 bits/ 8 bits	Serial
CPU bus timing		2 MHz for 5-V operation; 1 MHz for 3-V operation	1 MHz	2 MHz for 5-V operation; 1 MHz for 3-V operation	2 MHz for 5-V operation; 1 MHz for 3-V operation	2 MHz for 5-V operation; 1 MHz for 3-V operation
Package		QFP-1420-80 TQFP-1414-80 80-pin bare chip	LQFP-2020-144 144-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip	QFP-1420-128 TCP-128 128-pin bare chip	QFP-1420-100 TQFP-1414-100 100-pin bare chip

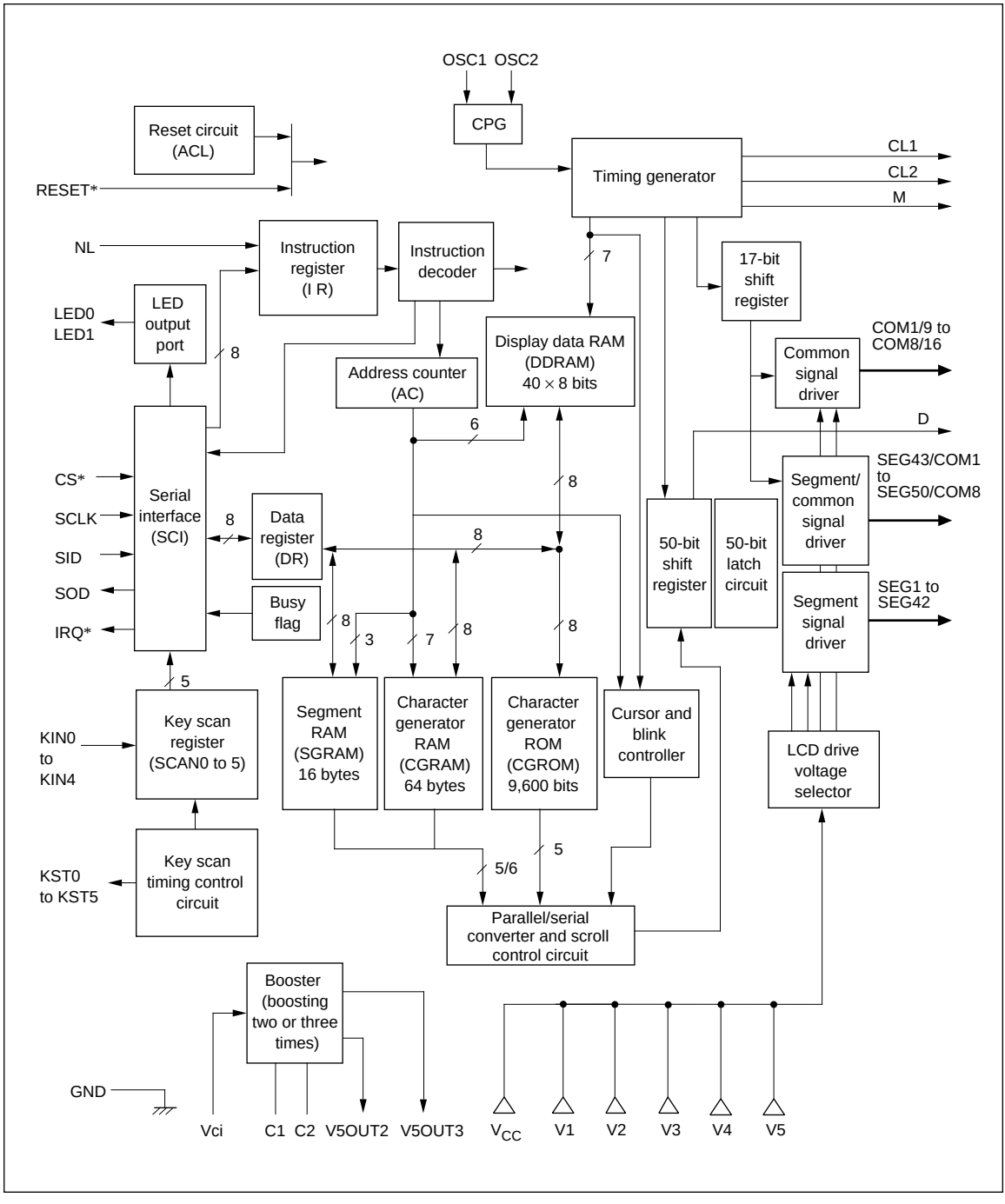
Key Input Sampling and LED Display



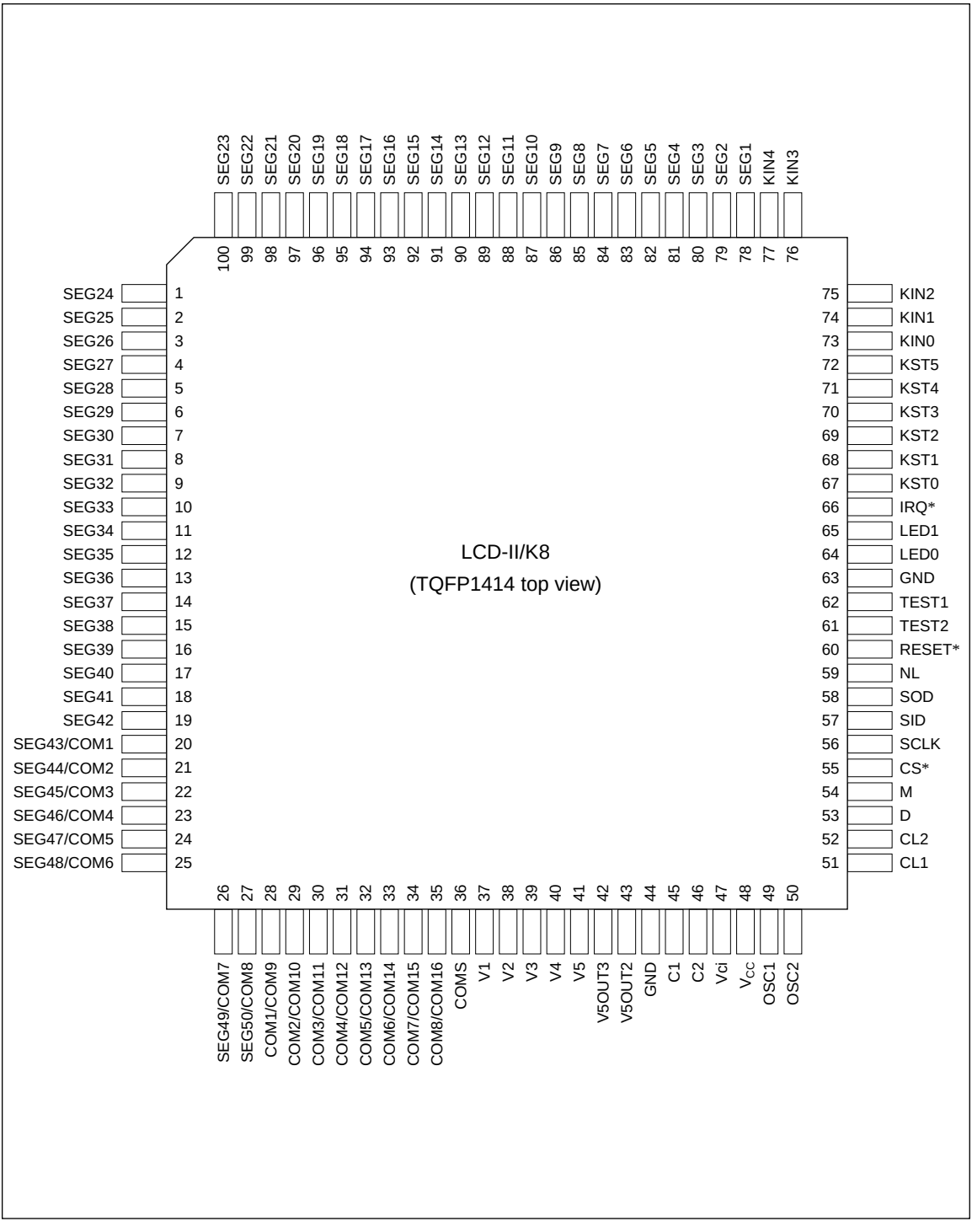
Application Example for Car Stereo

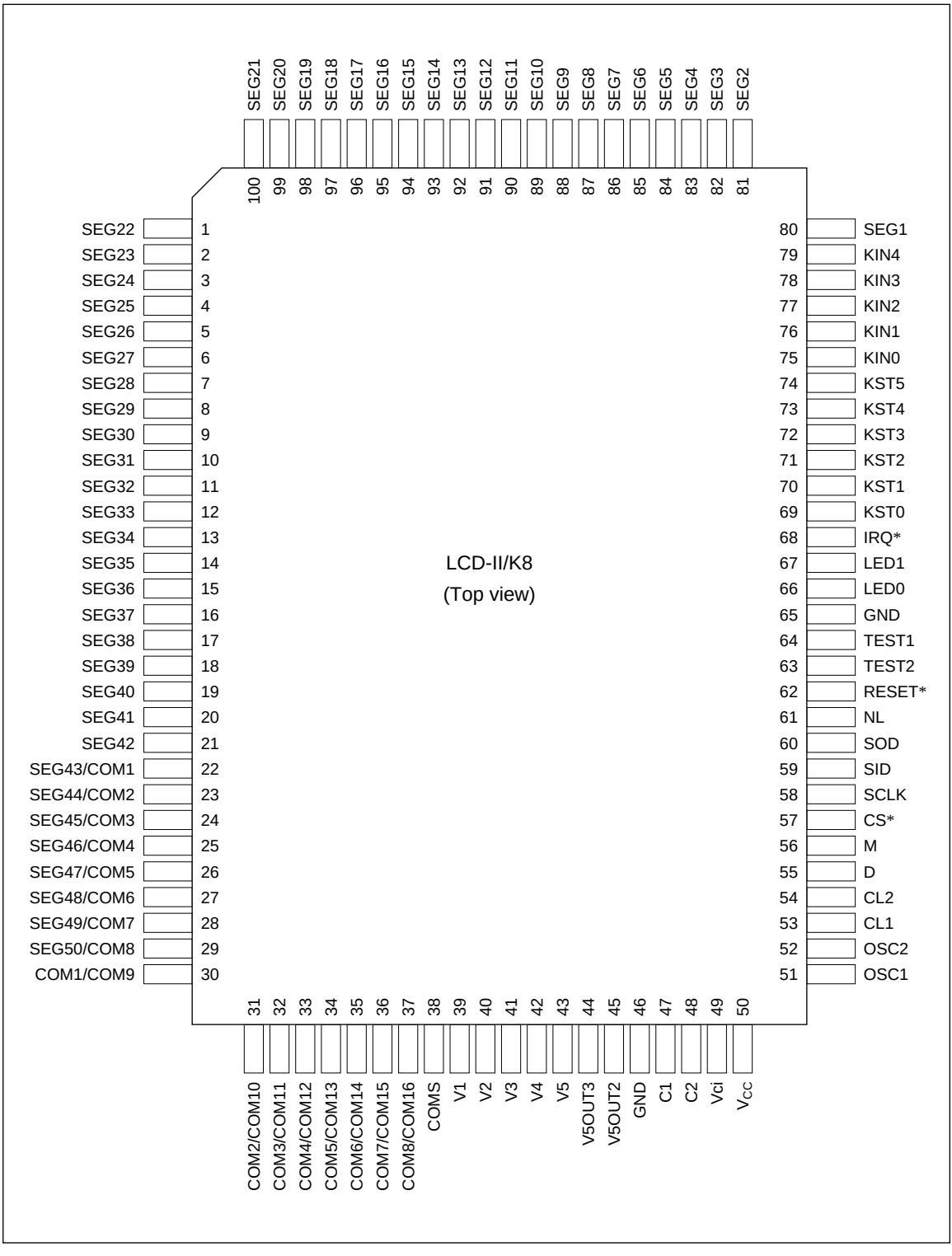


Block Diagram

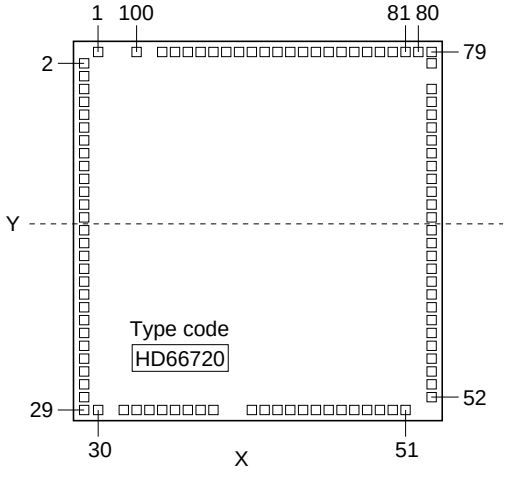


Pin Arrangement




LCD-II/K8
(Top view)
1 SEG22
2 SEG23
3 SEG24
4 SEG25
5 SEG26
6 SEG27
7 SEG28
8 SEG29
9 SEG30
10 SEG31
11 SEG32
12 SEG33
13 SEG34
14 SEG35
15 SEG36
16 SEG37
17 SEG38
18 SEG39
19 SEG40
20 SEG41
21 SEG42
22 SEG43/COM1
23 SEG44/COM2
24 SEG45/COM3
25 SEG46/COM4
26 SEG47/COM5
27 SEG48/COM6
28 SEG49/COM7
29 SEG50/COM8
30 COM1/COM9
31 COM2/COM10
32 COM3/COM11
33 COM4/COM12
34 COM5/COM13
35 COM6/COM14
36 COM7/COM15
37 COM8/COM16
38 COMS
39 V1
40 V2
41 V3
42 V4
43 V5
44 V5OUT3
45 V5OUT2
46 GND
47 C1
48 C2
49 Vci
50 VCC
51 OSC1
52 OSC2
53 CL1
54 CL2
55 D
56 M
57 CS*
58 SCLK
59 SID
60 SOD
61 NL
62 RESET*
63 TEST2
64 TEST1
65 GND
66 LED0
67 LED1
68 IRQ*
69 KST0
70 KST1
71 KST2
72 KST3
73 KST4
74 KST5
75 KIN0
76 KIN1
77 KIN2
78 KIN3
79 KIN4
80 SEG1
81 SEG2
82 SEG3
83 SEG4
84 SEG5
85 SEG6
86 SEG7
87 SEG8
88 SEG9
89 SEG10
90 SEG11
91 SEG12
92 SEG13
93 SEG14
94 SEG15
95 SEG16
96 SEG17
97 SEG18
98 SEG19
99 SEG20
100 SEG21

HCD66720



Chip size (XxY): 5.60 mm × 6.0 mm
Coordinate: Pad center
Origin: Chip center
Pad size (X x Y): 100 μm × 100 μm

(Unit: μm)

Pad No.	Function	Coordinate X	Coordinate Y
1	SEG22	–2400	2877
2	SEG23	–2677	2700
3	SEG24	–2677	2500
4	SEG25	–2677	2300
5	SEG26	–2677	2100
6	SEG27	–2677	1900
7	SEG28	–2677	1700
8	SEG29	–2677	1500
9	SEG30	–2677	1300
10	SEG31	–2677	1100
11	SEG32	–2677	900
12	SEG33	–2677	700
13	SEG34	–2677	500
14	SEG35	–2677	300
15	SEG36	–2677	100
16	SEG37	–2677	–100
17	SEG38	–2677	–300
18	SEG39	–2677	–500
19	SEG40	–2677	–700
20	SEG41	–2677	–900
21	SEG42	–2677	–1100
22	SEG43/COM1	–2677	–1300
23	SEG44/COM2	–2677	–1500
24	SEG45/COM3	–2677	–1700
25	SEG46/COM4	–2677	–1900
26	SEG47/COM5	–2677	–2100
27	SEG48/COM6	–2677	–2300
28	SEG49/COM7	–2677	–2677
29	SEG50/COM8	–2677	–2877
30	COM1/COM9	–2400	–2877
31	COM2/COM10	–1900	–2877
32	COM3/COM11	–1700	–2877
33	COM4/COM12	–1500	–2877
34	COM5/COM13	–1300	–2877

Pad No.	Function	Coordinate X	Coordinate Y
35	COM6/COM14	–1100	–2877
36	COM7/COM15	–900	–2877
37	COM8/COM16	–700	–2877
38	COMS	–500	–2877
39	V1	–150	–2853
40	V2	100	–2853
41	V3	300	–2853
42	V4	500	–2853
43	V5	800	–2853
44	V5OUT3	1020	–2809
45	V5OUT2	1200	–2809
46	GND	1400	–2790
47	C1	1600	–2853
48	C2	1800	–2809
49	VCI	2000	–2809
50	VCC	2200	–2853
51	OSC1	2400	–2853
52	OSC2	2653	–2700
53	CL1	2653	–2500
54	CL2	2653	–2300
55	D	2653	–2100
56	M	2653	–1900
57	CS*	2653	–1700
58	SCLK	2653	–1500
59	SID	2653	–1300
60	SOD	2653	–1100
61	NL	2653	–900
62	RESET*	2653	–700
63	TEST2	2653	–500
64	TEST1	2653	–300
65	GND	2653	–30
66	LED0	2653	174
67	LED1	2653	350
68	IRQ*	2653	540

Pad No.	Function	Coordinate X	Coordinate Y
69	KST0	2653	730
70	KST1	2653	920
71	KST2	2653	1110
72	KST3	2653	1300
73	KST4	2653	1500
74	KST5	2653	1700
75	KIN0	2653	1900
76	KIN1	2653	2100
77	KIN2	2653	2300
78	KIN3	2653	2653
79	KIN4	2653	2853
80	SEG1	2400	2877
81	SEG2	1900	2877
82	SEG3	1700	2877
83	SEG4	1500	2877
84	SEG5	1300	2877
85	SEG6	1100	2877
86	SEG7	900	2877
87	SEG8	700	2877
88	SEG9	500	2877
89	SEG10	300	2877
90	SEG11	100	2877
91	SEG12	–100	2877
92	SEG13	–300	2877
93	SEG14	–500	2877
94	SEG15	–700	2877
95	SEG16	–900	2877
96	SEG17	–1100	2877
97	SEG18	–1300	2877
98	SEG19	–1500	2877
99	SEG20	–1700	2877
100	SEG21	–1900	2877

Pin Functions

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
CS*	1	I	MPU	Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
SCLK	1	I	MPU	Acts as a serial clock input (receive).
SID	1	I	MPU	Inputs serial data during serial mode.
IRQ*	1	O	MPU	Generates key scan interrupt signal.
SOD	1	O	MPU	Outputs (transmits) serial data during serial mode. Open this pin if reading (transmission) is not performed.
SEG_1 to SEG_{42}	42	O	LCD	Acts as a segment output signal.
SEG_{43}/ COM_1 to SEG_{50}/ COM_8	8	O	LCD	Acts as segment output during 1-line display mode. Acts as common output during 2-line display mode.
COM_1/ COM_9 to COM_8/ COM_{16}	8	O	LCD	Acts as common output during 1-line display mode. Acts as common output during 2-line display mode.
COMS	1	O	LCD	Common output signal for segment (icon).
CL1	1	O	Extension driver	Outputs the extension driver latch pulse.
CL2	1	O	Extension driver	Outputs the extension driver shift clock.
D	1	O	Extension driver	Outputs extension driver data; data from the 51st dot on is output during single-line display, and data from the 43rd dot on is output during two-line display.
M	1	O	Extension driver	Outputs the extension driver AC signal.
KST0* to KST5*	6	O	Key matrix	Generates strobe signals for latching data from the key matrix at specific time intervals.
KIN0* to KIN4*	5	I	Key matrix	Samples key state from key matrix synchronously with strobe signals.
LED0* to LED1*	2	O	LEDs	LED display control signals; can also be used as a general output port.
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{CC} –V5 = 11 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC1/OSC2	2	—	Oscillation resistor clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC1.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Keep this voltage within the range: 2.0 V to 4.5 V without exceeding V_{CC}.
V5OUT2	1	O	V5 pin/ Booster capacitor	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitor	External capacitor should be connected here when using the booster.
RESET*	1	I	—	Reset pin. When active (low), this pin turns the display off and initializes the registers.
NL	1	I	—	Number of display lines. One line is displayed when this pin is low (1/9 duty), and two lines are displayed when this pin is high (1/17 duty).
TEST	2	I	—	Test pin. Should be wired to ground.

Block Function

System Interface

The HD66720 interfaces with the system through a three-line clock-synchronous serial method. This greatly decreases the number of interface connections with the MPU because all data transmission/reception, such as setting registers, writing data to RAM, and reading key-scan data can be performed with three control signals.

The HD66720 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for the display data RAM (DD RAM), the character generator RAM (CG RAM), and the segment RAM (SEG RAM). The IR can only be written to by the MPU, and cannot be read from.

The DR temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the DR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by an internal operation. The DR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. When address information is written into the IR, data is read and then stored into the DR from DD RAM, CG RAM, or SEG RAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DD RAM, CG RAM, or SEG RAM at the next address is sent to the DR for the next read from the MPU.

These two registers can be selected by the RS bit in start byte data in synchronized serial interface (table 2). For detail, refer to Transferring Serial Data.

Busy Flag (BF)

When the busy flag is 1, the HD66720 is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/W = 1 (table 2), the busy flag is output from DB7. The next instruction must be written after ensuring that the busy flag is 0.

Key Scan Register (SCAN0 to SCAN5)

Scanning from the key matrix senses the key state at the rising edge of key strobe signals (KST0 to KST5) output from the HD66720. These strobe signals sample 5 states: KIN0 to KIN4, enabling key scan of 30 types.

Key states KIN0 to KIN4 sampled by key strobe signal KST0 is latched to register SCAN0. In the same way, data sampled with strobe signals KST1 to KST5 are latched to registers SCAN1 to SCAN5, respectively. For details, refer to Key Scan Control.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB_7) and key scan register (DB_0 to DB_4)
1	0	DR write as an internal operation (DR to DD RAM, CG RAM, or SEGRAM)
1	1	DR read as an internal operation (DD RAM, CG RAM, or SEGRAM to DR)

Address Counter (AC)

The address counter (AC) assigns addresses to DD RAM, CG RAM, or SEGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DD RAM, CG RAM, and SEG RAM is also determined concurrently by the instruction.

After writing into (reading from) DD RAM, CG RAM, or SEG RAM, the AC is automatically incremented by 1 (decremented by 1).

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 40 × 8 bits, or 40 characters. The area in display data RAM (DD RAM) that is not used for display can be used as buffer data RAM when scrolling.

The DD RAM address (ADD) is set in the address counter (AC) as a hexadecimal number, as shown in figure 1.

The relationship between DD RAM addresses and positions on the liquid crystal display is described and shown on the following pages for a variety of cases.

- 1-line display (NL = low)

  — Case 1: When there are fewer than 40 display characters, the display begins at the beginning of DD RAM. For example, when 10 5-dot font-width characters are displayed using one HD66720, the display is generated as shown in figure 3.

  When a display shift is performed, the DD RAM addresses shift as shown.

  When 8 6-dot font-width characters are displayed using one HD66720, the display is generated as shown in figure 3.

  When a display shift is performed, the DD RAM addresses shift as shown.

  — Case 2: Figure 4 shows the case where the HD66720 and the 40-output extension driver are used to display 15 6-dot font-width characters.

  When a display shift is performed, the DD RAM addresses shift as shown in the figure.

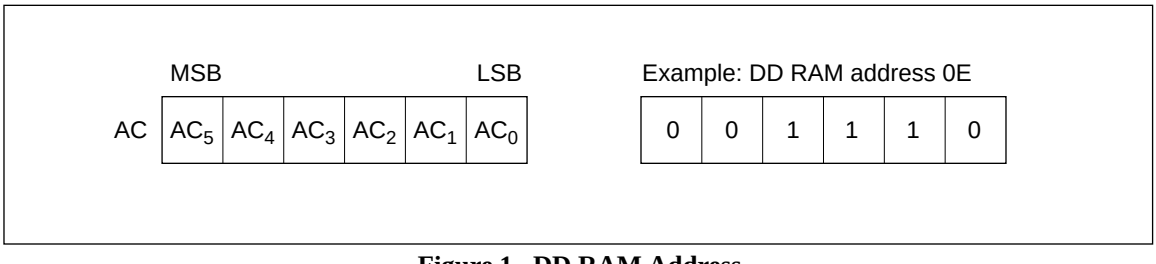


Figure 1 DD RAM Address

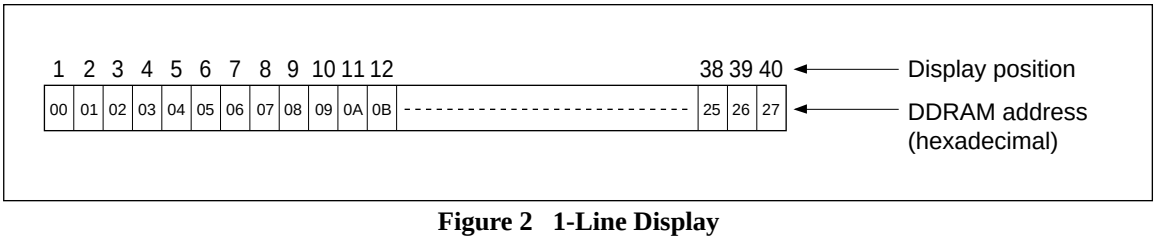


Figure 2 1-Line Display

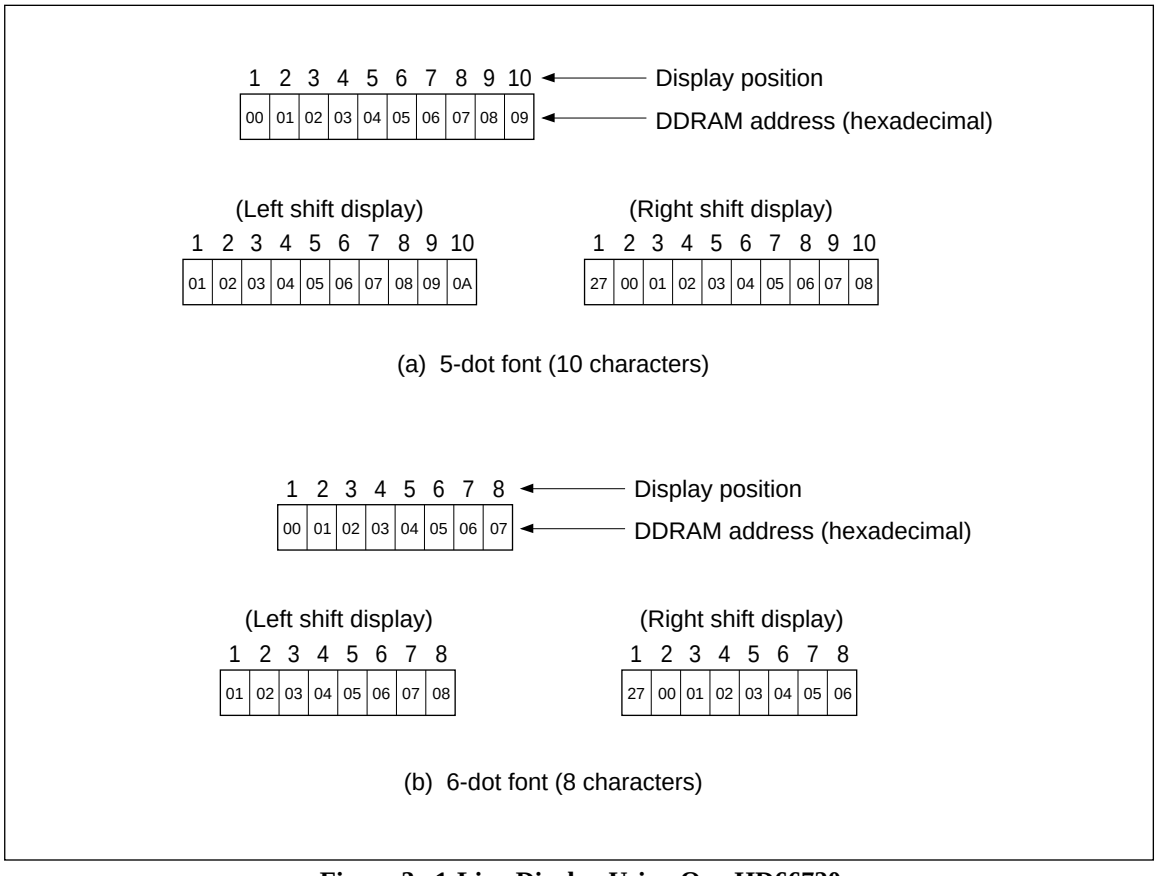


Figure 3 1-Line Display Using One HD66720

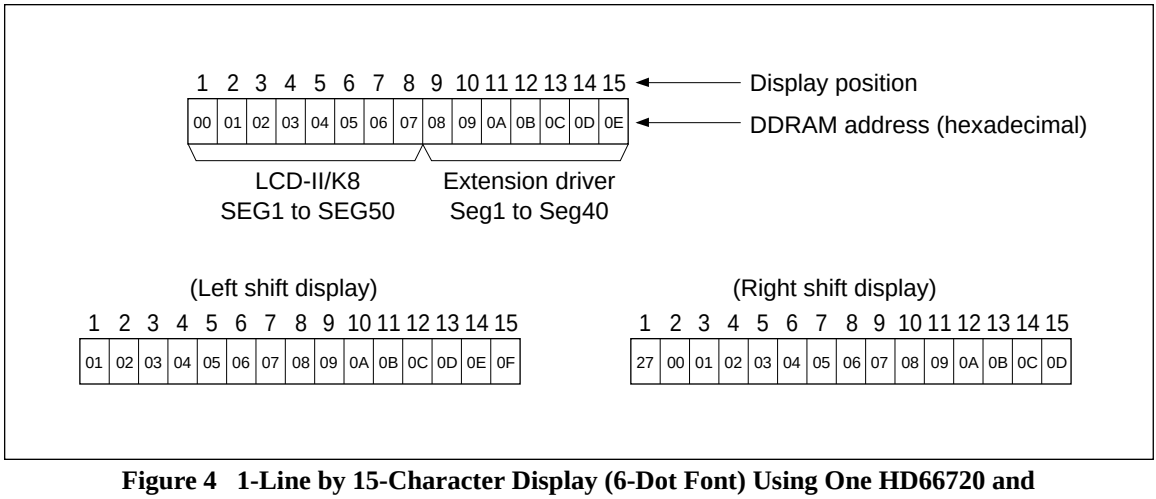


Figure 4 1-Line by 15-Character Display (6-Dot Font) Using One HD66720 and One Extension Driver

- 2-line display (NL = 1)

  — Case 1: The first line is displayed from COM1 to COM8, and the second line is displayed from COM9 to COM16. Note that the last address of the first line and the first address of the second line are not consecutive. Figure 6 shows an example where a 5-dot font-width 8 × 2-line display is performed using one HD66720.

  When a display shift is performed, the DD RAM addresses shift as shown.

  — Case 2: Figure 6 shows an example where a 5-dot font-width 16 × 2-line display is performed using one HD66720 and one extension driver.

  When a display shift is performed, the DDRAM addresses shift as shown.

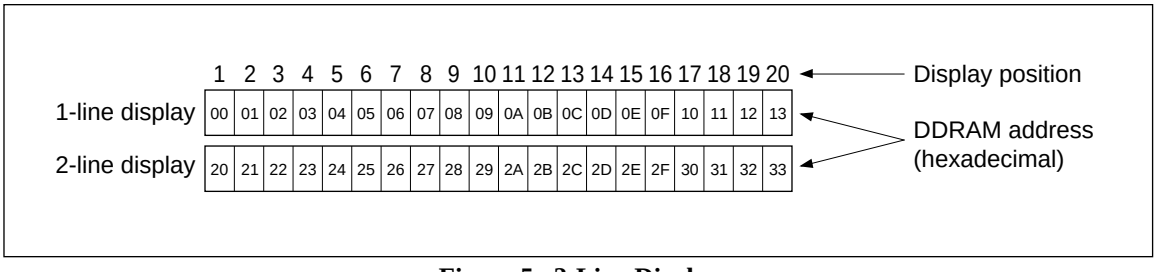


Figure 5 2-Line Display

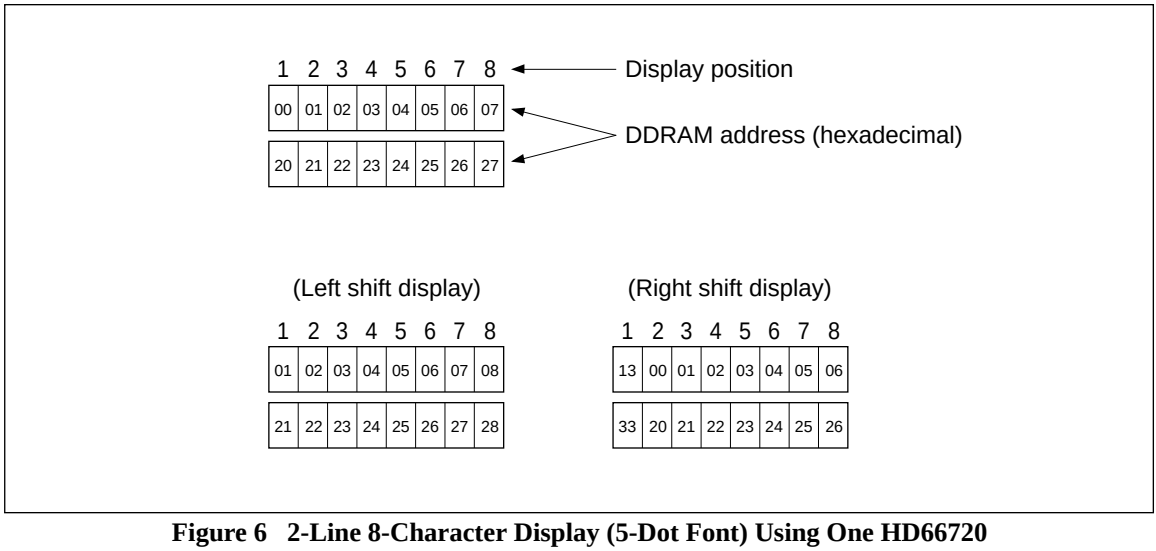


Figure 6 2-Line 8-Character Display (5-Dot Font) Using One HD66720

Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 8 dot character patterns from 8-bit character codes (table 3 to 5). It can generate 240 5 × 8 dot character patterns. User-defined character patterns are also available using a mask-programmed ROM (see Modifying Character Patterns).

Character Generator RAM (CG RAM)

The character generator RAM allows the user to redefine the character patterns. In the case of 5 × 8 characters, up to eight may be redefined.

Write the character codes at the addresses shown as the left column of table 6 to show the character patterns stored in CG RAM.

See table 6 for the relationship between CG RAM addresses and data and display patterns.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to enable control of segments such as an icon and a mark by the user program. Data is read from SEG RAM and is output via the COMS pin to perform segment display. As shown in table 7, bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM. Scrolling or display shifting will not be performed.

SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

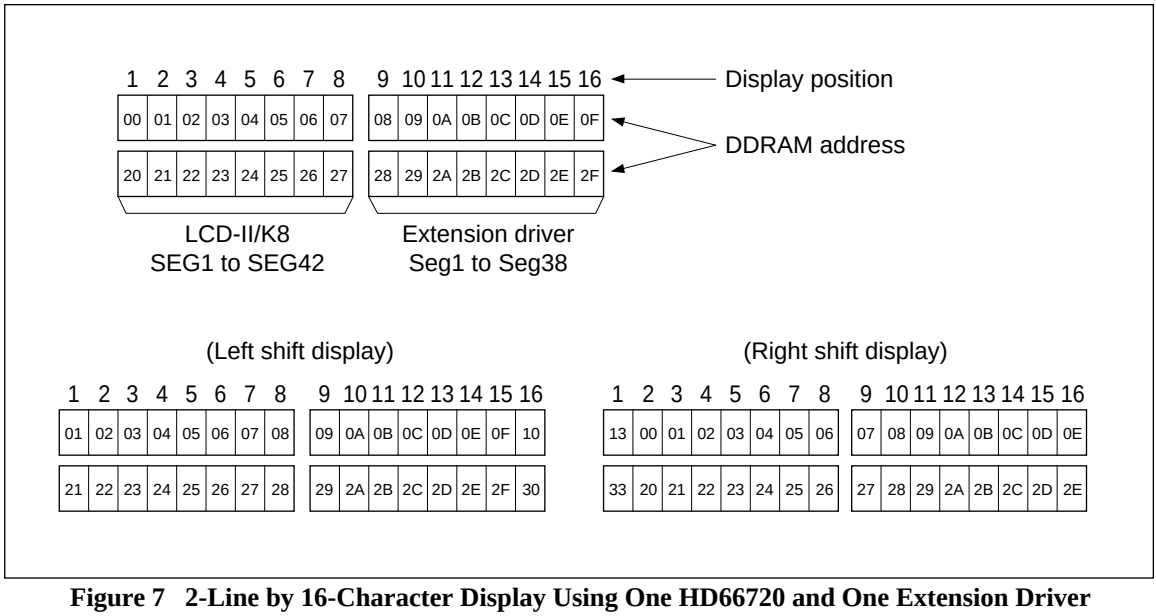


Figure 7 2-Line by 16-Character Display Using One HD66720 and One Extension Driver

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DD RAM, CG ROM, CG RAM, and SEG RAM. RAM read timing for display and internal operation timing by MPU access are generated in a time sharing method. Therefore, when writing data to DD RAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of common signal drivers and segment signal drivers. For a 1-line display, there will be 9 common signals and 16 segment signals. For a 2-line display, there will be 17 common signals and 42 segment signals. If the NL pin is set, display lines can be selected automatically.

Character pattern data is sent serially through a 50-bit (42-bit) shift register and latched when all needed data has arrived. The latched data then enables the LCD driver to generate drive waveform outputs.

Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66720 drives from the head display.

Table 3 Relationship between Character Codes and Character Patterns (ROM Code: A03)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 4 Relationship between Character Codes and Character Patterns (ROM Code: A01)

Lower Bits \ Upper Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)															
xxxx0001	CG RAM (2)															
xxxx0010	CG RAM (3)															
xxxx0011	CG RAM (4)															
xxxx0100	CG RAM (5)															
xxxx0101	CG RAM (6)															
xxxx0110	CG RAM (7)															
xxxx0111	CG RAM (8)															
xxxx1000	CG RAM (1)															
xxxx1001	CG RAM (2)															
xxxx1010	CG RAM (3)															
xxxx1011	CG RAM (4)															
xxxx1100	CG RAM (5)															
xxxx1101	CG RAM (6)															
xxxx1110	CG RAM (7)															
xxxx1111	CG RAM (8)															

Table 5 Relationship between Character Codes and Character Patterns (ROM Code: A02)

Upper Bits / Lower Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)																
xxxx0001	CG RAM (2)																
xxxx0010	CG RAM (3)																
xxxx0011	CG RAM (4)																
xxxx0100	CG RAM (5)																
xxxx0101	CG RAM (6)																
xxxx0110	CG RAM (7)																
xxxx0111	CG RAM (8)																
xxxx1000	CG RAM (1)																
xxxx1001	CG RAM (2)																
xxxx1010	CG RAM (3)																
xxxx1011	CG RAM (4)																
xxxx1100	CG RAM (5)																
xxxx1101	CG RAM (6)																
xxxx1110	CG RAM (7)																
xxxx1111	CG RAM (8)																

Note: The character codes of the characters enclosed in the bold frame are the same as those of the first edition of the ISO8859 and the character code compatible.

Table 6 Relationships between CG RAM Address, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

a) When character pattern is 5 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	Character pattern (1)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	Character pattern (8)
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1				0	0	0	0	0	

a) When character pattern is 6 × 8 dots

Character code (DDRAM data)								CGRAM address						MSB CGRAM data LSB								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	0	1	0	0	0	1	Character pattern (1)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	0	1	0	0	0	1	Character pattern (8)
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
											0	1	1			0	0	1	0	1	0	
											1	0	0			0	0	0	1	0	0	
											1	0	1			0	0	0	1	0	0	
											1	1	0			0	0	0	1	0	0	
											1	1	1			0	0	0	0	0	0	

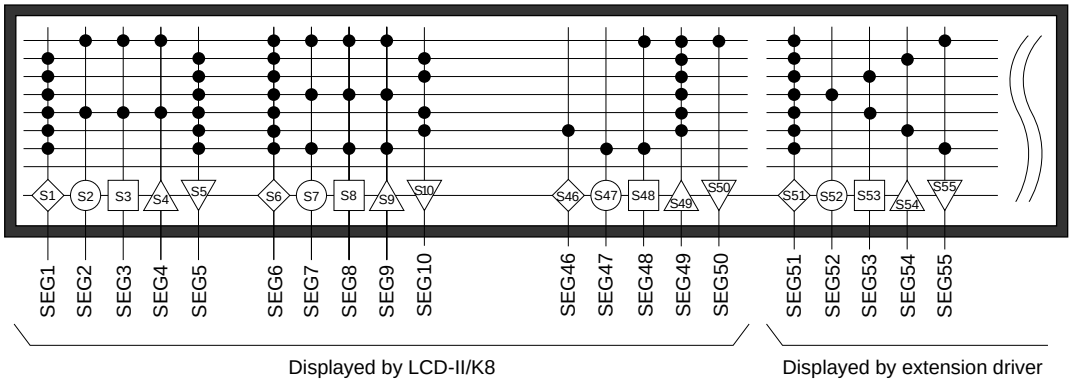
Notes:
1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).
2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.
3. The character data is stored with the rightmost character element in bit 0, as shown in the figure above. Characters of 5 dots in width (FW = 0) are stored in bits 0 to 4, and characters of 6 dots in width (FW = 1) are stored in bits 0 to 5.
4. When the upper four bits (bits 7 to 4) of the character code are 0, CGRAM is selected. Bit 3 of the character code is invalid (*). Therefore, for example, the character codes (00)H and (08)H correspond to the same CGRAM address.
5. A set bit in the CG RAM data corresponds to display selection, and 0 to non-selection.
6. When the BE bit of the function set register is 1, pattern blinking control of the lower six bits is controlled using the upper two bits (bits 7 and 6) in CG RAM. When bit 7 is 1, of the lower six bits, only those which are set are blinked on the display. When bit 6 is 1, a bit 4 pattern can be blinked as for a 5-dot font width, and a bit 5 pattern can be blinked as for a 6-dot font width.

Table 7 Relationship between SEGRAM Addresses and Display Patterns

SEGRAM address				SEGRAM data															
				a) 5-dot font width								b) 6-dot font width							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	*	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	*	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	*	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	*	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	*	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	*	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	*	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	*	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	*	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	*	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	*	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	*	S56	S7	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	*	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	*	S66	S67	S68	S69	S70	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	B1	B0	*	S71	S72	S73	S74	S75	B1	B0	S85	S86	S87	S88	S89	S90
1	1	1	1	B1	B0	*	S76	S77	S78	S79	S80	B1	B0	S91	S92	S93	S94	S95	S96
				Blinking control			Pattern on/off					Blinking control			Pattern on/off				

Notes:
1. Data set to SEG RAM is output when COMS is selected.
2. S1 to S96 are pin numbers of the segment output driver. S1 is positioned to the left of the display. When the HD66720 is used by one chip, segments from S1 to S50 and S1 to S42 are displayed for a 1-line display and a 2-line display, respectively. An extension driver displays the segments after S50 and S42.
3. After S80 output at 5-dot font and S96 output at 6-dot font, S1 output is repeated again.
4. As for a 5-dot font width, lower five bits (D4 to D0) are display on/off information of each segment. For a 6-dot character width, the lower six bits (D5 to D0) are the display information for each segment.
5. When the BE bit of the function set register is 1, pattern blinking of the lower six bits is controlled using the upper two bits (bits 7 and 6) in SEG RAM. When bit 7 is 1, only a bit set to 1 of the lower six bits is blinked on the display. When bit 6 is 1, only a bit 4 pattern can be blinked as for a 5-dot font width, and only a bit 5 pattern can be blinked as for 6-dot font width.
6. Bit 5 (D5) is invalid for a 5-dot font width.
7. Set bits in the SEG RAM data correspond to display selection, and zeros to non-selection.

i) 5-dot font width (FW = 0)



ii) 6-dot font width (FW = 1)

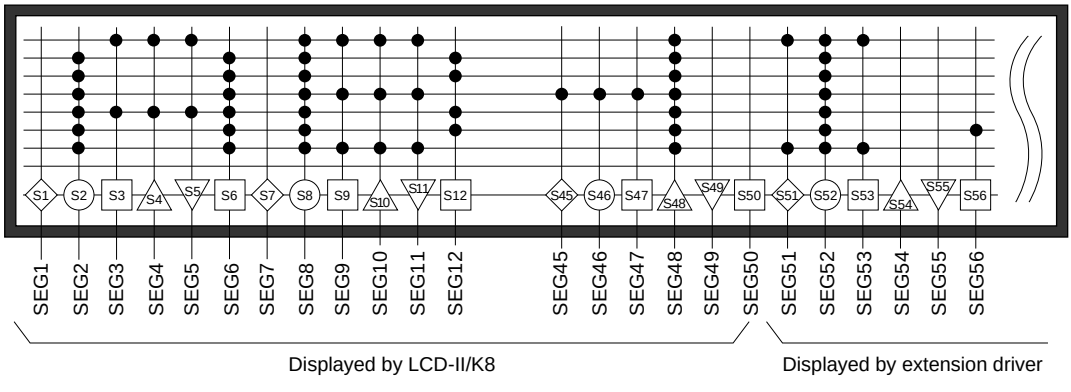


Figure 8 Correspondence between SEG RAM and Segment Display

- Cursor/Blink Control Circuit

  The cursor/blink (or white-black inversion) control is used to produce a cursor or a flashing area on the display at a position corresponding to the location in stored in the address counter (AC).

  For example (figure 9), when the address counter is (08)H, a cursor is displayed at a position corresponding to DDRAM address (08)H.

Note: Cursor/blink/black and white inversion is performed even when the address counter (AC) is selecting CG RAM or SEG RAM. However, in that case, cursor/blink/black and white inversion does not have any meaning.

- Scroll Control Circuit

  The scroll control circuit is used to perform a smooth-scroll in units of dots. When the number of characters to be displayed is greater than that possible at one time on the liquid crystal module, this horizontal smooth scroll can be used to display all characters. Since display lines to scroll can be specified by the register function, random lines can only be scrolled in 2-line mode. Refer to Horizontal Dot Scroll, for details.

- LED Output Control

  The HD66720 has two register-controlled general-purpose output ports. Like other registers, these ports can be set by the MPU via a serial interface to control LED illumination, so there is no need for special control signals.

Oscillator

The HD66720 has a built-in R-C oscillator that can be operated with the addition of a single external resistor. Since this resistor is externally mounted, it can be adjusted to produce the required frequency. Note that changing the operating frequency will effect the frame refresh frequency, the blink rates of the cursors, segments and characters, and the key scan frequency.

The system can also be synchronized with other equipment by inputting an external clock.

LCD Booster Circuit

The LCD booster circuit produces a drive voltage for the LCD by boosting the standard supply voltage by two or three times. All that is needed to operate this circuit is either two or three (depending on the boost factor) external capacitors of about 1 µF each. When driving a large LCD that draws a high load current, there will be an excessive voltage drop at the output of the booster—if this occurs, please use an external LCD power supply.

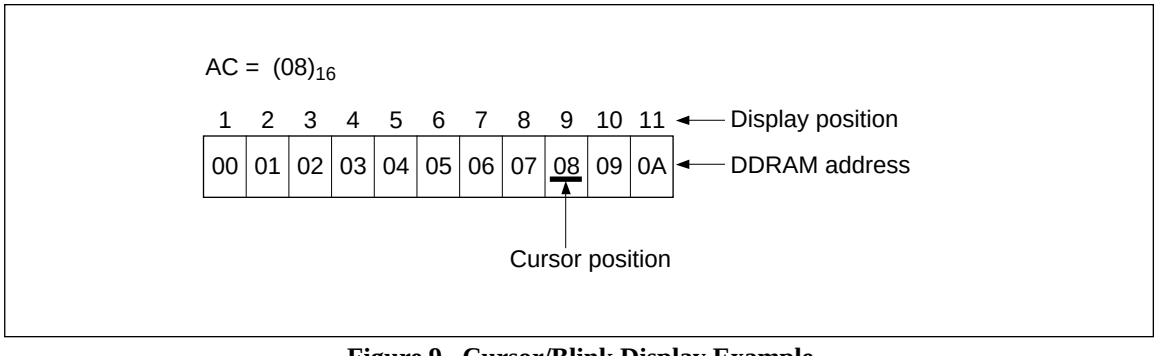


Figure 9 Cursor/Blink Display Example

Modifying Character Patterns

Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 10:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI will proceed at Hitachi.

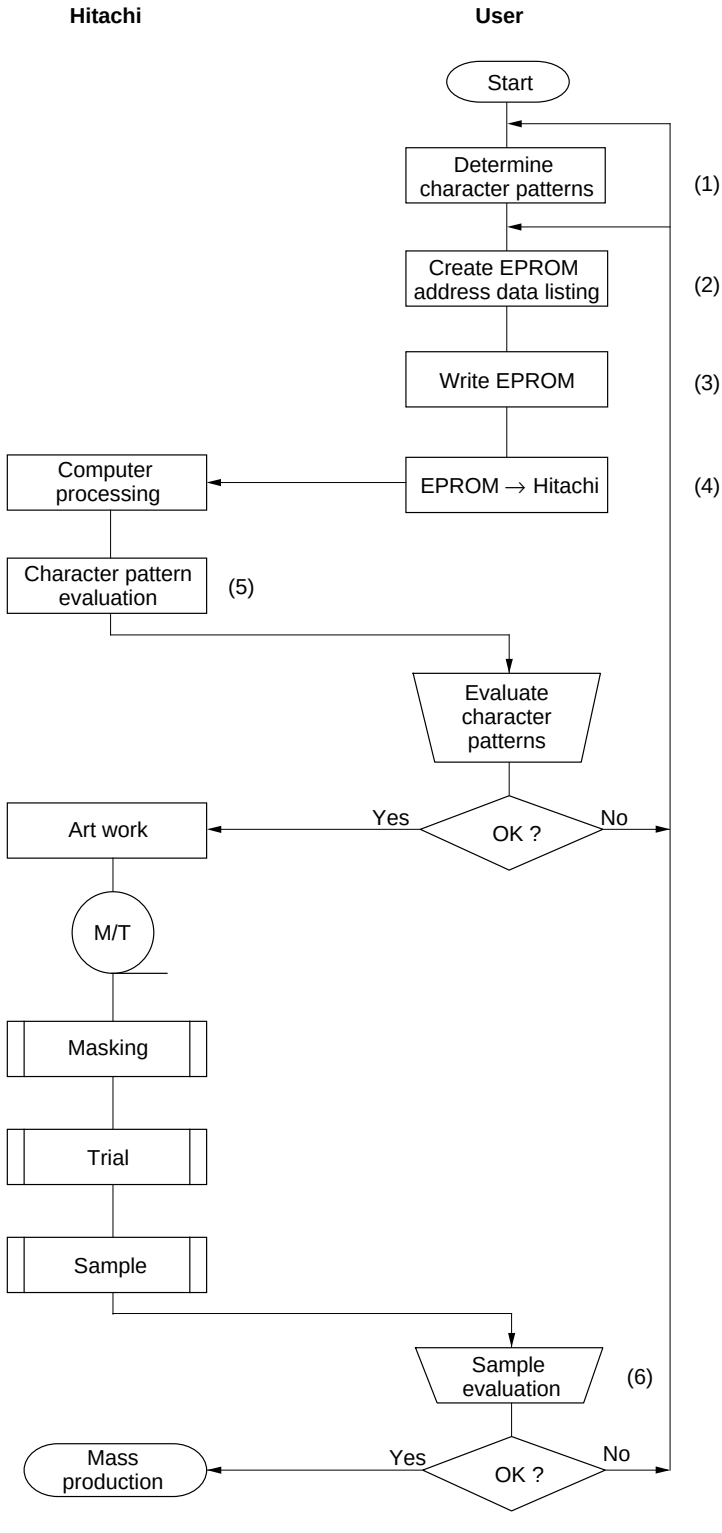


Figure 10 Character Pattern Development Procedure

Programming Character Patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM.

- Programming to EPROM

  The HD66720 character generator ROM can generate 240 5 × 8 dot character patterns. Table 8 shows correspondence between the EPROM address, data, and the character pattern.

- Handling unused character patterns

1. **EPROM data outside the character pattern area:** This is ignored and so any data is acceptable because it does not affect display operation using the character generator ROM.
2. **EPROM data in CG RAM area:** Always fill with zeros.
3. **Treatment of unused user patterns in the HD66720 EPROM:** According to the user application, these are handled in either of two ways:
   a. **When unused character patterns are not programmed:** If an unused character code is written into DD RAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b. **When unused character patterns are programmed as 0s:** Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

Table 8 Correspondence Example between EPROM Address

EPROM Address												Data				
												MSB				LSB
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	O_0
0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
								0	0	0	1	1	0	0	0	1
								0	0	1	0	1	0	0	0	1
								0	0	1	1	0	1	0	1	0
								0	1	0	0	0	0	1	0	0
								0	1	0	1	0	0	1	0	0
								0	1	1	0	0	0	1	0	0
								0	1	1	1	0	0	0	0	0

Character code 0 Line position

Notes:
1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_2 to A_0 specify the line position of the character pattern. EPROM address A_3 should be set to 0.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
5. The eighth line is also stored in the CGROM, and should also be programmed. If the eighth line is used for a cursor, this data should all be set to zero.
6. EPROM data bits O_7 to O_5 are invalid. 0 should be written in all bits.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66720 can be controlled by the MPU. Before starting internal operation of the HD66720, control information is temporarily stored in these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66720 is determined by signals sent from the MPU. These signals, which include register selection bit (RS), read/write bits (R/W), and the data bus bits (DB_0 to DB_7), make up the HD66720 instructions (table 13). There are four categories of instructions that:

- Designate HD66720 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66720 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system efficiently.

When an instruction is being executed for internal operation (BF = 1), no instruction other than the busy flag/scan data instruction can be executed.

Adjust the transmission rate so that the last bit of the next instruction is transmitted after executing the current instruction. Refer to table 13 Instruction for instruction execution times. The execution times depend on the operation frequency (oscillation frequency). When using the R-C oscillator, be careful when determining the transmission rate, because it will vary greatly by the power supply voltage, operating temperature, and manufacturing tolerances.

Instruction Description

Clear Display

Clear display writes space code (20)H (character pattern for character code (20)H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

Return Home

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed).

Entry Mode Set

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM and SEG RAM.

S: Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1 during DD RAM write. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM and SEG RAM does not shift the display. If S is 0, the display does not shift.

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	0	0	1

Figure 11 Clear Display Instruction

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	0	1	0

Figure 12 Return Home Instruction

RS	R/W	DB_7							DB_0
0	0	0	0	0	0	0	1	I/D	S

Figure 13 Entry Mode Set Instruction

Display On/Off Control

When extension register enable bit (RE) is 0, bits D, C, and B are accessed.

D: The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, and can be displayed instantly by setting D to 1.

C: The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font.

B: The character indicated by the cursor blinks when B is 1. The blinking is displayed as switching between all blank dots and displayed characters at a speed of 384-ms intervals when fOSC is 150 kHz with a 5 dot font width. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to the reciprocal of either f_{cp} or f_{OSC}. For example, when f_{cp} is 180 kHz, 384 × 150/180 = 320 ms.)

Extension Function Set

When the extended register enable bit (RE) is 1, FW, FR, and B/W bits shown are accessed. Once these registers are accessed, the set values are held even if the RE bit is set to zero.

FW: When FW is 1, each displayed character is controlled with a 6-dot width. The user font in CG RAM is displayed with a 6-bit character width from bits 5 to 0. As for fonts stored in CG ROM, no display area is assigned to the rightmost bit, and the font is displayed with a 5-dot character width. If the FW bit is changed, data in DD RAM and CG RAM is destroyed. Therefore, set FW before data is written to RAM. When font width is set to 6 dots, the frame frequency decreases to 5/6 compared to 5-dot time. See Oscillator for details. FW can only be set at the head of a program before any other instructions (except for Read Busy Flag & Scan Data). If the value of bit FW is modified after executing other instruction, the data in RAM may be damaged.

FR: When FR is 1, the display data stored in CG ROM/CG RAM/SEG RAM is reflected horizontally. Select FR according to how the LSI is mounted. The display location of each character does not change.

B/W: When B/W is 1, the character at the cursor position is cyclically displayed with black-white inversion. At this time, bits C and B in display on/off control register are “Don’t care”. When f_{cp} or f_{osc} is 150 kHz, display is changed by switching every 384 ms.

	RS	R/W	DB_7						DB_0
RE = 0	0	0	0	0	0	0	1	D	C	B

Figure 14 Display On/Off Control Instruction

	RS	R/W	DB_7						DB_0
RE = 1	0	0	0	0	0	0	1	FW	FR	B/W

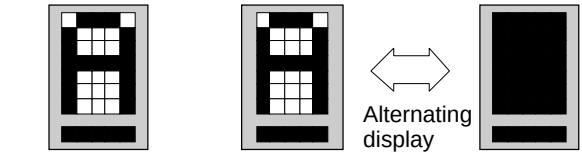
Figure 15 Extended Function Set Instruction

Cursor or Display Shift

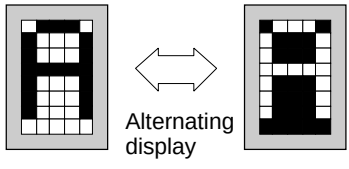
Only when the extended register bit (RE) is 0, the S/C and R/L bits can be set.

S/C, R/L: Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 9). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 20th digit of the first line.

Note that, all line displays will shift at the same time. When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position. When this instruction is executed, extended register enable bit (RE) is reset. The address counter (AC) contents will not change if only a display shift is performed.

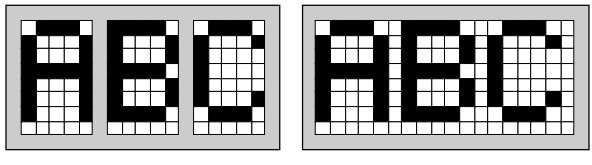


i) Cursor display example ii) Blink display example

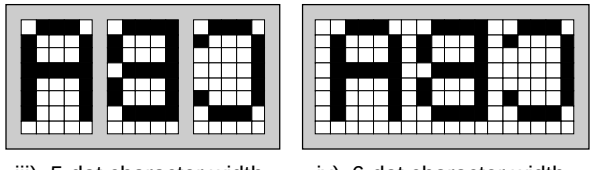


iii) White-black inverting display example

a) Cursor blink width control



i) 5-dot character width (without mirror reflection) ii) 6-dot character width (without mirror reflection)



iii) 5-dot character width (with mirror reflection) iv) 6-dot character width (with mirror reflection)

b) Font width control

Figure 16 Example of Display Control

Scroll/LED Control

Only when the extended register bit (RE) is 1, the LED and HSE bits can be set.

LED: This bit controls the LEDs. The data set in bits LED0 and LED1 is reversed and output from pins LED0 and LED1. In other words, if 1 is set in bit LED0, a low level is output from pin LED0. This register function can also be used as a general output port instead of LED control.

HSE: This bit specifies which display line or lines are to be dot shifted by the amount indicated in the set scroll quantity register. When HSE is 1 the first line scrolls and when HSE2 is 1 the second line scrolls.

Table 9 Cursor or Display Shift Function

S/C	R/L	Description
0	0	Shifts the cursor position to the left (AC is decremented by one)
0	1	Shifts the cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

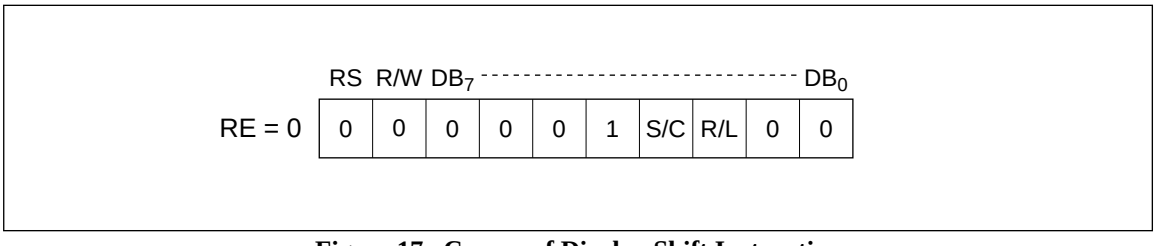


Figure 17 Cursor of Display Shift Instruction

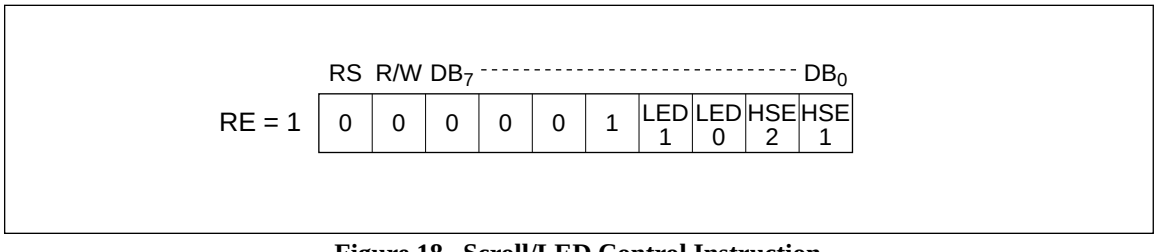


Figure 18 Scroll/LED Control Instruction

Function Set

Only when the extended register enable bit (RE) is 0, the KF bit can be accessed, and only when 1, the BE and the LP bits can be accessed. Bits IRE and SLP can be accessed regardless of RE.

IRE: When bit IRE is 1, key scan interrupts are generated. When a key is pressed, pin IRQ becomes low level.

SLP: When SLP is 1, the LSI enters sleep mode. During sleep mode, the display is disabled because the internal operation clock is divided by 16. However, the key scan cycle is not affected. For details, refer to Sleep Mode. In this mode, the frame frequency is also divided by 16, and a scanning line may appear. To avoid this, the LCD driving voltage (V_{LCD}) should be cut off.

RE: When bit RE is 1, extension function set register, scroll/LED control register, set scroll quantity register, the set SEG RAM address register, and bit BE in the function set register, can be accessed. When bit RE is 0, the registers described above cannot be accessed, and the data in these registers is held.

KF: When RE is 0, these bits specify the key scan cycle. Set these bits according to the mechanical characteristic of the keys. The key scan cycles relies on the operation cycles(oscillation frequency). Table 10 shows the key scan cycles for the case when the operation frequency (oscillation frequency) is 160 kHz.

BE: When bit RE is 1, this bit can be rewritten. When this bit is 1, the user font in CG RAM and the segment in SEG RAM can be blinked according to the upper two bits of CG RAM and SEG RAM.

LP: When bit RE is 1, this bit can be rewritten. When LP is set to 1, the HD66720 operates in low power mode. In 1-line display mode, the HD66720 operates by dividing the oscillation frequency by four, and in a 2-line display mode, the HD66720 operates at the oscillation frequency divided by two. Thus, 10 characters at the most are displayed in one line. According to these operations, instruction execution takes four times or twice as long. When performing display shift and smooth scroll during low power mode, the resulting display will differ from the normal mode display (refer to Low Power Mode for details). When this LP bit is changed, data in RAMs may be broken, so re-write data into RAMs.

Table 10 Key Scan Cycle

KF1	KF0	Key Scan Cycle
0	0	10 ms
0	1	5 ms
1	0	20 ms
1	1	40 ms

*: For the case when f_{cp} (f_{osc}) is 160 kHz.

	RS	R/W	DB_7							DB_0
RE = 0	0	0	0	0	1	IRE	SLP	RE	KF1	KF0
RE = 1	0	0	0	0	1	IRE	SLP	RE	BE	LP

Figure 19 Function Set Instruction

Set CGRAM Address

A CG RAM address can be set while the RE bit is cleared to 0.

Set CG RAM address sets the address indicated by binary AAAAAA into the address counter. After this address set, CG RAM can be written to or read from by the MPU.

Set SEG RAM Address

Only when the extended register enable (RE) bit is 1, the SEG RAM address can be set.

The SEG RAM address in the binary form AAAA is set to the address counter. After this address set, SEG RAM can be written to or read from by the MPU.

Set DD RAM Address

A DD RAM address can be set while the RE bit is cleared to 0.

Set DD RAM address sets the DD RAM address binary indicated by AAAAAAA into the address counter. After this address set, DD RAM can be written to or read from by the MPU.

When NL is low (1-line display), AAAAAA can be H(00) to H(27). When NL is high (2-line display), AAAAAA can be H(00) to H(13) for the first line, and H(20) toH(33) for the second line.

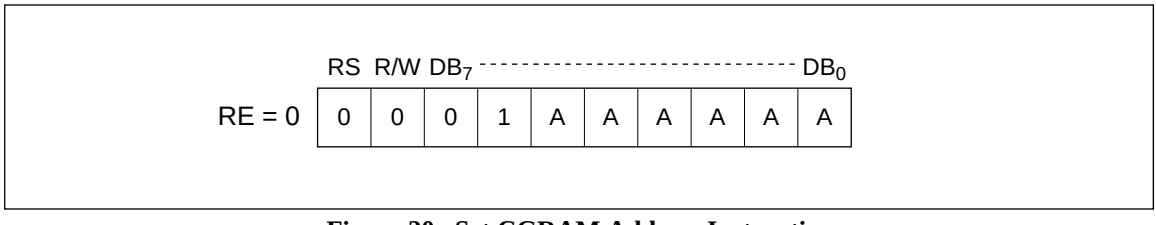


Figure 20 Set CGRAM Address Instruction

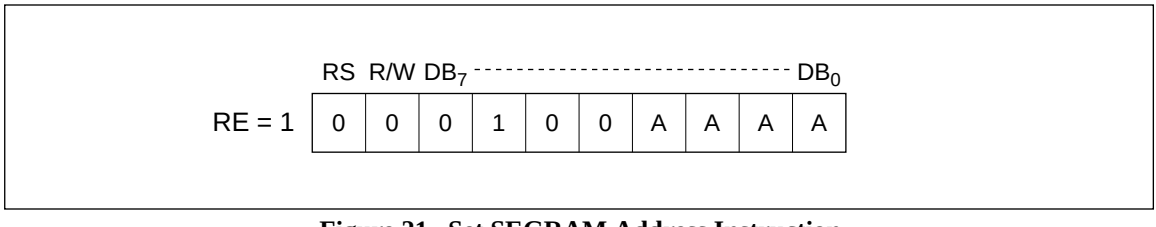


Figure 21 Set SEGRAM Address Instruction

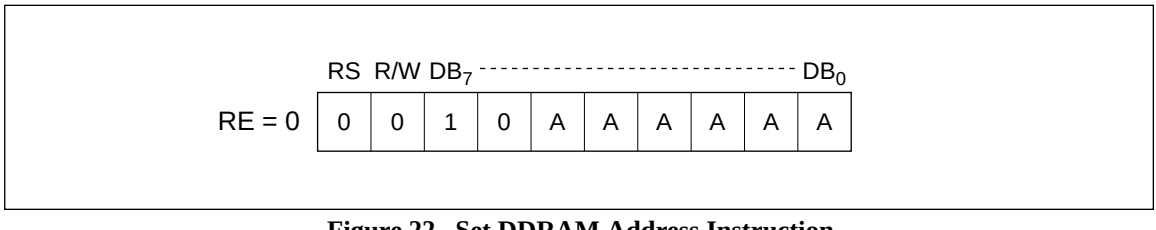


Figure 22 Set DDRAM Address Instruction

Set Scroll Quantity

When extended register enable bit (RE) is 1, PS 1/0 and HDS4 to HDS0 can be set.

PS: PS1 and PS0 specify the number of characters at the left side of the display that are unaffected by horizontal scrolls and are left intact while the rest of the display is scrolled (table 11).

HDS: HDS4 to HDS0 specify horizontal scroll quantity to the left of the display in dot units. The HD66720 uses the unused DD RAM area to execute a desired horizontal smooth scroll from 1 to 24 dots (table 12).

Note: When performing a horizontal scroll as described above by connecting an extension driver, the maximum number of characters per line decreases by the quantity corresponding to the specified scroll distance.

Table 11 Partial Smooth Scroll

PS1	PS0	Description
0	0	FIxes all characters
0	1	Fixes leftmost character in smooth scroll
1	0	Fixes the two leftmost characters in smooth scroll
1	1	Fixes the three leftmost characters in smooth scroll

Table 12 Smooth Scroll Quantity

HDS4	HDS3	HDS2	HDS1	HDS0	Description
0	0	0	0	0	No shift
0	0	0	0	1	Shifts the display position to the left by one dot
0	0	0	0	0	Shifts the display position to the left by two dots
0	0	0	1	1	Shifts the display position to the left by three dots
		•			
		•			
1	0	1	1	1	Shifts the display position to the left by 23 dots
1	*	*	*	*	Shifts the display position to the left by 24 dots

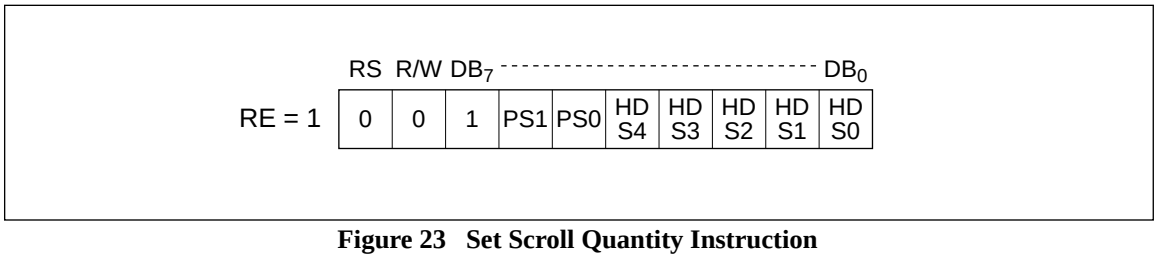


Figure 23 Set Scroll Quantity Instruction

Read Busy Flag & Scan Data

Scan data SD4 to SD0 latches into scan registers SCAN0 to SCAN5 and scan cycle state SF1 and SF0 is read sequentially. Refer to Key Scan Control for details. At the same time, busy flag (BF) is read. When BF is 1, the HD66720 is still processing an instruction already accepted, and does not accept another instruction until BF becomes 0. Adjust the transfer rate so that the HD66720 receives the last bit of the next instruction after BF has become 0.

Write Data to CG RAM, DD RAM, or SEG RAM

This instruction writes 8-bit binary data DDDDDDDD to CG RAM, DD RAM or SEG RAM. CG RAM, DD RAM or SEG RAM is selected by the previous specification of the address set instruction (set CG RAM address/set DD RAM address/set SEG RAM address). After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift direction.

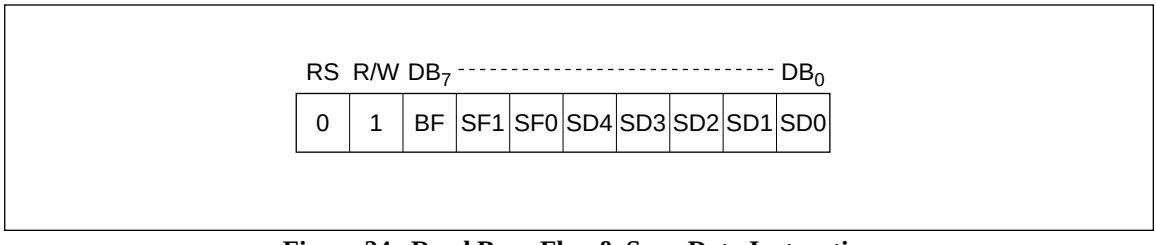


Figure 24 Read Busy Flag & Scan Data Instruction

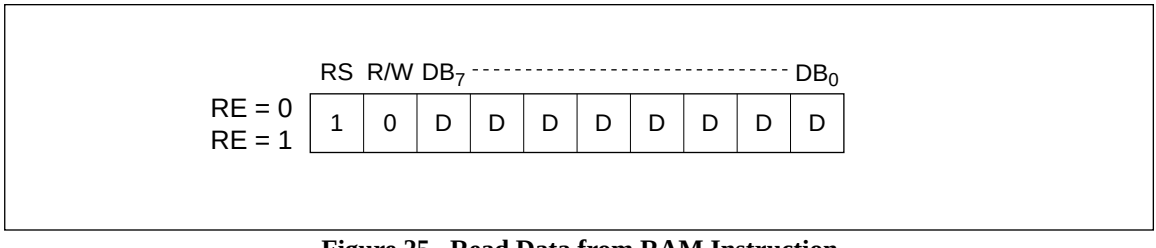


Figure 25 Read Data from RAM Instruction

Read Data from CG, DD, or SEG RAM

This instruction reads 8-bit binary data DDDDDDDD from CG RAM, DD RAM, or SEG RAM. CG RAM, DD RAM or SEG RAM is selected by the previous specification of the address set instruction. If no address is specified, the first data read will be invalid. When executing serial read instructions, data is normally read from the next address. An address set instruction need not be executed just before this read instruction when shifting the cursor by a cursor shift instruction (when reading from DD RAM). A cursor shift instruction is the same as a set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, a display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented after write instructions to CG, DD or SEG RAM. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to read data correctly, execute either an address set instruction or a cursor shift instruction (only with DD RAM), or alternatively, execute a preliminary read instruction to ensure the address is correctly set up before accessing the data.

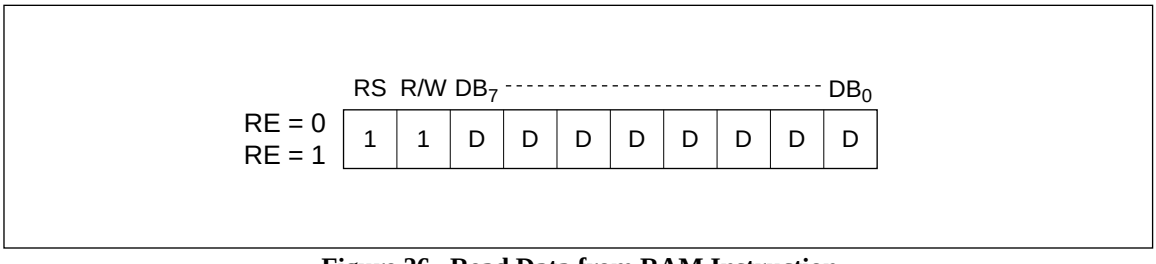


Figure 26 Read Data from RAM Instruction

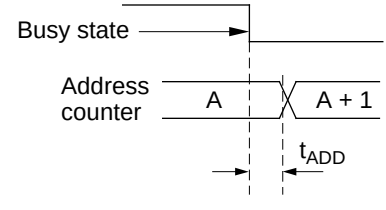
Table 13 Instructions

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 160 kHz)
Clear display	0/1	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	2.67 ms
Return home	0/1	0	0	0	0	0	0	0	0	1	0	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	2.67 ms
Entry mode set	0/1	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	63 µs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C), and blinking of cursor position character (B).	63 µs
Extension function set	1	0	0	0	0	0	0	1	FW	FR	B/W	Sets a font width (FW), font reverse (FR), and a black-white inverting cursor (B/W).	63 µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DD RAM contents.	63 µs
Scroll/LED output control	1	0	0	0	0	0	1	LED	LED	HSE	HSE	Specifies which display lines to undergo horizontal smooth scroll and controls the output of LED.	63 µs
Function set	0	0	0	0	0	1	IRE	SLP	RE	KF	KF	Set interrupt enable (IRE) sleep mode (SLP), extension register write enable (RE). Sets key scan cycle (KF) and extension register write enable.	63 µs
	1	0	0	0	0	1	IRE	SLP	RE	BE	LP	Sets CG RAM/SEG RAM blinking enable (BE), and low-power mode (LP).	63 µs
Set CGRAM address	0	0	0	0	1	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	A_{CG}	Sets CG RAM address. CG RAM data is sent and received after this setting.	63 µs
Set SEGRAM address	1	0	0	0	1	0	0	A_{SEG}	A_{SEG}	A_{SEG}	A_{SEG}	Sets SEG RAM address. SEG RAM data is sent and received after this setting.	63 µs

Table 13 Instructions (cont)

Instruction	RE Bit	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{OSC} is 160 kHz)
Set DDRAM address	0	0	0	1	0	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	A_{DD}	Sets DD RAM address. DD RAM data is sent and received after this setting.	63 µs
Set scroll quantity	1	0	0	1	PS	PS	HDS	HDS	HDS	HDS	HDS	Sets horizontal dot scroll quantity (HDS) and partial scroll characters (PS).	63 µs
Read busy flag & scan data	0/1	0	1	BF	SF	SF	SD	SD	SD	SD	SD	Reads busy flag (BF), data in scan register (SD), and scan state (SF).	0 µs
Write data to RAM	0/1	1	0			Write data						Writes data into DD RAM, CG RAM, or SEG RAM.	63 µs t_{ADD} = 9.3 µs*
Read data from RAM	0/1	1	1			Read data						Reads data from DD RAM, CG RAM, or SEG RAM.	63 µs t_{ADD} = 9.3 µs*

I/D	= 1: Increment	LP	= 1: Low-power mode
I/D	= 0: Decrement	BF	= 1: Internally operating
S	= 1: Accompanies display shift	BF	= 0: Instructions acceptable
D	= 1: Display on	DD RAM	: Display data RAM
C	= 1: Cursor on	ADD	: DDRAM corresponding to cursor address
B	= 1: Blink on		
FW	= 1: 6-dot font width	CG RAM	: Character generator RAM
FR	= 1: Horizontal font reflection	A_{CG}	: CG RAM address
B/W	= 1: Black-white inverting cursor on	SEGRAM	: Segment RAM
S/C	= 1: Display shift	A_{SEG}	: Segment RAM address
S/C	= 0: Cursor move	HSE	: Specifies horizontal scroll lines
R/L	= 1: Shift to the right	HDS	: Horizontal dot scroll quantity
R/L	= 0: Shift to the left	PS	: Specifies partial scroll quantity
IRQ	= 1: Interrupt (IRQ) generation enable	LED	: LED control
SLP	= 1: Sleep mode	KF	: Key scan cycle
RE	= 1: Extension register write enable	SD	: Key scan data
BE	= 1: CGRAM/SEGRAM blinking enable	SF	: Key scan state



t_{ADD} depends on the operation frequency
$t_{ADD} = 1.5/f_{cp}$ or f_{osc} (sec)

Figure 27 t_{ADD} State

Note: 1. *After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag is cleared.

It_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.

2. The execution time mentioned above are for the case of 5-dot font. With a 6-dot font, it will take 20% more to execute an instruction. The execution time will also change if the frequency changes. For example, the execution time will be reduced to 80% when f is 200 kHz.

Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD66720 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after V_{CC} rises to 4.5 V or 40 ms after the V_{CC} rises to 2.7 V.

1. Clear display
   (20)H to all DDRAM

2. Function set
   IRE = 0: Interrupt (IRQ) generation disable
   SLP = 0: Clear sleep mode
   RE = 0: Extension register write disable
   KF = 0: Key scan cycle 10 ms
   BE = 0: CGRAM/SEGRAM blinking off
   LP = 0: Not in low power mode

3. Display on/off control
   D = 0: Display off
   C = 0: Cursor off
   B = 0: Blinking off

4. Entry mode set
   I/D = 1: Increment by 1
   S = 0: No shift

5. Extension function set
   FR = 0: Without font reverse
   B/W = 0: Normal cursor (8th line)

6. Scroll/LED control
   HSE = 00: Scroll unable
   LED = 00: LED output level = high

7. Set scroll quantity
   HDS = 00000: Not scroll

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66720.

Initializing by Hardware Reset Input

The HD66720 also has a reset input pin (RESET*). If this pin is made low during operation, an internal reset and initialization is performed except for key scan cycle setting bit (KF). A hardware reset can turn off display when the HD66720 is switched off. A reset input is ignored, however, during internal reset after power-on. In other words, the internal reset has priority. The level of the reset pin must always be pulled up to V_{CC} when the hardware reset input is not used.

Transferring Serial Data

A three-line clock-synchronous transfer method is used. The HD66720 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66720 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the HD66720 can be reset and serial transfer synchronized by making chip select (CS*) high. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single HD66720 interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial data lines (SID and SOD). In this case, chip select (CS*) should be fixed to low.

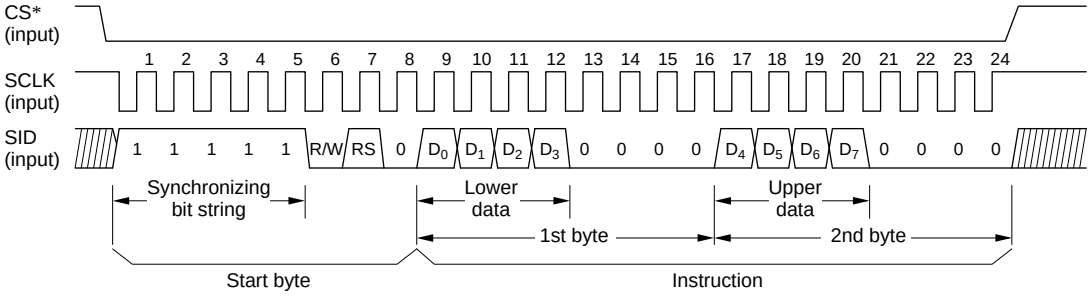
The transfer clock (SCLK) is independent from operational clock (CLK) of the HD66720. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see continuous transfer) must be considered since the HD66720 does not have an internal transmit/ receive buffer.

To begin with, transfer the start byte. By receiving five consecutive bits (synchronizing bit string) at the beginning of the start byte, the transfer counter of the LCD-II/K8 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/W bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail in the following.

a) Serial data input (receiving)



b) Serial data output (transmitting)

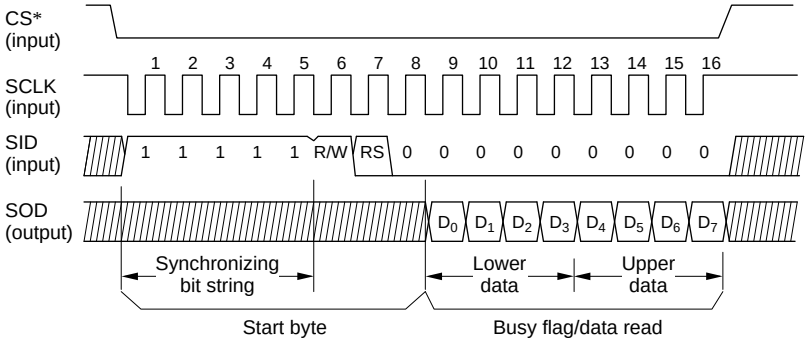


Figure 28 Basic Procedure for Transferring Serial Data

- Receiving (write)

  After receiving the start synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are continuously received with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

- Transmitting (read)

  After receiving the synchronizing bit string, the R/W bit (= 0), and the RS bit with the start byte, 8-bit read data is transmitted from pin SOD in the same way as receiving. When read data is continuously transmitted with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

  If data is read when bit RS is set to 0, scan data latched into SCAN0 to SCAN5 resisters is transmitted as the lower 5-bit data. After receiving the start byte, transmission starts from data in SCAN resister latched at KST0 strobe. After transmitting data from the SCAN5 register, SCAN0 data is retransmitted.

  When reading RAM data with bit RS set to 1, it is necessary to wait for at least the duration of a RAM data read period.

  During transmission (data output), the SID input is continuously monitored for a start synchronizing bit string (11111). Once this has been detected, the R/W and RS bits are received. Accordingly, 0 must always be input to SID when transmitting data continuously.

- Continuous Transfer

  When instructions are continuously received with the R/W bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

  After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it. To execute the next instruction, the instruction execution time of theHD66720 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

  In addition, if the next unit of data is read before read execution of previous data is completed for busy flag/scan data`/RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, it is possible to transfer without reading the busy flag if the burden of polling on the CPU needs to be removed. In this case, insert a transfer wait between instructions so that the current instruction first completes execution.

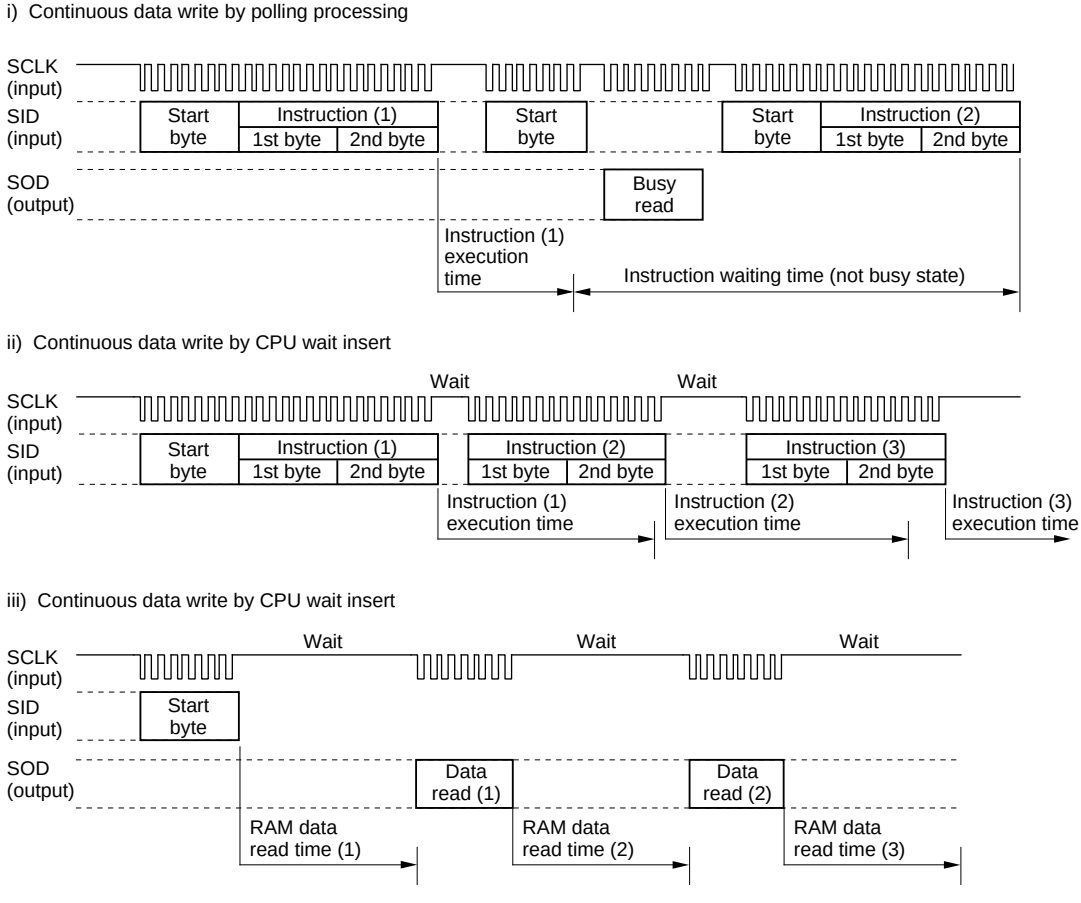


Figure 29 Procedure for Continuous Data Transfer

Key Scan Control

The key matrix scanner senses the key states at each rising edge of the key strobe signals (KST) that are output by the HD66720. The key strobe signals are output as time-multiplexed signals from KST0 to KST4. After passing through the key matrix, these strobe signals are used to sample the key status on five inputs KIN0 to KIN4, enabling up to 30 keys to be scanned.

The states of inputs KIN0 to KIN4 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST5 is latched into registers SCAN1 to SCAN5, respectively.

The generation cycle and pulse width of the key strobe signals depends on the operating frequency (oscillation frequency) of the HD66720 and the key scan cycle determined by KF0 and KF1. For example, when the operating frequency is 150 kHz and KF0 and KF1 are both 0, the generation cycle is 10 ms and the pulse width is 1.7 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are also changed in inverse proportion.

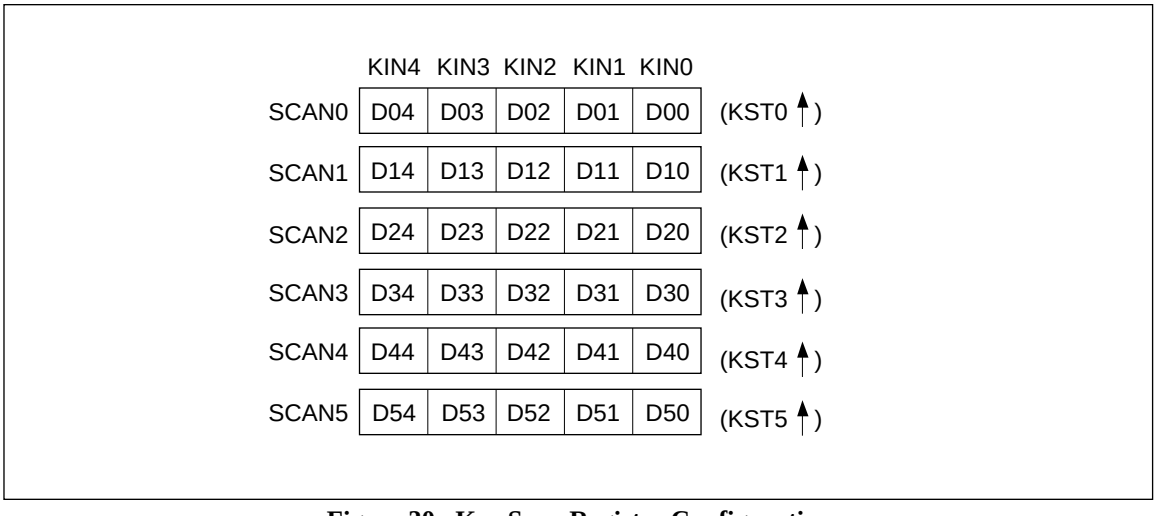


Figure 30 Key Scan Register Configuration

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width, software should be used to ensure that the scanned data has been read two or three times in succession before it is assumed to be valid. Multiple keypress combinations should also be processed in software. Note that any multiple key combination is possible, however, if the key combination creates a cross pattern the scanned data will include unnecessary data. For example, if keys D12, D11, and D22 are pressed simultaneously, key D21 will also be pressed. The input pins KIN0 to KIN4 are pulled up to V_{CC} by MOS transistors (see Electrical Characteristics). External resistors may also be required to pull up the voltages further when the internal pull-ups are insufficient due to noise margins or other reasons.

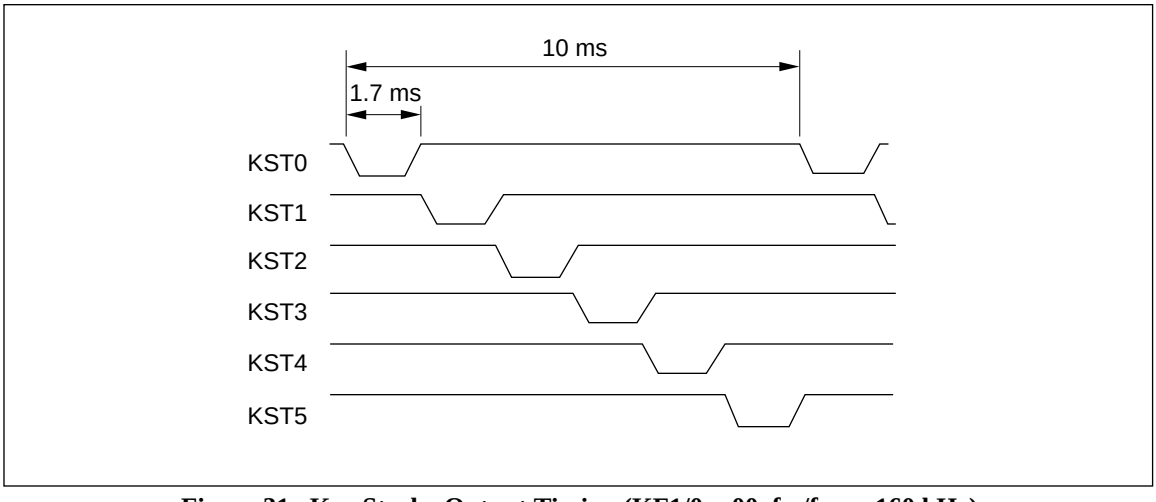


Figure 31 Key Strobe Output Timing (KF1/0 = 00, f_{cp}/f_{osc} = 160 kHz)

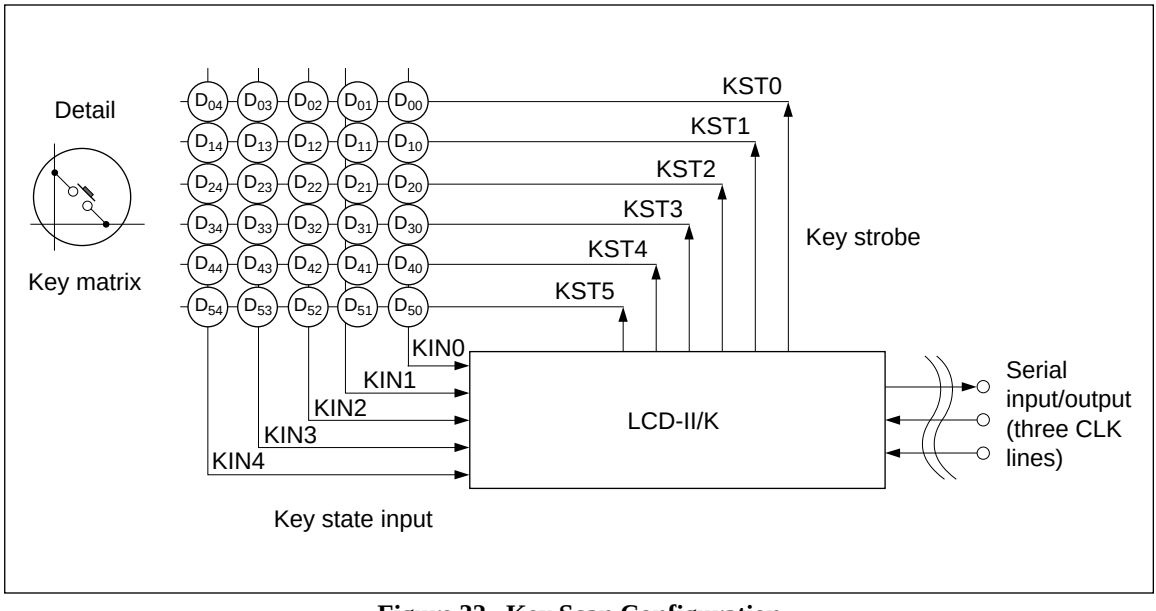


Figure 32 Key Scan Configuration

The key-scanned data is read via a three-line clock synchronous serial interface using the following procedure. First of all, a start byte is transferred. This must contain five bits of 1 (synchronous bit string), a transfer direction bit (R/W) of 1, a register select bit (RS) of 1, and one bit of 0 in that order. The synchronizing bit string is used to reset the transfer counter of the HD66720, thus synchronizing the serial transfer.

After the HD66720 has received the above start byte, it reads scan data SD0 to SD4 from the SCAN0 register starting from the LSB. The HD66720 reads data from SCAN1, SCAN2, SCAN3, SCAN4, and SCAN5 in that order. After reading SCAN5, the HD66720 starts at SCAN0 again.

The HD66720 transfer counter can also be reset to synchronize serial transfer by driving the chip select (CS*) high. In this case, the data currently transferred is cleared; therefore, transfer the start byte again to restart the transfer.

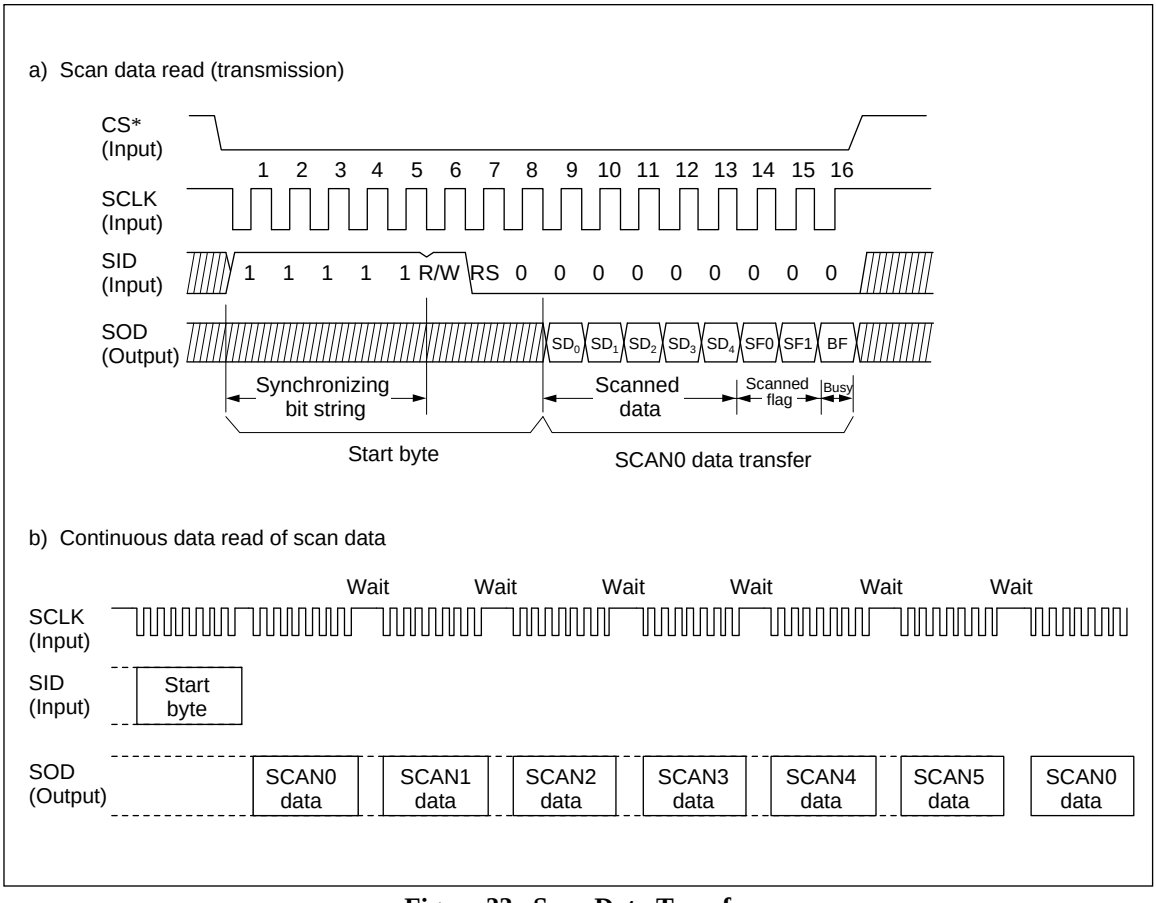


Figure 33 Scan Data Transfer

Key Scan Interrupt (Wake-Up Function)

If the MPU has set the interrupt enable bit (IRE) to 1, the LCD sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to low level. An interrupt signal can be generated by pressing any key in a 30-key matrix. The interrupt level continues to be output during the key-scan cycle in which the key is being pushed.

Key scanning is performed and interrupts can occur during LCD-II/K8 sleep mode (SLP = “1”). The interrupt signal from LCD-II/K8 can trigger the MPU even though the whole system is in a sleep state (or standby state), thus, minimizing power consumption.The LCD cannot be displayed when the LCD-II/K8 is in sleep mode. Refer to Sleep Mode for details.

The output pin of IRQ* is pulled up to the V_{CC} with a MOS of 50 kΩ; however, pull up can be made stronger by adding external resistors as needed. Interrupts may occur if noise occurs in KIN input during key scanning. Interrupts maybe inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

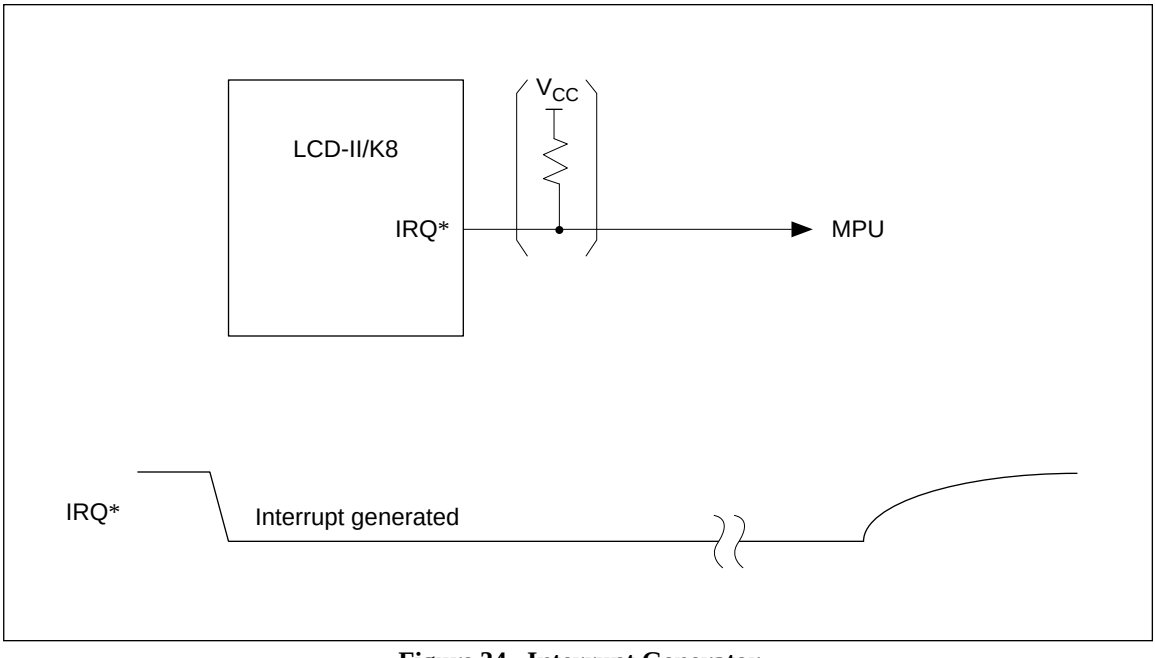


Figure 34 Interrupt Generator

Extension Driver LSI Interface

The number of displayed characters can be increased by using an extension driver. For example, by adding a single HD44100R extension driver with 40 LCD driver output, a 2-line 16 character display with a 5-dot font width can be achieved Moreover, a maximum 2-line 20 character or single-line 40 character display can be achieved by increasing the number of extension drivers.

The extension driver can be interfaced with signals CL1, CL2, D1 and M. The following figure shows an example of LCD-II/K8 and an HD44100R. The extension driver displays data from the 51st dot in 1-line display mode, and from the 43rd dot in 2-line display mode. The extension driver can be driven by the LCD-II/K8; however, the output voltage drop of the booster circuit increases as the load on the booster circuit increases.

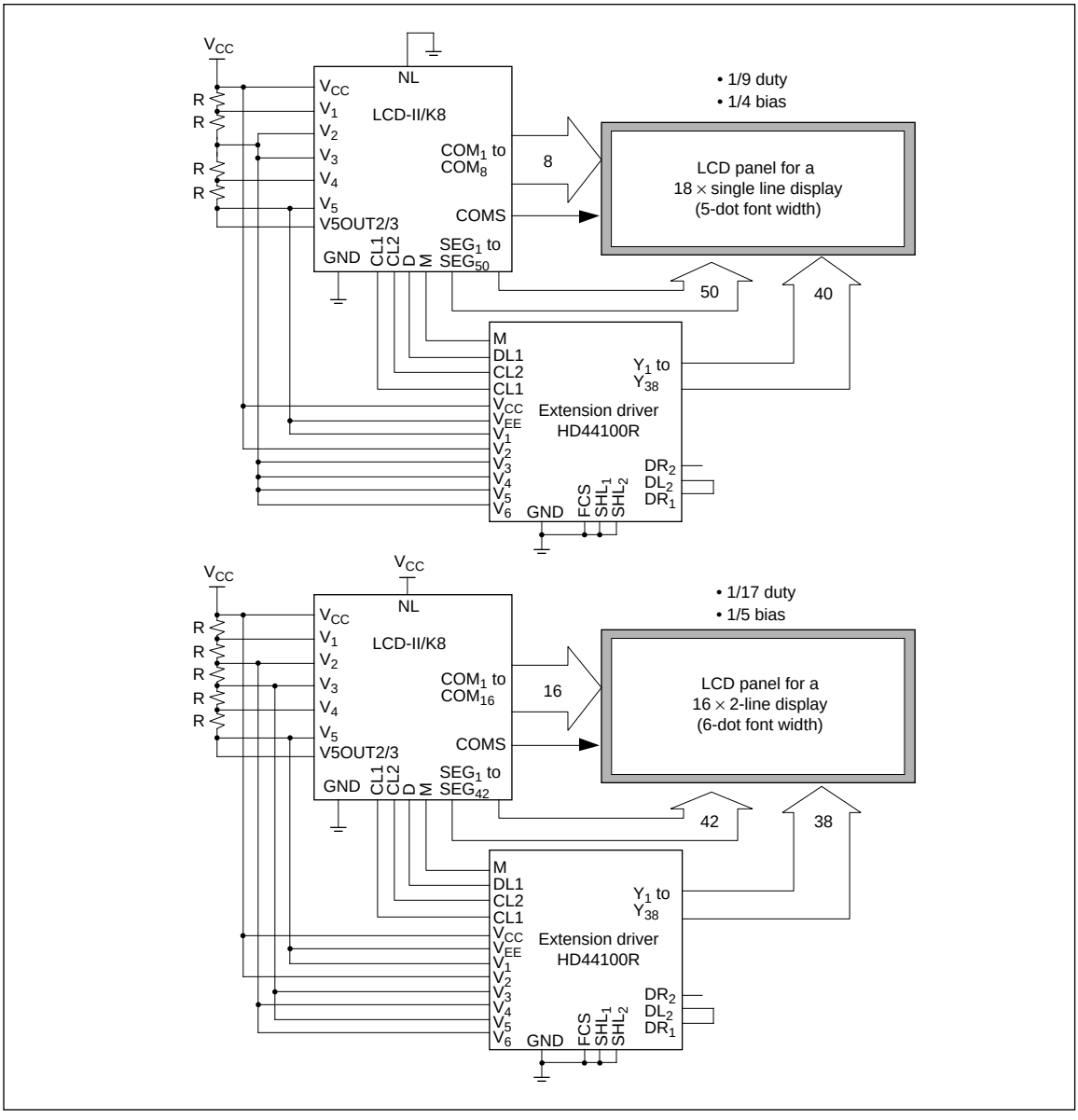


Figure 35 HD66720 and the Extension Driver (HD44100R) Connection

Interface to the Liquid Crystal Display

Set the number of display lines with the N bit and the font width with the FW bit. The relationship between the number of display lines and register values is given below.

Table 14 Relationship between Display Lines, EXT Pin, and Register Setting

		5-Dot Font					6-Dot Font						
				Register Setting					Register Setting				
Lines	Char.	Seg-ment	Extension Driver	N	RE	FW	Seg-ment	Extension Driver	N	RE	FW	Scroll Display	Duty Cycle
1	8	50	—	0	0	0	50	—	0	1	1	Enabled	1/9
	10	50	—	0	0	0	90	1	0	1	1	Enabled	1/9
	12	80	1	0	0	0	90	1	0	1	1	Enabled	1/9
	16	80	1	0	0	0	96	2	0	1	1	Enabled	1/9
	20	80	2	0	0	0	96	2	0	1	1	Enabled	1/9
	40	80	4	0	0	0	96	5	0	1	1	Disabled	1/9
2	8	42	—	1	0	0	82	1	1	1	1	Enabled	1/17
	12	80	1	1	0	0	82	1	1	1	1	Enabled	1/17
	16	80	1	1	0	0	96	2	1	1	1	Enabled	1/17
	20	80	2	1	0	0	96	2	1	1	1	Disabled	1/17

Note: — means not required.

Example of 5-Dot Font Width Connection

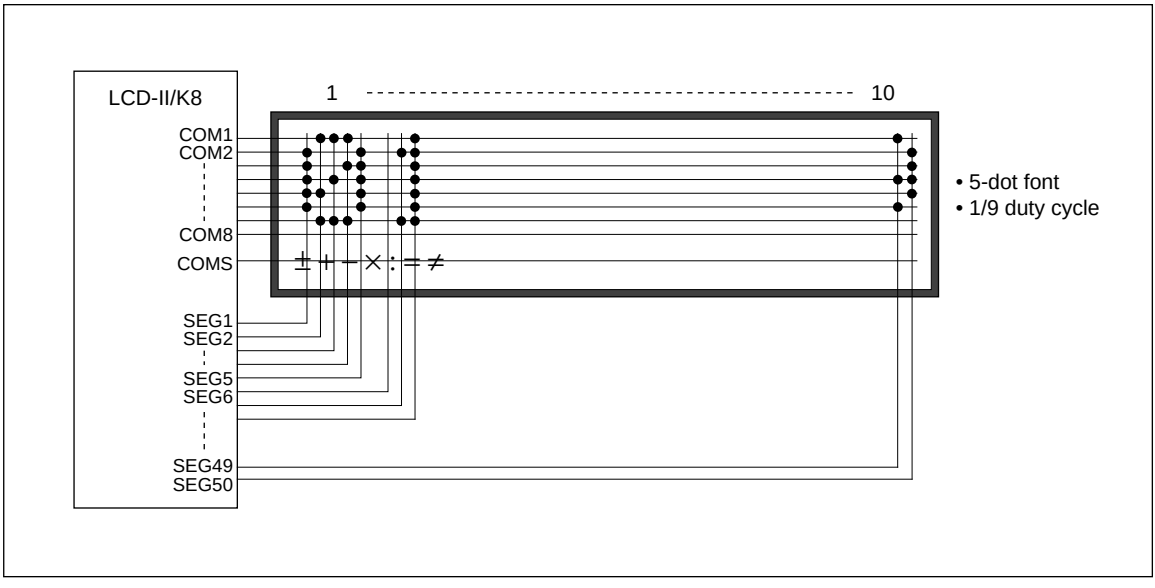


Figure 36 10 × 1-Line + 50-Segment Display

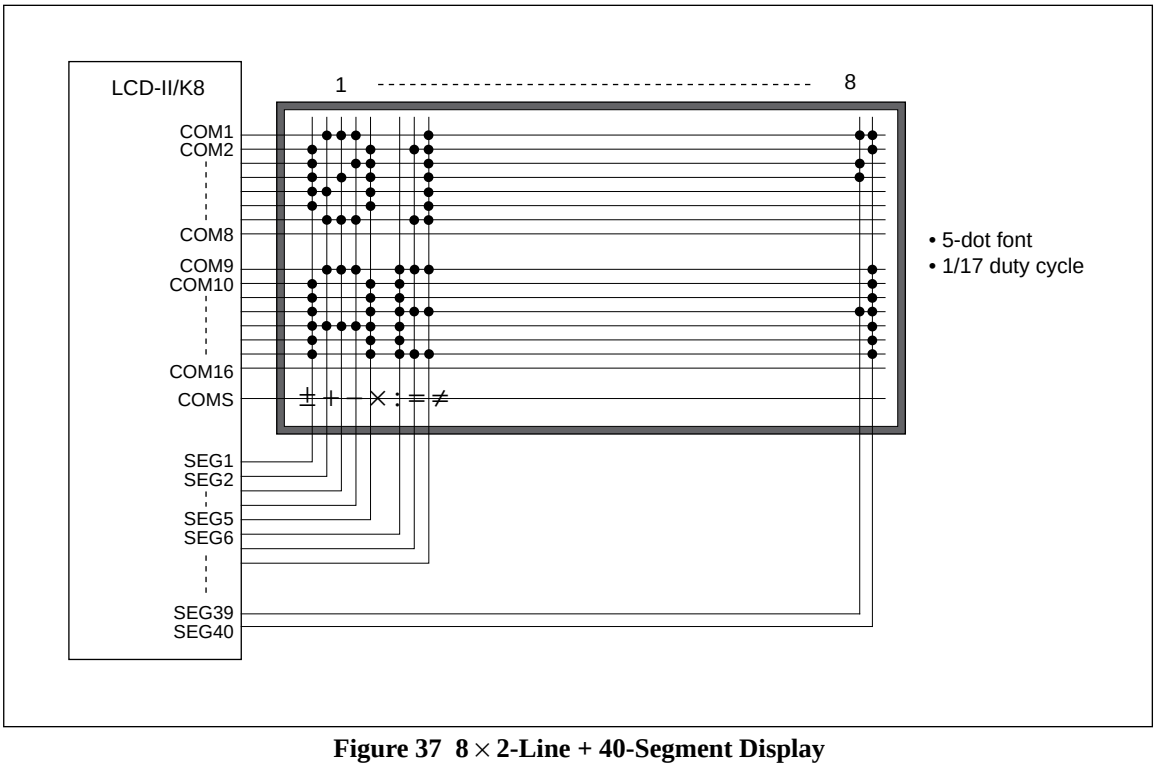


Figure 37 8 × 2-Line + 40-Segment Display

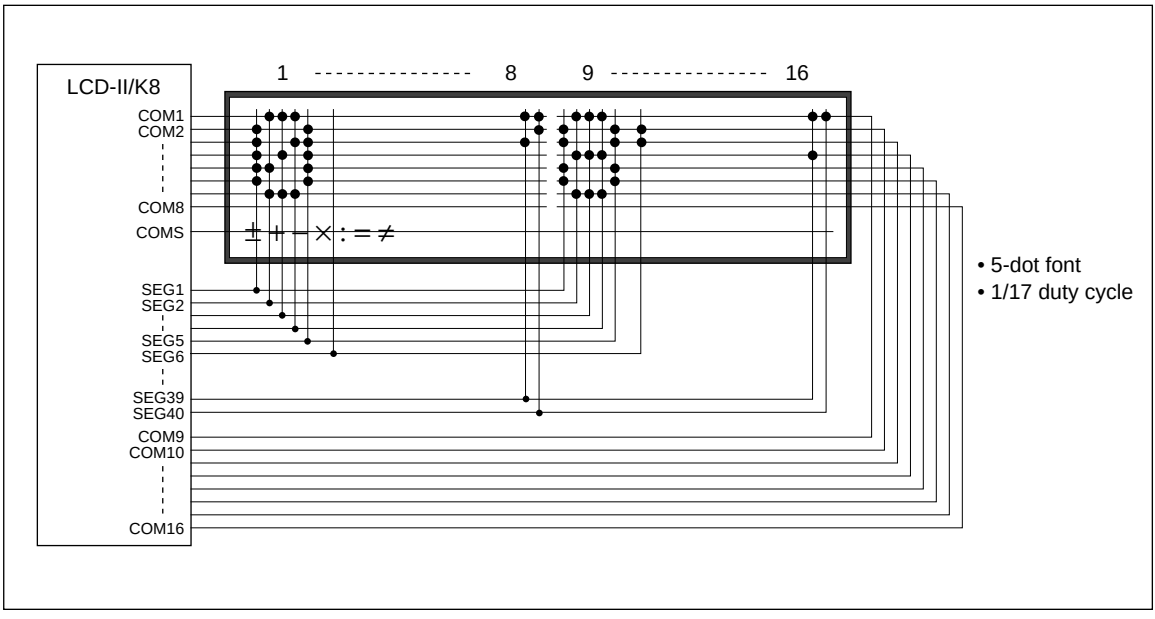


Figure 38 16 × 1-Line + 40-Segment Display (Using the 8 × 2-line Operation Mode)

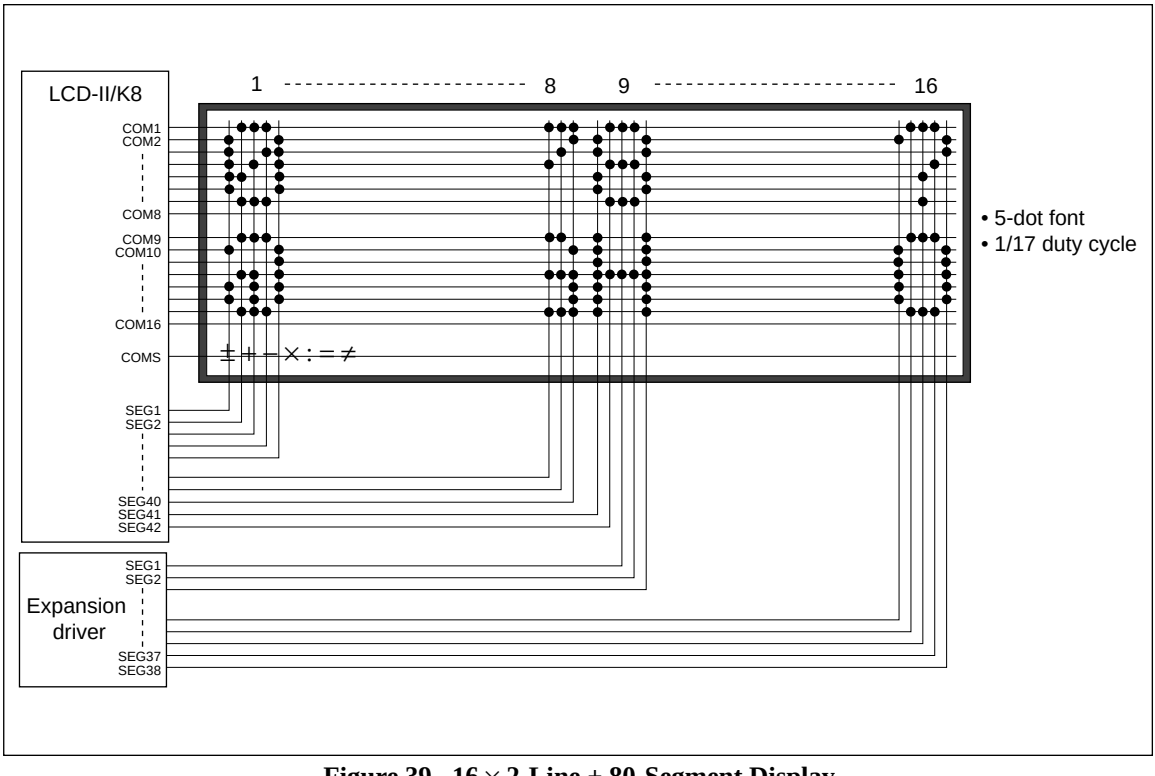


Figure 39 16 × 2-Line + 80-Segment Display

Example of 6-dot font width connection

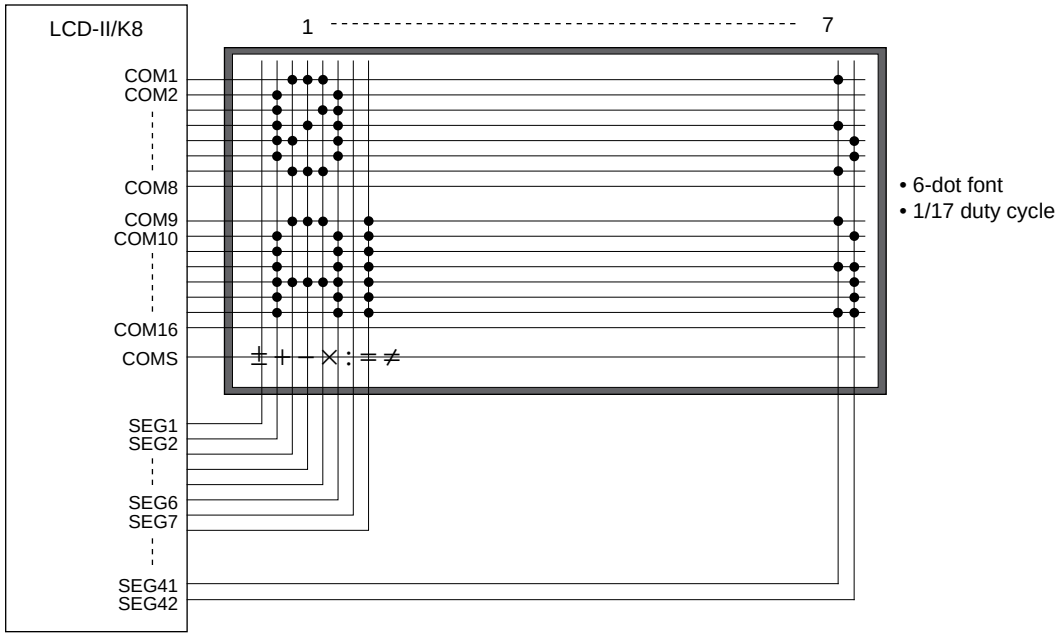


Figure 40 7 × 2-Line + 42-Segment Display

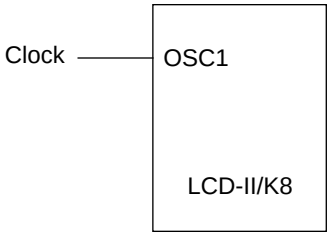
Table 15 Relationship between Oscillation Circuit and Liquid Crystal Display Frame Frequency

		1-Line Display		2-Line Display	
		5-Dot Font Width	**6-Dot Font Width**	**5-Dot Font Width**	**6-Dot Font Width**
1-Line Selection period	Normal mode	200 clock cycles	240 clock cycles	100 clock cycles	120 clock cycles
	LP mode	50 clock cycles	60 clock cycles	50 clock cycles	60 clock cycles
Frame frequency		88.9 Hz	74.1 Hz	94.1 Hz	78.4 Hz

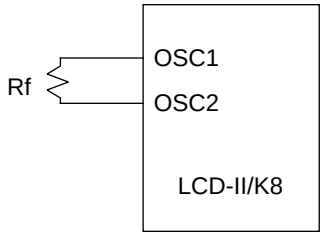
Note: The above values are obtained when the oscillation frequency is 160 kHz (1 clock cycle is 6.25 µs).

Oscillator

1) When an external clock is used



2) When an internal oscillator is used

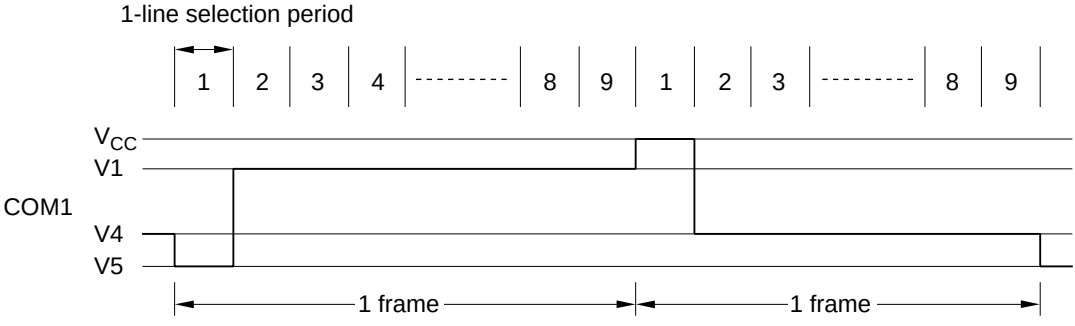


The oscillator frequency can be adjusted by an oscillator resistor (Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases. The recommended oscillator resistance is as follows.

- Rf = 200 kΩ ± 2% (V_{CC} = 5 V)
- Rf = 160 kΩ ± 2% (V_{CC} = 3 V)

Figure 41 Oscillator

(1) 1/9 duty cycle



(2) 1/17 duty cycle

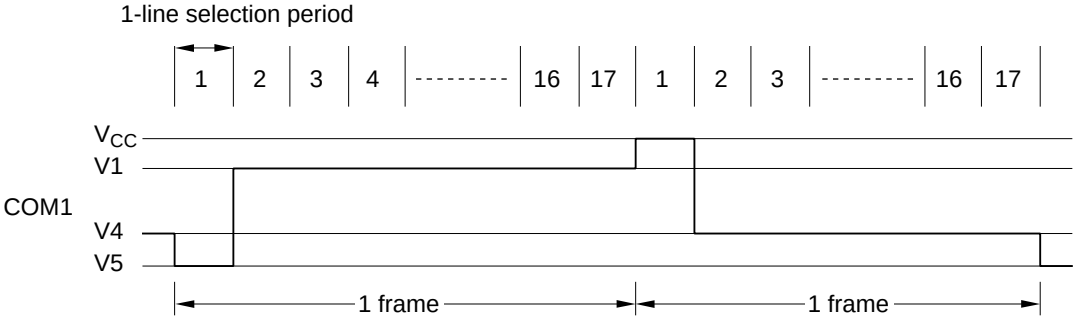


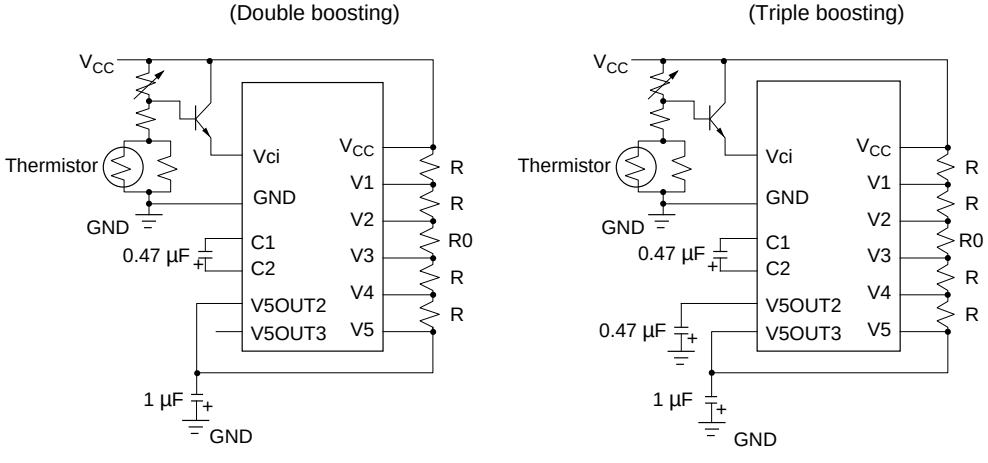
Figure 42 Frame Frequency

Power Supply for Liquid Crystal Display Drive

The LCD-II/K8 incorporates a booster for raising the LCD voltage 2-3 times that of the reference voltage input below V_{CC}. A 2-3 times boosted voltage can be obtained by externally attaching 2 or 3 capacitors.

If the LCD panel is large and needs a large amount of drive current, the value of bleeder resistor that generate the V1 to V5 potential are made smaller. However, the load current in the booster and the voltage drop increases in this case.

We recommend setting the resistance value of each bleeder larger than 4.7 kΩ and to hold down the DC load current to 0.4 mA if using a booster circuit. An external power supply should supply LCD voltage if the DC load current exceeds 0.7 mA. Refer to Electrical Characteristics showing the relationship between the load current and booster voltage output.



Notes:
1. The reference voltage input (Vci) must be set below the power supply (V_{CC}).
2. Current that flows into reference voltage input (Vci) is 2-3 times larger than the load current flowing through a bleeder resistor. Note that a reference voltage drop occurs due to the current flowing into the Vci input when a reference voltage (Vci) is generated by resistor division.
3. The amount of output voltage (V5OUT2/V5OUT3) drop of a booster circuit also increases as the load current flowing through bleeder resistors increases. Thus, set the bleeder resistance as large as possible (4.7 kΩ or greater) without affecting display picture quality.
4. Adjust the reference voltage input (Vci) according to the fluctuation of booster characteristics because the output voltage (V5OUT2/V5OUT3) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors and manufacturing tolerance. Refer to Electrical Characteristics for details.
5. Adjust the reference voltage input (Vci) so that the output voltage (V5OUT2/V5OUT3) after boosting will not exceed the absolute maximum rating of liquid crystal power supply voltage (13 V).
6. Make sure that you connect polarized capacitors correctly.

Figure 43 Example of Power Supply for Liquid Crystal Display Drive (with Internal Boost Circuit)

Table 16 Duty Factor and Bleeder Resistor Value for Power Supply for Liquid Crystal Display Drive

Item		Data	
Number of Lines		1	2
Duty factor		1/9	1/17
Bias		1/4	1/5
Bleeder resistance value	R	R	R
	R0	To be short-circuited	R

Note: R changes depending on the size of a liquid crystal panel. Normally, R must be 5 kΩ to 10 kΩ.

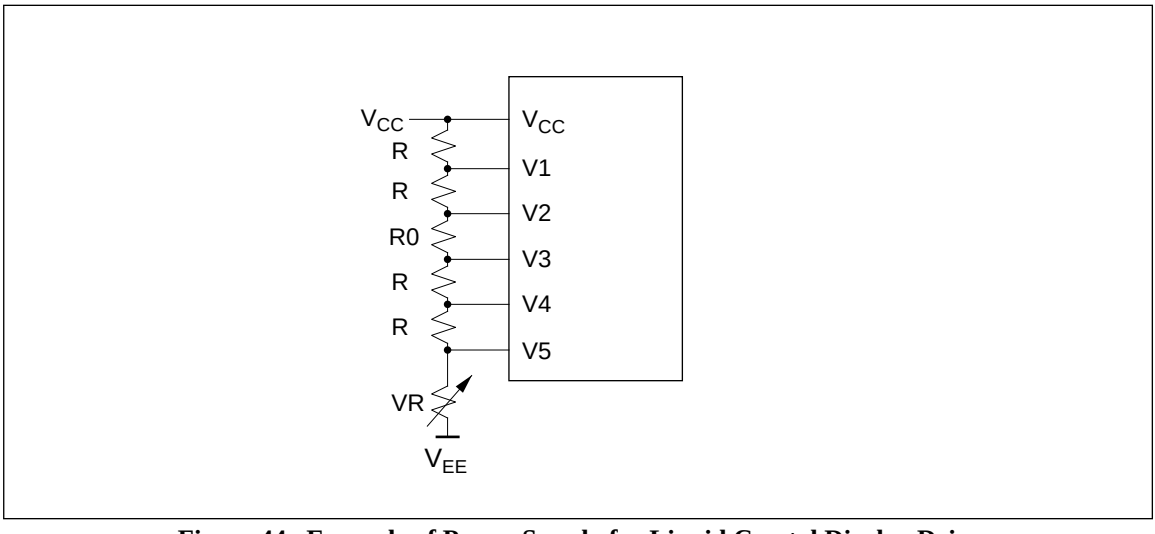


Figure 44 Example of Power Supply for Liquid Crystal Display Drive (with External Power Supply)

Font Display Control

The font width can be specified as 5 dots or 6 dots by setting the font width bit (FW) when the extension register is enabled (RE = 1). Although all fonts stored in CGROM have a 5-dot width, a smoother scroll can be displayed with a 6-dot wide font. Display data stored in CGROM/CGRAM/SEGRAM can be displayed as a mirror image (reflection) in the horizontal direction by setting the font reverse bit (FR). Select according to the LSI mounting method. Set character codes in DDRAM by software since the display read-order of DDRAM does not change.

Horizontal Dot Scroll

Dot unit scrolls are performed by setting the horizontal dot scroll bit (HDS) when the extension register is enabled (RE = 1). By combining this with scroll enable registers, smooth horizontal scrolling in the unit of display line can be performed. In this case, smoother scroll can be performed for a 6-dot font-width display.

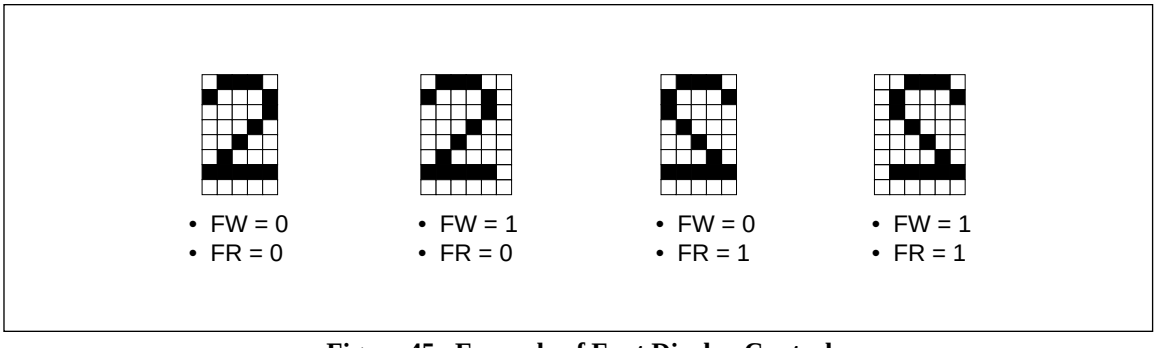


Figure 45 Example of Font Display Control

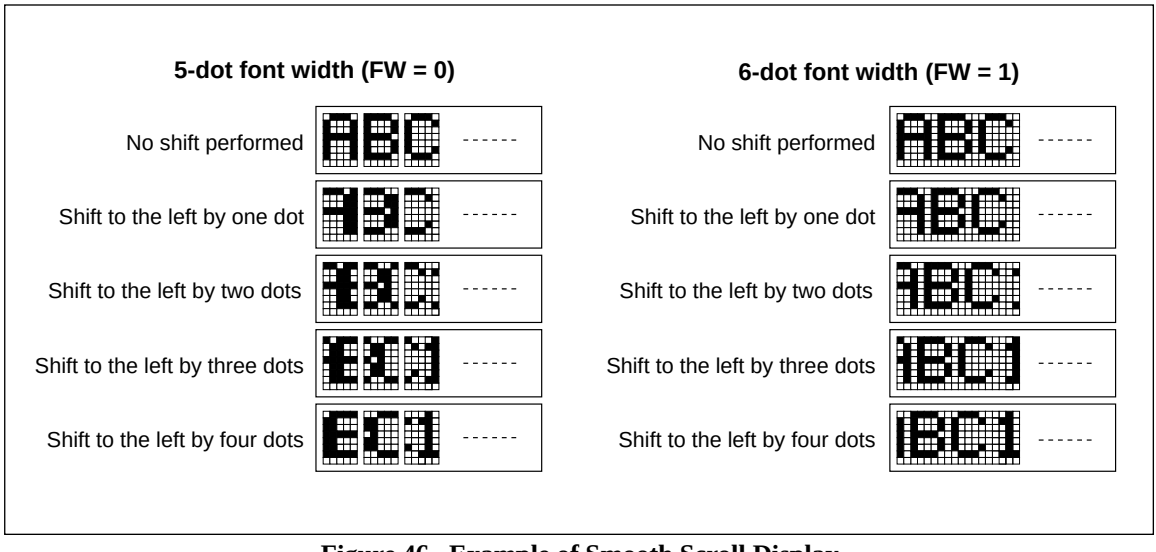
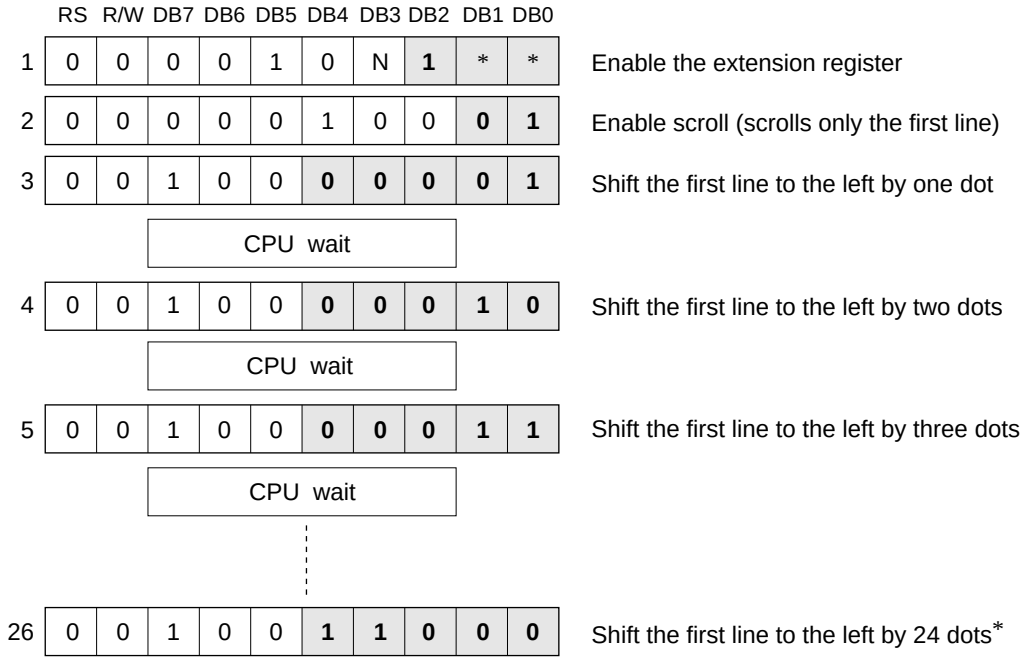


Figure 46 Example of Smooth Scroll Display

Smooth Scroll to the Left

The following shows an example of smooth scroll to the left for no font reflection (FR = 0) and a 6-dot font width (FW = 1). Because the maximum setting for dot smooth scroll (HDS) is 24 dots, scrolling for more than this number can be achieved by shifting to the left by four characters with a display shift instruction or by moving the data in DD RAM by four characters, rewriting them, and then scrolling again. When shifting the display character position with a display shift instruction, the 1st and 2nd line are shifted at the same time and then displayed.

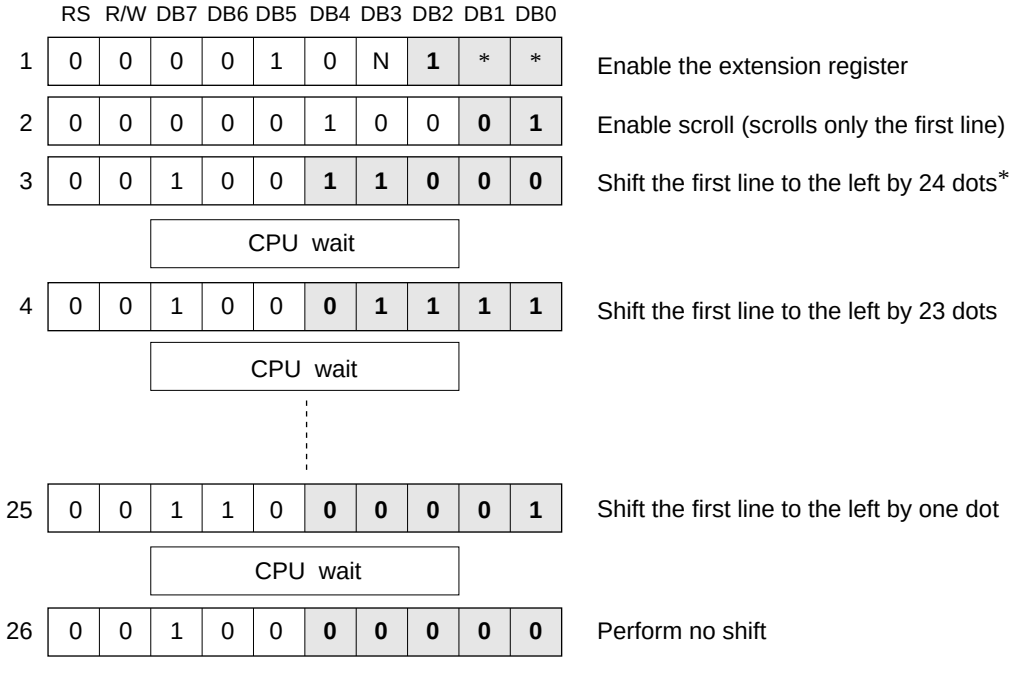


Note: * The sum of the number of characters displayed on the liquid crystal panel and the number of scroll characters must be smaller than the maximum number of display digits.
For example, when 16-digit, 2 lines are displayed with 6-dot font, the maximum number of display digits will be 20, and 4 characters maximum (24 dots) can be specified for scrolling.

Figure 47 Method of Smooth Scroll to the Left

Smooth Scroll to the Right

The following shows an example of smooth scroll to the right for no font reflection (FR = 0) and a 6-dot font width (FW = 1). Because the setting for dot smooth scroll (HDS) specifies a scroll to the left, scrolling to the right can be performed by first shifting the display character position to the right by four characters with a display shift instruction, or by moving the data in DDRAM for only lines to be scrolled by four characters, rewriting, and then scrolling from the 24th dot. When shifting the display character position with a display shift instruction, the 1st and 2nd line are shifted at the same time and then displayed.



Note: * The sum of the number of characters displayed on the liquid crystal panel and the number of scroll characters must be smaller than the maximum number of display digits.
For example, when 16-digit, 2 lines are displayed with 6-dot font, the maximum number of display digits will be 20, and 4 characters maximum (24 dots) can be specified for scrolling.

Figure 48 Method of Smooth Scroll to the Right

Partial Smooth Scroll (Limiting the Number of Characters Scrolled)

Partial smooth scroll displays some characters as fixed and the remaining ones in a horizontal smooth scroll. Here, only the number of left-most characters specified by the PS I/O bits can be fixed. The following shows an example of a smooth scroll performed in dot units from the second character to the eighth character with the PS1/O set to 01 so that the left-most character on the display panel is fixed. For a 2-line display, partial smooth scroll is performed for the display line specified by the scroll enable bits (SE2/1).

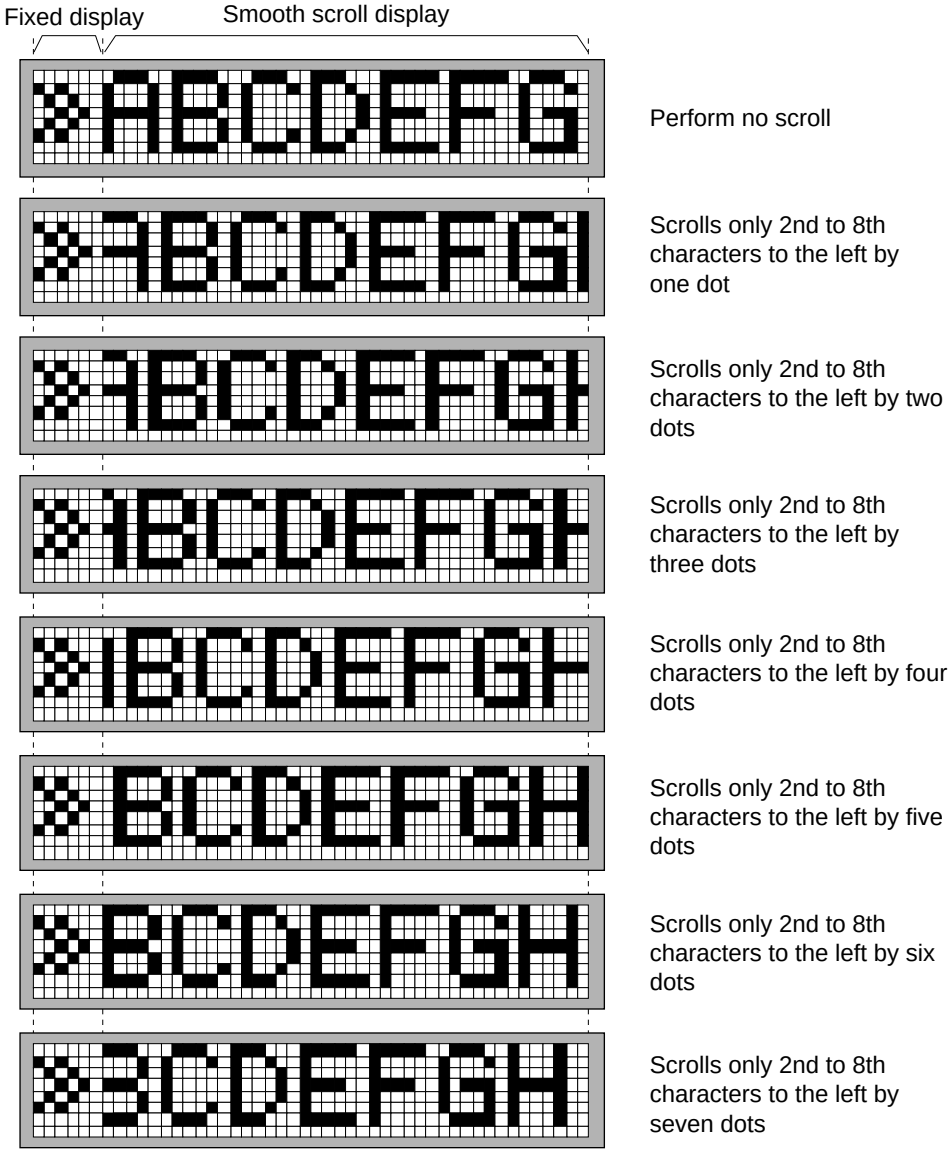


Figure 49 Partial Smooth Scroll

Low Power Mode

The HD66720 enters low power mode by setting the low-power mode bit (LP) to 1. During low-power mode, as the internal operation frequency is divided by 2 (1-line display mode) or by 4 (2-line display mode), the execution time of each instruction becomes two times or four times longer than normal. Be careful when writing instructions without performing busy flag checking.

During low power mode, a maximum of 10 characters are displayed per line. The DDRAM setting value become invalid from the 11th character. Note that the display differs from normal mode when display shifts or horizontal smooth scrolls are performed.

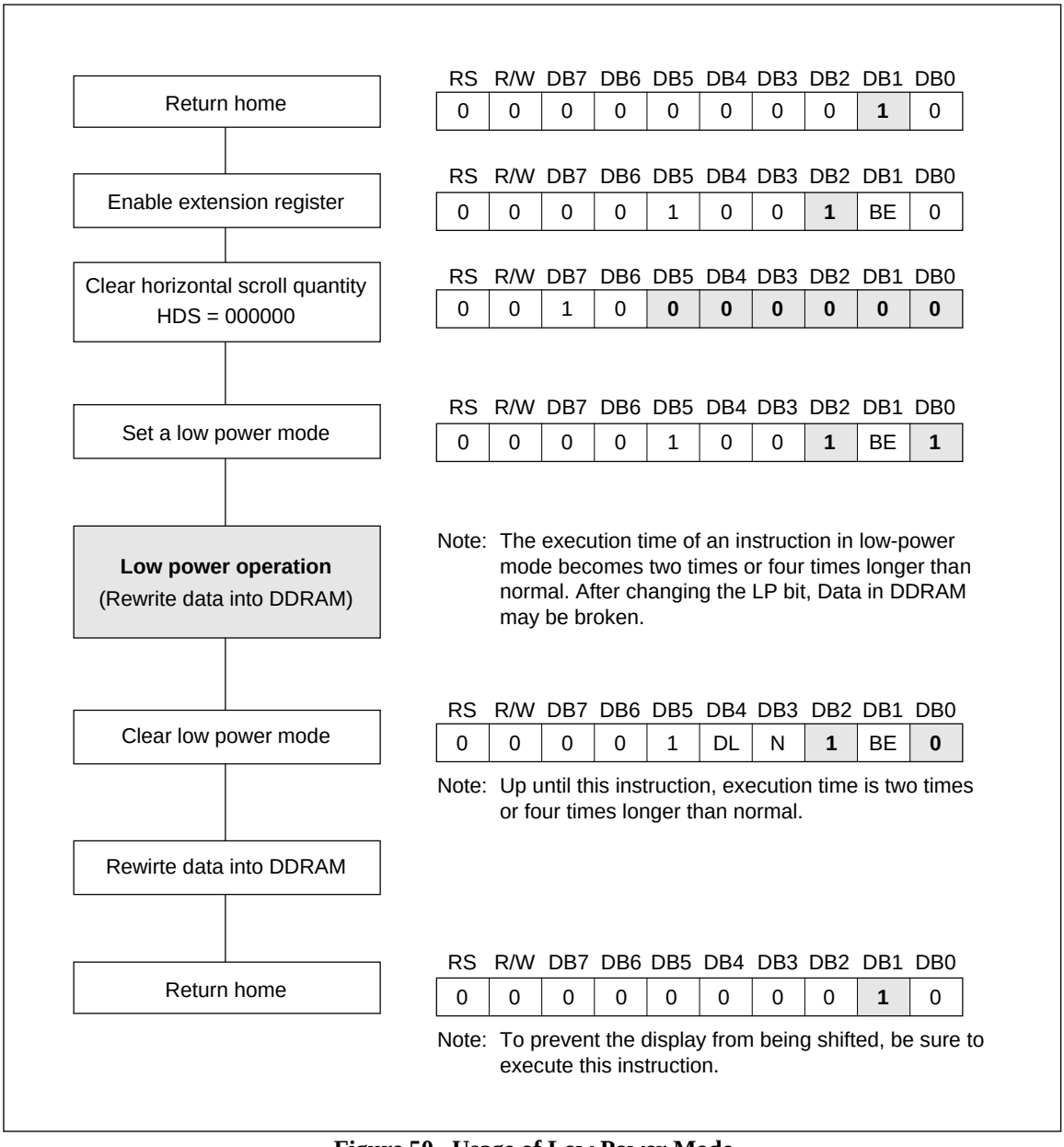


Figure 50 Usage of Low Power Mode

Sleep Mode

The HD66720 enters sleep mode by setting the sleep mode bit (SLP) to 1. During sleep mode, the display controller and LCD internal operation frequency is divided by 16, significantly reducing consumption current. However, the LCD will not perform normally at this time because the LCD frame frequency is also divided by 32, and the display should be turned off (D = 0). In this case, a scanning line may appear. To avoid this, the LCD driving voltage (V_{LCD}) should be cut off. The VLCD can be decreased by controlling the voltage of the Vci terminal flowing into the internal booster. In addition, execution time of each instruction becomes 16 times longer, and caution is needed when writing instructions without performing busy flag checking. The key scan circuit during sleep mode operates at the usual operation frequency. Key scan such as power-on keys can be performed by suppressing consumption current during system standby.

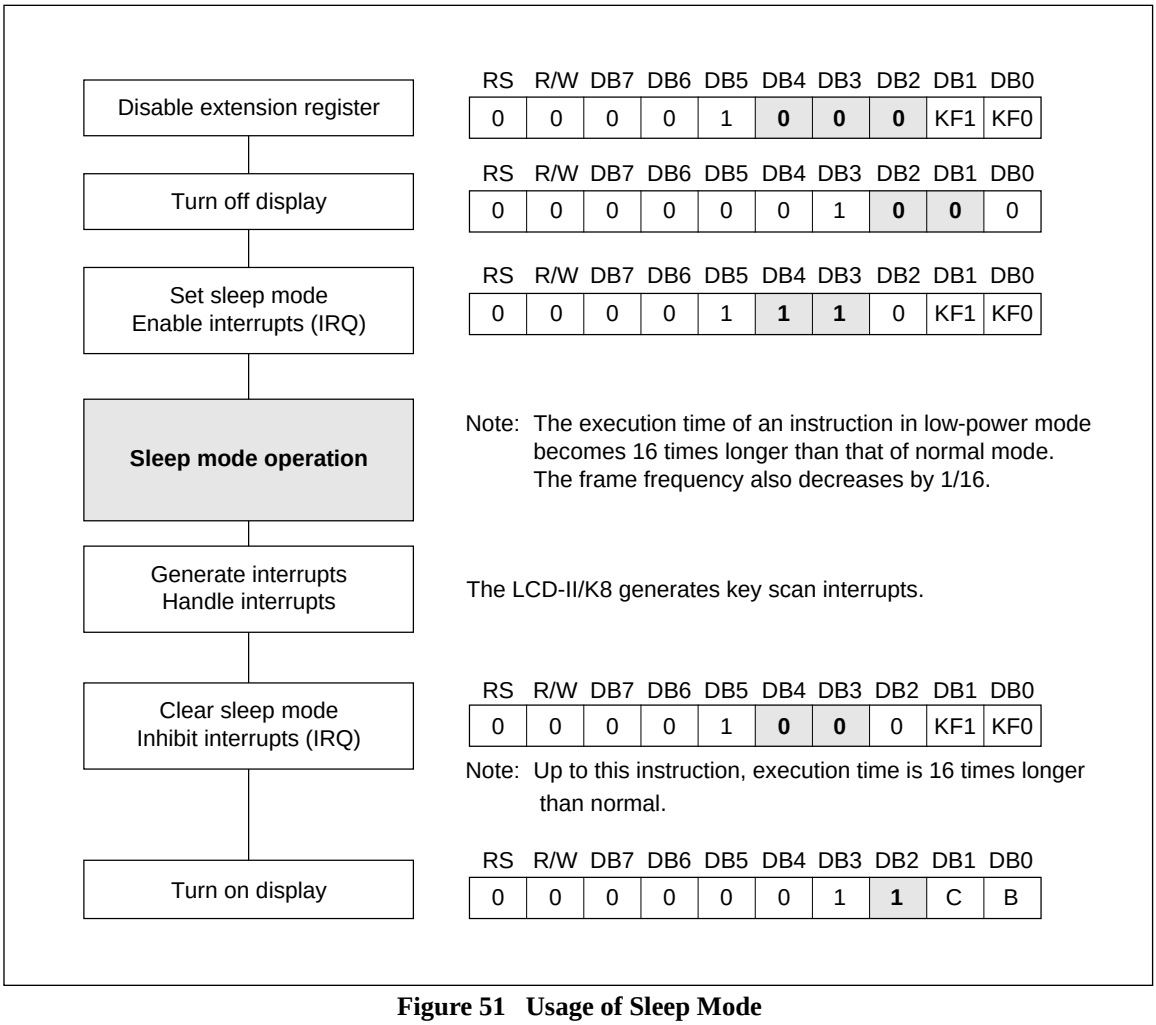


Figure 51 Usage of Sleep Mode

Relationship between Instruction and Display

Table 17 10-Digit × 1-Line Display Example with Internal Reset

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66720 is initialized by the internal reset circuit)											Initialized. No display.
2	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
3	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right when writing to the RAM. Display is not shifted.
4	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	H_	Writes H. DD RAM has already been selected by initialization.
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	1	HI_	Writes I.
	. . . . .										. . . . .	
6	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.
7	Entry mode set	0	0	0	0	0	0	0	1	1	1	HITACHI_	Sets mode to shift display at the time of write.
8	Write data to CG RAM/DD RAM	1	0	0	0	1	0	0	0	0	0	ITACHI _	Writes a space.

Table 17 10-Digit × 1-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
9	Write data to CG RAM/DD RAM										ITACHI M_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
	. . . . .										. . . . .	
10	Write data to CG RAM/DD RAM										MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
11	Cursor or display shift										MICROCO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	0	0		
12	Cursor or display shift										MICROCO	Shifts only the cursor position to the left.
	0	0	0	0	0	1	0	0	0	0		
13	Write data to CG RAM/DD RAM										ICROCO	Writes C. The display moves to the left.
	1	0	0	1	0	0	0	0	1	1		
14	Cursor or display shift										MICROCO	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	1	1	0	0		
15	Cursor or display shift										MICROCO_	Shifts the display and cursor position to the right.
	0	0	0	0	0	1	0	1	0	0		
16	Write data to CG RAM/DD RAM										ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
	. . . . .										. . . . .	
17	Return home										HITACHI	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Table 18 8-Digit × 2-Line Display Example with Internal Reset

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
1	Power supply on (the HD66720 is initialized by the internal reset circuit)											Initialized. No display.
2	Display on/off control	0	0	0	0	0	1	1	1	0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
3	Entry mode set	0	0	0	0	0	0	1	1	0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the RAM. Display is not shifted.
4	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	0	H_	Writes H. DD RAM has already been selected by initialization.
	. . . . .											. . . . .	
5	Write data to CG RAM/DD RAM	1	0	0	1	0	0	1	0	0	1	HITACHI_	Writes I.

Table 18 8-Digit × 2-Line Display Example with Internal Reset (cont)

Step No.	Instruction RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Display	Operation
6	Set DDRAM address										HITACHI _	Sets the DDRAM address so that the cursor positioned on the head of the second line.
	0	0	1	1	0	0	0	0	0	0		
7	Write data to CG RAM/DD RAM										HITACHI M_	Writes a space.
	1	0	0	1	0	0	1	1	0	1		
	. . .										. . .	
8	Write data to CG RAM/DD RAM										HITACHI MICROCO_	Writes O.
	1	0	0	1	0	0	1	1	1	1		
9	Entry mode set										HITACHI MICROCO_	Sets mode to shift display at the time of write.
	0	0	0	0	0	0	0	1	1	1		
10	Write data to CG RAM/DD RAM										ITACHI ICROCOM_	Writes M.
	1	0	0	1	0	0	1	1	0	1		
11	Return home										HITACHI MICROCOM	Returns both display and cursor to the original position (address 0).
	0	0	0	0	0	0	0	0	1	0		

Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary. Note that instructions are not accepted for 80 ms in 3-V operation or for 40 ms in 5-V operation after power is on since the HD66720 is in an internal reset state. Send an instruction after waiting for an appropriate amount of time after power-on.

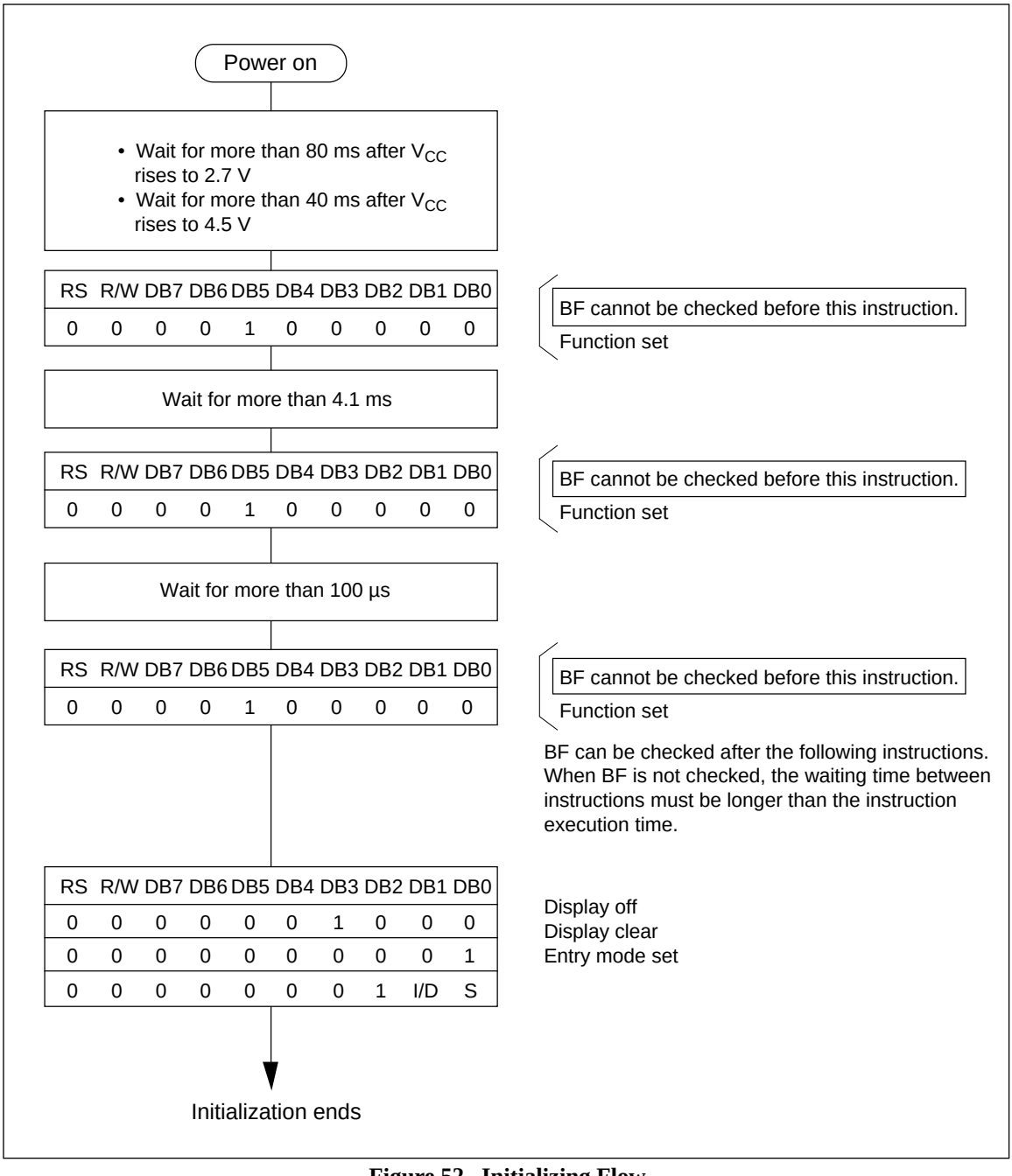


Figure 52 Initializing Flow

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +13.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} +0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (1) (except OSC1)	V_{IH1}	0.7V_{CC}	—	V_{CC}	V		5, 6
Input low voltage (1) (except OSC1)	V_{IL1}	–0.3	—	0.2V_{CC}	V	V_{CC} = 2.7 to 3.0 V	5, 6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC1)	V_{IH2}	0.7V_{CC}	—	V_{CC}	V		7
Input low voltage (2) (OSC1)	V_{IL2}	—	—	0.2V_{CC}	V		7
Output high voltage (1) (except KST, IRQ*)	V_{OH1}	0.75V_{CC}	—	—	V	$-I_{OH}$ = 0.1 mA	5, 8
Output high voltage (2) (KST, IRQ*)	V_{OH2}	0.7V_{CC}	—	—	V	$-I_{OH}$ = 1 µA	5, 10
Output low voltage (1) (except KST, LED, IRQ*)	V_{OL1}	—	—	0.2V_{CC}	V	I_{OL} = 0.1 mA	5, 9
Output low voltage (2) (KST, IRQ*)	V_{OL2}	—	—	0.2V_{CC}	V	I_{OL} = 0.5 mA	5, 10
Output low voltage (3) (LED 0/1)	V_{OL3}	—	—	1.2	V	I_{OL} = 10 mA, V_{CC} = 3 V	5, 11
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA (COM)	12
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA (SEG)	12
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	13
Pull-up MOS current (KIN0-KIN4)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	5, 14
Current consumption — Normal display	I_{CC1}	—	85	170	µA	Rf oscillation, external clock V_{CC} = 3V, f_{OSC} = 160 kHz	15, 16
Current consumption — Sleep mode	I_{CC2}	—	40	100	µA		
LCD voltage	V_{LCD1}	3.0	—	11.0	V	V_{CC}–V5, 1/5 bias	17

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	V_{ci} = 4.5 V, I_O = 0.25 mA, T_a = 25°C	20
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.8	—	V	V_{ci} = 3 V, I_O = 0.25 mA, T_a = 25°C	20
Input voltage	V_{Ci}	2.0	—	4.5	V		20

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	100	150	400	kHz		18
	External clock duty cycle	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
Rf oscillation	Clock oscillation frequency	f_{OSC}	120	160	210	kHz	R_f = 160 kΩ, V_{CC} = 3 V	19

Serial Interface Timing (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 53
Serial clock high level width	t_{SCH}	400	—	—	ns	
Serial clock low level width	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	0	—	—		

Serial Interface Timing (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 53
Serial clock high level width	t_{SCH}	200	—	—	ns	
Serial clock low level width	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	0	—	—		

Segment Extension Signal Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 54
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
Clock rise/fall time		t_{ct}	—	—	100		

Key Scan Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Key strobe low level width	5-dot font width	t_{KLW}	—	200Tc	—	ms	Figure 55
	6-dot font width	t_{KLW}	—	240Tc	—		
Key strobe frequency	5-dot font width	t_{KC}	—	1200Tc	—		
	6-dot font width	t_{KC}	—	1440Tc	—		

Note: Tc = $1/f_{osc}$

Reset Timing (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 56

Power Supply Conditions Using Internal Reset Circuit

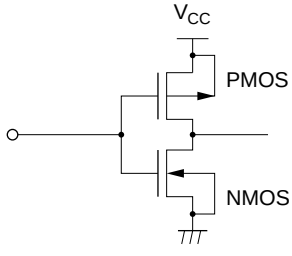
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rCC}	0.1	—	10	ms	Figure 57
Power supply off time	t_{OFF}	1	—	—		

Electrical Characteristics Notes

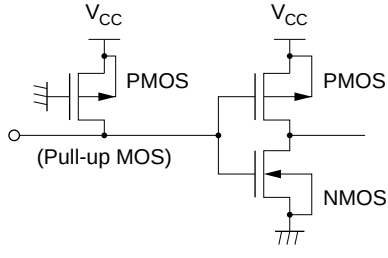
1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic conditions are exceeded, the LSI may malfunction or cause poor reliability.
2. $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

Input pin

Applies to pins SCLK, CS*, SID, and TEST1/2

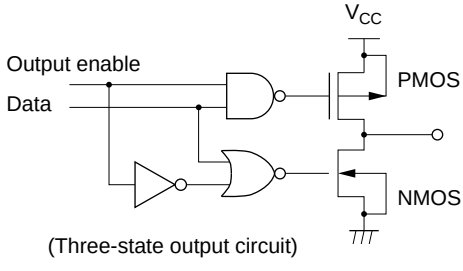


Applies to pins KIN0 to KIN4 and RESET*



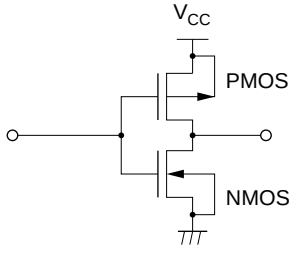
Output pin

Applies to pin SOD



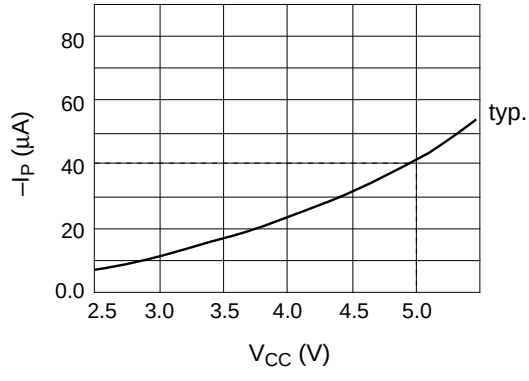
(Three-state output circuit)

Applies to pins CL1, CL2, M, D, KST0 to KST5, IRQ*, and LED0/1

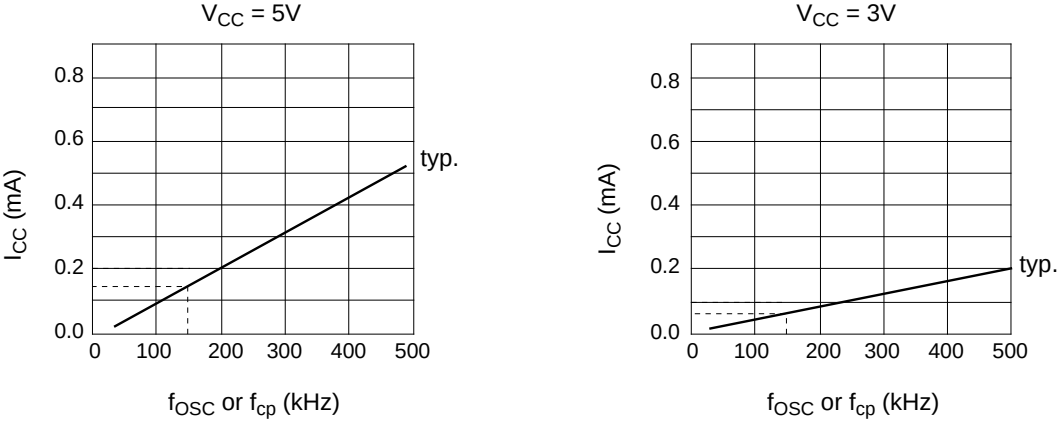


6. Applies to input pins, excluding the OSC_1 pin. However, the TEST1/2 pins must be grounded (GND).
7. Applies to the OSC_1 pin.
8. Applies to output pins, excluding pins KST0 to KST5 and LCD output pins.
9. Applies to output pins, excluding pins KST0 to KST5, pins LED0/1, and LCD output pins.
10. Applies to pins KST0 to KST5.

11. Applies to LED0/1 output pins.
12. Applies to resistor values (RCOM) between power supply pins V_{CC}, V1, V4, V5 and common signal pins (COM1 to COM16 and COMS), and resistor values (RSEG) between power supply pins V_{CC}, V2, V3, V5, and segment signal pins (SEG1 to SEG42).
13. Current that flows through pull-up MOS and output drive MOS is excluded.
14. Applies to the pull-up MOS of pins KIN0 to KIN4. The following shows the relationship between the power supply voltage (V_{CC}) and pull-up MOS current ($-I_p$) (referential data).

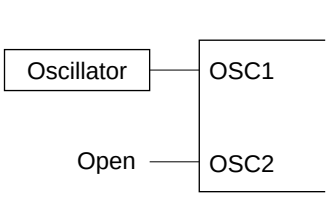


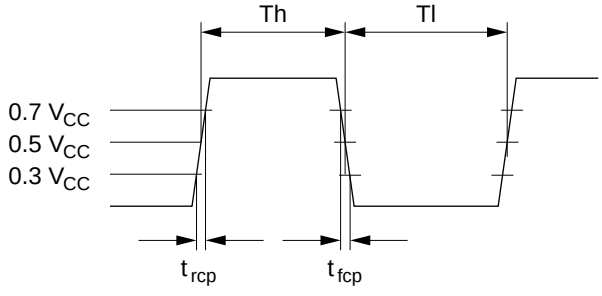
15. This excludes the current flowing through the I/O section. The input level must always be at a specified high or low level because through current increases if the CMOS input is left floating.
16. The following shows the relationship between the operation frequency (f_{OCS} or f_{cp}) and current consumption (I_{CC}).



17. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.

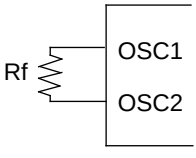
18. Applies to the external clock input.





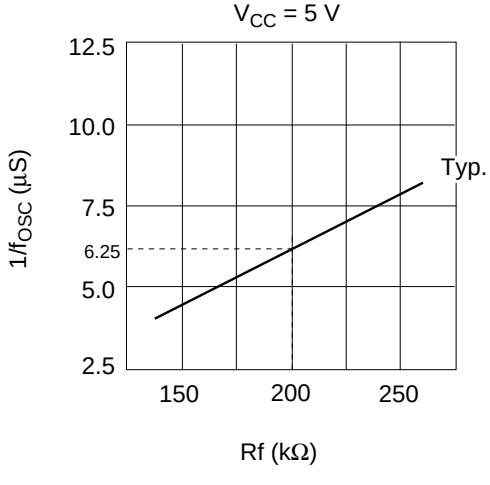
$$\text{Duty cycle} = \frac{Th}{Th + Tl} \times 100\%$$

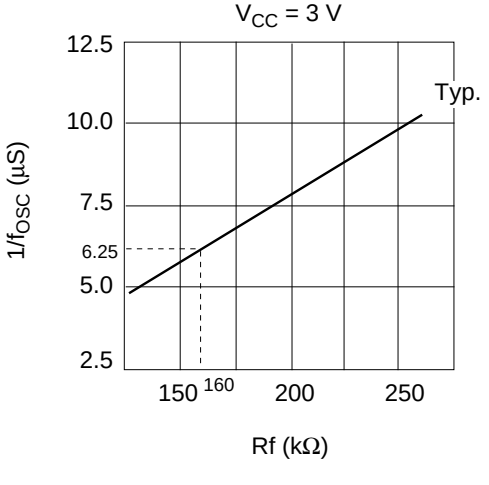
19. Applies to internal oscillator operations when oscillator Rf is used.



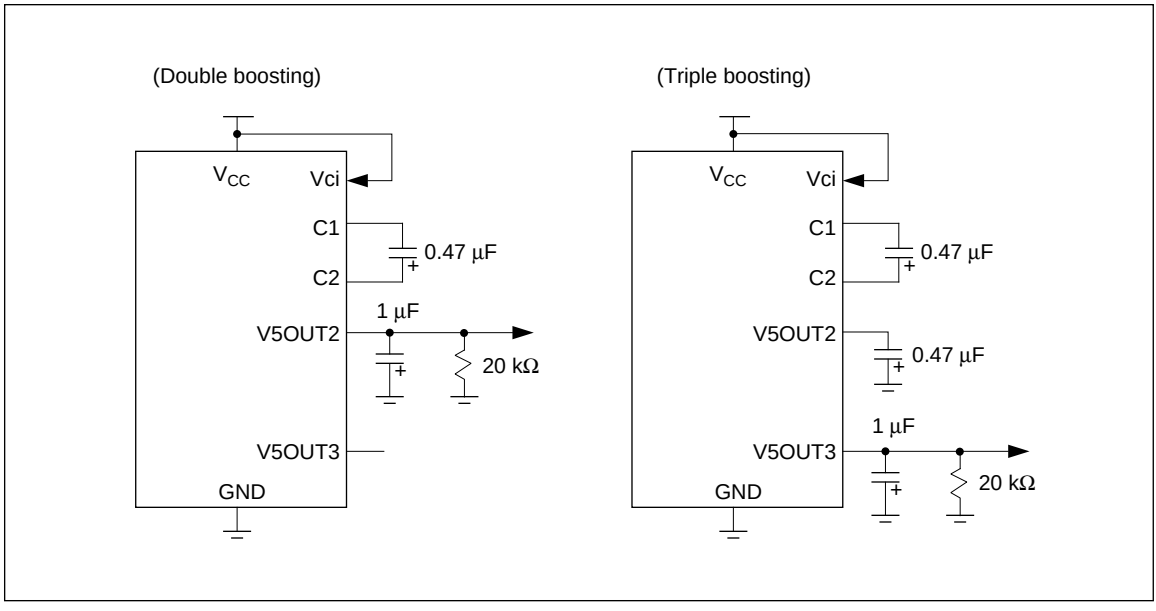
Rf: 160 kΩ ± 2% (when V_{CC} = 3 V to 4 V)
Rf: 200 kΩ ± 2% (when V_{CC} = 4 V to 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

The following shows the relationship between the Rf oscillator resistor value and oscillator frequency (referential data).



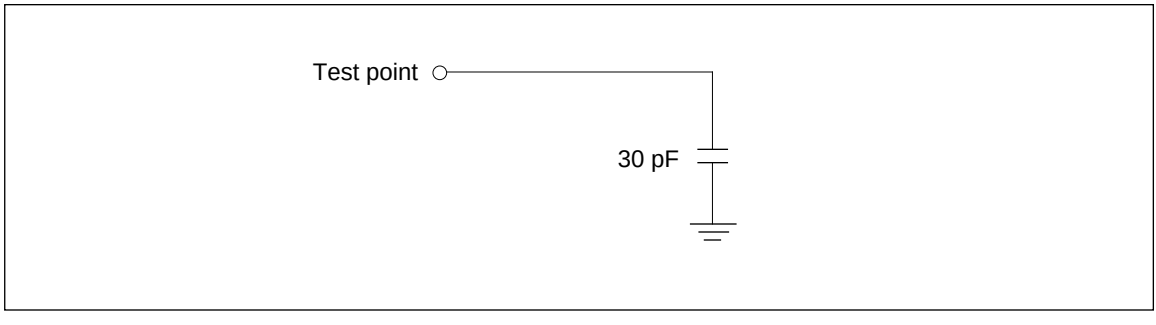


20. Booster characteristics test circuits are shown below.



Load Circuits

AC Characteristics Test Load Circuits



Timing Characteristics

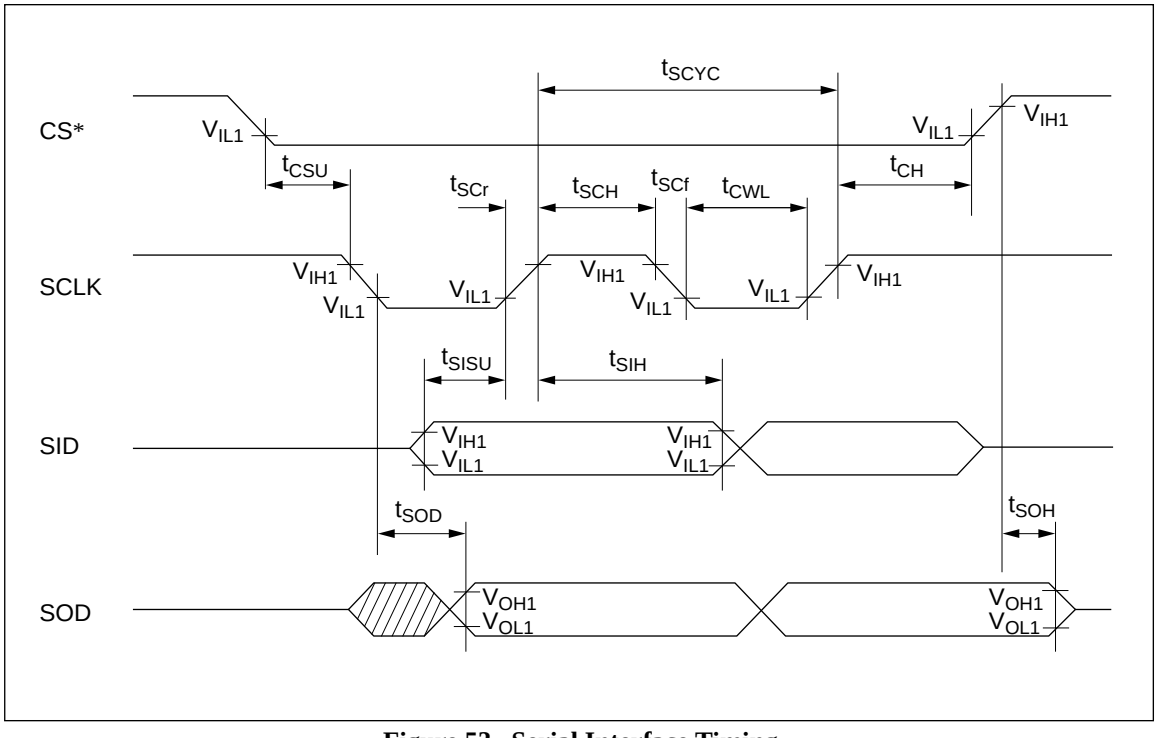


Figure 53 Serial Interface Timing

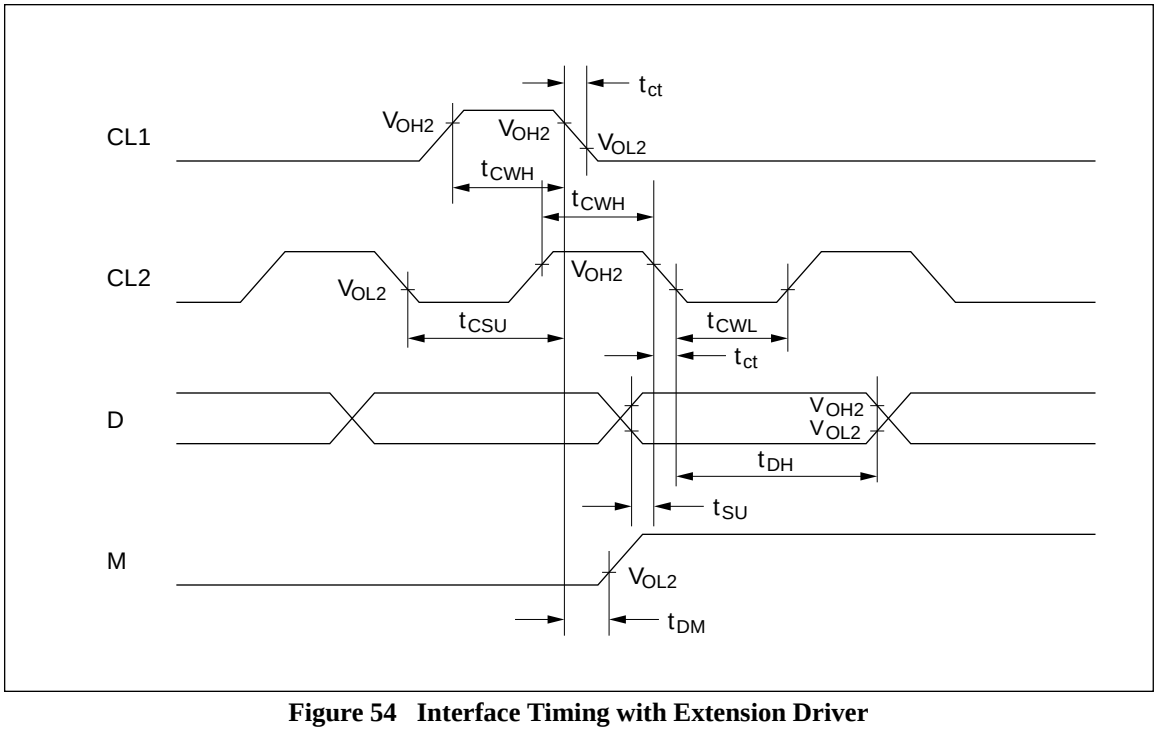


Figure 54 Interface Timing with Extension Driver

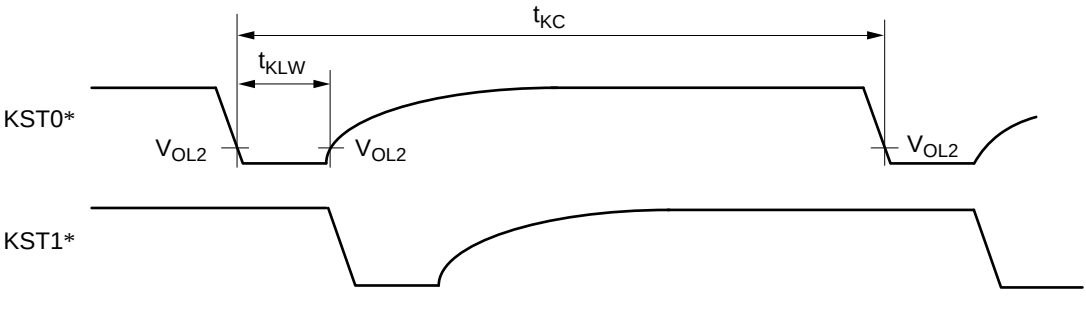
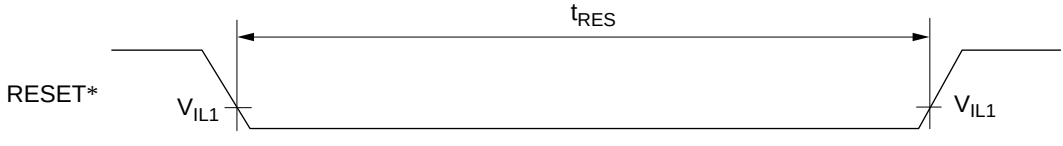
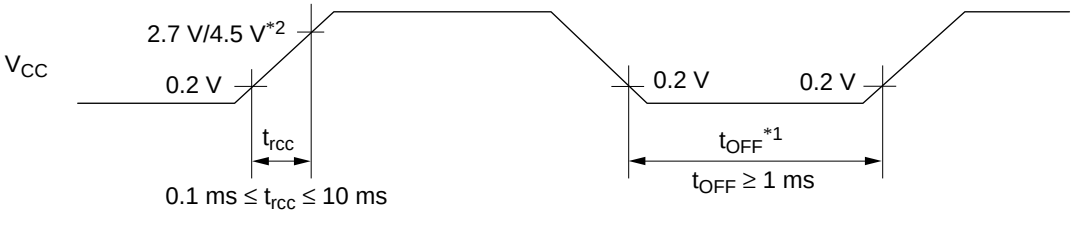


Figure 55 Key Strobe Timing



Note: When power is supplied, initializing by the internal reset circuit has priority. Accordingly, the above RESET* input is ignored during internal reset period.

Figure 56 Reset Timing



Notes:
1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.
3. If the above electrical conditions are not satisfied, the internal reset circuit will not operate normally. In this case, initialize by instruction. (Refer to Initializing by Instruction.)

Figure 57 Power Supply Sequence